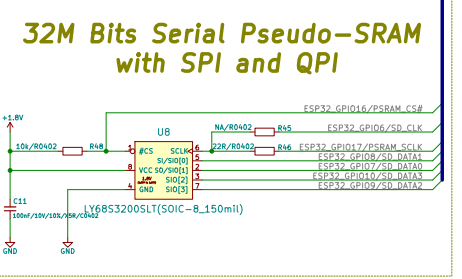
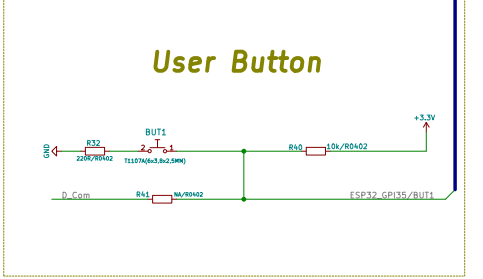
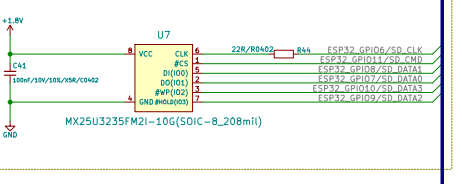
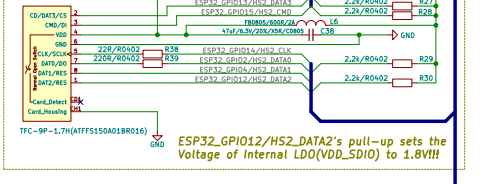
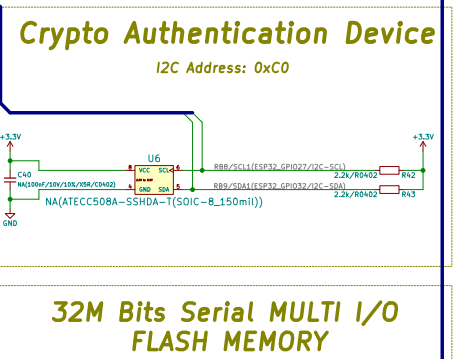
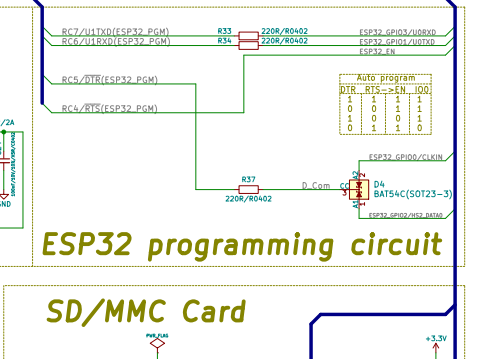
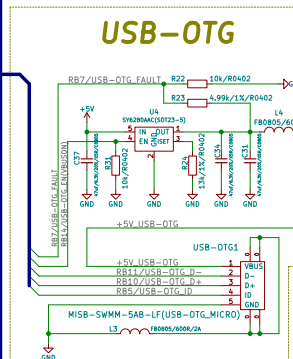
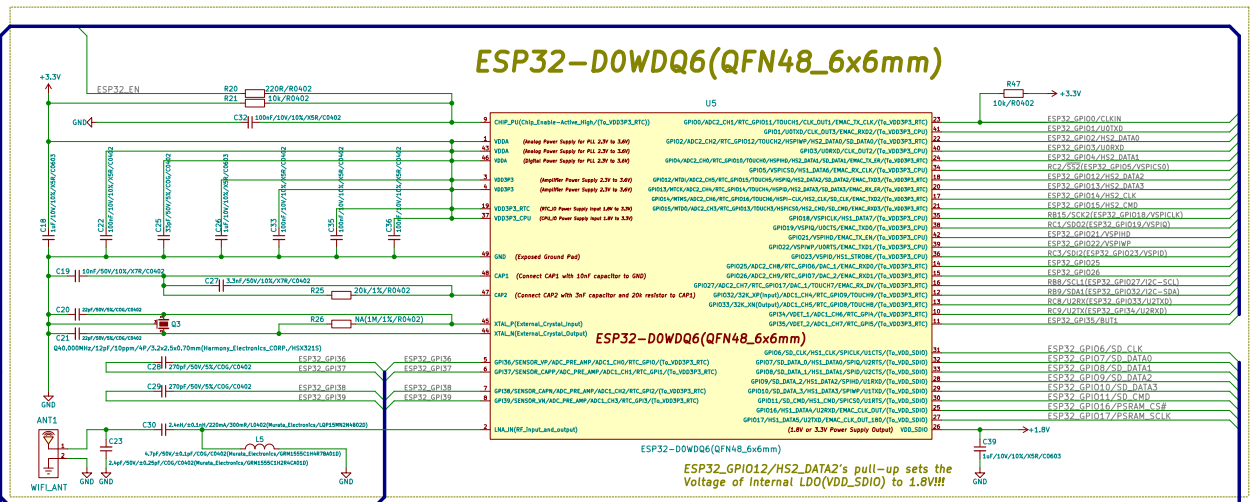
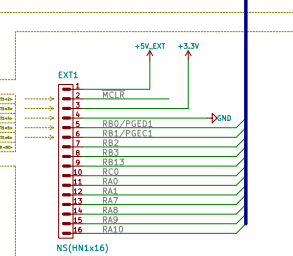


The following PIC32MX270F256DT-I/PT registers must be configured as follows:

- DEVCFG0's bits ICESSEL<1:0> to be set to: 11 = PGEC1/PGED1 pair is used;
- DEVCFG3's bit FUSBDIO to be set to: 1 = USBID pin is controlled by the USB module;
- IEC0's bit INT0 to be set to: 1, i.e. INT0 - External Interrupt is enabled;
- DEVCFG3's bit VBUSONIO to be set to: 1 = VBUSON pin is controlled by the USB module;
- RPC1R<3:0> to be set to: 0100 = SD02, i.e. RC1 = SD02;
- RPC2R<3:0> to be set to: 0100 = SS2, i.e. RC2 = SS2;
- SD0R<3:0> to be set to: 0111 = RP01, i.e. RC4 = SD02;
- RPC4R<3:0> to be set to: 0001 = U1R15, i.e. RC4 = U1R15 or use a GPIO function for RC4;
- Use GPIO function for RC5/DTR;
- U1R0R<3:0> to be set to: 0101 = RP06, i.e. RC6 = U1R1;
- RPC7R<3:0> to be set to: 0001 = U1TX, i.e. RC7 = U1TX;
- U2R0R<3:0> to be set to: 0110 = RP08, i.e. RC8 = U2TX;
- RPC9R<3:0> to be set to: 0010 = U2TX, i.e. RC9 = U2TX;
- Set up all other PIC32MX270F256DT-I/PT registers so that to be enabled and correctly configured all other used peripherals;

The components related to both crystal oscillators are consistent to the recommended in the PIC32MX270F256DT-I/PT's datasheets!



Bootstrapping Pins Informations

Software Selectable Pins		
Interface	Signal	Pin
EMAC	EMAC_MDIO	Any GPIO
	EMAC_MDC	
	EMAC_CRS	
	EMAC_CRS_	
I2C	DC02TS_0A_	Any GPIO
	DC02TS_0B_	
	DC02TS_1A_	
	DC02TS_1B_	
	DC02TS_2A_	
	DC02TS_2B_	
General Purpose SPI	HSPICLK_	Any GPIO
	HSPICLK_	
	HSPICLK_	
	HSPICLK_	
	HSPICLK_	
	HSPICLK_	
	HSPICLK_	
	HSPICLK_	
	HSPICLK_	
	HSPICLK_	
For more information refer to exp_worm32_release_en.pdf.		

Internal Bootstrapping Resistors			
MTDI/GPIO12:		Pull-Up	
GPIO0:		Pull-Up	
GPIO2:		Pull-Up	
GPIO4:		Pull-Up	
MTDI/GPIO15:		Pull-Up	
GPIO15:		Pull-Up	

		Voltage of Internal Bootstrapping Resistors	
Pin	Default	3.3V	1.8V
GPIO/MTDI	Pull-Down	0	1
		Resistor Value	
Pin <th>Default</th> <td>SPI Flash Read</td> <td>Readwrite Read</td>	Default	SPI Flash Read	Readwrite Read
GPIO	Pull-Up	0	0
GPIO	Pull-Down	Don't-care	Don't-care
		Bootstrapping Logic on MTDI Purging Booting	
Pin <th>Default</th> <td>GPIO Register</td> <td>GPIO Register</td>	Default	GPIO Register	GPIO Register
GPIO/MTDI	Pull-Up	1	0
		Timing of MTDI Read	
Pin <th>Default</th> <td>Falling-edge-output</td> <td>Falling-edge-output</td>	Default	Falling-edge-output	Falling-edge-output
GPIO/MTDI	Pull-Up	0	1
GPIO	Pull-Up	0	0

Bootstrapping P Settings				
		Falling-edge-output		Falling-edge-output
		GPIO Register	GPIO Register	
		0	1	
		0	0	