CMOS Sensor Acquisition

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1 Core Overview

The `cmos_sensor_acquisition` core is a configurable Qsys system that makes it simple to connect a CMOS sensor to a host processor & memory system.

It combines 3 sub-cores to create a *single*-component CMOS sensor acquisition system easily instantiable in Qsys:

- `cmos_sensor_input`
- `dc_fifo`
- `msgdma`

The core comes with a set of C library interfaces that can be used to configure it and start its various operations.

2 CMOS Sensors

A CMOS sensor outputs 4 signals with which it is possible to sample its data:

- `clock`
- `frame_valid (1-bit)`
- `line_valid (1-bit)`
- `data (n-bit)`

Figure 1 shows the relationship between the different signals for 2 frames that contains 2 rows and 3 columns each.

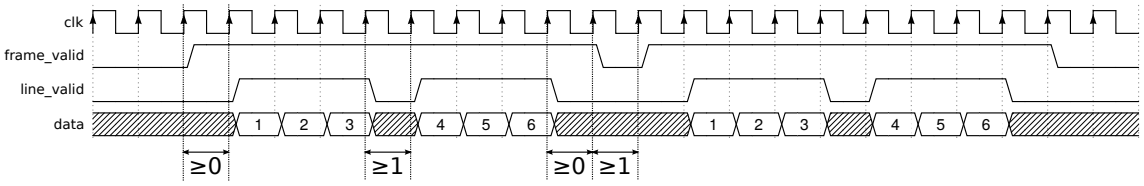

Figure 1: CMOS sensor output signals for two 3×2 frames with a pixel depth of 3 bits. Spacing requirements between the various signals are specified in clock cycles.

3 Block Diagram

Figure 2 shows the connections between the 3 main building blocks that compose the `cmos_sensor_acquisition` core.

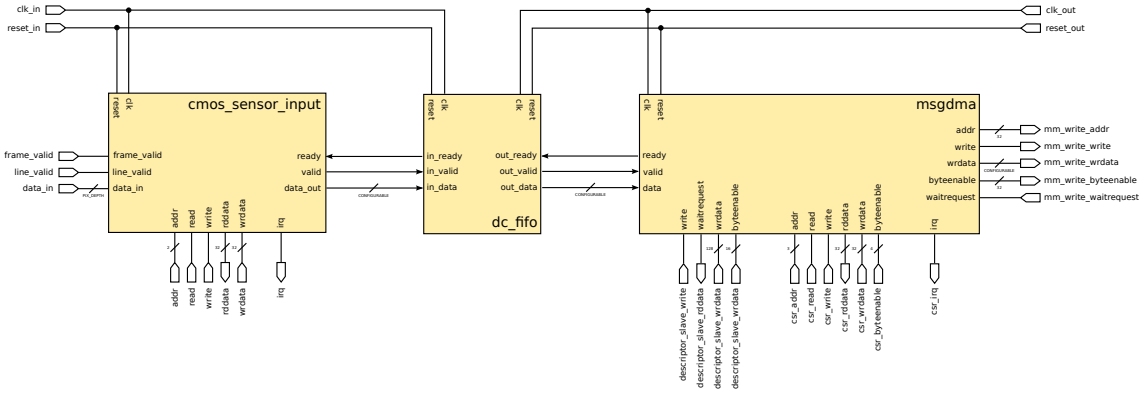

Figure 2: High-level block diagram.

4 Qsys Interface

Figure 3 shows the Qsys configuration interface for the core.

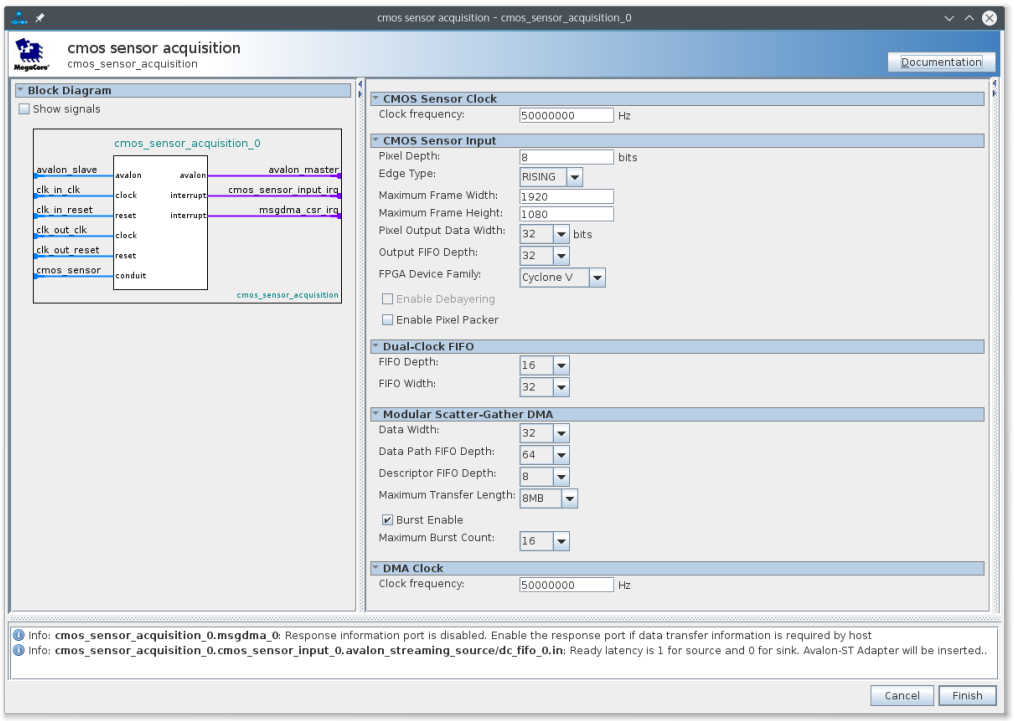

Figure 3: Qsys Configuration Interface.

It can be configured through 17 parameters, shown in Table 1.

Core	Parameter	Type	Values	Default Value
cmos_sensor_input	PIX_DEPTH	Positive	1, 2, 3, ..., 32	8
	SAMPLE_EDGE	String	"RISING", "FALLING"	"RISING"
	MAX_WIDTH	Positive	2, 3, 4, ..., 65535	1920
	MAX_HEIGHT	Positive	1, 2, 3, ..., 65535	1080
	OUTPUT_WIDTH	Positive	8, 16, 32, ..., 1024	32
	FIFO_DEPTH	Positive	8, 16, 32, ..., 1024	32
	DEVICE_FAMILY	String	"Cyclone V", "Cyclone IV E"	"Cyclone V"
	DEBAYER_ENABLE	Boolean	FALSE, TRUE	FALSE
	PACKER_ENABLE	Boolean	FALSE, TRUE	FALSE
dc_fifo	FIFO_DEPTH	Positive	16, 32, 64, ... , 4096	16
	FIFO_WIDTH	Positive	8, 16, 32, ... , 1024	32
msgdma	DATA_WIDTH	Positive	8, 16, 32, ... , 1024	32
	DATA_FIFO_DEPTH	Positive	16, 32, 64, ... , 4096	64
	DESCRIPTOR_FIFO_DEPTH	Positive	8, 16, 32, ... , 1024	8
	MAX_BYTE	Positive	1KB, 2KB, 4KB, ..., 2GB	8MB
	BURST_ENABLE	Boolean	FALSE, TRUE	TRUE
	MAX_BURST_COUNT	Positive	2, 4, 8, ... , 1024	16

Table 1: Qsys parameters.

5 Results

All benchmarks results below were obtained using the default core parameter values shown in Table 1.

The system was benchmarked on a `"Cyclone IV E"`-class device, and was able to successfully capture a frame with a resolution of 1920×1080 pixels under the following timing constraints:

- 10 MHz `cmos_sensor_input` clock
- `FRAME_FRAME_BLANK = 1`
- `FRAME_LINE_BLANK = 0`
- `LINE_LINE_BLANK = 1`
- `LINE_FRAME_BLANK = 0`
- `cmos_sensor_input packer` disabled.
- 50 MHz `msgdma` clock

Note that no camera on the market can actually output frames with such tight frame-frame, frame-line, line-line, and line-frame timings. The benchmark was rather performed for demonstration purposes to show that the design is able to capture frames under tight constraints.

Furthermore, note that the `cmos_sensor_input` packer was *not* enabled, which would have allowed one to divide the pressure on the memory system by at least a factor of 2. It is recommended to always enable this option, but again, it was left out for demonstration purposes to show the performance of the core.