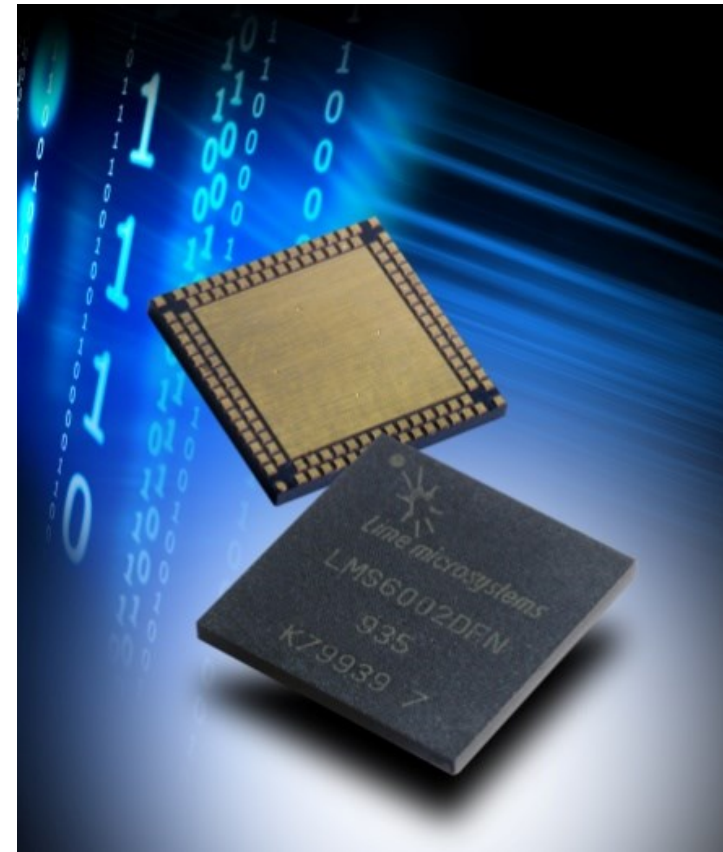


Improving RxVGA2 DC Offset Calibration Stability

Measured on UWCT board

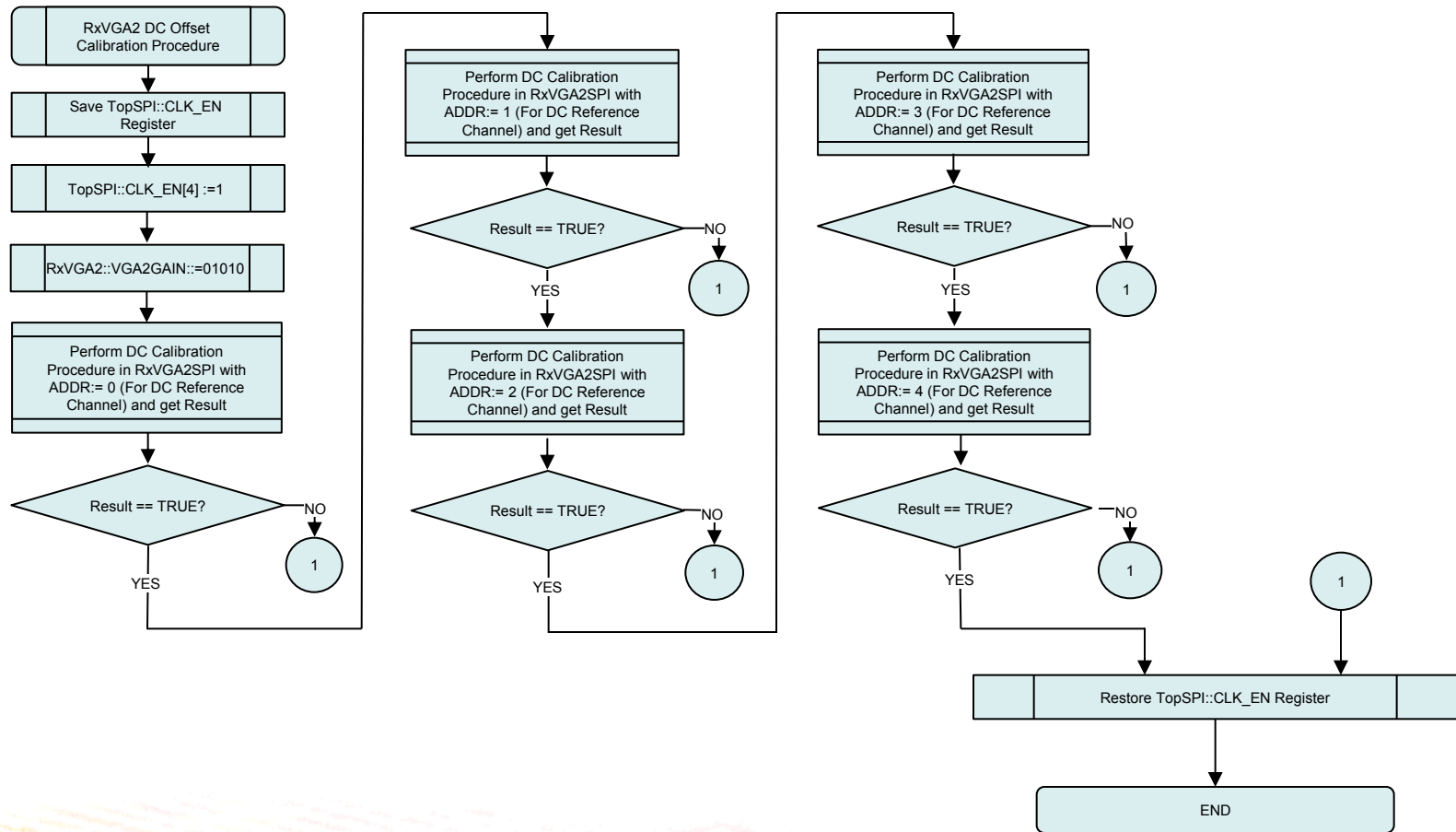


Introduction

- Default RxVGA2 DC offset calibration method gives unstable calibration results.
- The noise, which is introduced in every VGA2 gain stage (Stage A and Stage B), may cause instability of comparators in calibration loop.
- To reduce noise, every VGA2 gain stage is reprogrammed before calibration. Test description:
 - Set VGA2 A stage gain to 18dB and VGA2 B stage to 0dB
 - Run auto cal for channel I and Q, on VGA2 A stage only.
 - Save Cal Results.
 - Set VGA2 A stage gain to 0dB and VGA2 B stage to 18dB.
 - Run auto cal for channel I and Q, on VGA2 B stage only.
 - Save Cal Results.
 - Calibration executed 100 times to check repeatability.
- Both RXVGA2 calibration methods are tested and compared.

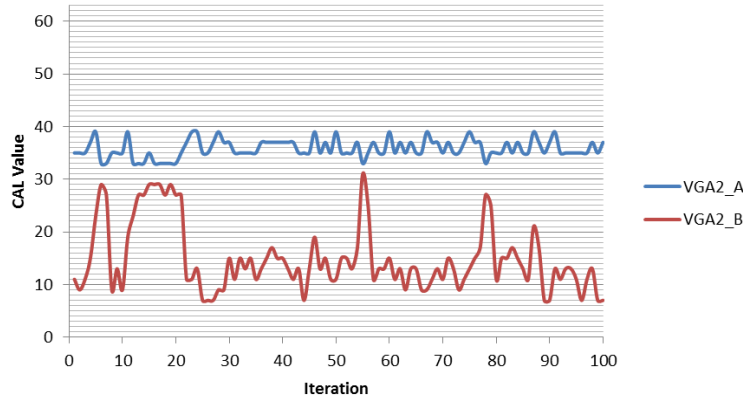
Default RCVGA2 Calibration Method

Calibration Algorithm Block Diagram

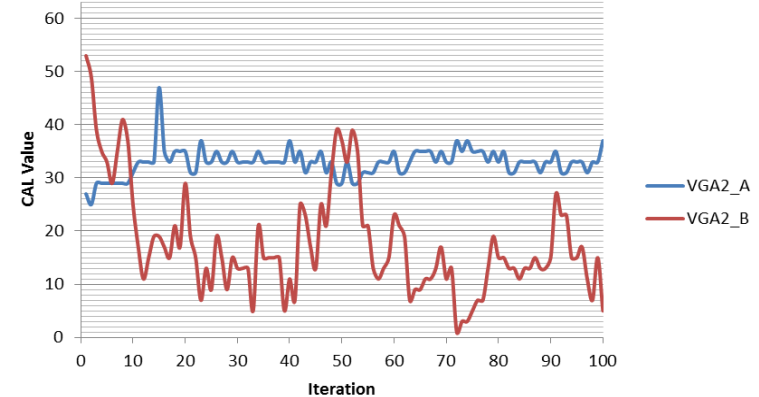


Calibration Test Results

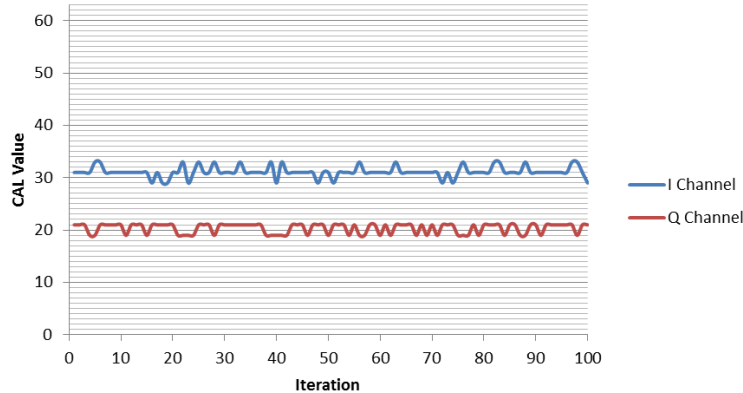
Rx I Channel VGA2 Cal Values



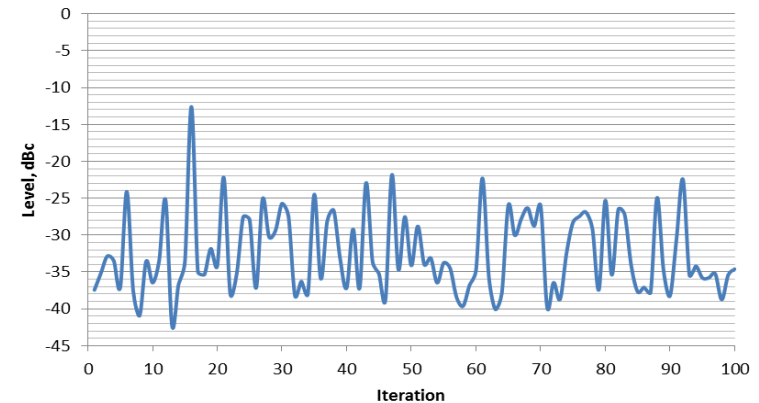
Rx Q Channel VGA2 Cal Values



Rx LPF Cal Values

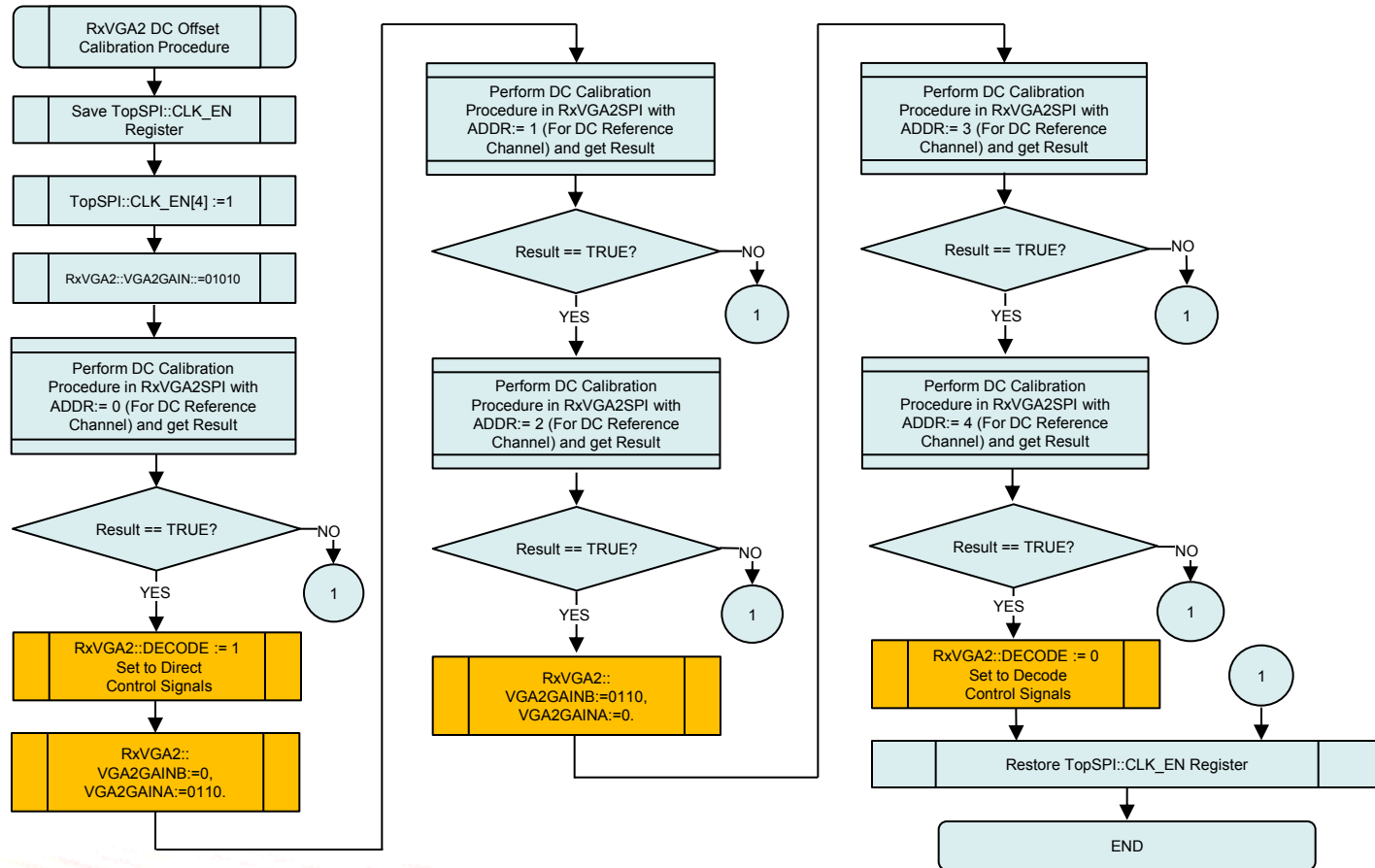


LO Leakage Level



Improved RXVGA2 Calibration Method

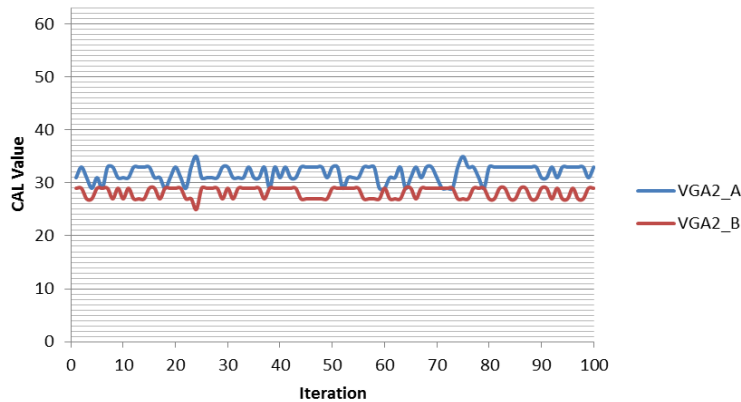
Improved Calibration Algorithm Block Diagram



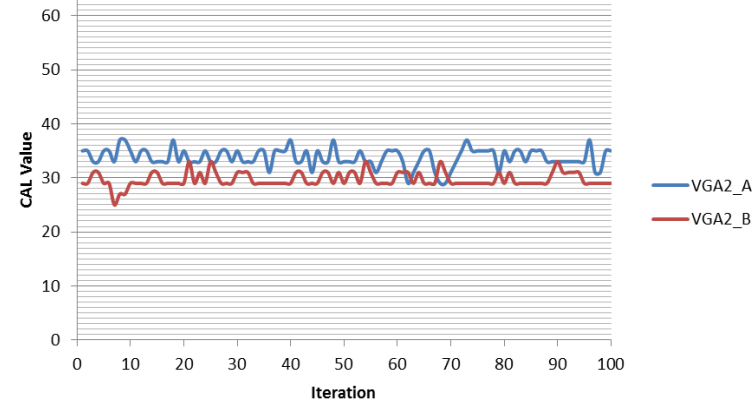
* Yellow blocks indicates the calibration algorithm modifications.

Calibration Test Results

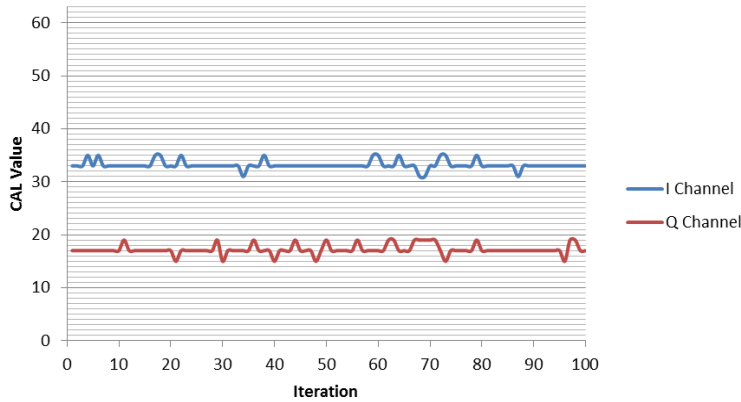
Rx Q Channel VGA2 Cal Values



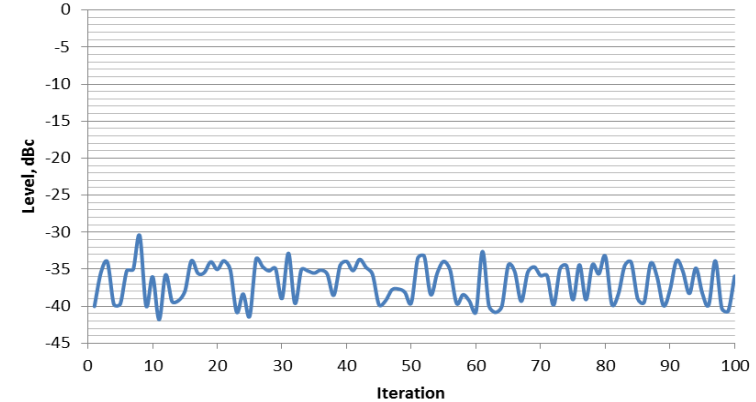
Rx I Channel VGA2 Cal Values



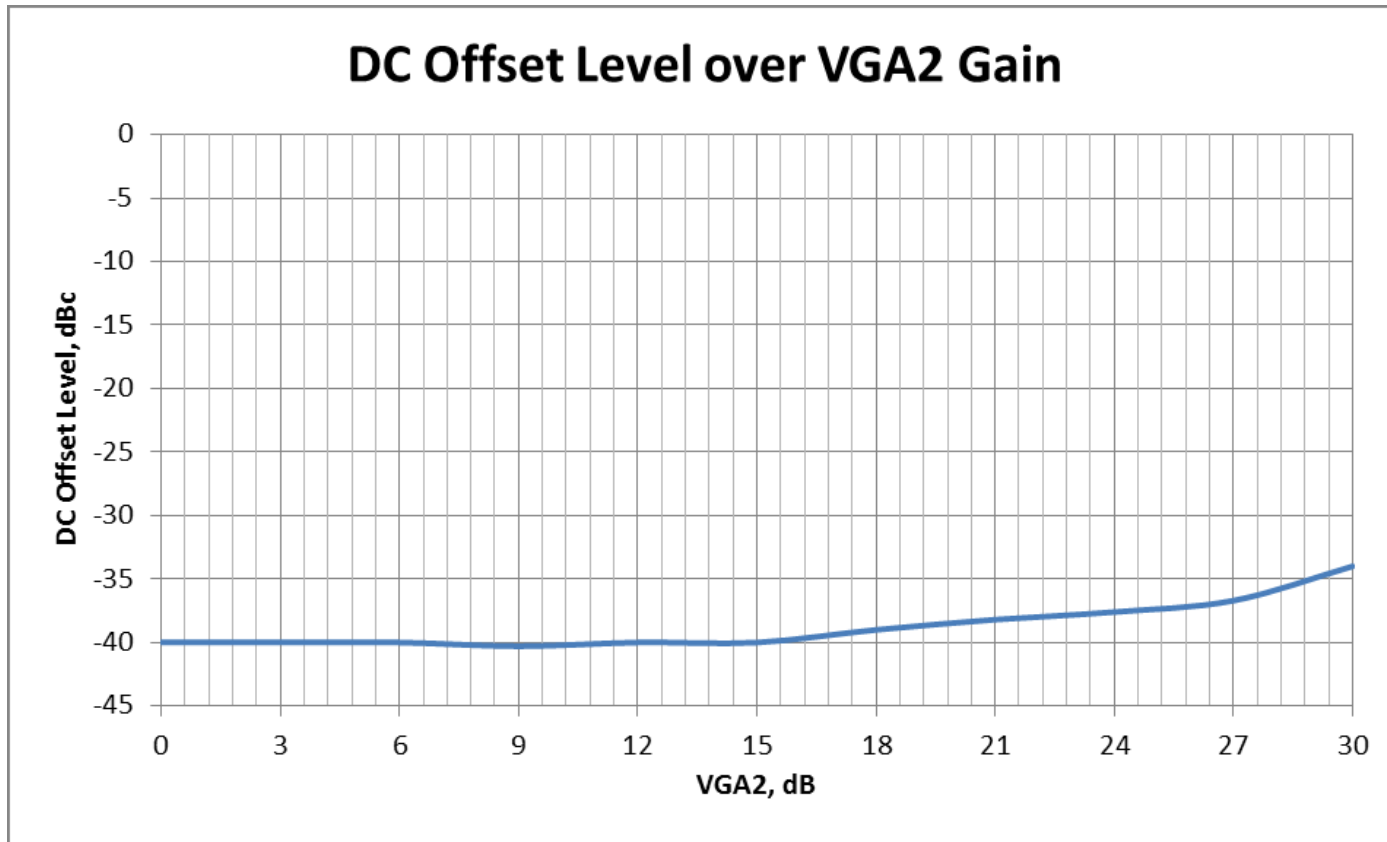
Rx LPF Cal Values



LO Leakage Level



DC Offset Level Versus RXVGA2 Gain



Conclusion

- New RXVGA2 calibration algorithm improved calibration stability. Calibration values vary $\sim \pm 2$ values over 100 iterations.
- DC offset level variation reduced using new calibration method.
- The residual DC offset has to be removed by implementing averaging filter in baseband/FPGA.

Appendix: Correcting RX I and Q DC Levels

Software in the receiver baseband is required to calibrate the DC level on the I and Q channel. The process of applying DC level adjustment to the I & Q channel is an optional requirement for fine tuning purposes only. The methodology of correcting the DC levels is shown in the diagram below.

