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# S – Parameter measurements of the LMS6002D Transceiver

## *Application Note*

| | |
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# Contents

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Corrections.

# 1

# Introduction

The LMS6002DFN is a versatile RF transceiver IC continuously covering a bandwidth of 300MHz to 3800MHz. This document provides a description of de-embedded 2-port S-parameter files provided for the design of matching networks in common RF CAD and EM simulators such as ADS, Sonnet EM and Microwave Office.

A brief description of the measurement procedure is given in Section 3. The S-parameters measurements are presented in Section 4. An example simulation demonstrating accuracy is given in Section 5. Detailed device settings used for the measurements are given in the Appendix.

## 1.1    S-parameter accuracy

Vector Network Analysers use a well defined calibration kit and procedure to ensure accuracy of S-parameter measurements at the connector of the instrument's cables. The de-embedding process can introduce errors into the derived de-embedded files. By using the de-embedded S-parameters to simulate one of the inputs of the Lime's Universal Wireless Communication Tool (UWCT) kit [1] and comparing it to measurements, we provide an evaluation of the de-embedded S-parameter accuracy.

## 1.2    Limitations of S-parameter measurements

Although de-embedded S-parameters provide a fast way to design a matching network, it does not contain any noise data for optimisation of noise and sensitivity. In designs where noise figure is critical it may be necessary to optimise the matching network component values to get the best noise figure or sensitivity. Alternatively it is possible to use one of Lime's reference designs for the best performance.

Although the RF outputs can also be described by S-parameters and are included in this report, it is not recommended for the design of the RF output. Like most power output stages, best performance is obtained through load pull rather than conjugate matching.

# 2

# Lime's De-embedded s-parameter files

## 2.1    LNA Files

All three LNAs have differential inputs.  Each port on the s2p file corresponds to one of the differential terminals.  For best results the LNAs should be matched differentially as shown in Figure 1.  Note the matching network also DC isolates the LNA from ground.
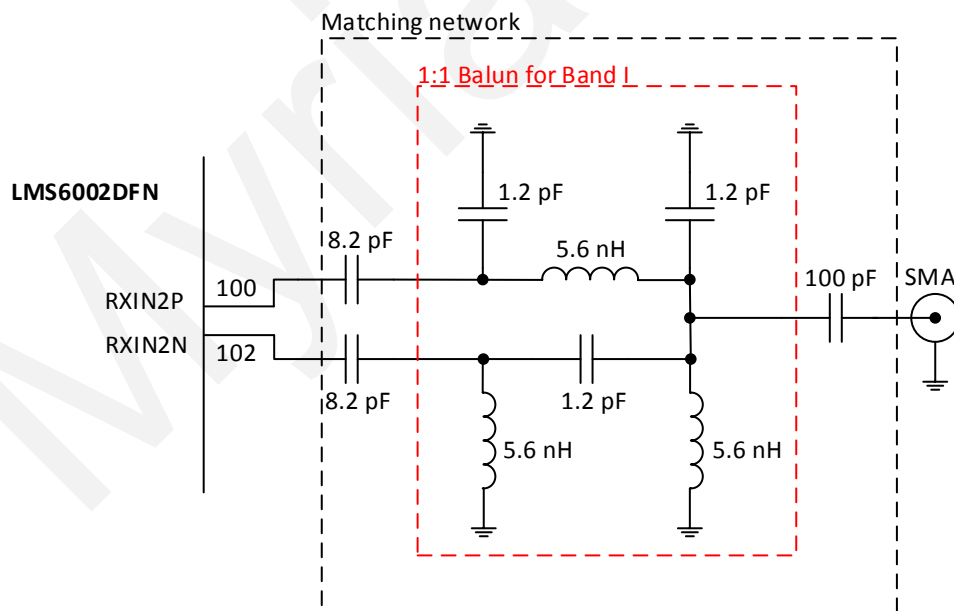


Figure 1 π-type matching network used for LNA2 matching in evaluation board

s2p files are provided for each LNA on the LMS6002DFN for a variety of gain settings. For a full list of register settings used for each file please see Appendix 1.

LNA1a.s2p (Max Gain)
LNA1b.s2p (Mid Gain)
LNA1c.s2p (Bypass)

LNA2a.s2p (Max Gain)
LNA2b.s2p (Mid Gain)
LNA2c.s2p (Bypass)

LNA3a.s2p (Max Gain)
LNA3b.s2p (Mid Gain)

The narrow band inputs, LNA1 and LNA2, are very similar, with small differences in wire bonding. LNA3 is broadband and has a different S-parameter behaviour compared to LNA1 and LNA2.

## 2.2    Mixer External Input Files

All Mixer External Inputs are differential inputs. Each port on the s2p file corresponds to one of the differential terminals. For best results the Mixer External Inputs should be matched differentially as shown in Figure 2. Note the matching network also DC isolates the mixer from ground.
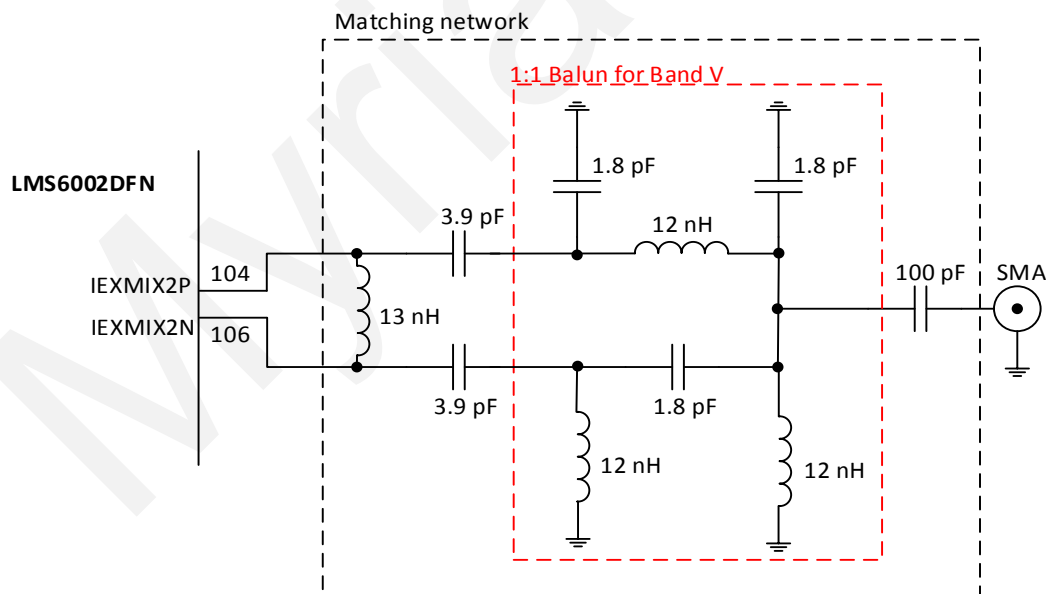


Figure 2 π-type matching network for external mixer input

ExMixa.s2p (internal termination disabled)

The two mixer external inputs are very similar with small differences in wire bonding.

## 2.3    Transmitter Output Files

All transmitter outputs are differential outputs. Each port on the s2p file corresponds to one of the differential terminals. For best results the transmitter outputs should be used differentially as shown in Figure 3. Note the output matching network also provides DC power to the output devices.
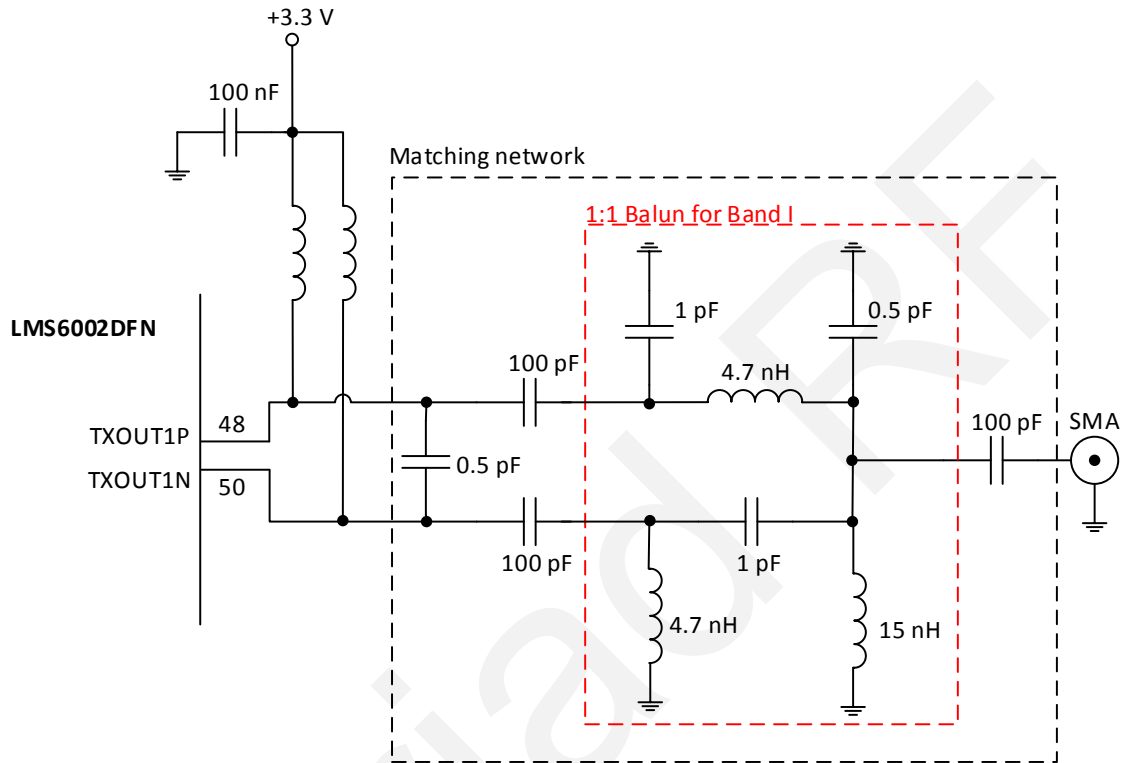


Figure 3 π-type matching network used for TXOUT1 matching in evaluation board

TX1a.s2p (Max gain, TxVGA2 set to 25 dB)
TX1b.s2p (Nominal gain, TxVGA2 set to 15 dB)
TX1c.s2p (Min gain, TxVGA2 set to 0 dB)

TX2a.s2p (Max gain, TxVGA2 set to 25 dB)
TX2b.s2p (Nominal gain, TxVGA2 set to 15 dB)
TX2c.s2p (Min gain, TxVGA2 set to 0 dB)

The two transmitter outputs are very similar with small differences in wire bonding.

# 3

# Measurements and de-embedding process

## 3.1    Measurement

A test fixture (Figure 4) was made for the characterisation of the LMS6002DFN S-parameters which included a stable low loss Rogers RO4350 layer for the RF microstrip tracks.  The test fixture also included a number of support test structures used to assist the de-embedding procedure.
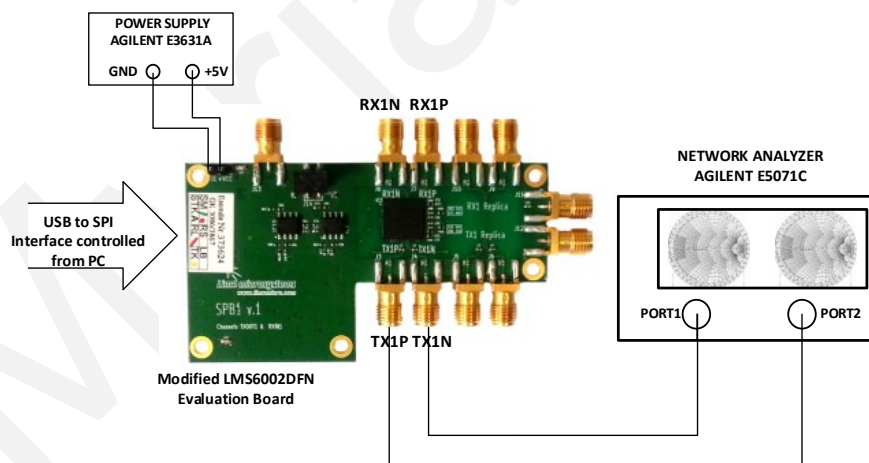


Figure 4 Network Analyzer measurement setup

2-port S-parameters measurements were made using an Agilent E5071C Vector Network Analyzer (VNA) calibrated with an automatic Short, Open, Line and Termination (SOLT) calibration kit (Agilent N4691B) over the frequency range of 10MHz to 4500MHz.

## 3.2    De-embedding process:

The de-embedding procedure removes the effects of test fixture SMA connectors, DC blocks, bias components and transmission lines from the measured S-parameter data. The de-embedding procedure was carried out in ADS.

# 4

# LMS6002DFN  S-Parameters

This section presents graphs of the de-embedded s-parameters in Figures 5 to 16.

## 4.1    LNA1 S-parameters



**m2**
freq=2.000GHz
S(3,3)=0.497 / -167.054
impedance = Z0 * (0.340 - j0.100)

**m1**
freq=1.000GHz
S(1,1)=0.659 / -93.379
impedance = Z0 * (0.374 - j0.870)

freq (10.00MHz to 4.500GHz)
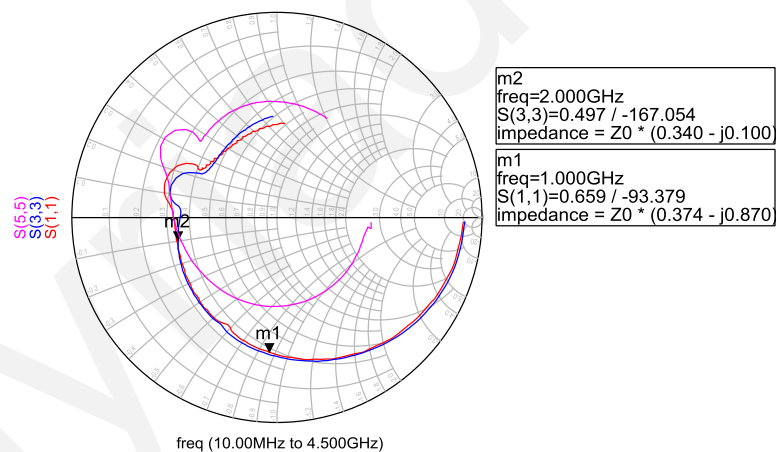
**Figure 5** LNA1 de-embedded S11 parameters. Max gain (red), Mid gain (blue line) and Bypass (magenta)
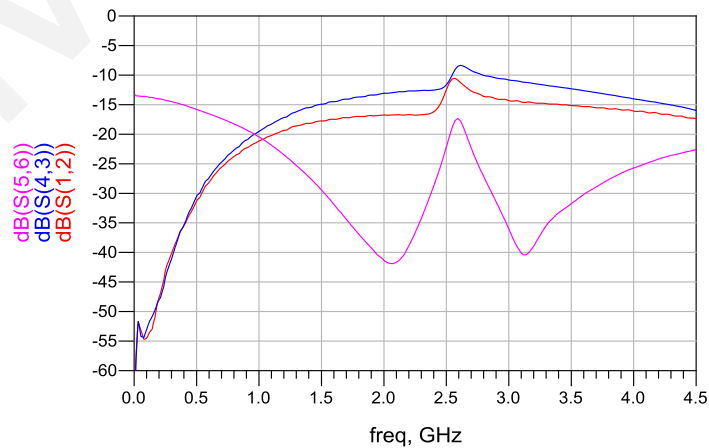


**Figure 6** LNA1 de-embedded S12. Max gain (red), Mid gain (blue) and Bypass (magenta)

## 4.2   LNA2 S-parameters



m2
freq=2.000GHz
S(3,3)=0.494 / -170.228
impedance = Z0 * (0.341 - j0.076)

m1
freq=1.000GHz
S(1,1)=0.659 / -93.379
impedance = Z0 * (0.374 - j0.870)

freq (10.00MHz to 4.500GHz)
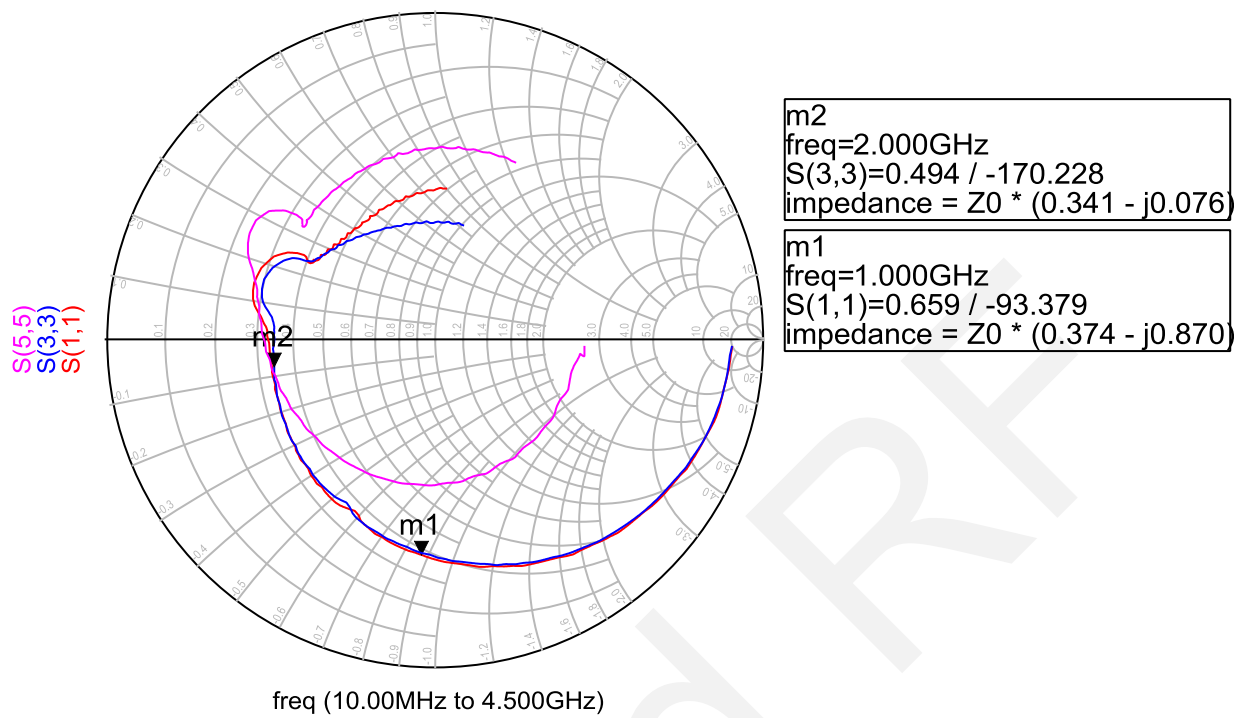
**Figure 7** LNA2 de-embedded S11 parameters. Max gain (red), Mid gain (blue) and Bypass (magenta).
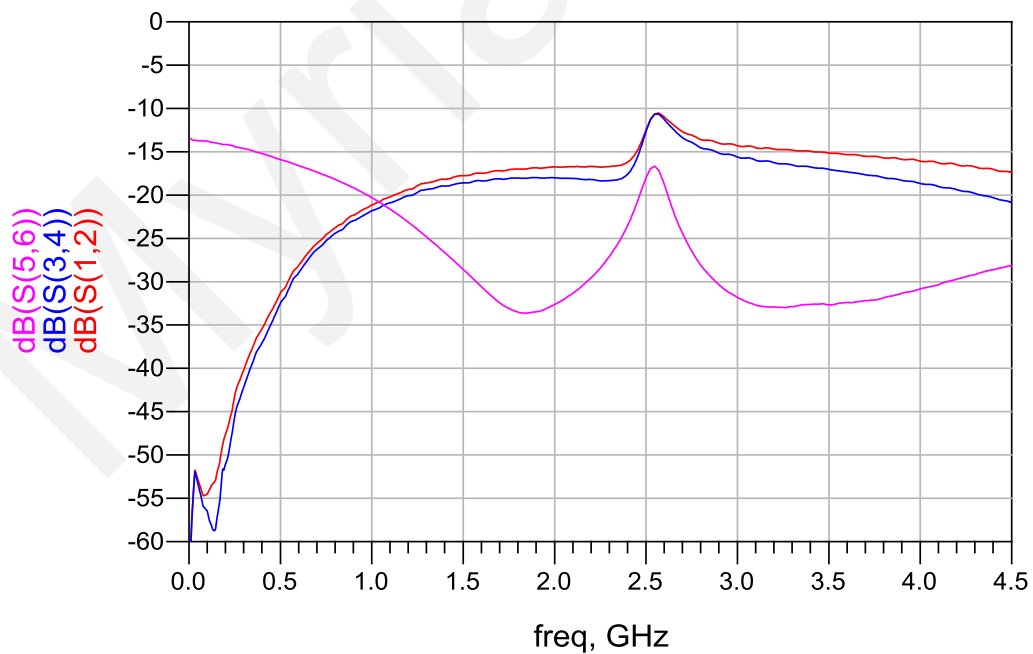


**Figure 8** LNA2 de-embedded S12. Max gain (red), Mid gain (blue) and Bypass (magenta)

## 4.3    LNA3 S-parameters



m2
freq=2.000GHz
S(3,3)=0.630 / -91.937
impedance = Z0 * (0.418 - j0.875)

m1
freq=1.000GHz
S(1,1)=0.693 / -42.010
impedance = Z0 * (1.155 - j2.058)

freq (10.00MHz to 4.500GHz)
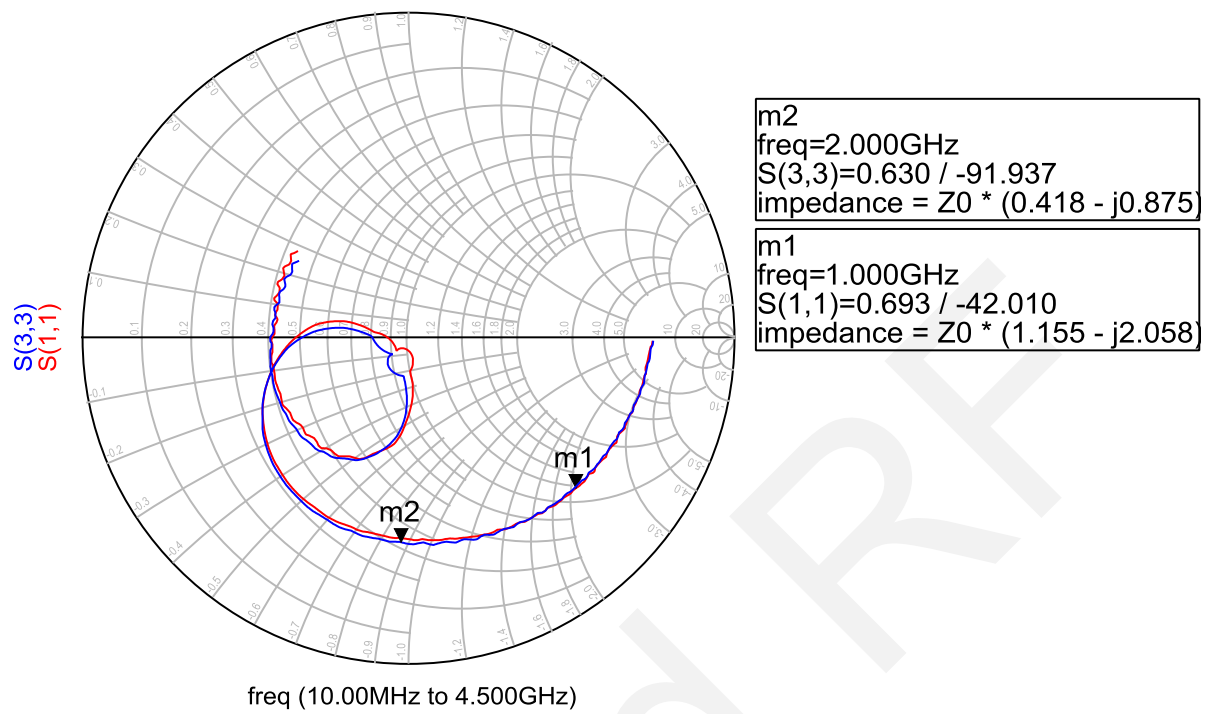
**Figure 9** LNA3 de-embedded S11 parameters. Max gain (red) and Mid gain (blue)
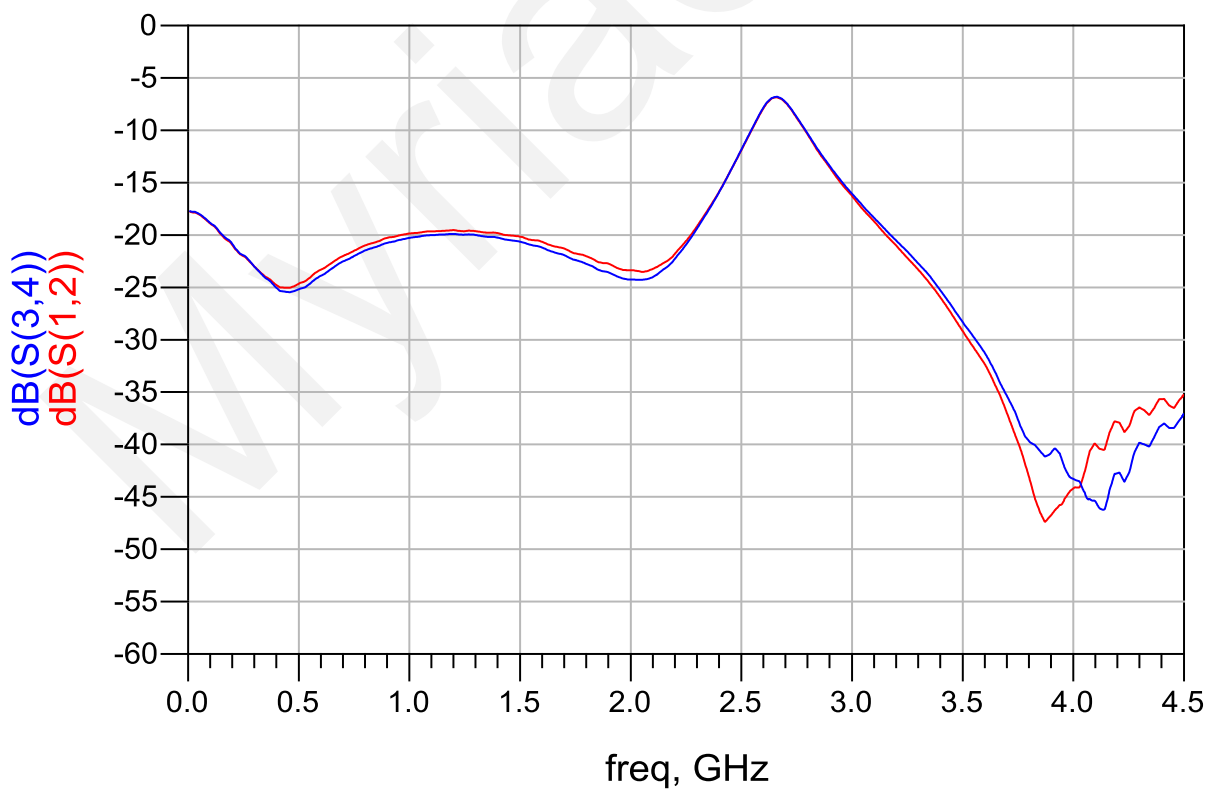


**Figure 10**  LNA3 de-embedded S12. Max gain (red) and Mid gain (blue)

## 4.4　Mixer input S-parameters



m2
freq=2.000GHz
S(3,3)=0.613 / -114.690
impedance = Z0 * (0.331 - j0.590)

m1
freq=1.000GHz
S(1,1)=0.900 / -49.778
impedance = Z0 * (0.294 - j2.122)

freq (10.00MHz to 4.500GHz)
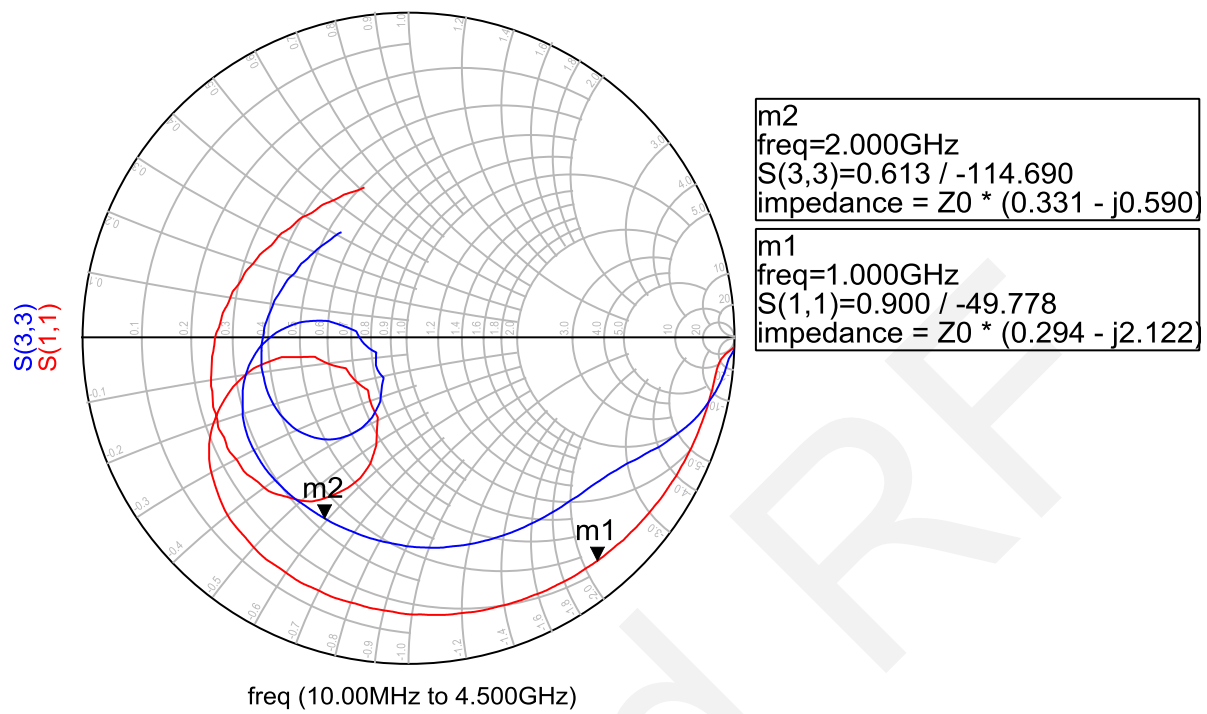
**Figure 11** Mixer input de-embedded S11 parameters. Mix input with (blue) and without (red) internal resistor termination.
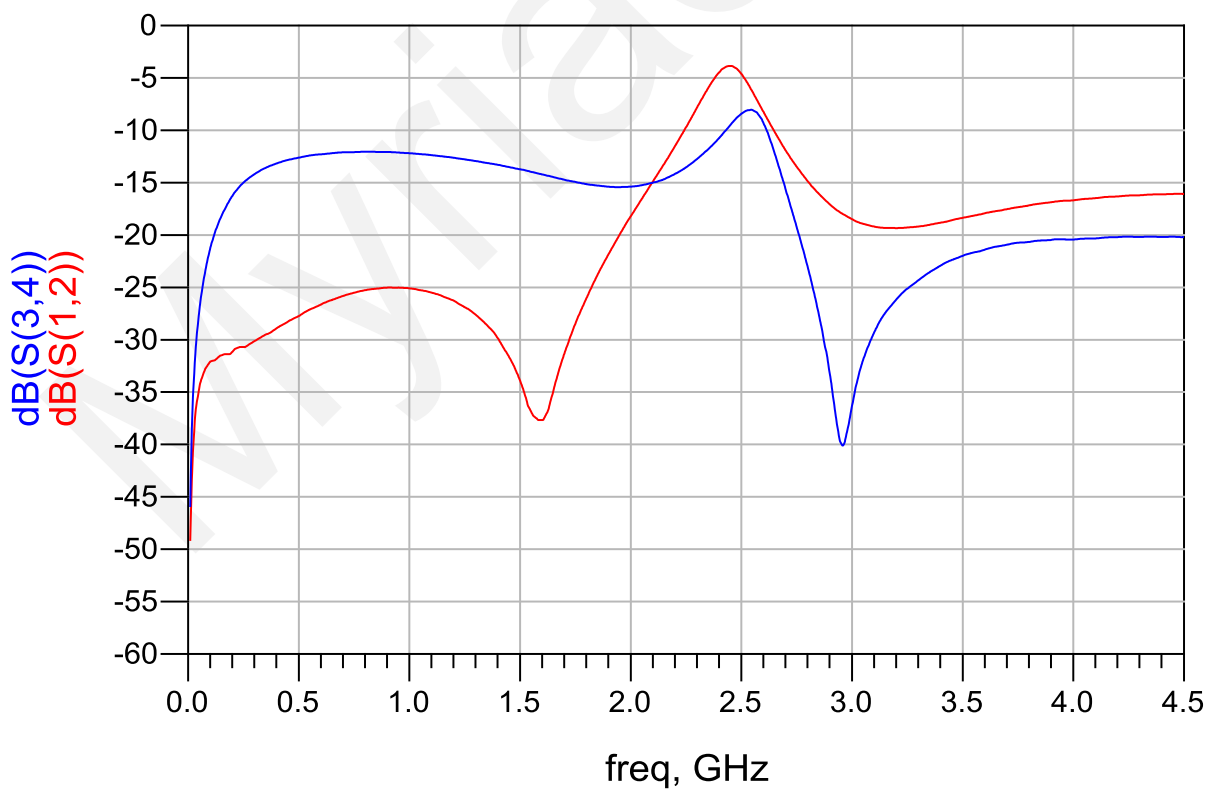


**Figure 12** LNA3 de-embedded S12. Mix input with (blue) and without (red) internal resistor termination

## 4.5   TX1 output S-parameters



m2
freq=2.000GHz
S(3,3)=0.864 / 174.025
impedance = Z0 * (0.073 + j0.052)

m1
freq=1.000GHz
S(1,1)=0.891 / -142.703
impedance = Z0 * (0.064 - j0.336)

freq (10.00MHz to 4.500GHz)
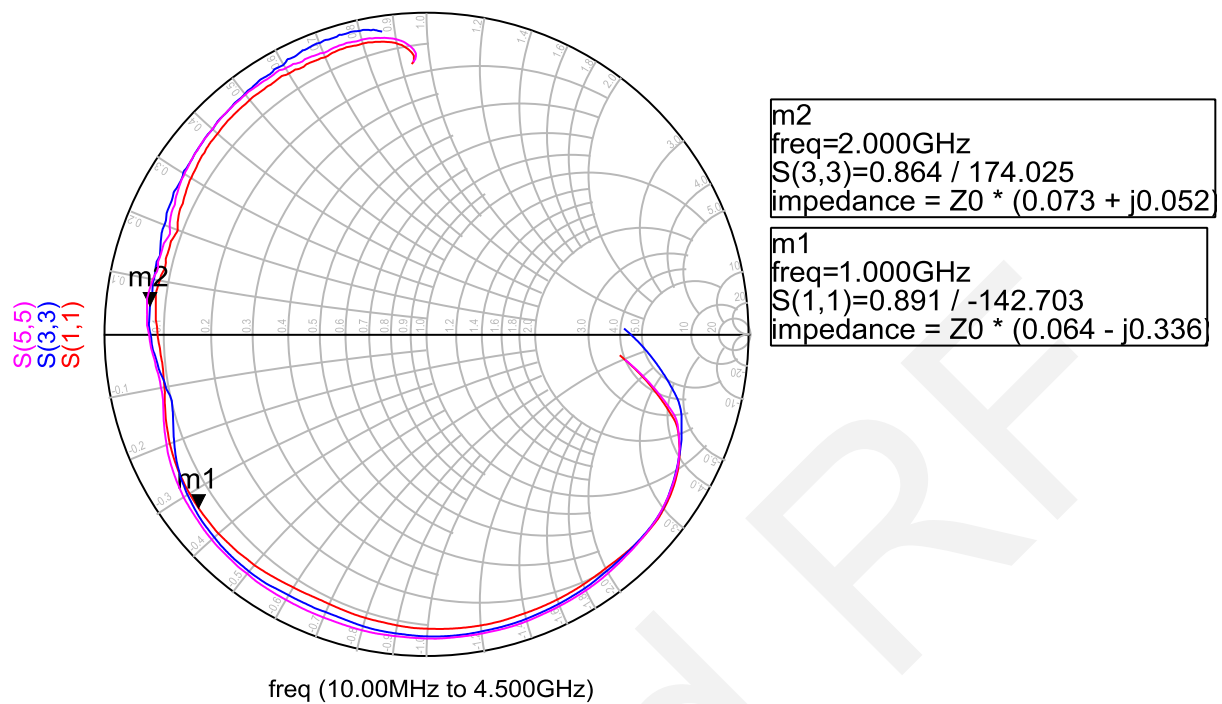
**Figure 13** TXout1 de-embedded S22. VGA2 set to 25 dB (red), VGA2 set 15 dB (blue) and VGA2 set to 0 dB (magenta)
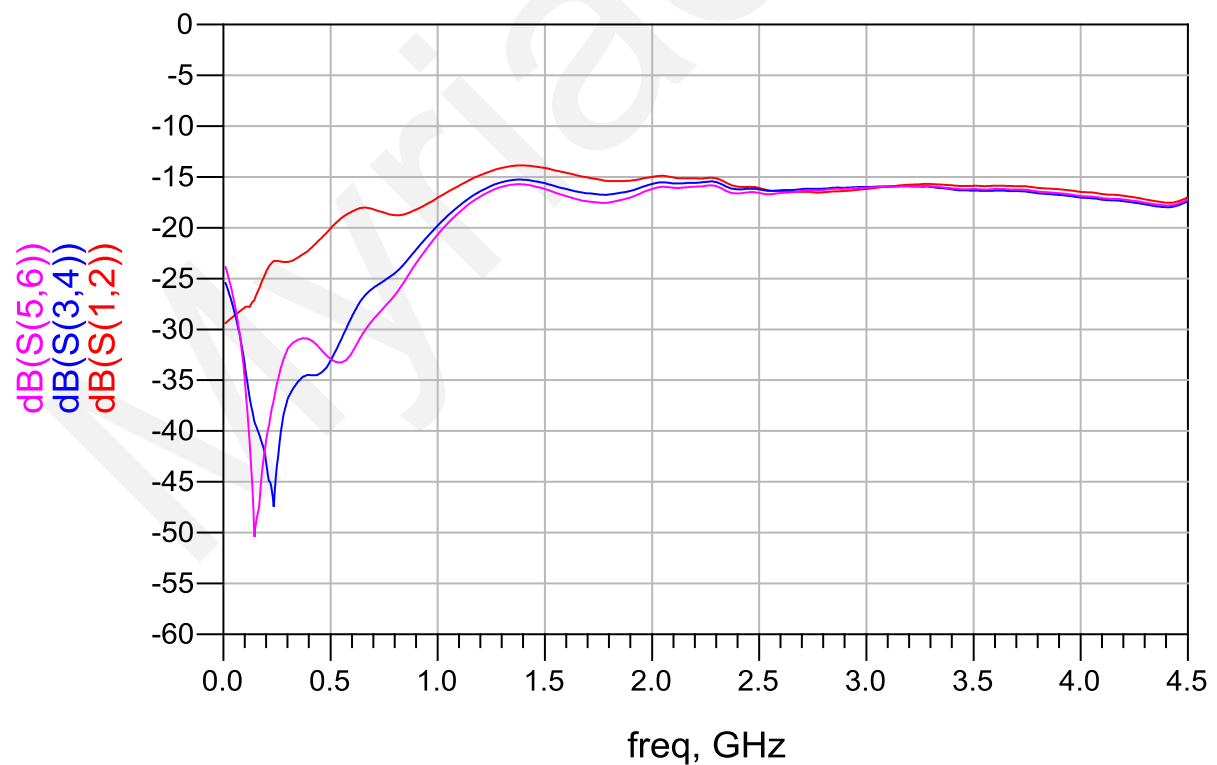


**Figure 14** TXout1 de-embedded S12. VGA2 set to 25 dB (red), VGA2 set 15 dB (blue line) and VGA2 set to 0 dB (magenta)

## 4.6　TX2 output S-parameters



m2
freq=2.000GHz
S(3,3)=0.865 / 169.561
impedance = Z0 * (0.073 + j0.091)

m1
freq=1.000GHz
S(1,1)=0.894 / -137.376
impedance = Z0 * (0.064 - j0.389)

S(5,5)
S(3,3)
S(1,1)

freq (10.00MHz to 4.500GHz)
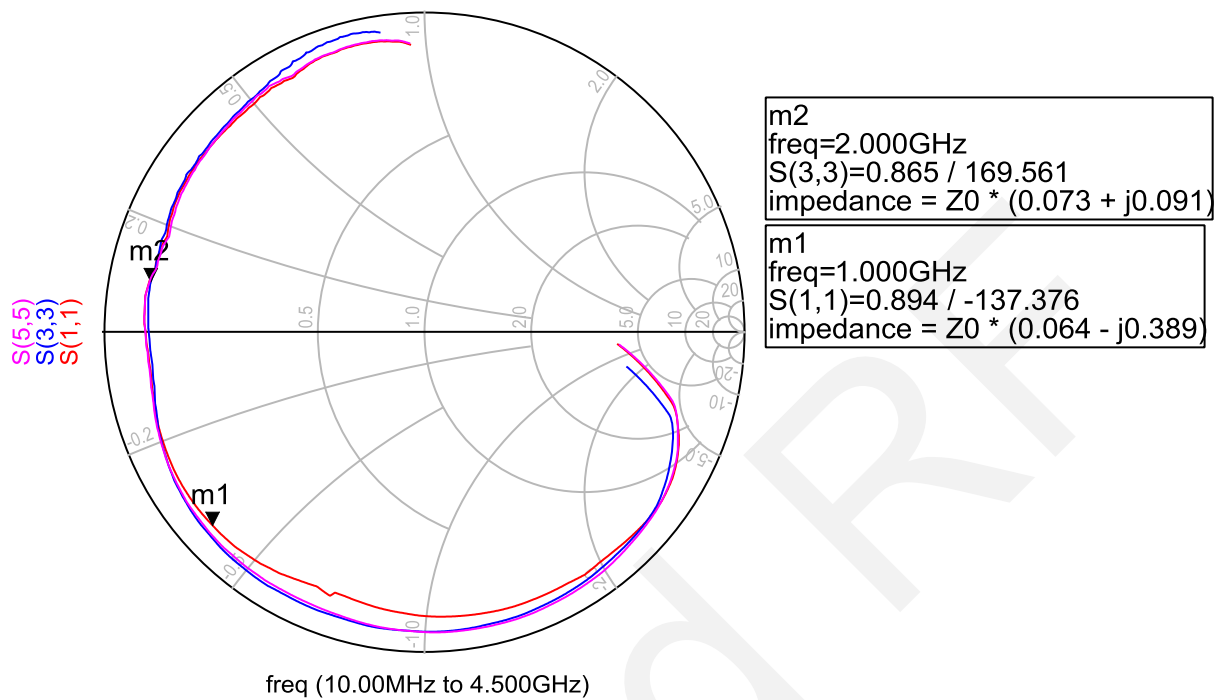
**Figure 15** TXout2 de-embedded S22. VGA2 set to 25 dB (red), VGA2 set 15 dB (blue) and VGA2 set to 0 dB (magenta).



dB(S(5,6))
dB(S(3,4))
dB(S(1,2))

freq, GHz
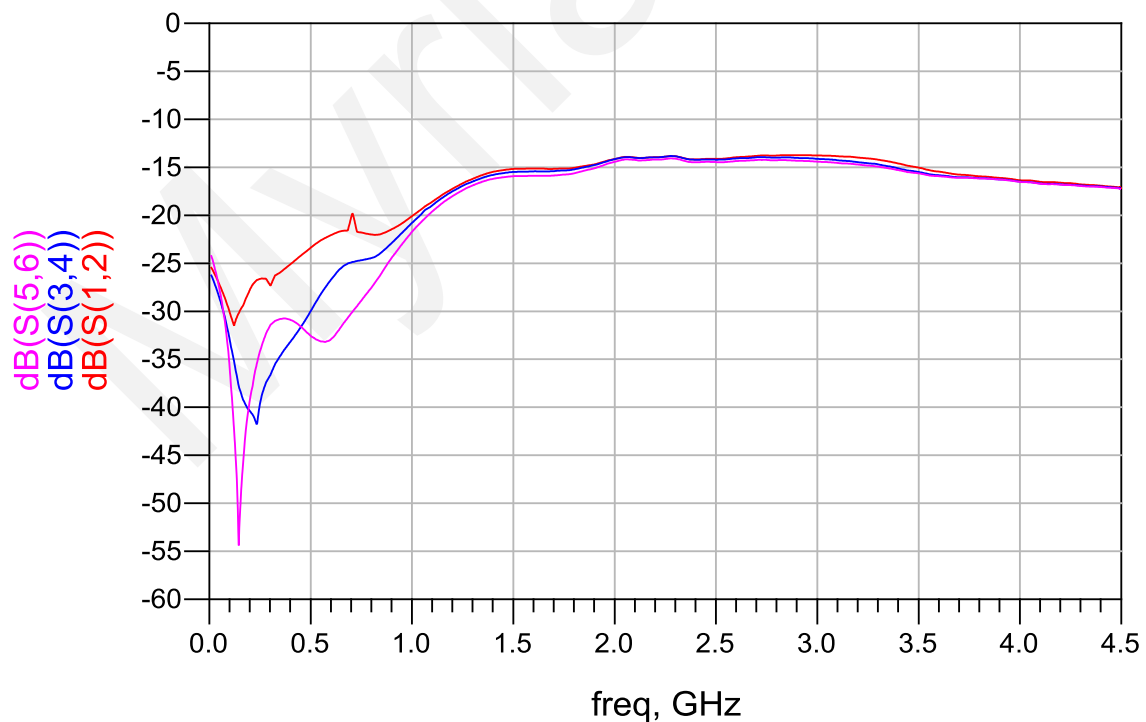
**Figure 16** TXout2 de-embedded S12. VGA2 set to 25 dB (red), VGA2 set 15 dB (blue) and VGA2 set to 0 dB (magenta)

# 5

# Lime's De-embedded s-parameter files

## 5.1    Verification

The LNA2 input of the Universal Wireless Communication Tool (UWCT) kit was used to verify measured LMS6002DFN S-parameters.

A microstrip model was made in ADS of the LNA2 port on the UWCT board.    The de-embedded S-parameters of Section 4.2 were added to represent the input port of the LMS6002DFN.   The simulated and measured 1-port S-parameters are plotted together in Figure 17.   Note that the matching network has been optimized for Band I W-CDMA sensitivity.
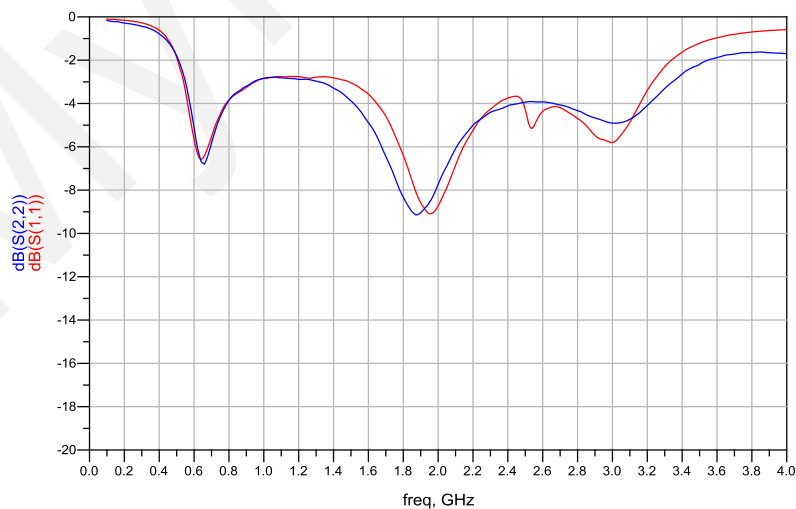


**Figure 17** LNA2 reflection coefficient (S11) simulated with de-embedded s-parameters (red) and measured (blue)

# Appendix 1

## A1.1 Register configuration for LNA1a.s2p (Max Gain)

LMS6002DFN register configuration for LNA1a.s2p are shown in Table 1.

| Top Modules | |
|---|---|
| **Register Name** | **Register Value** |
| DC_REGVAL[5:0] | Read Only |
| RCCAL_LPFCAL[2:0] | Read Only |
| DC_LOCK[2:0] | Read Only |
| DC_CLBR_DONE | Read Only |
| DC_UD | Read Only |
| DC_CNTVAL[5:0] | Read Only |
| DC_START_CLBR | |
| DC_LOAD | |
| DC_SRESET | |
| DC_ADDR[2:0] | |
| VER[3:0] | Read Only |
| REV[3:0] | Read Only |
| DECODE | User Mode |
| SRESET | Inactive |
| EN | Enabled |
| STXEN | Powered Down |
| SRXEN | Enabled |
| TFWMODEA | 4 Wire |
| CLKSEL_LPFCAL | PLL Reference |
| PD_CLKLPFCAL | Powered Down |
| ENF_EN_CAL_LPFCAL | Enforce Mode Disabled |
| RST_CAL_LPFCAL | Reset State |
| EN_CAL_LPFCAL | Disabled |
| FORCE_CODE_CAL_LPFCAL[2:0] | 0X0 |
| BWC_LPFCAL[3:0] | 14MHz |
| BBBYP_RX | Disabled |
| LBEN_LPFIN_RX | Disabled |

| | |
|---|---|
| LBEN_VGA2IN_RX | Disabled |
| LBEN_OPIN_RX | Disabled |
| LBRFEN_RXFE[3:0] | Disabled |
| CLKSEL_LPFCAL | Closed (on) |
| CLK_EN[6] | PLLCLKOUT Disabled |
| CLK_EN[5] | LPF CALCORE Clk Disabled |
| CLK_EN[4] | Rx VGA2 DCCLK Disabled |
| CLK_EN[3] | Rx LPF DCCLK Disabled |
| CLK_EN[2] | Rx DSM SPI Enabled |
| CLK_EN[1] | Tx LPF DCCLK Disabled |
| CLK_EN[0] | Tx DSM SPI Disabled |
| FDDTDD | FDD |
| TDDMOD | Transmit |
| PDXCOBUF | XCO buffer powered up |
| SLFBXCOBUF | XCO buffer self bias enabled |
| BYPXCOBUF | XCO buffer active |
| PD[1] | PD_DCOREF_LPFCAL powered up |
| PD[0] | RF loop back switch powered down |
| **RxPLL Modules** | |
| **Register Name** | **Register Name Value** |
| NINT[8:0] | 126 |
| NFRAC[22:0] | 7995392 |
| DITHEN | Enabled |
| DITHN[2:0] | 0X1Bit(s) |
| EN | Enabled |
| AUTOBYP | Enabled |
| DECODE | User Mode |
| MODE | Fractional Mode |
| SELVCO[2:0] | Low Frequency |
| FRANGE[2:0] | Fvco/2 |
| SELOUT[1:0] | First |
| EN_PFD_UP | Enabled |
| OEN_TSTD_SX | Disabled |
| PASSEN_TSTOD_SD | Disabled |
| ICHP[4:0] | 1200 uA |
| BYPVCOREG | Bypassed |
| PDVCOREG | Powered Down |
| FSTVCOBG | Resistor Shorted |
| OFFUP[4:0] | 30uA |
| VOVCOREG[3:0] | 1.9V |
| OFFDOWN[4:0] | 0 uA |
| VCOCAP[5:0] | 15 |
| VTUNE_H | Read Only |
| VTUNE_L | Read Only |
| BCODE[5:0] | 12 |

| | |
|---|---|
| ACODE[3:0] | 0 |
| PD_VCOCOMP_SX | Enabled |
| ENLOBUF | Enabled |
| ENLAMP | Enabled |
| TRI | Normal Mode |
| POL | Normal |
| PFDPD | Enabled |
| ENFEEDDIV | Enabled |
| ENFEEDDIV | Inverted |
| BCLKSEL[1:0] | Feedback Div Out |
| BINSEL | NINT/NFRAC |
| BSTART | Read Only |
| BSTATE | Read Only |
| BSIG[22:16] | Read Only |
| BSIG[15:8] | Read Only |
| BSIG[7:0] | Read Only |
| **RxLPF Modules** | |
| **Register Name** | **Register Name Value** |
| DC_REGVAL[5:0] | Read Only |
| DC_LOCK[2:0] | Read Only |
| DC_CLBR_DONE | Read Only |
| DC_UD | Read Only |
| DC_CNTVAL[5:0] | Read Only |
| DC_START_CLBR | |
| DC_LOAD | |
| DC_SRESET | |
| DC_ADDR[2:0] | |
| BWC_LPF[3:0] | 14 MHz |
| EN | Enabled |
| DECODE | User Mode |
| BYP_EN_LPF | Normal Operation |
| DCO_DACCAL_LPF[5:0] | 0X1F |
| RCCAL_LPF[2:0] | 0X3 |
| PD_DCOCMP_LPF | DC Offset Comparator powered up |
| PD_DCODAC_LPF | DC Offset DAC powered up |
| PD_DCOREF_LPF | DC DAC Reference powered up |
| PD_FIL_LPF | LPF powered up |
| **RxVGA2 Modules** | |
| **Register Name** | **Register Value** |
| DC_REGVAL[5:0] | Read Only |
| DC_LOCK[2:0] | Read Only |
| DC_CLBR_DONE | Read Only |
| DC_UD | Read Only |
| DC_CNTVAL[5:0] | Read Only |
| DC_START_CLBR | |

| | |
|---|---|
| DC_LOAD | |
| DC_SRESET | |
| DC_ADDR[2:0] | |
| VCM[3:0] | 12 |
| EN | Enabled |
| DECODE | User Mode |
| MIXVGA2GAIN[4:0] | 3 dB |
| PD[9] | DC Current Regulator powered up |
| PD[8] | VGA2B DC Cal. DAC powered up |
| PD[7] | VGA2B DC Cal. Comp. powered up |
| PD[6] | VGA2A DC Cal. DAC powered up |
| PD[5] | VGA2A DC Cal. Comp. powered up |
| PD[4] | Band Gap powered up |
| PD[3] | Bypass Both VGAs powered up |
| PD[2] | Bypass VGA2B powered up |
| PD[1] | Bypass VGA2A powered up |
| PD[0] | Current Reference powered up |
| VGA2GAINB[3:0] | 0 dB |
| VGA2GAINA[3:0] | 3 dB |
| **RxFE Modules** | |
| **Register Name** | **Register Value** |
| DECODE | User Mode |
| EN | Enabled |
| IN1SEL_MIX_RXFE | To LNA Out |
| DCOFF_I_RXFE[6:0] | 0X7F |
| INLOAD_LNA_RXFE | Internal Load Active |
| DCOFF_Q_RXFE[6:0] | 0X7F |
| XLOAD_LNA_RXFE | External Load Disabled |
| IP2TRIM_I_RXFE[6:0] | 0X7F |
| IP2TRIM_Q_RXFE[6:0] | 0X7F |
| G_LNA_RXFE[1:0] | Max Gain |
| LNASEL_RXFE[1:0] | LNA 1 |
| CBE_LNA_RXFE[3:0] | 0X0 |
| RFB_TIA_RXFE[6:0] | 0X78 |
| CFB_TIA_RXFE[6:0] | 0X0 |
| RDLEXT_LNA_RXFE[5:0] | 0X1C |
| RDLINT_LNA_RXFE[5:0] | 0X37 |
| ICT_MIX_RXFE[3:0] | 0X7 |
| ICT_LNA_RXFE[3:0] | 0X7 |
| ICT_TIA_RXFE[3:0] | 0X7 |
| ICT_MXLOB_RXFE[3:0] | 0X7 |
| LOBN_MIX_RXFE[3:0] | 0X3 |
| RINEN_MIX_RXFE | Inactive |
| G_FINE_LNA3_RXFE[1:0] | +0 dB |
| PD_TIA_RXFE | TIA powered up |

| | |
|---|---|
| PD_MXLOB_RXFE | MXLOB powered up |
| PD_MIX_RXFE | MIX powered up |
| PD_LNA_RXFE | LNA powered up |
| **ADDC Modules** | |
| **Register Name** | **Register Value** |
| EN | Enabled |
| DECODE | User Mode |
| DAC Internal Out Load Resistor | 200 Ohms |
| DAC Ref Current Resistor | External |
| DAC Full Scale Output Control | 5 mA |
| Reference Bias Resistor Adjust | 20uA |
| Reference Bias UP | 1.0X |
| Reference Bias Down | 0 |
| Reference Gain Adjust | 1.50V |
| Common Mode Adjust | 960mV |
| Reference Buffer Boost | 1.0X |
| Input Buffer Disable | Disabled |
| Rx Fsync Polarity, frame start | 0 |
| Rx Interleave Mode | I, Q |
| DAC Clk Edge Polarity | Neg |
| Tx Fsync Polarity, frame start | 0 |
| Tx Interleave Mode | I, Q |
| ADC Sampling Phase | Rising Edge |
| Clock Non-Overlap Adjust | Nominal |
| ADC Bias Resistor Adjust | 20uA |
| Main Bias Down | 0 (Nom) |
| ADC Amp1 Stage1 Bias Up | 20uA |
| ADC Amp2-4 Stage1 Bias Up | 20uA |
| ADC Amp1 Stage2 Bias Up | 20uA |
| ADC Amp2-4 Stage2 Bias Up | 20uA |
| Quantizer Bias Up | 20uA |
| Input Buffer Bias Up | 20uA |
| Bandgap Temperature Coeff | 0 (Nom) |
| Bandgap Gain Control | 0 (Nom) |
| Reference Amps Bias Adjust | 20uA |
| Reference Amps Bias UP | 1.0X |
| Reference Amps Bias Down | 0 |
| Enable DAC | Enabled |
| Enable ADC1 (I Channel) | Enabled |
| Enable ADC2 (Q Channel) | Enabled |
| Enable ADC Reference | Enabled |
| Enable Master Reference | Enabled |

Table 1 LMS6002DFN register configuration for LNA1a.s2p (Max Gain)

## A1.2 Register configuration for LNA1b.s2p (Mid Gain)

The same as Table 1, except the Register values shown in Table 2.

| RxFE Modules | |
|---|---|
| **Register Name** | **Register Value** |
| G_LNA_RXFE[1:0] | Mid Gain |

Table 2 Modified register values for LNA1b.s2p (Mid Gain)

## A1.3 Register configuration for LNA1c.s2p (Bypass)

The same as Table 1, except the Register values shown in Table 3.

| RxFE Modules | |
|---|---|
| **Register Name** | **Register Value** |
| G_LNA_RXFE[1:0] | Bypass |

Table 3 Modified register values for LNA1c.s2p (Bypass)

## A1.4 Register configuration for LNA2a.s2p (Max Gain)

The same as Table 1, except the Register values shown in Table 4.

| RxPLL Modules | |
|---|---|
| **Register Name** | **Register Value** |
| SELOUT[1:0] | Second |
| **RxFE Modules** | |
| **Register Name** | **Register Value** |
| LNASEL_RXFE[1:0] | LNA 2 |

Table 4 Modified register values for LNA2a.s2p (Max Gain)

## A1.5 Register configuration for LNA2b.s2p (Mid Gain)

The same as Table 1, except the Register values shown in Table 5.

| RxPLL Modules | |
|---|---|
| **Register Name** | **Register Value** |
| SELOUT[1:0] | Second |
| **RxFE Modules** | |
| **Register Name** | **Register Value** |

| | |
|---|---|
| LNASEL_RXFE[1:0] | LNA 2 |
| G_LNA_RXFE[1:0] | Mid Gain |

Table 5 Modified register values for LNA2b.s2p (Mid Gain)

## A1.6 Register configuration for LNA2c.s2p (Bypass)

The same as Table 1, except the Register values shown in Table 6.

| RxPLL Modules | |
|---|---|
| **Register Name** | **Register Value** |
| SELOUT[1:0] | Second |
| **RxFE Modules** | |
| **Register Name** | **Register Value** |
| LNASEL_RXFE[1:0] | LNA 2 |
| G_LNA_RXFE[1:0] | Bypass |

Table 6 Modified register values for LNA2c.s2p (Bypass)

## A1.7 Register configuration for LNA3a.s2p (Max Gain)

The same as Table 1, except the Register values shown in Table 7.

| RxPLL Modules | |
|---|---|
| **Register Name** | **Register Value** |
| SELOUT[1:0] | Third |
| **RxFE Modules** | |
| **Register Name** | **Register Value** |
| LNASEL_RXFE[1:0] | LNA 3 |

Table 7 Modified register values for LNA3a.s2p (Max Gain)

## A1.8 Register configuration LNA3b.s2p (Mid Gain)

The same as Table 1, except the Register values shown in Table 8.

| RxPLL Modules | |
|---|---|
| **Register Name** | **Register Value** |
| SELOUT[1:0] | Third |
| **RxFE Modules** | |
| **Register Name** | **Register Value** |
| LNASEL_RXFE[1:0] | LNA 3 |
| G_LNA_RXFE[1:0] | Bypass |

Table 8 Modified register values for  LNA3b.s2p (Mid Gain)

## A1.9 Register configuration for ExMixa.s2p (internal termination disabled)

The same as Table 1, except the Register values shown in Table 10.

| RxPLL Modules | |
|---|---|
| **Register Name** | **Register Value** |
| SELOUT[1:0] | Second |
| **RxFE Modules** | |
| **Register Name** | **Register Value** |
| LNASEL_RXFE[1:0] | LNA 2 |
| IN1SEL_MIX_RXFE | To LNA Out |

Table 9 Modified register values for ExMixa.s2p (internal termination disabled)

## A1.10 Register configuration for ExMixa_Term.s2p (internal termination Enabled)

The same as Table 1, except the Register values shown in Table 10.

| RxPLL Modules | |
|---|---|
| **Register Name** | **Register Value** |
| SELOUT[1:0] | Second |
| **RxFE Modules** | |
| **Register Name** | **Register Value** |
| LNASEL_RXFE[1:0] | LNA 2 |
| IN1SEL_MIX_RXFE | To LNA Out |
| RINEN_MIX_RXFE | Active |

Table 10 Modified registers values for ExMixa_Term.s2p (internal termination Enabled)

## A1.11 Register configuration for TX1a.s2p (Max gain, TxVGA2 set to 25 dB)

LMS6002DFN register configuration for TX1a.s2p is shown in Table 111.

| TopModules | |
|---|---|
| **Register Name** | **Register Value** |
| DC_REGVAL[5:0] | ReadOnly |
| RCCAL_LPFCAL[2:0] | ReadOnly |
| DC_LOCK[2:0] | ReadOnly |
| DC_CLBR_DONE | ReadOnly |
| DC_UD | ReadOnly |

| | |
|---|---|
| DC_CNTVAL[5:0] | ReadOnly |
| DC_START_CLBR | |
| DC_LOAD | |
| DC_SRESET | |
| DC_ADDR[2:0] | |
| VER[3:0] | ReadOnly |
| REV[3:0] | ReadOnly |
| DECODE | UserMode |
| SRESET | Inactive |
| EN | Enabled |
| STXEN | Enabled |
| SRXEN | PoweredDown |
| TFWMODEA | 4Wire |
| CLKSEL_LPFCAL | PLLReference |
| PD_CLKLPFCAL | PoweredDown |
| ENF_EN_CAL_LPFCAL | EnforceModeDisabled |
| RST_CAL_LPFCAL | ResetState |
| EN_CAL_LPFCAL | Disabled |
| FORCE_CODE_CAL_LPFCAL[2:0] | 0X0 |
| BWC_LPFCAL[3:0] | 14MHz |
| BBBYP_RX | Disabled |
| LBEN_LPFIN_RX | Disabled |
| LBEN_VGA2IN_RX | Disabled |
| LBEN_OPIN_RX | Disabled |
| LBRFEN_RXFE[3:0] | Disabled |
| CLKSEL_LPFCAL | Closed(on) |
| CLK_EN[6] | PLLCLKOUTDisabled |
| CLK_EN[5] | LPFCALCOREClkDisabled |
| CLK_EN[4] | RxVGA2DCCLKDisabled |
| CLK_EN[3] | RxLPFDCCLKDisabled |
| CLK_EN[2] | RxDSMSPIDisabled |
| CLK_EN[1] | TxLPFDCCLKDisabled |
| CLK_EN[0] | TxDSMSPIEnabled |
| FDDTDD | FDD |
| TDDMOD | Transmit |
| PDXCOBUF | XCObufferpoweredup |
| SLFBXCOBUF | XCObufferselfbiasenabled |
| BYPXCOBUF | XCObufferactive |
| PD[1] | PD_DCOREF_LPFCALpoweredup |
| PD[0] | RFloopbackswitchpowereddown |
| **TxLPFModules** | |
| **Register Name** | **Register Value** |
| DC_REGVAL[5:0] | ReadOnly |
| DC_LOCK[2:0] | ReadOnly |
| DC_CLBR_DONE | ReadOnly |

| | |
|---|---|
| DC_UD | ReadOnly |
| DC_CNTVAL[5:0] | ReadOnly |
| DC_START_CLBR | |
| DC_LOAD | |
| DC_SRESET | |
| DC_ADDR[2:0] | |
| BWC_LPF[3:0] | 14MHzMHz |
| EN | Enabled |
| DECODE | UserMode |
| BYP_EN_LPF | NormalOperation |
| DCO_DACCAL_LPF[5:0] | 0X1F |
| TX_DACBUF_EN | TXDACBufferspoweredup |
| RCCAL_LPF[2:0] | 0X3 |
| PD_DCOCMP_LPF | DCOffsetComparatorpoweredup |
| PD_DCODAC_LPF | DCOffsetDACpoweredup |
| PD_DCOREF_LPF | DCDACReferencepoweredup |
| PD_FIL_LPF | LPFpoweredup |
| **TxRFModules** | |
| **Register Name** | **Register Value** |
| EN | Enabled |
| DECODE | UserMode |
| VGA1GAIN[4:0] | -14dB |
| VGA1DC_I[7:0] | 0mV |
| VGA1DC_Q[7:0] | 0mV |
| VGA2PA | PA1Selected |
| PD_DRVAUX | PoweredDown |
| PD_PKDET | PoweredDown |
| VGA2GAIN[4:0] | 25dB |
| ENVD[2] | ReferenceDC |
| ENVD[1:0] | AUXPAEDoutput |
| PKDBW[3:0] | 0 |
| LOOPBBEN[1:0] | SwitchesOpen |
| FST_PKDET | Switchopen |
| FST_TXHFBIAS | Switchopen |
| ICT_TXLOBUF[3:0] | 4 |
| VBCAS_TXDRV[3:0] | 0 |
| ICT_TXMIX[4:0] | 12 |
| ICT_TXDRV[4:0] | 12 |
| PW_VGA1_I | VGA1Ipoweredup |
| PW_VGA1_Q | VGA1Qpoweredup |
| PD_TXDRV | PA1,PA2,AUXPAEnabled |
| PD_TXLOBUF | TxLOBUFEnabled |
| PD_TXMIX | MIXandVGA2poweredup |
| VGA1GAINT[7:0] | -14dB |
| G_TXVGA2[8:0] | 0 |

Table 11 Register configuration for TX path

## A1.12  Register configuration for TX1b.s2p (Nominal gain, TxVGA2 set to 15 dB)

The same as Table 1, except the Register values shown in Table 12.

| TxFE Modules | |
|---|---|
| **Register Name** | **Register Value** |
| VGA2GAIN[4:0] | 15dB |

Table 12 Modified register values for TX1b.s2p (Nominal gain, TxVGA2 set to 15 dB)

## A1.13  Register configuration for TX1c.s2p (Min gain, TxVGA2 set to 0 dB)

The same as Table 1, except the Register values shown in Table 13.

| TxFE Modules | |
|---|---|
| **Register Name** | **Register Value** |
| VGA2GAIN[4:0] | 0 dB |

Table 13 Modified register values for TX1c.s2p (Min gain, TxVGA2 set to 0 dB)

## A1.14  Register configuration for TX2a.s2p (Max gain, TxVGA2 set to 25 dB)

The same as Table 1, except the Register values shown in Table 14.

| TxFE Modules | |
|---|---|
| **Register Name** | **Register Value** |
| VGA2PA | PA2Selected |

Table 14 Modified register values for TX2a.s2p (Max gain, TxVGA2 set to 25 dB)

## A1.15  Register configuration for TX2b.s2p (Nominal gain, TxVGA2 set to 15 dB)

The same as Table 1, except the Register values shown in Table 15.

| TxFE Modules | |
|---|---|
| **Register Name** | **Register Value** |
| VGA2PA | PA2Selected |
| VGA2GAIN[4:0] | 15 dB |

Table 15 Modified register values for TX2b.s2p (Nominal gain, TxVGA2 set to 15 dB)

## A1.16 Register configuration for TX2c.s2p (Min gain, TxVGA2 set to 0 dB)

The same as Table 1, except the Register values shown in Table 16.

| TxFE Modules | |
| --- | --- |
| **Register Name** | **Register Value** |
| VGA2PA | PA2Selected |
| VGA2GAIN[4:0] | 0 dB |

Table 16 Modified register values for TX2c.s2p (Min gain, TxVGA2 set to 0 dB)

# References

[1]  http://www.limemicro.com/products/wireless_comms_toolkit.php?sector=consumer