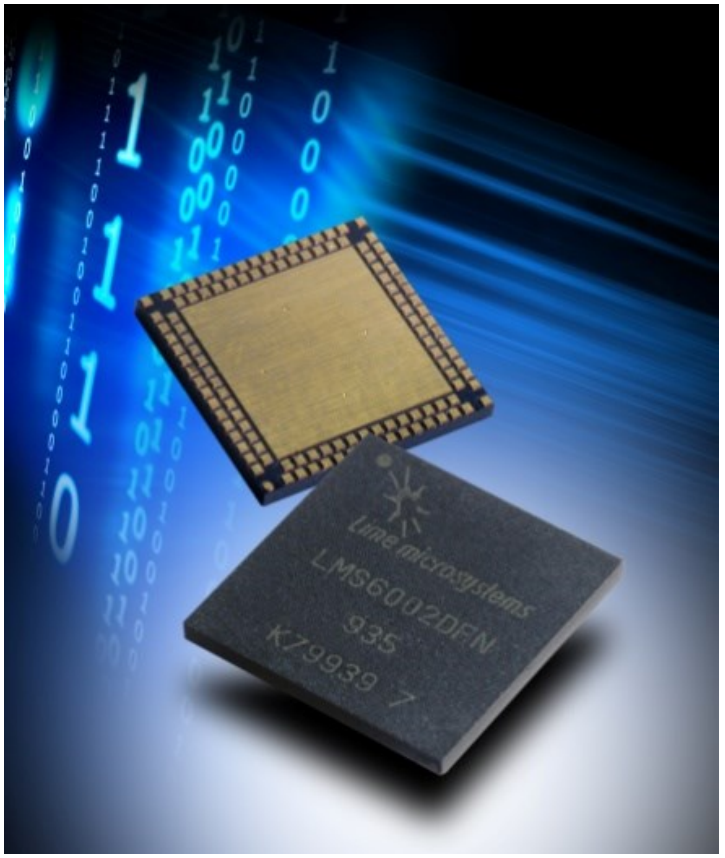
LMS6002D PLL Settling time

Measured on evaluation board with 100KHz and 200KHz Loop Filter



Setup

LMS6002DFN settings:

Rx PLL frequency	1950MHz
Active LNA	LNA2
LNA gain	Max Gain
LPF BW	10MHz
ICP	1200uA and 2400uA
Tx PLL frequency	1950MHz
LPF BW	10 MHz
ICP	1200uA and 2400uA
FDD/TDD Selection	TDD
TDD Mode Selection	Variable

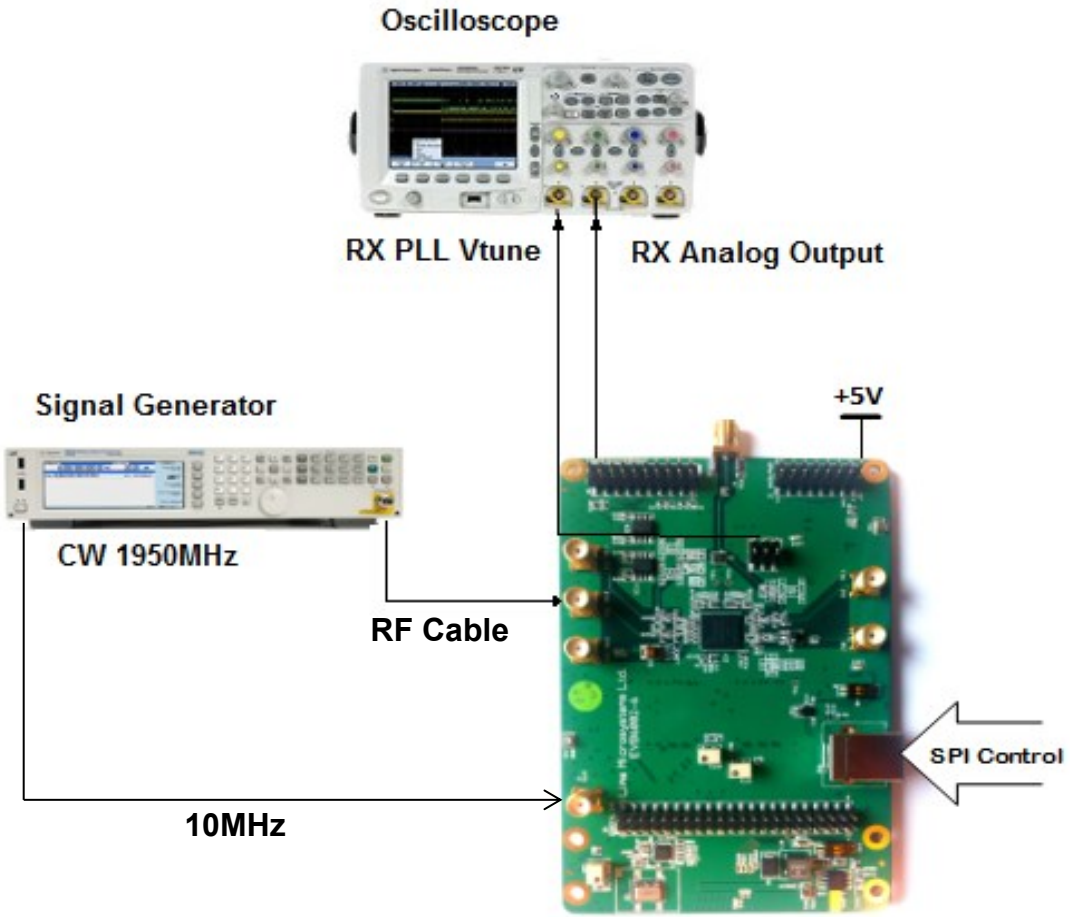
Hardware modification:

TXVDDVCO18 (pin 60) and RXVDDVCO18 (pin 84) to single 1.8V supply via 22 Ohm.

PLL Loop Filter BW:
100KHz
200KHz

Generator settings:

Frequency	1950MHz
Amplitude	-60dBm
Modulation	CW



100KHz Loop Filter Measurements

Charge Pump Current set to **1200uA**

Phase Noise with 100KHz Loop Filter

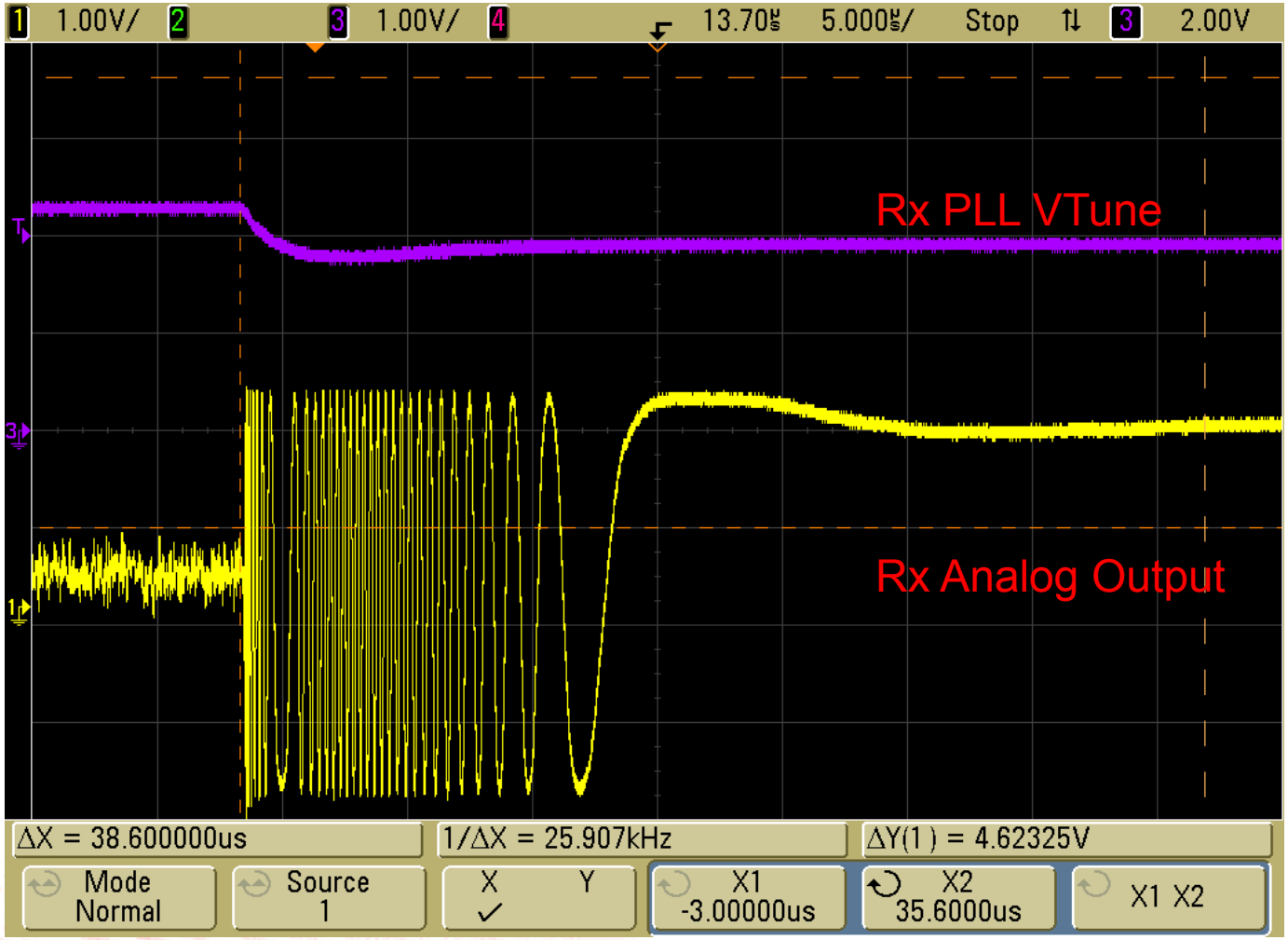
Integrated Phase Noise with 100KHz Loop Filter

Integrated Phase Noise – 1.148 Deg

Measured Rx PLL Settling Time

Note:
When Rx PLL settles to 1950MHz after switching from Tx to Rx TDD mode we should expect DC at RX Analog Output.

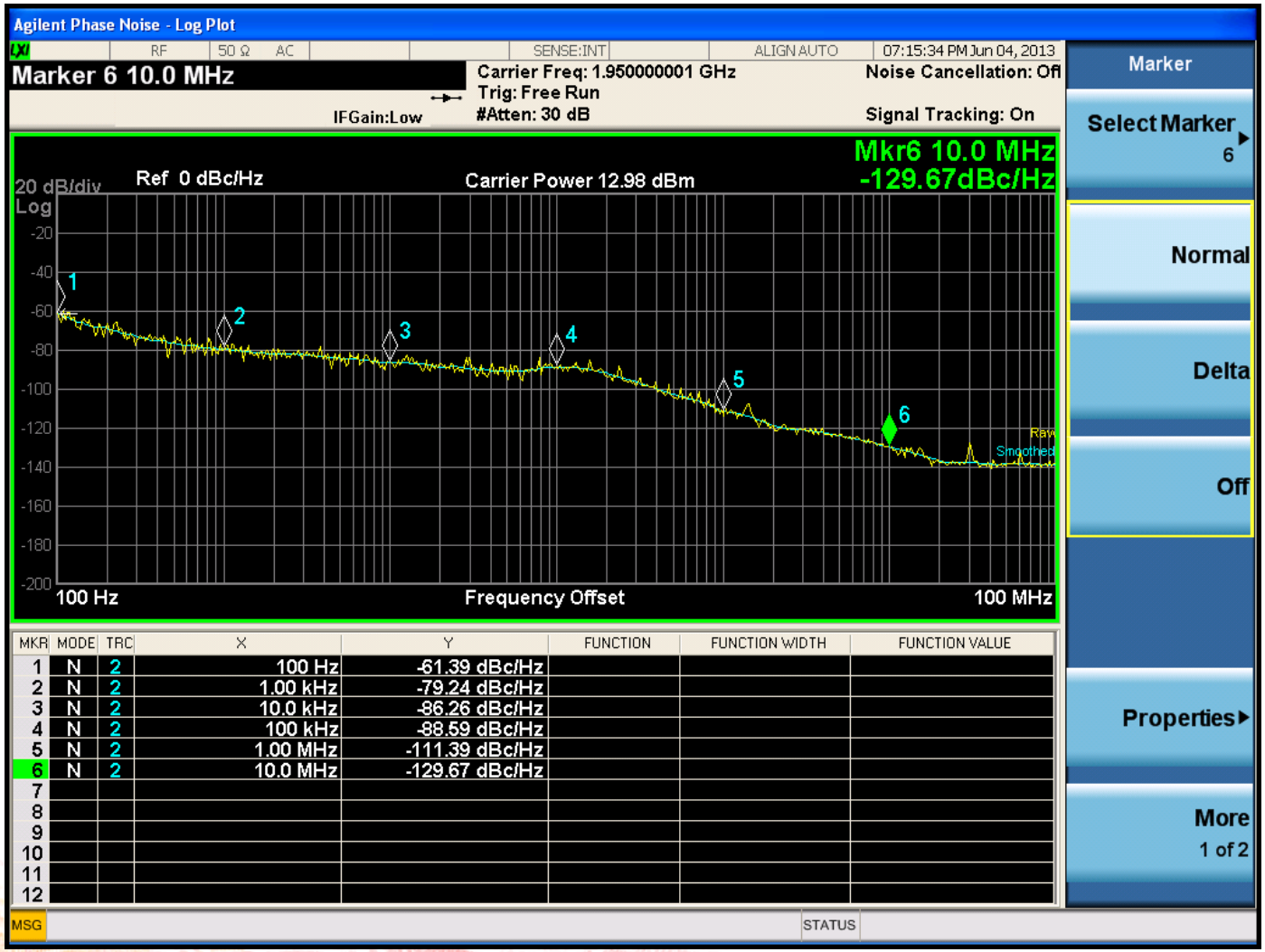
Measured Settling Time is ***38.6us***.



200KHz Loop Filter Measurements

Charge Pump Current set to **1200uA**

Phase Noise with 200KHz Loop Filter



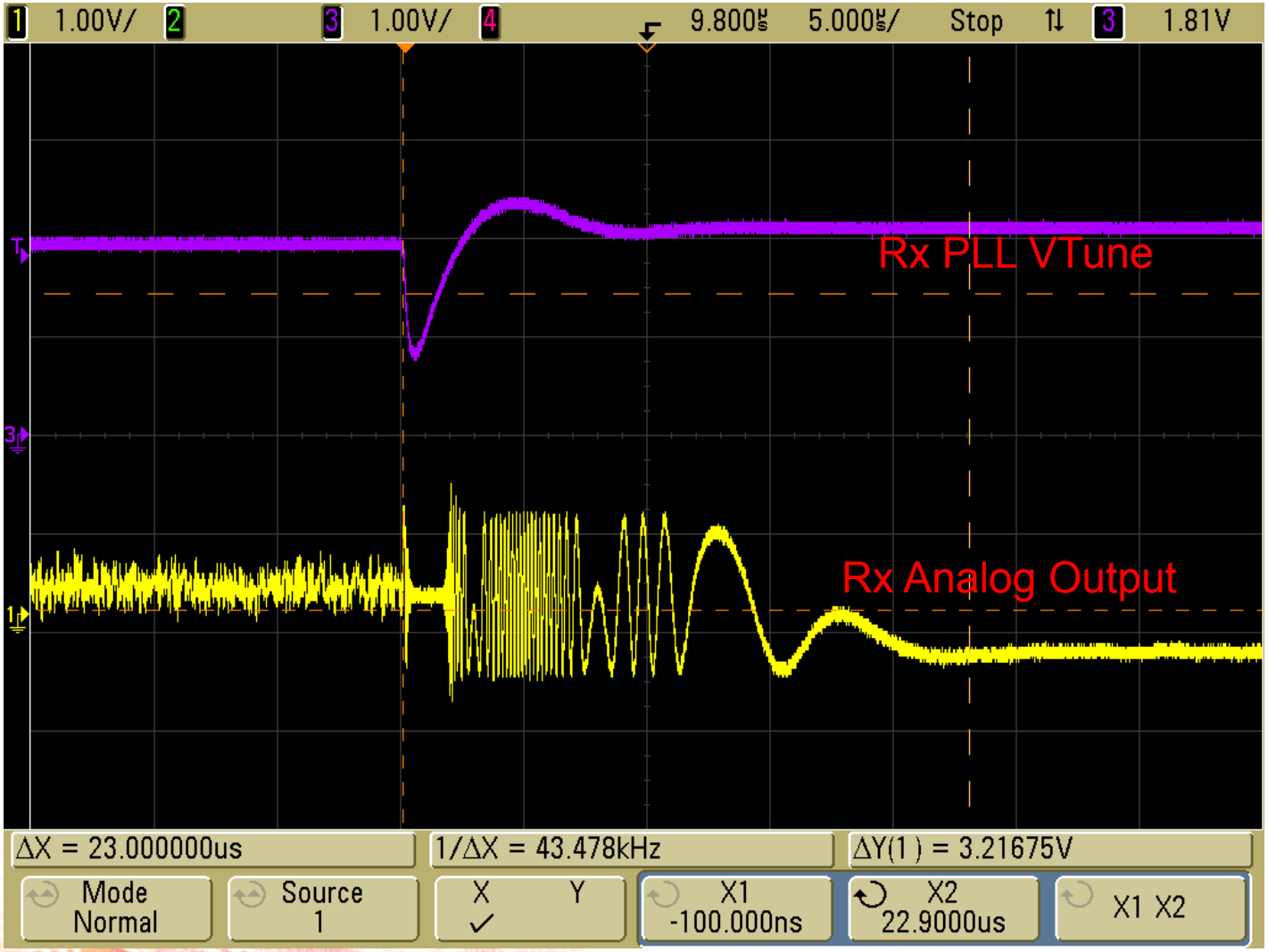
Integrated Phase Noise with 200KHz Loop Filter

Integrated Phase Noise – 1.308 Deg

Measured Rx PLL Settling Time

Note:
When Rx PLL settles to 1950MHz after switching from Tx to Rx TDD mode we should expect DC at RX Analog Output.

Measured Settling Time is ***23us***.



200KHz Loop Filter Measurements

Charge Pump Current set to **2400uA**

Phase Noise with 200KHz Loop Filter,

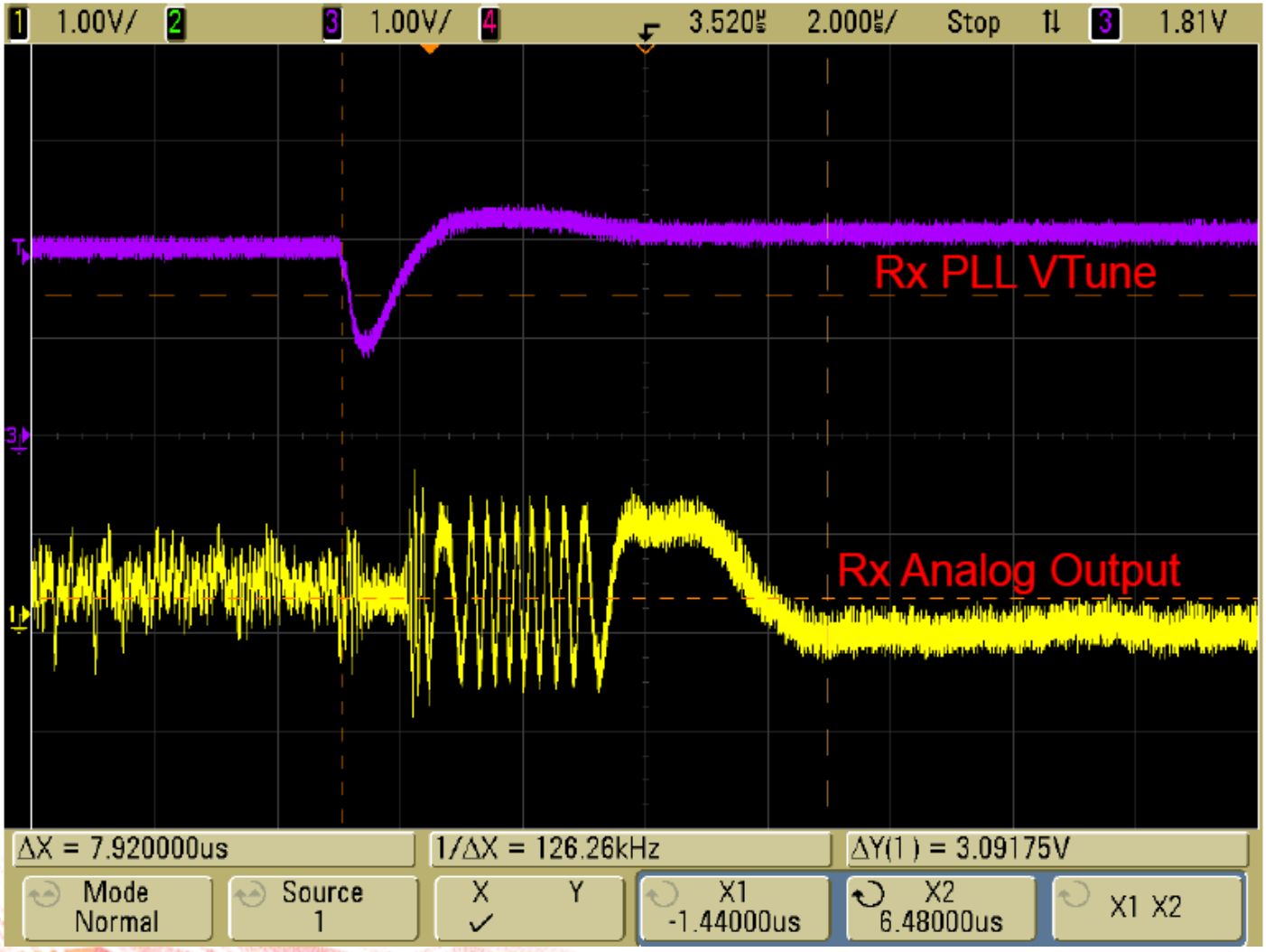
Integrated Phase Noise with 200KHz Loop Filter

Integrated Phase Noise – 1.348 Deg

Measured Rx PLL Settling Time

Note:
When Rx PLL settles to 1950MHz after switching from Tx to Rx TDD mode we should expect DC at RX Analog Output.

Measured Settling Time is ***8us***.



Loop Filters

Filetr BW 100kHz :
C1 – 470pF
C2 – 8.2nF
R2 – 820Ohm
R3 – 1.2kOhm
C3 – 150pF

Filetr BW 200kHz :
C1 – 47pF
C2 – 1.2nF
R2 – 1.5kOhm
R3 – 2.2kOhm
C3 – 22pF