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## **Xillybus core generation for LimeSDR-PCIE board**

***- Guide -***

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# Revision History

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Initial version

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# 1

## Introduction

This document describes Xillybus core generation and instantiation for LimeSDR-PCIE board. Document consists of a chapters that describes steps to generate and download required files for LimeSDR-PCIE\_lms7\_trx project.

Xillybus documentation [[1](#)], [[2](#)], [[3](#)], can be found in links provided in this document reference.

# 2

## Xillybus core generation

Xillybus core has to be generated before downloading. This chapter describes steps and parameters required to generate Xillybus PCIE core.

### 2.1 Signing Up

Xillybus requires to fill up free registration form in order to download generated core. Go to link <http://xillybus.com/ipfactory/signup>, fill required fields (Figure 1) and confirm registration via received eMail.

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### IP Core Factory – Sign up!

Hello, Anonymous User

Email address:  Password:

☐ Remember me [Forgot your password?](#) [Sign up!](#)

My saved IP cores


Email address:

Password:

Re-type password:

- Your email address is your user name at this site
- Gmail and other free mail addresses are OK
- This email address is authenticated on the next step
- Please use an address you really check: Only very few messages, related directly to creating custom IP cores, will be sent there.

Type the characters you see in the picture below.

Verification:  (try another one) (audio)

Letters are not case-sensitive

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Figure 1 Registration form

## 2.2 Creating new IP core

After successful registration, go to IP core Factory page <http://xillybus.com/ipfactory/>, fill parameters as shown in Figure 2 and click *Create!*.

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### IP Core Factory – Create new IP core

Hello, Anonymous User Email address:  Password:  [Login!](#)  
[Remember me](#) [Forgot your password?](#) [Sign up!](#)

My saved IP cores

IP core's name (for reference in this site only):

Target device family: Altera Cyclone IV with 4x lanes Operating system: Linux and Windows

Initial template: Demo bundle setting

[Create!](#)

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Figure 2 Create new IP core dialog

## 2.3 Setting core parameters

After new core creation in next dialog click *Edit* to change settings for each device files (Figure 3).

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### IP Core Factory – List of device files for IP core "myipcore\_demo"

Hello, (manage) [Log out](#)

My saved IP cores

#### Core summary

Name	Status	Target device family	Operating system
myipcore_demo	( edit attributes   replicate   delete   generate core )	Altera Cyclone IV with 4x lanes	Linux and Windows

[Open for changes](#) [Add a new core](#)

#### Device files

Name	Direction	Data width	Expected BW	Autoset	Details
xillybus_read_32	( edit   replicate   delete )	32 bits	195 MB/s	Yes	Data acquisition / playback (20 ms)
xillybus_write_32	( edit   replicate   delete )	32 bits	180 MB/s	Yes	Data acquisition / playback (20 ms)
xillybus_read_8	( edit   replicate   delete )	8 bits	1 MB/s	Yes	General purpose
xillybus_write_8	( edit   replicate   delete )	8 bits	1 MB/s	Yes	General purpose
xillybus_mem_8	( edit   replicate   delete )	8 bits	102.400 kB/s	Yes	Address/data interface (5 address bits)
		8 bits	102.400 kB/s	Yes	Address/data interface (5 address bits)

[Add a new device file](#)

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Figure 3 File editing

In *Edit* dialog (Figure 4) fill following parameters for corresponding file and click *Update!*.  
To enter all parameters *Autoset internals* has to be unchecked:

**For xillybus\_read\_32:**

- Device file's name - read\_32
- Direction - Upstream (FPGA to host)
- Use - Data acquisition / playback
- Data width - 32 bits
- Expected bandwidth - 195
- Autoset internals - unchecked
- Asynchronous/synchronous - Asynchronous
- Number of buffers - 256
- Size of each buffer - 8 kB

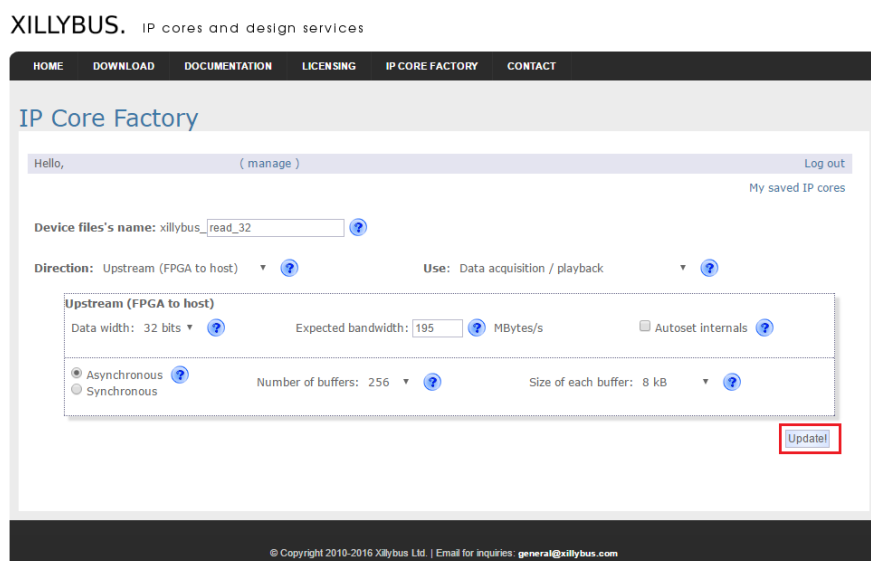


Figure 4 xillybus\_read\_32 file editing

Edit rest of the files with following parameters:

**For xillybus\_write\_32:**

- Device file's name - write\_32
- Direction - Downstream (host to FPGA)
- Use - Data acquisition / playback
- Data width - 32 bits
- Expected bandwidth - 180
- Autoset internals - unchecked
- Asynchronous/synchronous - Asynchronous
- Number of buffers - 256
- Size of each buffer - 8 kB
- DMA acceleration - None

**For xillybus\_read\_8:**

- Device file's name - read\_8
- Direction - Upstream (FPGA to host)
- Use - General purpose
- Data width - 8 bits

- 
- Expected bandwidth - 1
  - Autoset internals - unchecked
  - Asynchronous/synchronous - Asynchronous
  - Number of buffers - 4
  - Size of each buffer - 4 kB

**For xillybus\_write\_8:**

- Device file's name - write\_8
- Direction - Downstream (host to FPGA)
- Use - General purpose
- Data width - 8 bits
- Expected bandwidth - 1
- Autoset internals - unchecked
- Asynchronous/synchronous - Asynchronous
- Number of buffers - 4
- Size of each buffer - 4 kB
- DMA acceleration - None

**For xillybus\_mem\_8:**

- Device file's name - mem\_8
- Direction - Bidirectional
- Use - Address/data interface (5 address bits)
- Upstream (FPGA to host)
  - Data width - 8 bits
  - Expected bandwidth - 0.1
  - Autoset internals - unchecked
  - Asynchronous/synchronous - Synchronous
  - Number of buffers - 4
  - Size of each buffer - 4kb
- Downstream (host to FPGA)
  - Data width - 8 bits
  - Expected bandwidth - 0.1
  - Autoset internals - unchecked
  - Asynchronous/synchronous - Synchronous
  - Number of buffers - 4
  - Size of each buffer - 4kb
  - DMA acceleration - None

After updating all files click *generate core* (Figure 5). Check core status and download it when available (Figure 6).



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## IP Core Factory — List of device files for IP core "myipcore\_dem"

Hello,
( manage )
Log out

My saved IP cores

### Core summary

Name	Status	Target device family	Operating system
myipcore_dem	( edit attributes   replicate   delete )	( generate core )	Linux and Windows
Open for changes		Altera Cyclone IV with 4x lanes	

( + ) Add a new core

### Device files

Name	Direction	Data width	Expected BW	Autoset	Details
xillybus_read_32 ( edit   replicate   delete )					
	Upstream (FPGA to host)	32 bits	195 MB/s	No	Asynchronous, 256 x 8 kB = 2 MB Data acquisition / playback
xillybus_write_32 ( edit   replicate   delete )					
	Downstream (host to FPGA)	32 bits	180 MB/s	No	Asynchronous, 256 x 8 kB = 2 MB DMA acceleration: None Data acquisition / playback
xillybus_read_8 ( edit   replicate   delete )					
	Upstream (FPGA to host)	8 bits	1 MB/s	No	Asynchronous, 4 x 4 kB = 16 kB General purpose
xillybus_write_8 ( edit   replicate   delete )					
	Downstream (host to FPGA)	8 bits	1 MB/s	No	Asynchronous, 4 x 4 kB = 16 kB DMA acceleration: None General purpose
xillybus_mem_8 ( edit   replicate   delete )					
	Upstream (FPGA to host)	8 bits	102.400 kB/s	No	Synchronous, 4 x 4 kB = 16 kB Address/data interface (5 address bits)
	Downstream (host to FPGA)	8 bits	102.400 kB/s	No	Synchronous, 4 x 4 kB = 16 kB DMA acceleration: None Address/data interface (5 address bits)

( + ) Add a new device file

Figure 5 Core generation

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## IP Core Factory — Your saved IP cores

Hello,
( manage )
Log out

My saved IP cores

Name	Status	Target device family	Operating system
myipcore_demo (5)	Download	Altera Cyclone IV with 4x lanes	Linux and Windows

( + ) Add a new core

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Figure 6 Download status

# 3

## Quartus project files

This chapter describes steps to include Xillybus core to Quartus project

### 3.1 Quartus files

Steps to include Xillybus core files into Quartus project.

- Extract downloaded .zip file “*corebundle-myipcore\_demo.zip*” (*myipcore\_demo* – name that was entered during core generation).
- Place file *xillybus.v* to Quartus project directory *limesdr-pcie\_xillybus\_core/*
- Place file *xillybus\_core.qxp* to Quartus project directory *limesdr-pcie\_xillybus\_core/*
- Open Quartus *LimeSDR-PCIE\_lms7\_trx* project and select Project→ Add/Remove Files in Project and add files *xillybus.v* and *xillybus\_core.qxp* to Quartus project (Figure 7).
- Recompile project.

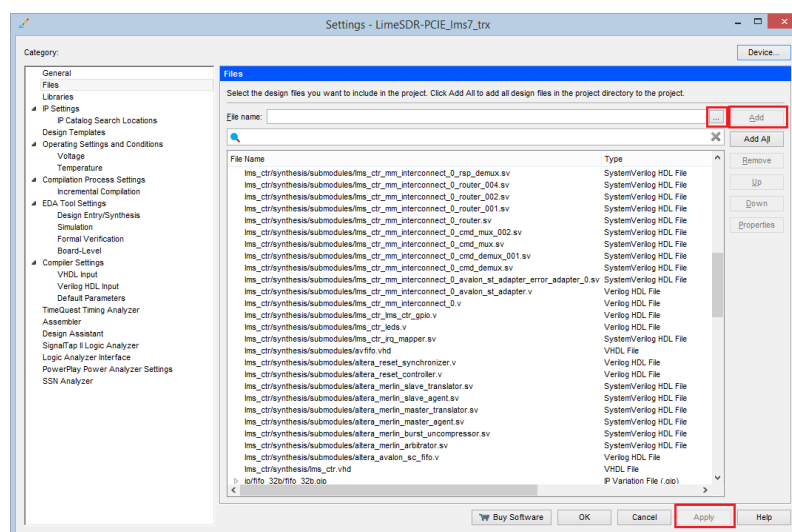


Figure 7 Adding files to Quartus project

# 4

## References

1. Xillybus documentation files: <http://xillybus.com/doc>
2. Getting started with Xillybus on a Windows host:  
[http://xillybus.com/downloads/doc/xillybus\\_getting\\_started\\_windows.pdf](http://xillybus.com/downloads/doc/xillybus_getting_started_windows.pdf)
3. Getting started with Xillybus on a Linux host:  
[http://xillybus.com/downloads/doc/xillybus\\_getting\\_started\\_linux.pdf](http://xillybus.com/downloads/doc/xillybus_getting_started_linux.pdf)