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PulseRain M10 Board

Hardware Manual

Oct, 2017

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Acronyms and Abbreviations

Acronyms / Abbreviations	Definition
ACK	Acknowledge
ADC	Analog to Digital Converter
BCD	Binary-Coded Decimal
BIST	Built-in Self Test
CISC	Complex Instruction Set Computer
CODEC	Coder-Decoder
DPTR	Data Pointer
DTMF	Dual Tone Multi Frequency
ENIG	Electroless Nickel Immersion Gold
FPGA	Field Programmable Gate Array
I2C	Inter-Integrated Circuit
IO	Input and Output
IRQ	Interrupt Request Line
ISA	Instruction Set Architecture
ISR	Interrupt Service Routine
JTAG	Joint Test Action Group
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LSB	Least Significant Bit
MCU	Microcontroller Unit
MSB	Most Significant Bit
NOP	No Operation
OCD	On-chip Debugger
PC	Personal Computer or Program Counter
PCB	Printed Circuit Board
PSW	Program Status Word
PWM	Pulse Width Modulation
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances
SDCC	Small Device C Compiler
SFR	Special Function Register
SRAM	Static Random-Access Memory
UART	Universal Asynchronous Receiver-Transmitter
Wi-Fi	Wireless Fidelity

1 Introduction

Over the past 10 years, FPGA device has grown into main stream. Instead of using a hardcore MCU, embedding a soft-core MCU into FPGA, with all the peripherals customized, is now within the reach of makers. And that's where PulseRain M10 comes into play, an open source design down to the silicon level!

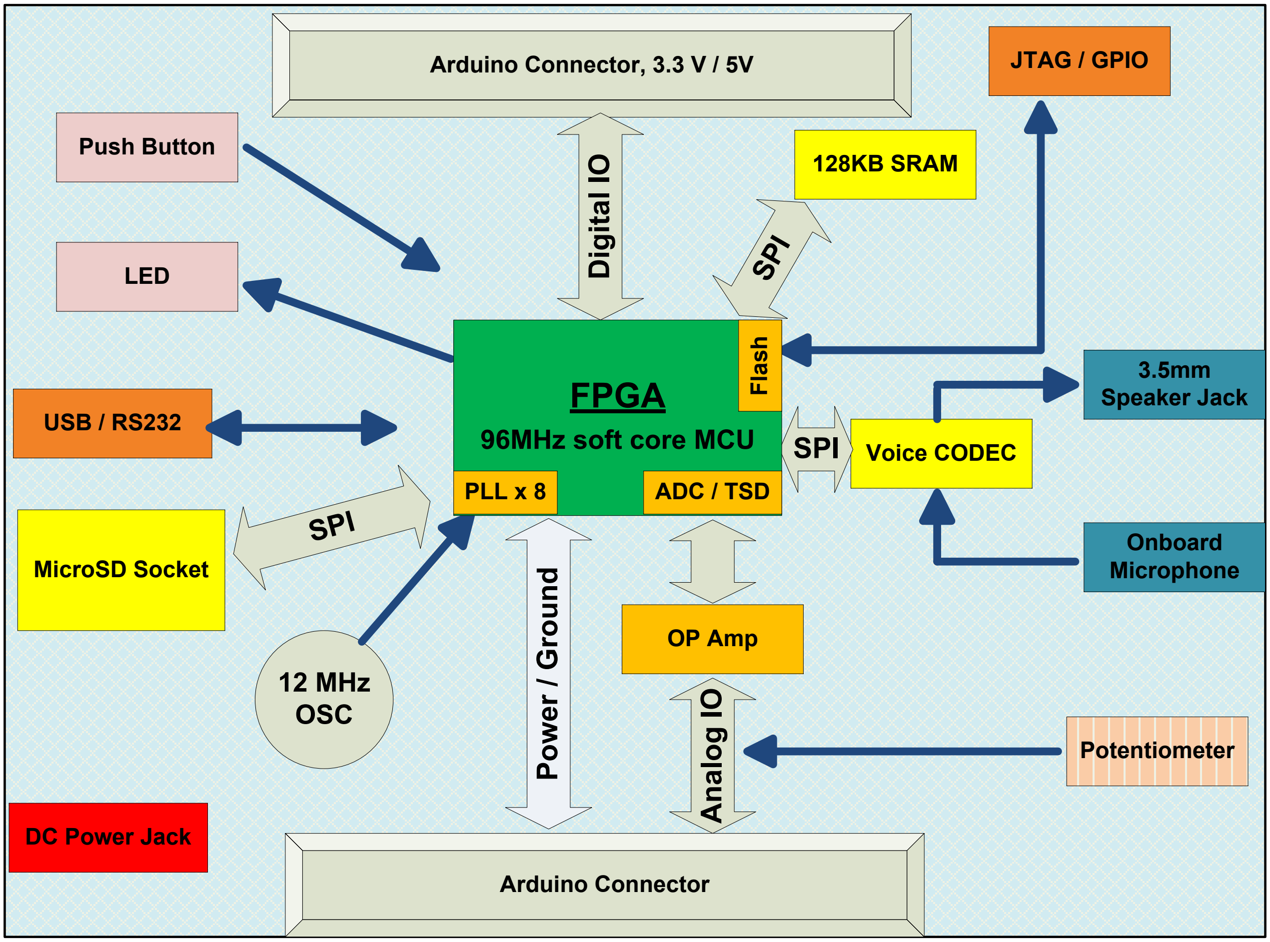

Figure 1-1 The Whole Picture

As illustrated in Figure 1-1, the M10 board takes a distinctive technical approach by embedding an open source soft MCU core (96MHz) into an Intel MAX10 FPGA, while offering an Arduino compatible software interface and form factors. And it features onboard resources like voice CODEC, microSD socket, SRAM, onchip ADC etc., and it also supports dual IO voltages (3.3V / 5V).

The M10 board can serve as a core module and can easily morph into various cool things. In fact, it can completely replace Arduino in all respects. And this document serves as its hardware manual.

2 Form Factor

The M10 board has a form factor that is compatible with the Arduino UNO Rev 3. The mechanical metrics for the M10 board are as following in Table 2-1:

Metric Name	Value	Description
Width	2.1 Inch	The width of the PCB
Length	3.2 Inch	The length of the PCB
PCB Thickness	62 mil	Thickness of the finished PCB
Maximum Height	0.5 Inch	The sum of maximum component height on both sides of the PCB

Table 2-1 Mechanical Metrics

There are 4 mounting holes on the M10 board, and their positions are compatible with those on the Arduino UNO Rev 3. The coordinates of those mounting holes are shown in Figure 2-1. (All Units are in Inch.)

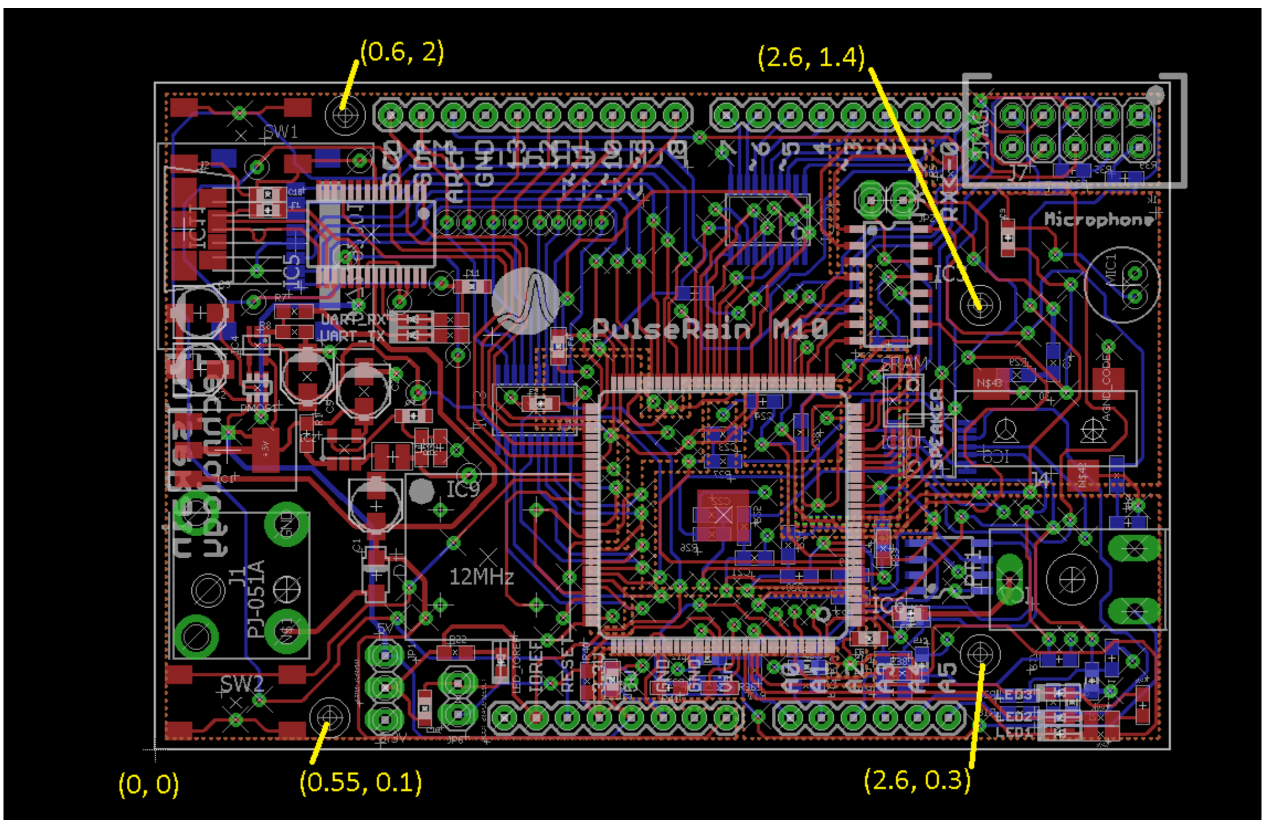

Figure 2-1 The Mounting Holes of M10 (All Units are in Inch)

3 PCB

The basic metrics of the M10 PCB are shown below in Table 3-1:

Metric Name	Value	Description
Width	2.1 Inch	The width of the PCB
Length	3.2 Inch	The length of the PCB
PCB Thickness	62 mil	Thickness of the finished PCB
Num of layers	4	2 signal layers. 1 Power layer, 1 Ground layer
Solder Mask Color	Blue	Blue solder mask on both sides
Surface Finish	ENIG - RoHS	Electroless Nickel Immersion Gold – RoHS
Copper Weight	1 oz	
Minimum Trace Width	8 mil	
Num of Blind Vias	0	All Vias are through-hole vias
Number of Micro Vias	0	
Minimum Trace Clearance	8 mil	

Table 3-1 PCB Metrics

4 Power

The power of M10 board can be supplied either from the low-profile DC jack or from the microUSB port, as shown in Figure 4-1 and Figure 4-2. And the block diagram of the power regulation circuit is shown in Figure 4-3.

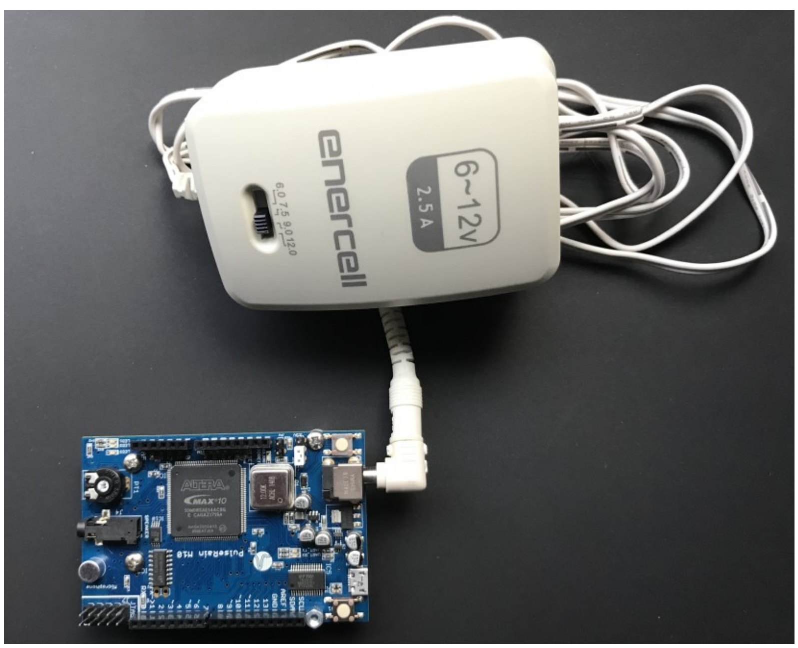

Figure 4-1 Supply Power through DC Jack

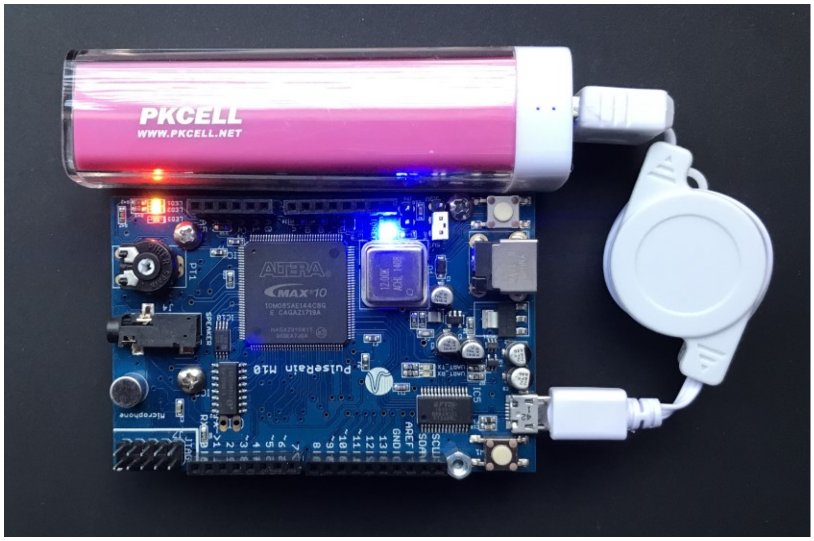

Figure 4-2 Supply Power through microUSB

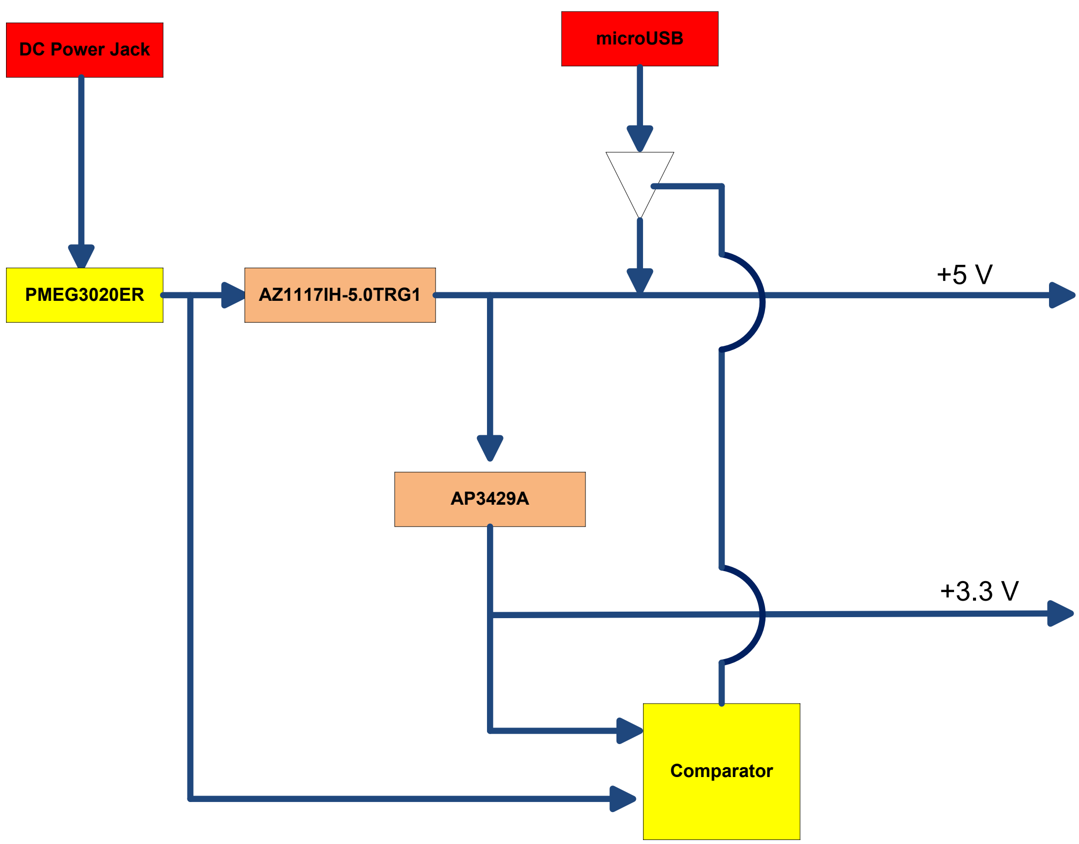

Figure 4-3 Power Regulation Block Diagram

As illustrated in Figure 4-3, the power from the DC jack will first go through a Schottky rectifier (PMEG3020ER). The purpose of this rectifier is to protect the rest of the circuit from accidental polarity reverse. The incoming DC power (6.5V – 15V) will then go through a LDO (AZ1117IH, with an output current up to **1.35A**) to get a stable +5V output. And this +5V output will also produce a +3.3V through a step-down buck converter (AP3429A).

And instead of using the DC Jack and LDO to produce +5V rail, the +5V could also come from the microUSB port. The comparator in Figure 4-3 will determine which power source to be the active one. When both the DC Jack power and the USB power are present, the power from the DC Jack will always prevail and become the active power source.

5 Major Components

The M10 board has the following major components: (The packages of those components are carefully chosen to avoid BGA or QFN packages.)

- Intel/Altera MAX10 FPGA (with on-chip A/D Converter and Temperature Sensor Diode)
- 12MHz Crystal Oscillator
- 2 Push Button
- 6 LEDs
- USB/UART Bridge (FT232R)
- Voice CODEC, onboard microphone and Speaker Jack
- 1Mbit Serial SRAM
- microSD Socket
- 3.3 V / 5V voltage translator to support dual IO voltage
- OpAmp and Potentiometer for Analog Input
- IO connectors that are compatible with Arduino UNO Rev 3
- JTAG Header for the FPGA
- Jumpers for IO voltage selection and FPGA programming

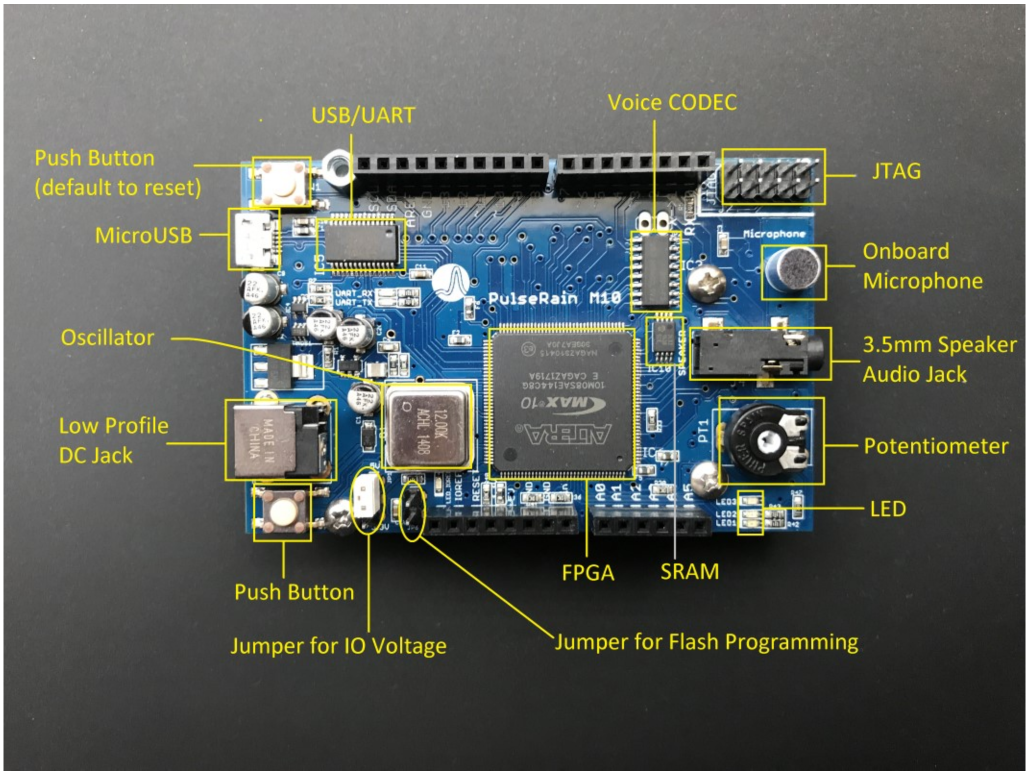

Figure 5-1 Major Components (Top Side)

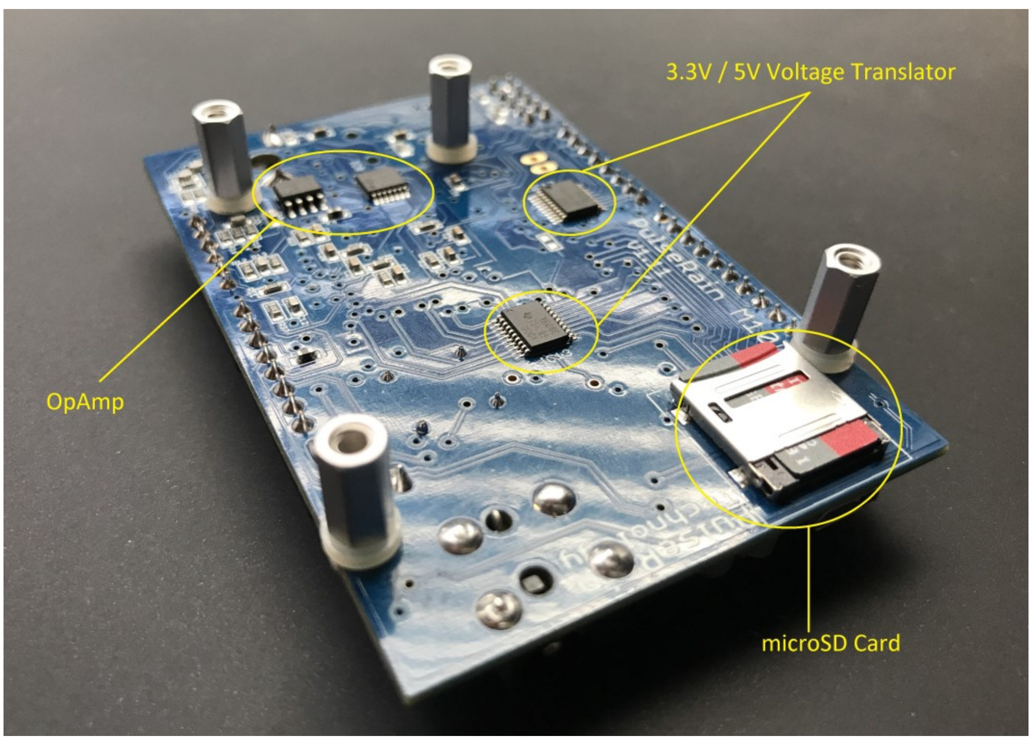

Figure 5-2 Major Components (Bottom Side)

5.1 Clock and Reset

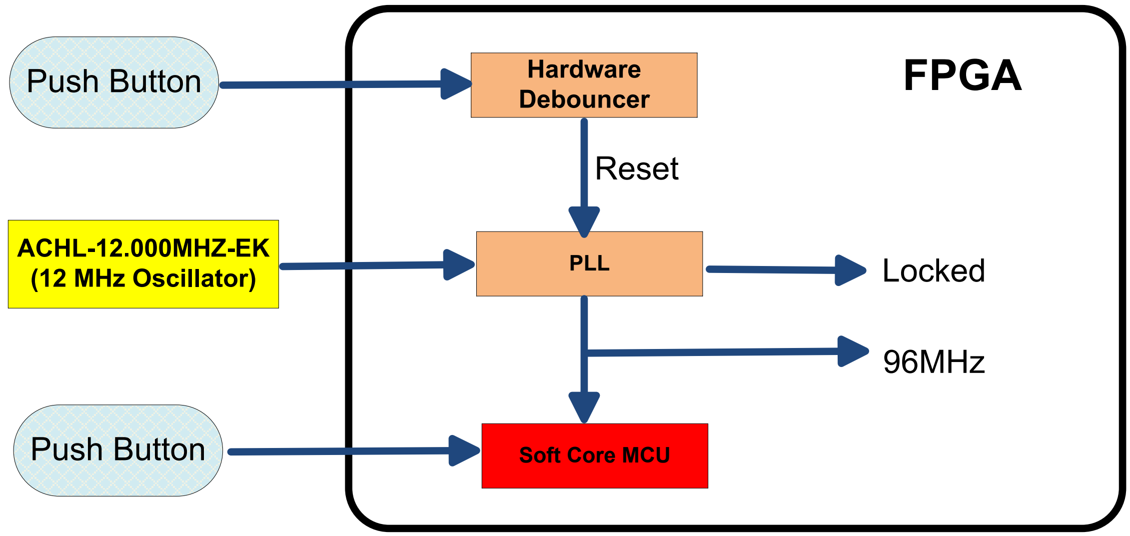

Figure 5-3 Clock and Reset

As illustrated in Figure 5-3, the FPGA's PLL is fed by the 12MHz onboard oscillator to produce an internal clock of 96MHz. The FP51-1T processor core and peripherals are all driven by this 96MHz clock.

As shown in Figure 5-1, there are two push buttons available on the M10 board. One is located close to the microUSB connector. The other is located next to the DC Jack. To follow Arduino convention, the one close to the microUSB will be used as the default reset button. And inside the FPGA, the input from this reset button will go through a hardware de-bouncer before it is used to reset the PLL. (The PLL's "locked" output will be used to reset the rest of the circuit.)

On the other hand, the push button next to the DC Jack can be used for general purpose input. And it can be handled inside the soft core MCU by software de-bouncing approach.

5.2 LED

There are 6 LEDs on the M10 board, and they are assigned as the following:

- UART_RX (Red), UART_TX (Green)
  Those two LEDs are located next to the FT232RL chip (USB/UART bridge). They are the activity indication for the micro-USB port.

- IO Power Indicator (Blue)
  This LED is located close to the jumper for IO voltage selection. It will be on when the IO pins are powered (3.3V or 5V).

- General Purpose LED (Blue, Red and Green)
  Those 3 LEDs are located close to the onboard microphone, as illustrated in Figure 5-1.

5.3 USB / UART Bridge

The M10 board can interface with a host computer through microUSB port, for which a USB/UART bridge chip (FT232R) is used. The FT232RL can support a baud rate up to 921600 bps, and the details of this chip can be found in Ref [3].

The M10's FPGA has UART controller that can communicate with the FT232RL. The technical details of the UART controller can be found in

Ref [13]: PulseRain M10 – Serial Port, Technical Reference Manual, Doc# TRM-0922-01005, Rev 1.0.0, 09/2017, https://github.com/PulseRain/M10SerialAUX/raw/master/extras/M10_Serial_TRM.pdf

5.4 Voice CODEC, Onboard Microphone and Speaker Jack

5.4.1 Analog Interface

The M10 board carries a voice CODEC (Si3000) from the Silicon Lab. And it has been integrated with an onboard microphone (CMC-5044PF-A) and a 3.5 mm speaker jack for analog in and out, as illustrated in Figure 5-4.

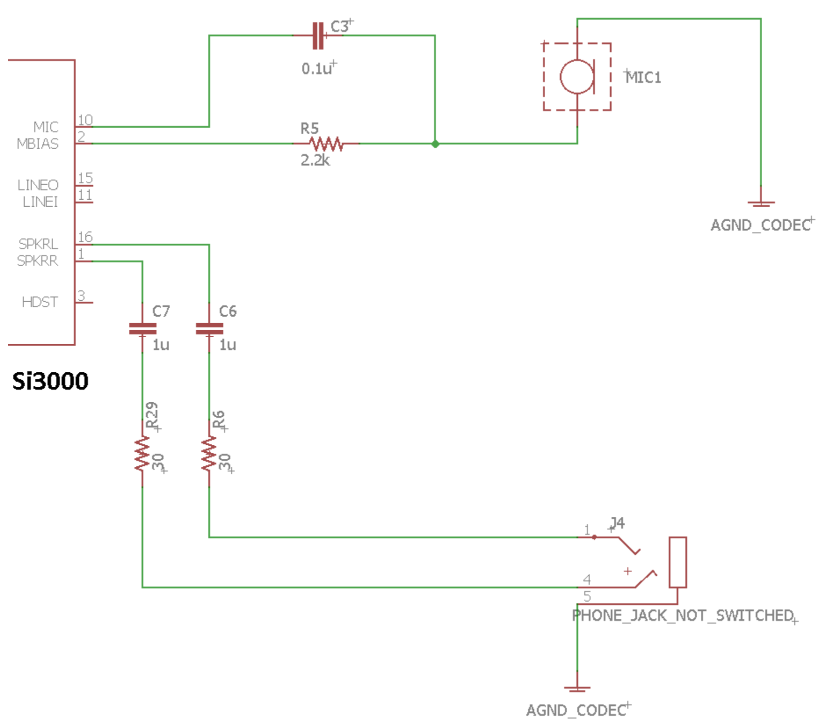

Figure 5-4 Si3000 Analog Interface

Users can hook a headset or active speaker to the 3.5 mm speaker jack for voice output.

5.4.2 Digital Interface

The voice CODEC's digital interface is connected to the FPGA, with the following signal pins:

- MCLK: the master clock (4MHz), from FPGA to Si3000
- SCLK: the slave clock (2048KHz), from Si3000 to FPGA. The SCLK runs at 256 bits per frame. For M10 board, the **default sample rate is set to be 8KHz**, so 8KHZ * 256 = 2048KHz
- FSYNC_N: Frame Sync, level sensitive signal that goes all the way low during the active cycles
- SDO: Serial Data from Si3000 to FPGA
- SDI: Serial Data from FPGA to Si3000

The datasheet of Si3000 (Ref [4]) suggests to put pull-up or pull-down resistors on SDO and SCLK for Serial Mode selection (The Si3000 on the M10 board currently works in the slave mode.). Those pull-up and pull-down resistors are omitted on the M10 board as the FPGA can provide weak pull-up in its pin assignment. And the SDO can be driven to low by default. The Verilog code for the SCLK and SDO are as following:

```
assign Si3000_SCLK = (Si3000_RESET_N) ? 1'bZ : 1'b0;
assign Si3000_SDO = (Si3000_FSYNC_N) ? 1'b0 : 1'bZ;
```

List 5-1 SCLK and SDO assignment for Si3000

And the rest of the details for Si3000 digital interface can be found in

Ref [8]: PulseRain M10 – Voice CODEC, Technical Reference Manual, Doc# TRM-0922-01001, Rev 1.0.3, 09/2017, https://github.com/PulseRain/M10CODEC/raw/master/extras/M10_CODEC_TRM.pdf

In addition, with a DTMF software library, the voice CODEC can be used for DTMF decoding. The technical details of the DTMF decoding can be found in

Ref [12]: PulseRain M10 – DTMF, Technical Reference Manual, Doc# TRM-0922-01002, Rev 1.0.0, 09/2017 https://github.com/PulseRain/M10DTMF/raw/master/extras/M10_DTMF_TRM.pdf

5.5 Serial SRAM

The M10 board carries a 1Mbit Serial SRAM from Microchip (Part Number 23LC1024), and the FPGA has full access to this SRAM. The correspondent technical details can be found in

Ref [11]: PulseRain M10 – SRAM, Technical Reference Manual, Doc# TRM-0922-01004, Rev 1.0.0, 09/2017 https://github.com/PulseRain/M10SRAM/raw/master/extras/M10_SRAM_TRM.pdf

5.6 microSD

With a soft-core MCU, a microSD controller inside FPGA, plus a software library, the M10 board is capable of accessing the microSD card at file system level. The details of the microSD controller and the correspondent software library can be found in

Ref [7]: PulseRain M10 – microSD, Technical Reference Manual, Doc# TRM-0922-01006, Rev 1.0.0, 09/2017 https://github.com/PulseRain/M10SD/raw/master/extra/M10_SD_TRM.pdf

5.7 IOs

5.7.1 IO Voltage

The M10's FPGA (Intel/Altera MAX10) only supports 3.3V IO. But with the onboard voltage translator (TXS0108E, Ref [15]), dual IO voltage (3.3 V / 5V) is supported.

The output of TXS0108E is actually an open drain circuit, with a pull-up resistor of 40 kΩ when it is driving low, and 4 kΩ when it is driving high (Ref [15]). For those who design shields for the M10 board, those pull-up resistance values need to be taken into account. For example, some shields will have a LED in serial with a pull-down resistor connected directly to the IO pin for toggle activity display, and the pull-down resistor in this case should be chosen carefully with a value that keeps enough margin for IO logic level.

In addition, some of the IO pins on the M10 board are configured to be in PWM mode by default. And the details of the PWM controller and software library can be found in

Ref [6]: PulseRain M10 – PWM, Technical Reference Manual, Doc# TRM-0922-01009, Rev 1.0.1, 10/2017 https://github.com/PulseRain/M10PWM/raw/master/extras/M10_PWM_TRM.pdf

Please note that the maximum continuous output current for TXS0108E is only 50mA (Ref [15]). If larger current is needed, such as driving a DC motor, the user can adopt a H-bridge driver, such as the one in Ref [16]. (With H bridge, the DC motor can also be driven in both directions.)

5.7.2 IO Pin Map

The M10 board has an IO pin map that is compatible with that of Arduino UNO Rev 3. The details of the IO pin map can be found below in Figure 5-5:

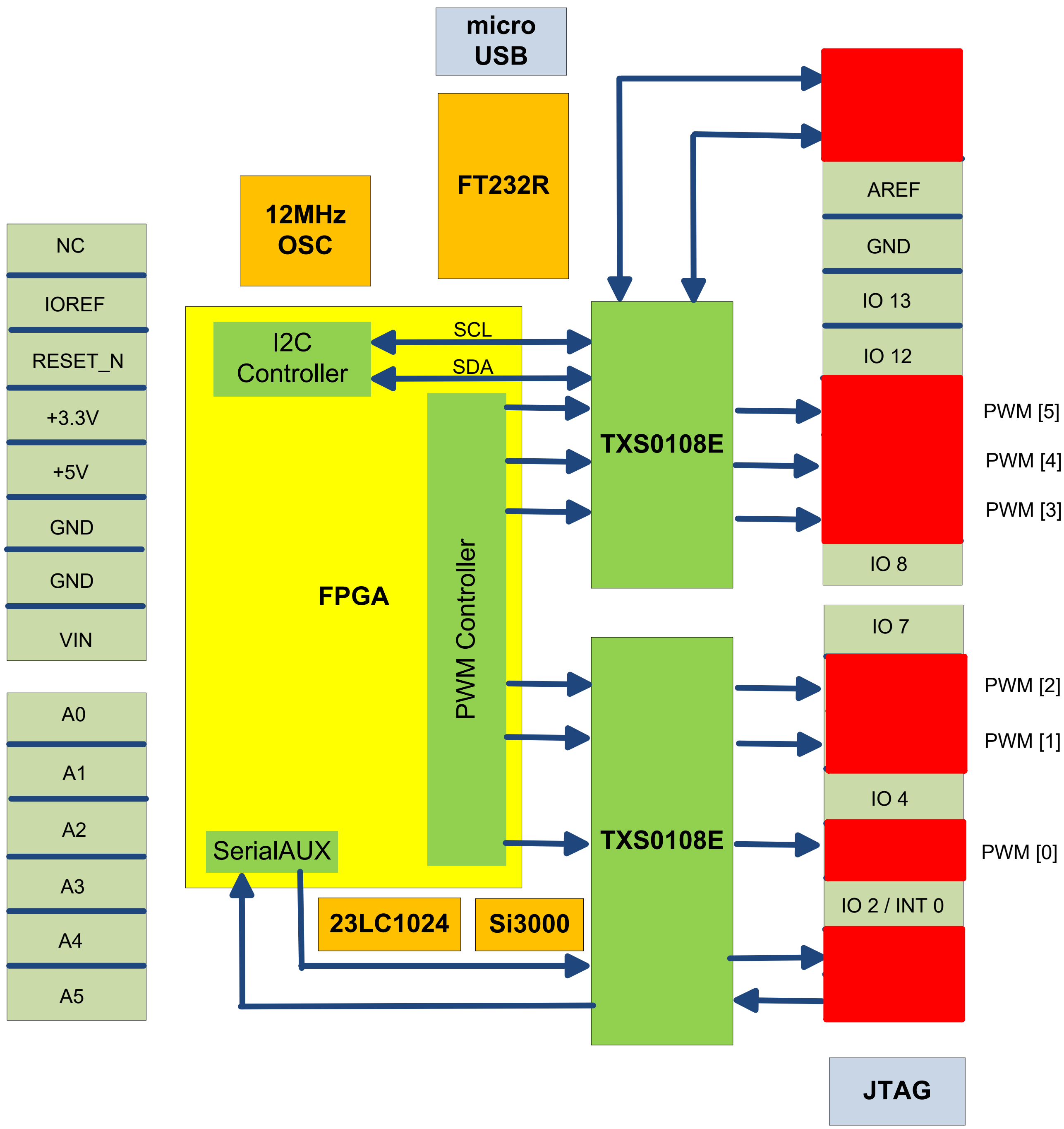

Figure 5-5 IO Pin Map

5.8 FPGA

5.8.1 Overview

The brain of the M10 board is an Intel/Altera MAX10 FGPA, with the part number 10M08SAE144C8G. It has a 144-pin EQFP package, with on-chip A/D Converter and TSD (Temperature Sensor Diode). It also has 8K Logic Elements and 378Kb Block RAM.

What makes MAX10 standing out is that it also has on-chip flash memories to store both the configuration image and user image, while traditional FPGA devices usually require external no-volatile memories or standalone microprocessors to act as a configuration agent.

And the flash memory of the MAX10 device has the following 3 sections:

- CFM0 (Configuration Flash Memory 0)
- CFM1 (Configuration Flash Memory 1)
- UFM (User Flash Memory)

Out of the Factory, the M10's FPGA has the following production images burned-in:

Flash Memory Section	Description
CFM0	The bootstrap image to configure CFM1 and UFM
CFM1	The image for PulseRain FP51-1T MCU
UFM	The program to be loaded into the soft-core MCU's code RAM during power up. By default, it will contain a BIST program.

Table 5-1 Factory Image for FPGA

The selection between CFM0 and CFM1 is determined by the jumper setting (JP6, See Section 5.10 for more detail.). By default, JP6 is open, and CFM1 will be active during power up.

By default, CFM1 will carry a FPGA image that contains PulseRain Technology's FP51-1T soft-core MCU, with 32KB code RAM (instruction RAM) and 8KB data RAM. The UFM for 10M08SAE144C8G is also 32KB, which will be used to store the default program to run on the MCU.

During power up, after the FPGA is configured with CFM1, the 32KB content in UFM will be loaded into the code RAM, and the PC (program counter) will be reset to start executing instruction on address zero. Usually, a branch instruction will be placed in address zero to jump to the beginning of the bootloader or C runtime library.

5.8.2 Onchip ADC

The FPGA's on-chip A/D converter is a SAR (successive approximation register) type converter that can run at a sample rate up to 1MHz. On the M10 board, its default sample rate is set to be 50kHz with a 2MHz clock input.

As illustrated in Figure 5-5, the M10 board has 6 analog input that supports 5V input, but the FPGA only supports 3.3V input. To scale the voltage, external OpAmps have been placed in front of these analog input pins. And for the first analog input channel (A0 in Figure 5-5), a potentiometer is also installed to make the input gain adjustable. For more details of the OpAmp and potentiometer circuit, please see:

Ref [9]: PulseRain M10 – ADC, Technical Reference Manual, Doc# TRM-0922-01003, Rev 1.0.0, 09/2017 https://github.com/PulseRain/M10ADC/raw/master/extra/M10_ADC_TRM.pdf

5.8.3 Onchip TSD (Temperature Sensor Diode)

Among the multiple channels of on-chip ADC, one of them is for the TSD (Temperature Sensor Diode). The details of using TSD to gauge temperature can also be found in Ref [9].

5.8.4 Soft-Core MCU

The product FPGA image of the M10 board carries PulseRain Technology's FP51-1T soft-core MCU. The FP51-1T is a high performance 8-bit MCU core, compatible with Intel 8051 ISA. With a crafty RISC implementation, this FP51-1T can achieve single clock cycle execution for most instructions, while pushing the clock rate above 96MHz. It also features an OCD (On Chip Debugger) that supports code downloading, single step execution, hardware breakpoint etc.

For more information of the FP51-1T MCU, please see:

Ref [17]: PulseRain FP51-1T Microcontroller – Technical Reference Manual, Doc# TRM-0923-00001, Rev 1.0.0, 09/2017,
https://github.com/PulseRain/Arduino_M10_IDE/raw/master/docs/PulseRain_8_bit_MCU_TRM.pdf

5.8.5 Port List and Pin Assignment

The port list and pin assignment for the FPGA (FP51-1T MCU Rev A0) is shown in Table 5-2:

Group Name	Signal Name	In/Out	Bit Width	Description	FPGA Pin
Clock / Reset	osc_in	Input	1	Oscillator input, 12 MHz	88
	push_button	Input	1	push button for reset	74
IO Port	P0 [7 : 0]	Input	8	IO Port 0	[59, 135, 25, 56, 24, 54, 22, 21]
	P1 [7 : 0]	Input	8	IO Port 1	[131, 100, 130, 99, 85, 106, 105, 92]
UART	UART_RXD	Input	1	RX pin for the main serial port	75
	UART_TXD	Output	1	TX pin for the main serial port	79
	UART_AUX_RXD	Input	1	RX pin for the auxiliary serial port	50

Group Name	Signal Name	In/Out	Bit Width	Description	FPGA Pin
	UART_AUX_TXD	Output	1	TX pin for the auxiliary serial port	52
Debug	debug_led	Output	1	General Purpose Blue Led	132
SRAM	mem_so	Input	1	SRAM Serial Out.	32
	mem_si	Output	1	SRAM Serial In.	28
	mem_hold_n	Output	1	SRAM Hold, active low.	26
	mem_cs_n	Output	1	SRAM chip select, active low.	29
	mem_sck	Output	1	SRAM Serial clock.	27
Voice CODEC	Si3000_SDO	Input	1	CODEC Serial Data Out.	44
	Si3000_SDI	Output	1	CODEC Serial Data In.	45
	Si3000_SCLK	Input	1	CODEC Serial Clock.	38
	Si3000_MCLK	Output	1	CODEC Main Clock.	41
	Si3000_FSYNC_N	Input	1	CODEC Frame Sync, active low.	43
	Si3000_RESET_N	Output	1	CODEC reset, active low.	39
microSD Card	SD_SPI_CS	Output	1	SD Card chip select, active low	69
	SD_SPI_CLK	Output	1	SD Card SPI clock	65
	SD_SPI_DO	Input	1	Serial data from SD card to FPGA	64
	SD_SPI_DI	Output	1	Serial data from FPGA to SD card	66
	SD_SPI_DAT1	Output	1	Not Used	62
	SD_SPI_DAT2	Output	1	Not Used	70
I2C	I2C_SDA	In/Out	1	SDA for I2C	101
	I2C_SCL	In/Out	1	SCL for I2C	102
PWM	PWM_OUT [5 : 0]	Output	6	PWM output	[98, 96, 93, 58, 57, 55]
GPIO	JTAG_PIN6	Output	1	GPIO on JTAG connector	46
	JTAG_PIN7	Output	1		60
	JTAG_PIN8	Output	1		47

Table 5-2 FPGA Port List and Pin Assignment

5.8.6 FPGA Image Download

As mentioned in Ref [18], the traditional solutions for in-field upgrade all have their shares of shortcoming. And to challenge the status quo, PulseRain Technology has come up with the solution for "M10 High Speed Configuration".

The procedures for program the M10 with new FPGA image or user flash image (UFM) can be found in

Ref[14]: PulseRain M10 – Quick Start Guide, Doc#QSG-0922-0039, Rev 1.1, 09/2017
https://github.com/PulseRain/Arduino_M10_IDE/blob/master/docs/M10_quick_start.pdf

And the technical details for M10 high speed configuration can be found in

Ref [18]: M10 High Speed Configuration, Doc# TRM-0922-3029, Rev 1.0.0, 11/2017,
https://github.com/PulseRain/M10_high_speed_config_rtl/raw/master/docs/M10_high_speed_config_TRM.pdf

5.8.7 Simulation

To run the RTL simulation for the FPGA design, please follow the procedures mentioned in

Ref[14]: PulseRain M10 – Quick Start Guide, Doc#QSG-0922-0039, Rev 1.1, 09/2017
https://github.com/PulseRain/Arduino_M10_IDE/blob/master/docs/M10_quick_start.pdf

5.9 Repository

The schematic and PCB design files can be found in the following repository:

https://github.com/PulseRain/M10_PCB

And the repository for FP51-1T soft-core MCU can be found in

https://github.com/PulseRain/Mustang

5.10 Jumpers Settings

The FPGA programming mode and IO Voltage can be controlled by JP1 and JP6, as shown below in Table 5-3 and Figure 5-6.

Function	JP1	JP6
FPGA Program	N/A	ON
5V IO	5 V	OFF
3.3V IO	3.3 V	OFF

Table 5-3 Jumper Setting

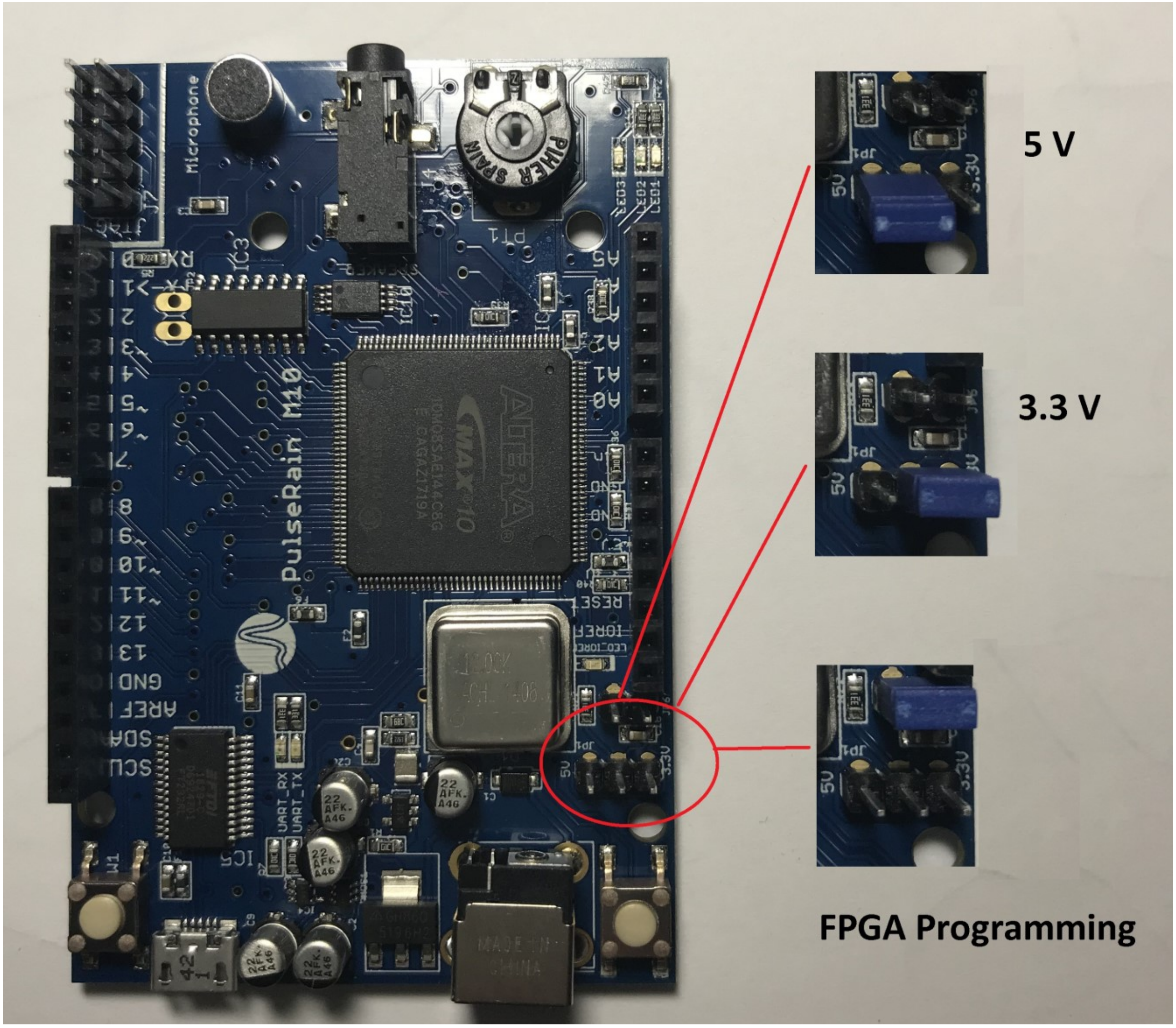

Figure 5-6 Jumper Setting