Multiplexed Comparator Example Project
1.0

Features

- Monitors multiple signals using a single comparator
- Analog multiplexer is used to change input and threshold signals
- Hardware solution and does not require CPU time

General Description

This example project is a PSoC Creator starter design. It shows how you can use PSoC 4 to create Multiplexed Comparator using Analog Hardware Mux, Comparator, IDAC, Control logic and Latch logic block without any CPU intervention. Control logic is implemented using Lookup Table (LUT) based decoder and counter component.

Development Kit Configuration

This example project is designed to run on the CY8CKIT-042 kit from Cypress Semiconductor. A description of the kit, along with more example programs and ordering information, can be found at http://www.cypress.com/go/cy8ckit-042.

The project requires configuration settings changes to run on other kits from Cypress Semiconductor. Table 1 is the list of the supported kits. To switch from CY8CKIT-042 to any other kit, change the project's device with the help of Device Selector called from the project's context menu.

Table 1. Development Kits vs Parts

Development Kit	Device
CY8CKIT-042	CY8C4245AXI-483
CY8CKIT-042-BLE	CY8C4247LQI-BL483
CY8CKIT-044	CY8C4247AZI-M485
CY8CKIT-046	CY8C4248BZI-L489

The pin assignments for the supported kits are in Table 2.

Table 2. Pin Assignment

Pin Name	Development Kit			
	CY8CKIT-042	CY8CKIT-042 BLE	CY8CKIT-044	CY8CKIT-046
Threshold	P1[1]	P1[1]	P1[7]	P1[1]
Input_1	P2[0]	P0[0]	P0[0]	P0[0]
Input_2	P2[1]	P0[5]	P0[1]	P0[1]
Input_3	P2[2]	P0[2]	P0[2]	P0[2]
Input_4	P2[3]	P0[4]	P0[3]	P0[3]
Threshold_1	P1[2]	P1[2]	P1[2]	P1[2]
Threshold_2	P1[3]	P1[3]	P1[3]	P1[3]
Threshold_3	P1[4]	P1[4]	P2[0]	P2[0]

Pin Name	Development Kit			
	CY8CKIT-042	CY8CKIT-042 BLE	CY8CKIT-044	CY8CKIT-046
Threshold_4	P1[5]	P1[5]	P2[1]	P2[1]
Channel_1	P3[0]	P3[0]	P3[0]	P3[0]
Channel_2	P3[1]	P3[1]	P3[1]	P3[1]
Channel_3	P3[4]	P3[4]	P3[4]	P4[4]
Channel_4	P3[5]	P3[5]	P3[5]	P4[5]

The following steps should be performed to observe the project operation:

1. Set Jumper J9 (J16 for CY8CKIT-042-BLE) to 5.0V position.
2. Connect four input signals to Input_1, Input_2, Input_3 and Input_4
3. Connect resistances R1(2.2K), R2(4.4K), R3(6.8K) and R4(8K) to Threshold_1, Threshold_2, Threshold_3 and Threshold_4, respectively as Figure 1 shows.
4. Observe the combined threshold signal on Threshold using an oscilloscope
5. Observe four output signals on Channel_1, Channel_2, Channel_3 and Channel_4

Note A note about a bonded pin appears during project compilation for the CY8CKIT-042-BLE kit, CY8CKIT-044 kit, which is expected taking into account the pins available for the user on these kits.

Project Configuration

The example project consists of Analog Hardware Mux (AmuxHw), Comparator, IDAC, Control logic and latch logic block. Control logic is implemented using LUT based decoder and counter component. The top design schematic is shown in Figure 1 and Figure 2. Amux_Input and Amux_Th components are used to select input signals and corresponding comparator thresholds. The comparator is used to compare the input signal with the threshold signal and generate output signal accordingly. The IDAC is used to generate threshold voltages for comparison. Sync Component synchronizes the comparator output with the high frequency clock.

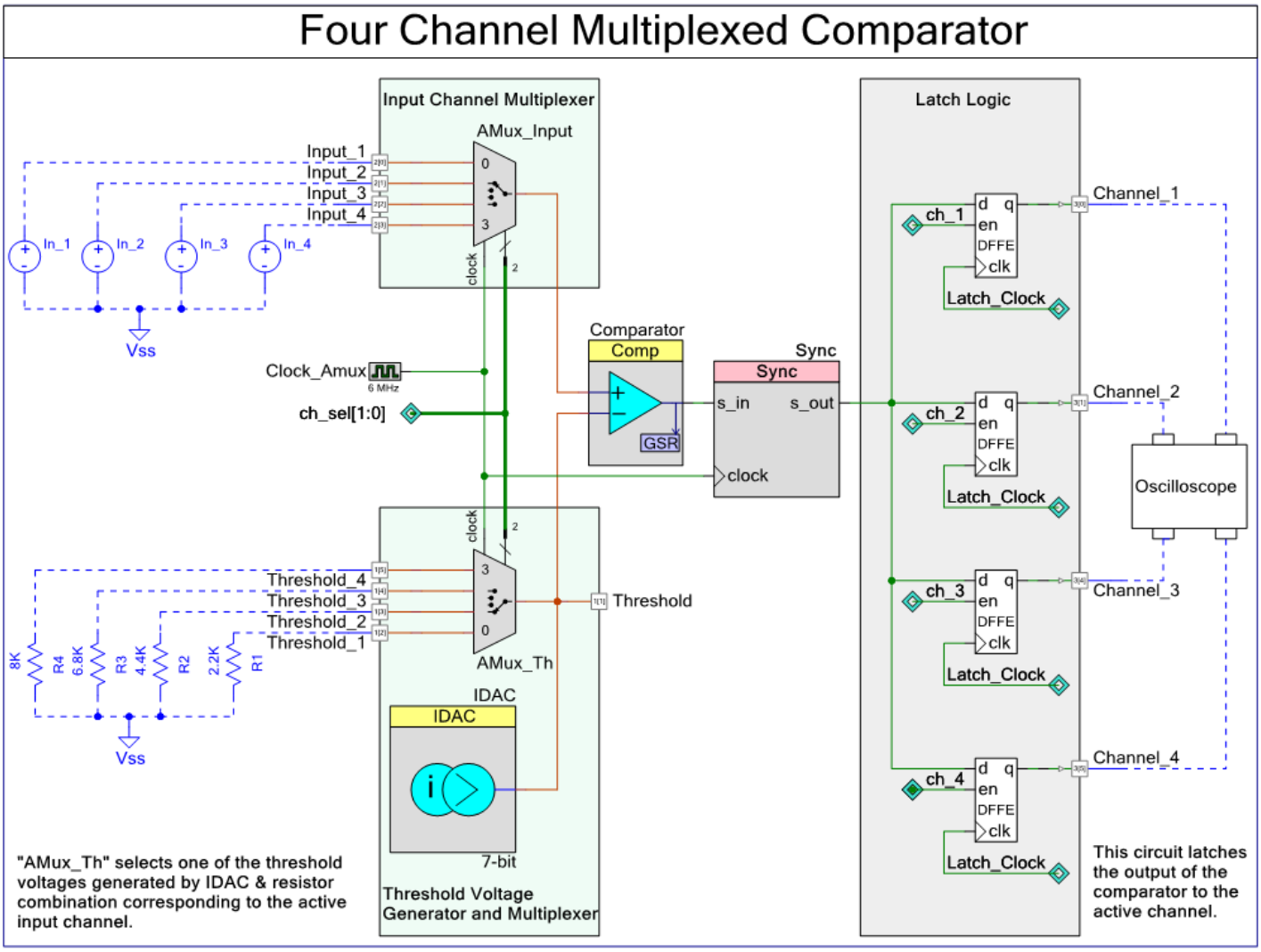

Figure 1. Top Design Schematic – Multiplexed Comparator (Page 1)

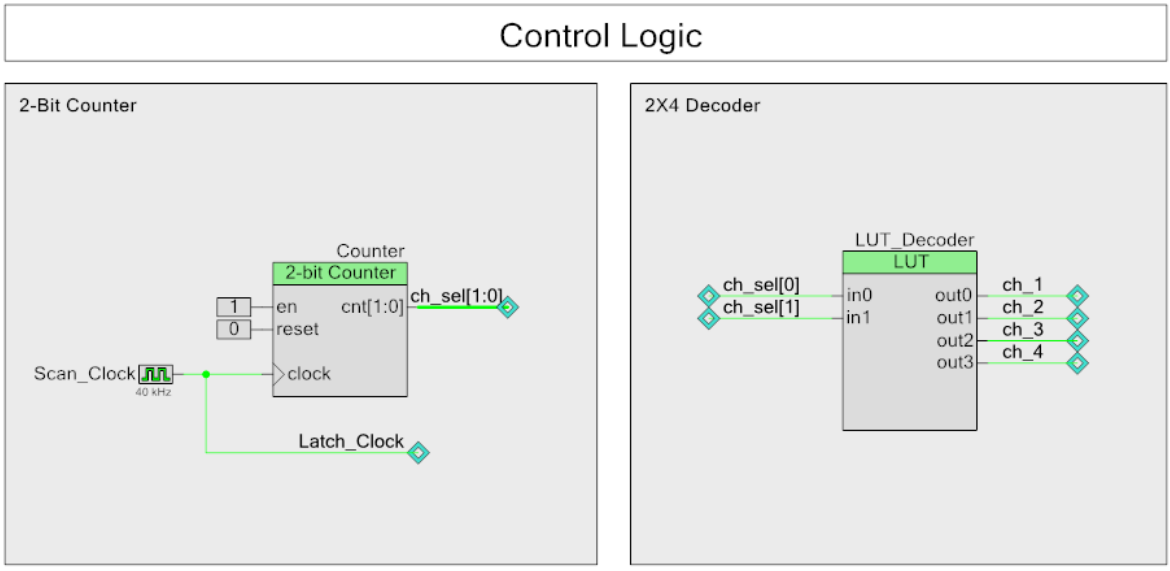

Figure 2. Top Design Schematic – Control Unit (Page 2)

The Analog Hardware Mux components are configured as 4 channel single ended mux mode. The comparator is configured in Fast speed non-inverting mode. Figure 3 shows the

IDAC component configuration window. Counter component is used to control the select line of multiplexer and LUT is implemented as decoder to control the output channel (LUT_Decoder). The D Flip-Flop latches the output signal till the next scan of the same channel.

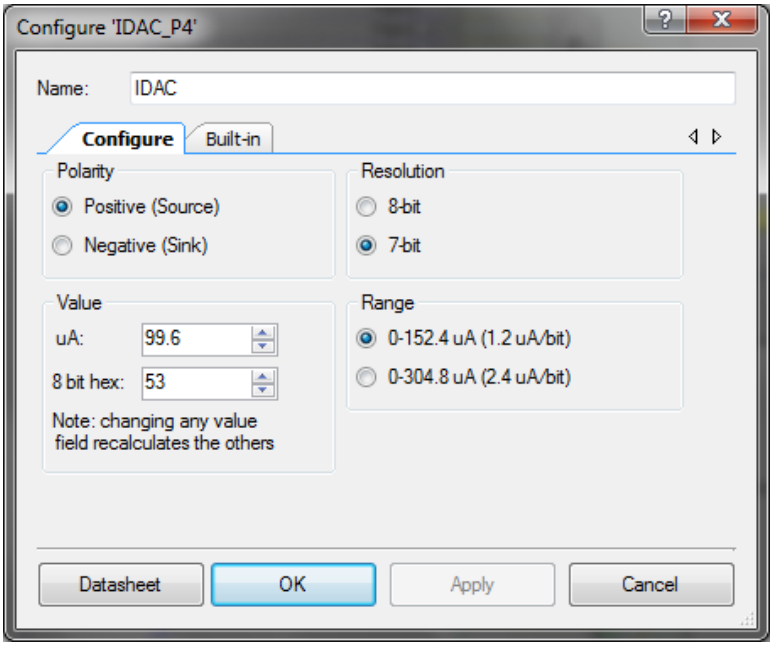

Figure 3. IDAC_P4 Component Configuration

Project Description

In the main function all components are started. Once started, at each clock pulse multiplexer sequentially switches input signals and threshold voltages. Threshold voltages are generated by the resistances connected to the IDAC through multiplexer. The input signal is compared to the corresponding threshold voltage and the output is fed to the latch logic block. Latch clock and channel select signal latches the comparator output to the active channel.

Expected Results

Threshold voltage fed to the comparator is like a staircase depending upon the resistances used. Resistance 2.2K, 4.4K, 6.8K and 8K are connected to reference pins as described in development kit configuration section with IDAC sourcing current of 100 micro-amps. Table 1 describes the threshold voltage levels generated using the resistors used. The input, threshold signal's and output waveform is shown in figure 4. The project is designed for Input signal frequency below 1 KHz.

S.No.	Resistor Value	Threshold Voltage (IDAC sourcing 100 uA current)
1	2.2 kΩ	~220 mV
2	4.4 kΩ	~440 mV
3	6.8 kΩ	~680 mV
4	8 kΩ	~800 mV

Table 1. Threshold Voltage Values

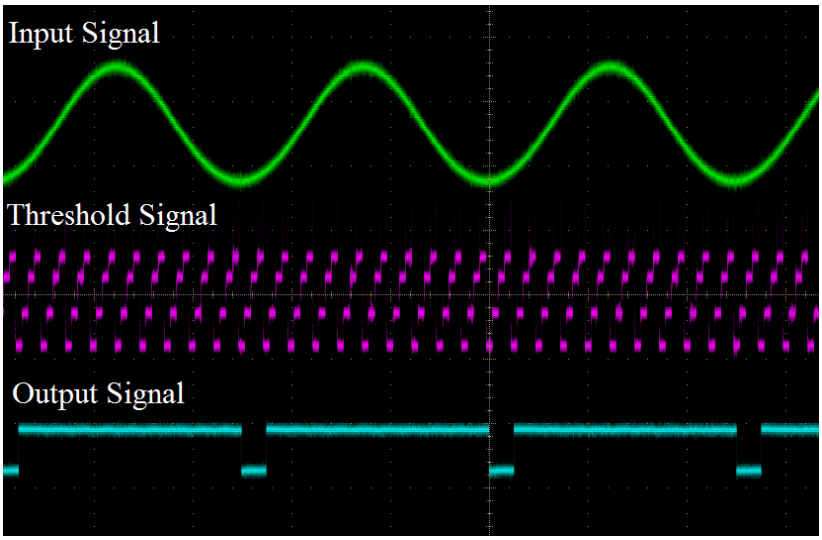

Figure 4. Output signal for 1KHz, $1V_{PP}$ input signal

Schematic

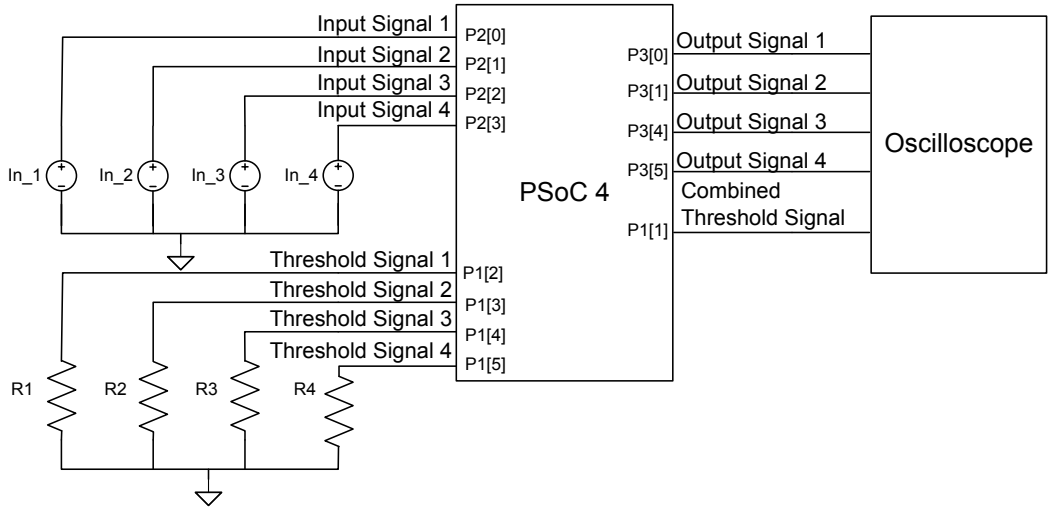

Figure 5. Connection Schematic

Note: Resistors below 20 kΩ can be used to generate threshold voltage as per the equation 'V=IR'.

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