SAM9G25 Microcontroller Schematic Check List

1. Introduction

This application note is a schematic review check list for systems embedding the Atmel® AT91SAM ARM®-based SAM9G25 Embedded MPU.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the SAM9G25. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.

AT91SAM ARM-based Embedded MPU

Application Note

11129A–ATARM–29-Jul-11

2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the SAM9G25 Microcontroller on Atmel's Web site.

Table 2-1 gives the associated documentation needed to support full understanding of this application note.

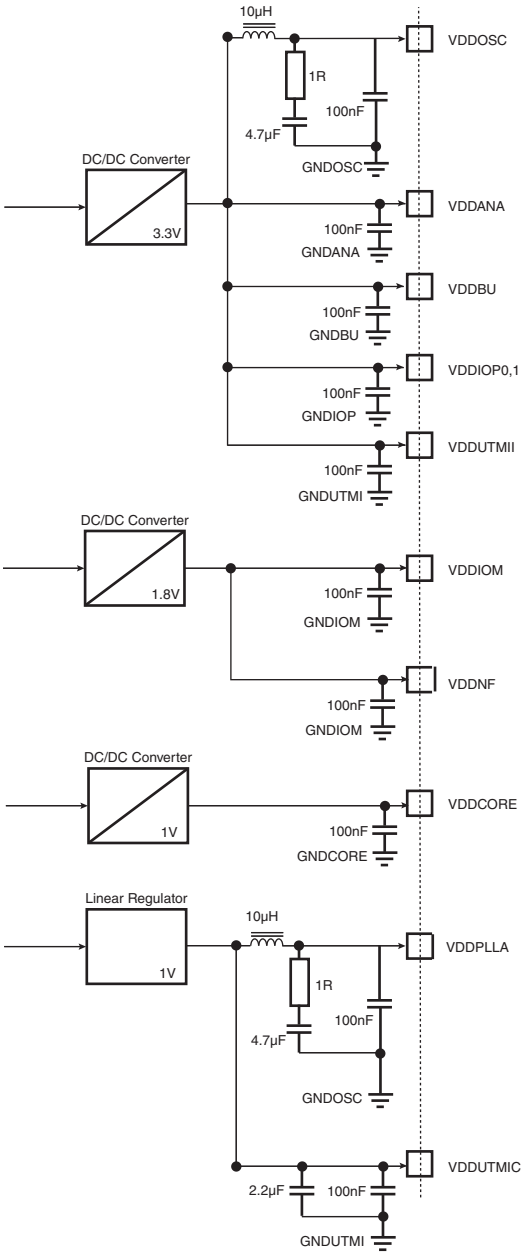
Table 2-1. Associated Documentation

Information	Document Title
User Manual Electrical/Mechanical Characteristics Ordering Information Errata	AT91SAM ARM-based Embedded MPU - SAM9G25 Datasheet
Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM9EJ-S™ Technical Reference Manual ARM926EJ-S™ Technical Reference Manual
Evaluation Kit User Guide	SAM9G25-EK User Guide

3. Schematic Check List

CAUTION: The AT91SAM9 board design must comply with the power-up and power-down sequence guidelines provided in the datasheet to guarantee reliable operation of the device.

1.0V, 1.8V and 3.3V Power Supplies Schematic Example(1)

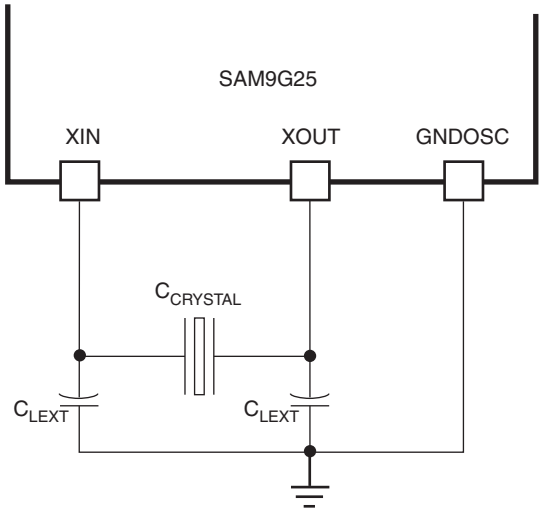


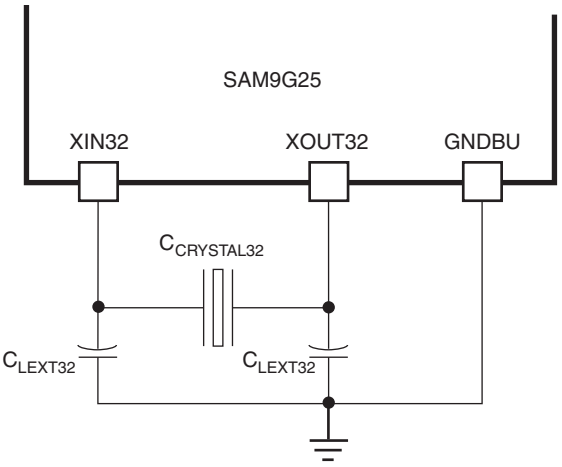
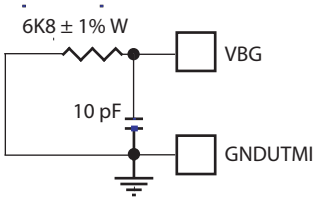
(1) These values are given only as a typical example

þ	Signal Name	Recommended Pin Connection	Description
	VDDCORE	0.9V to 1.1V Decoupling capacitor (100 nF)[1][2]	Powers the device. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop. Supply ripple must not exceed 20 mVrms.
	VDDPLLA	0.9V to 1.1V Decoupling/filtering RLC circuit[1]	Powers the PLLA cell. The VDDPLLA power supply pin draws small current, but it is noise sensitive. Care must be taken in VDDPLLA power supply routing, decoupling and also on bypass capacitors. Supply ripple must not exceed 10 mVrms.
	VDDNF	1.65V to 1.95V or 3.0V to 3.6V Decoupling capacitor (100 nF)[1][2]	The VDDNF power supply the NAND Flash I/Os
	VDDBU	1.8V to 3.6V Decoupling capacitor (100 nF)[1][2]	Powers the Backup unit. (Slow Clock Oscillator, On-chip RC and a part of the System Controller). Supply ripple must not exceed 30 mVrms.
	VDDOSC	1.65V to 3.6V Decoupling/Filtering RLC circuit[1]	Powers the main oscillator cells. The VDDOSC power supply pin draws small current, but it is noise sensitive. Care must be taken in VDDOSC power supply routing, decoupling and also on bypass capacitors. Supply ripple must not exceed 30 mVrms.
	VDDIOM	1.65V to 1.95V or 3.0V to 3.6V Decoupling capacitor (100 nF)[1][2]	Powers the External Memory Interface I/O lines. Dual voltage range supported. The I/O drives are selected by programming the EBI_DRIVE field in the CCFG_EBICSA register. At power-up, the high drive mode for 3.3V memories is selected. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDUTMII	3V to 3.6V Decoupling capacitor (100 nF)[1][2]	Powers the USB device and host UTMI+ interface. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDUTMIC	0.9V to 1.1V Decoupling/Filtering capacitors (100 nF and 2.2µF)[1][2]	Powers the USB device and host UTMI+ core. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.

þ	Signal Name	Recommended Pin Connection	Description
	VDDIOP0 VDDIOP1	1.65V to 3.6V Decoupling/Filtering capacitors (100 nF)[1][2]	Powers the peripherals I/O lines. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDANA	3.0V to 3.6V Decoupling/Filtering RLC circuit[1] Application dependent	Powers the Analog to Digital Converter (ADC) and some PIOD I/O lines.
	GNDCORE	Core Chip Ground	GNDCORE pins are common to VDDCORE pins. GNDCORE pins should be connected as shortly as possible to the system ground plane.
	GNDBU	Backup Ground	GNDBU pin is provided for VDDBU pins. GNDBU pin should be connected as shortly as possible to the system ground plane.
	GNDIOM	DDR2 and EBI I/O Lines Ground	GNDIOM pins are common to VDDIOM and VDDNF pins. GNDIOM pins should be connected as shortly as possible to the system ground plane.
	GNDIOP	Peripherals and ISI I/O lines Ground	GNDIOP pins are common to VDDIOP0, VDDIOP1 pins. GNDIOP pins should be connected as shortly as possible to the system ground plane.
	GNDOSC	PLLA, PLLUTMI and Oscillator Ground	GNDOSC pin is provided for VDDOSC, VDDPLLA pins. GNDOSC pin should be connected as shortly as possible to the system ground plane.
	GNDUTMI	UDPHS and UHPHS UTMI+ Core and interface Ground	GNDUTMI pins are common to VDDUTMII and VDDUTMIC pins. GNDUTMI pins should be connected as shortly as possible to the system ground plane.
	GNDANA	Analog Ground	GNDANA pins are common to VDDANA pins. GNDANA pins should be connected as shortly as possible to the system ground plane.

Note: For more information please refer to the Core Power Supply POR Characteristics section of the SAM9G25 Datasheet.

þ	Signal Name	Recommended Pin Connection	Description
Clock, Oscillator and PLL			
	XIN XOUT 12 MHz Main Oscillator in Normal Mode	Crystals between 8 and 16 MHz USB High Speed (not Full Speed) Host and Device peripherals need a 12 MHz clock. Capacitors on XIN and XOUT (crystal load capacitance dependent)	Crystal load capacitance to check ($C_{CRYSTAL}$).  Example: for a 12 MHz crystal with a load capacitance of $C_{CRYSTAL}$= 15 pF, external capacitors are required: C_{LEXT} = 22 pF. Refer to the electrical specifications of the SAM9G25 Datasheet
	XIN XOUT 12 MHz Main Oscillator in Bypass Mode	XIN: external clock source XOUT: can be left unconnected USB High speed (not Full Speed) Host and Device peripherals need a 12 MHz clock.	VDDOSC square wave signal External clock source up to 50 MHz Duty Cycle: 40 to 60% Refer to the electrical specifications of the SAM9G25 Datasheet
	XIN XOUT 12 MHz Main Oscillator Only	XIN: can be left unconnected XOUT: can be left unconnected USB High speed (not Full Speed) Host and Device peripherals need a 12 MHz clock.	Typical nominal frequency 12 MHz Duty Cycle: 45 to 55% Refer to the electrical specifications of the SAM9G25 Datasheet

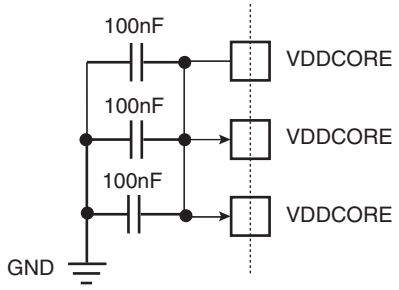
þ	Signal Name	Recommended Pin Connection	Description
	XIN32 XOUT32 Slow Clock Oscillator	32.768 kHz Crystal Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent)	Crystal load capacitance to check ($C_{CRYSTAL32}$).  Example: for a 32.768 kHz crystal with a load capacitance of $C_{CRYSTAL32}$= 12.5 pF, external capacitors are required: C_{LEXT32} = 19 pF. Refer to the electrical specifications of the SAM9G25 Datasheet
	XIN32 XOUT32 Slow Clock Oscillator in Bypass Mode	XIN32: external clock source XOUT32: can be left unconnected	VDDBU square wave signal External clock source up to 44 kHz Refer to the electrical specifications of the SAM9G25 Datasheet
	VBG	0.9 - 1.1V(5)	Bias Voltage Reference for USB To reduce as much as possible the noise on VBG pin please check the Layout consideration below: - VBG path as short as possible - ground connection to GNDUTMI  Refer to the Signal Description List of the SAM9G25 Datasheet

þ	Signal Name	Recommended Pin Connection	Description
ICE and JTAG[3]			
	TCK	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TMS	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TDI	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TDO	Floating	Output driven at up to $V_{VDDIOP0}$
	RTCK	Floating	Output driven at up to $V_{VDDIOP0}$
	NTRST	Please refer to the Pin Description of the SAM9G25 Datasheet	This pin is a Schmitt trigger input. Internal pull-up resistor to $V_{VDDIOP0}$ (100 kOhm).
	JTAGSEL	In harsh environments,[4] It is strongly recommended to tie this pin to GNDBU if not used or to add an external low-value resistor (such as 1 kOhm).	Internal pull-down resistor to GNDBU (15 kOhm). Must be tied to V_{VDDBU} to enter JTAG Boundary Scan.
Reset/Test			
	NRST	Application dependent. Can be connected to a push button for hardware reset.	**NRST is a bidirectional pin** (Schmitt trigger input). It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. By default, the **User Reset is enabled** after a General Reset so that it is possible for a component to assert low and reset the microcontroller. An internal pull-up resistor to $V_{VDDIOP0}$ (100 kOhm) is available for User Reset and External Reset control.
	TST	**In harsh environments,[4] It is strongly recommended to tie this pin to GNDBU if not used or to add an external low-value resistor (such as 1 kOhm)**	This pin is a Schmitt trigger input. Internal pull-down resistor to GNDBU (15 kOhm).
	BMS	Application dependent.	Must be tied to $V_{VDDIOP0}$ to boot from Embedded ROM. Must be tied to GNDIOP to boot from external memory (EBI Chip Select 0).

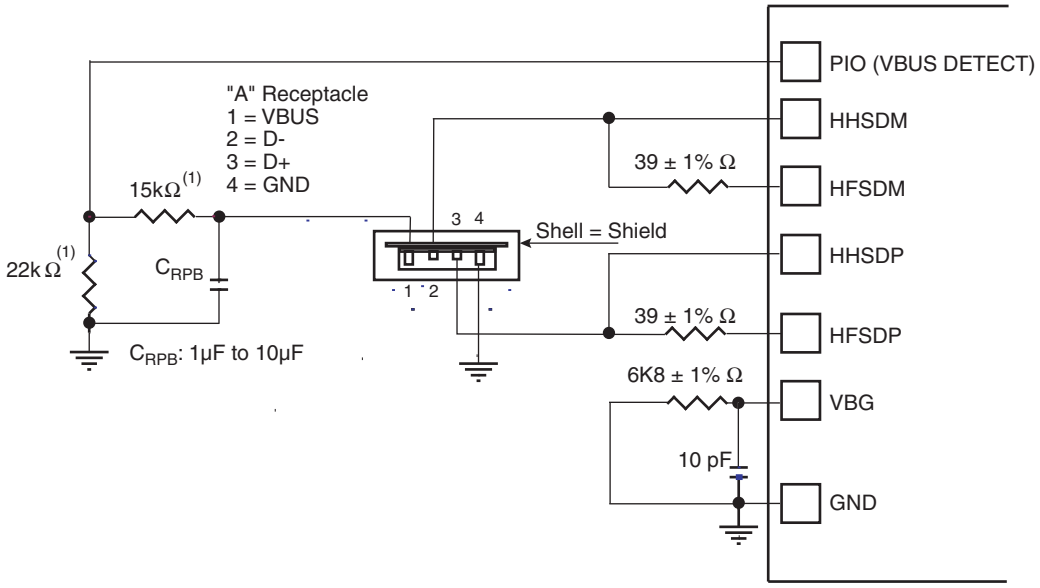
þ	Signal Name	Recommended Pin Connection	Description
Shutdown/Wakeup Logic			
	SHDN	Application dependent. A typical application connects the pin SHDN to the shutdown input of the DC/DC Converter providing the main power supplies.	This pin is a push-pull output. SHDN pin is driven low to GNDBU by the Shutdown Controller (SHDWC).
	WKUP	0V to V_{VDDBU}	This pin is an input-only. WKUP behavior can be configured through the Shutdown Controller (SHDWC).
PIO			
	PAx PBx PCx PDx	Application dependent.	All PIOs are pulled-up inputs (100 kOhms) at reset except those which are multiplexed with the Address Bus signals that require to be enabled as peripherals: Refer to the column “Reset State” of the Pin Description table in the I/O Description section of the SAM9G25 Datasheet. Schmitt Trigger on All Inputs To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at ‘0’ with internal pull-up disabled.
ADC			
	TSADVREF	2.4V to VDDANA Decoupling/Filtering capacitors. Application dependent	ADVREF is a pure analog input. To reduce power consumption, if ADC is not used: connect ADVREF to GNDANA.
EBI			
	D0-D31	Application dependent.	Data Bus (D0 to D31) D0-D15 lines are pulled-up inputs to V_{DDIOM} at reset. D16-D31 lines are pulled-up inputs to V_{VDDNF} at reset. Note: D16 to D31 are multiplexed with the PIOD controller.
	A0-A25	Application dependent.	Address Bus (A0 to A25) All address lines are driven to ‘0’ at reset. Note: A20 to A25 are multiplexed with the PIOD controller.

þ	Signal Name	Recommended Pin Connection	Description
DDR2 - SMC - SDRAM Controller - NAND Flash Support			
See “External Bus Interface (EBI) Hardware Interface” on page 12.			
USB High Speed Host (UHPHS)			
	HFSDPA/HFSDPB HHSDPA/HHSDPB	Application dependent.(5)	Integrated pull-down resistor to prevent over consumption when the host is disconnected.
	HFSDMA/HFSDMB HHSDMA/HHSDMB	Application dependent.(5)	Integrated pull-down resistor to prevent over consumption when the host is disconnected.
USB Full Speed Host (UHPHS)			
	HFSDPC	Application dependent.(5)	Integrated pull-down resistor to prevent over consumption when the host is disconnected.
	HFSDMC	Application dependent.(5)	Integrated pull-down resistor to prevent over consumption when the host is disconnected.
USB High Speed Device (UDPHS)			
	DHSDM/DFSDP	Application dependent(6)	Integrated programmable pull-up resistor. Integrated programmable pull-down resistor to prevent over consumption when the host is disconnected. To reduce power consumption, if USB Device is not used, connect the embedded pull-up.
	DHSDP/DFSDM	Application dependent(6)	Integrated programmable pull-down resistor to prevent over consumption when the host is disconnected. To reduce power consumption, if USB Device is not used, connect the embedded pull-down.

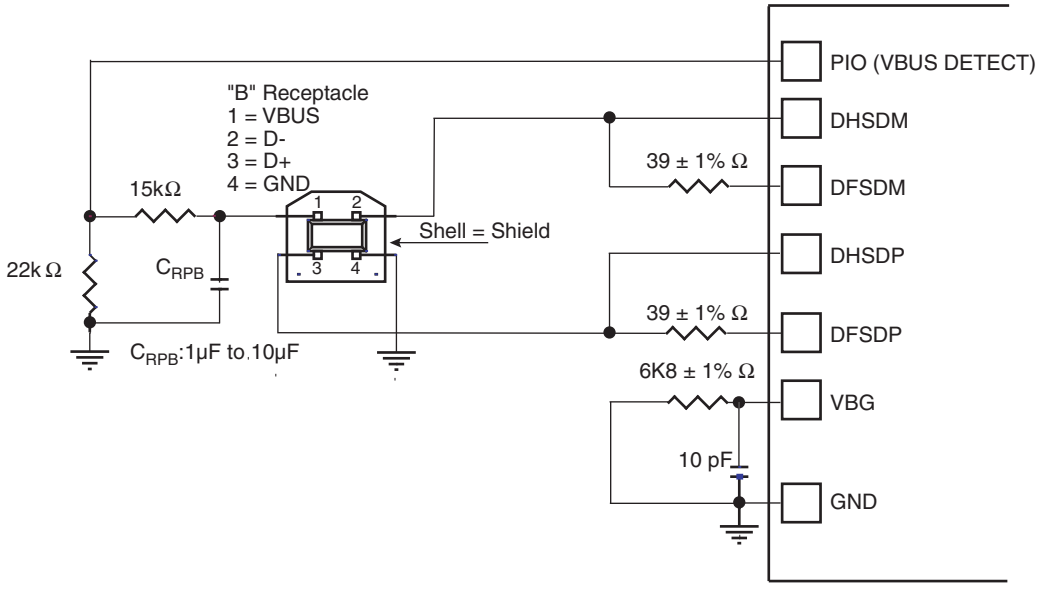
Notes: 1. These values are given only as a typical example.
2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



3. It is recommended to establish accessibility to a JTAG connector for debug in any case.
4. In a well-shielded environment subject to low magnetic and electric field interference, the pin may be left unconnected. In noisy environments, a connection to ground is recommended.
5. Example of USB High Speed Host connection:
   A termination 39 Ohm serial resistor must be connected to HFSDPx and HFSDMx. More details are in the USB Host High Speed Port section of the SAM9G25 Datasheet.



6. Typical USB High Speed Device connection:
   As there is an embedded pull-up, no external circuitry is necessary to enable and disable the 1.5 k Ohm pull-up.
   A termination 39 Ohm serial resistor must be connected to DFSDP and DFSDM. More details are in the USB High Speed Device Port section of the SAM9G25 Datasheet.



4. External Bus Interface (EBI) Hardware Interface

These tables detail the connections to be applied between the EBI pins and the external devices for each Memory Controller.

Table 4-1. EBI Pins and External Static Devices Connections

Signals: EBI_	Pins of the Interfaced Device					
	8-bit Static Device	2 x 8-bit Static Devices	16-bit Static Device	4 x 8-bit Static Devices	2 x 16-bit Static Devices	32-bit Static Device
Controller	**SMC**					
D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7
D8 - D15	–	D8 - D15	D8 - D15	D8 - D15	D8 - 15	D8 - 15
D16 - D23	–	–	–	D16 - D23	D16 - D23	D16 - D23
D24 - D31(5)	–	–	–	D24 - D31	D24 - D31	D24 - D31
A0/NBS0	A0	–	NLB	–	NLB(3)	BE0
A1/NWR2/NBS2/DQM2	A1	A0	A0	WE(2)	NLB(4)	BE2
A2 - A22(5)	A[2:22]	A[1:21]	A[1:21]	A[0:20]	A[0:20]	A[0:20]
A23 - A25(5)	A[23:25]	A[22:24]	A[22:24]	A[21:23]	A[21:23]	A[21:23]
NCS0	CS	CS	CS	CS	CS	CS
NCS1/DDRSDCS	CS	CS	CS	CS	CS	CS
NCS2(5)	CS	CS	CS	CS	CS	CS
NCS3/NANDCS	CS	CS	CS	CS	CS	CS
NCS4(5)	CS	CS	CS	CS	CS	CS
NCS5(5))	CS	CS	CS	CS	CS	CS
NRD	OE	OE	OE	OE	OE	OE
NWR0/NWE	WE	WE(1)	WE	WE(2)	WE	WE
NWR1/NBS1	–	WE(1)	NUB	WE(2)	NUB(3)	BE1
NWR3/NBS3/DQM3	–	–	–	WE(2)	NUB(4)	BE3

Notes:
1. NWR0 enables lower byte writes. NWR1 enables upper byte writes.
2. NWRx enables corresponding byte x writes (x = 0,1,2 or 3).
3. NBS0 and NBS1 enable respectively lower and upper bytes of the lower 16-bit word.
4. NBS2 and NBS3 enable respectively lower and upper bytes of the upper 16-bit word.
5. Multiplexed pins with PD15-PD31.

Table 4-2. EBI Pins and External Device Connections

Signals: EBI_	Pins of the Interfaced Device		
	DDR2/LPDDR	**SDRAM**	**NAND Flash**
Controller	**DDRC**	**SDRAMC**	**NFC**
D0 - D15	D0 - D15	D0 - D15	NFD0-NFD15(1)
D16 - D31	–	D16 - D31	NFD0-NFD15(1)–
A0/NBS0	–	–	–
A1/NWR2/NBS2/DQM2	–	DQM2	–

Table 4-2. EBI Pins and External Device Connections (Continued)

Signals: EBI_	Pins of the Interfaced Device		
Controller	**DDR2/LPDDR**	**SDRAM**	**NAND Flash**
	DDRC	**SDRAMC**	**NFC**
DQM0-DQM1	DQM0-DQM1	DQM0-DQM1	–
DQS0-DQM1	DQS0-DQS1	–	–
A2 - A10	A[0:8]	A[0:8]	–
A11	A9	A9	–
SDA10	A10	A10	–
A12	–	–	–
A13 - A14	A[11:12]	A[11:12]	–
A15	A13	A13	–
A16/BA0	BA0	BA0	–
A17/BA1	BA1	BA1	–
A18/BA2	BA2	BA2	–
A19-A20	–	–	–
A21/NANDALE	–	–	ALE
A22/NANDCLE	–	–	CLE
A23 - A24	–	–	–
A25	–	–	–
NCS0	–	–	–
NCS1/DDRSDCS	DDRCS	SDCS	–
NCS2	–	–	–
NCS3/NANDCS	–	–	CE
NCS4	–	–	–
NCS5	–	–	–
NANDOE	–	–	OE
NANDWE	–	–	WE
NRD	–	–	–
NWR0/NWE	–	–	–
NWR1/NBS1	–	–	–
NWR3/NBS3/DQM3	–	DQM3	–
CFCE1	–	–	–
CFCE2	–	–	–
SDCK	CK	CK	–
SDCK#	CK#	–	–
SDCKE	CKE	CKE	–
RAS	RAS	RAS	–
CAS	CAS	CAS	–
SDWE	WE	WE	–
Pxx[2]	–	–	CE
Pxx[2]	–	–	RDY

Notes: 1. A switch, NFD0_ON_D16, enables the user to select Nand Flash path on D0-D7 or D16-D24 depending on memory power supplies. this switch is located in the EBICSA register in the Bus Matrix User Interface.

2. Any PIO line.

5. AT91SAM Boot Program Hardware Constraints

See the Boot Strategies section of the SAM9G25 Datasheet for more details on the boot program.

5.1 AT91SAM Boot Program Supported Crystals (MHz)

A 12 MHz Crystal or external clock (in bypass mode) is mandatory in order to generate USB and PLL clocks correctly for the following boots.

5.2 NAND Flash Boot

Boot is possible if the first page contains a valid header or if it is ONFI compliant. For more details please check the section Nand Flash Boot of the SAM9G25 Datasheet.

Booting on a 16-bit NAND Flash devices is not possible.

Table 5-1. Pins Driven during NAND Flash Boot Program Execution

Peripheral	Pin	PIO Line
EBI CS3 SMC	NANDCS	PD4
EBI CS3 SMC	NAND ALE	A21
EBI CS3 SMC	NAND CLE	A22
EBI CS3 SMC	Cmd//Addr/Data	D[7:0] or D[23:16]

5.3 SD Card Boot

SD Card Boot supports all SD Card memories compliant with SD Memory Card Specification V2.0. This includes SDHC cards.

Table 5-2. Pins Driven during SD Card Boot Program Execution

Peripheral	Pin	PIO Line
MCI0	MCI0_CK	PA17
MCI0	MCI0_CD	PA16
MCI0	MCI0_D0	PA15
MCI0	MCI0_D1	PA18
MCI0	MCI0_D2	PA19
MCI0	MCI0_D3	PA20

5.4 Serial and DataFlash® Boot

Two kinds of SPI Flash are supported, SPI Serial Flash and SPI DataFlash.

The SPI Flash bootloader tries to boot on SPI0 Chip Select 0, first looking for SPI Serial Flash, and then for SPI DataFlash.

The SPI Flash Boot program supports:

- all Serial Flash devices
- all Atmel DataFlash devices

Table 5-3. Pins Driven during Serial or DataFlash Boot Program Execution

Peripheral	Pin	PIO Line
SPI0	MOSI	PA12
SPI0	MISO	PA11
SPI0	SPCK	PA13
SPI0	NPCS0	PA14

5.5 TWI EEPROM Boot

The TWI EEPROM Flash Boot program searches for a valid application in an EEPROM memory.

TWI EEPROM Boot supports all I2C-compatible EEPROM memories using 7 bits device (Address 0x50).

Table 5-4. Pins Driven during TWI EEPROM Boot Program Execution

Peripheral	Pin	PIO Line
TWI0	TWD0	PA30
TWI0	TWCK0	PA31

5.6 SAM-BA® Boot

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

Table 5-5. Pins Driven during SAM-BA Boot Program Execution

Peripheral	Pin	PIO Line
DBGU	DRXD	PA9
DBGU	DTXD	PA10

Revision History

Doc. Rev	Comments	Change Request Ref.
A	First issue	

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