SONY

Wideband (UHF-3800MHz) Configurable MMIC Power Amplifier (PA) Solution for LTE Terminal and Infrastructure Applications

CXGxxxx

Preliminary

Description

The CXGxxxx is an ultra wideband packaged PA capable of being configured in output power and gain for a range of applications including LTE mobile terminals, Machine-Machine applications and BS intrastructure requirements. The low knee voltage SONY GaAs JPHEMT process is used to achieve both high power and best-in-class efficiency over a wide range of operating voltage and output power distributions.

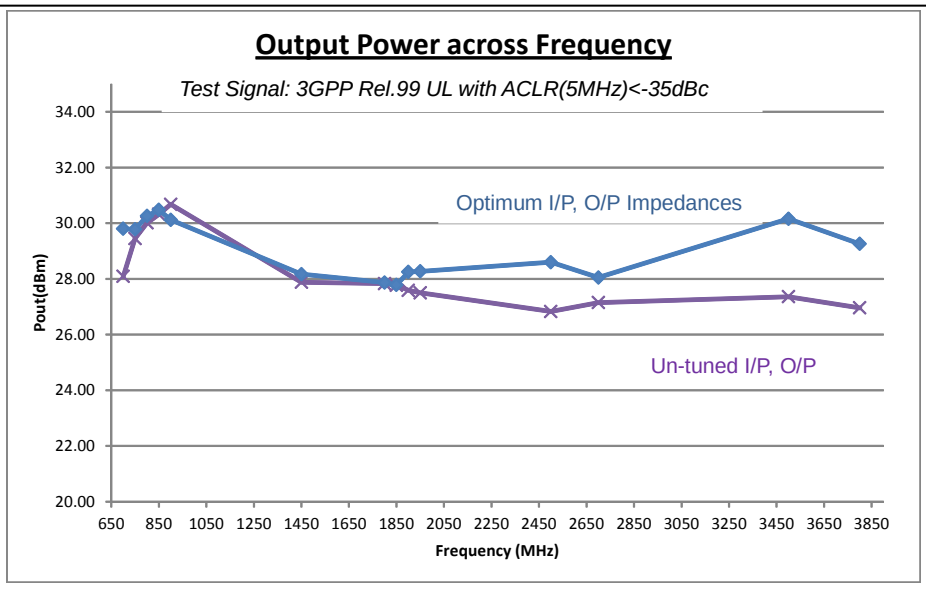
Applications:

- Wideband LTE Terminal: +28dBm typical
- Wideband Femto-Cell BS: +16dBm, +21dBm
- Wideband Enterprise BS +28dBm: based upon use of several devices
- Wideband Radio Requirements: White Space, ISM band

Features

- 3V or 5V operation (max of 6V). High efficiency operation down to below 1.5V for lower TX powers (eg <15dBm)
- Best in class efficiency when operated in either Linear or ET (Envelope Tracking) mode
- Supports all current 3GPP LTE bands in FDD or TDD mode
- Can be used as a final stage high efficiency ET or linear output stage for LTE terminals or as 2 stage for higher gain
- Linear output powers up to 31dBm depending upon PAPR. Maximum saturated power of 35dBm at 5V.
- Suitable as a wideband high efficiency driver for high power transmitters
- Femto-cell applications (16/21dBm): -50dBc ACLR (5MHz) with 10.6dB PAPR DL test signal and +16dBm O/P Power
- Small size (3.2 x 2.4 x 0.8 mm) plastic package.
- Standard additional passive components required for bias and matching
- Input and Output matches close to 50 Ohms across frequency but impedance tuning required to achieve optimum performance for application.
- Optimum matching across frequency can be achieved electronically using impedance tuner ICs (eg CXM3624UR)
- Lead-Free and RoHS Compliant.

Typical Characteristics



Typical Performance at 3.5V supply with Tuned I/P & O/P with 3GPP Rel.99 Uplink Signal & ACLR(5MHz) of <-35dBc:

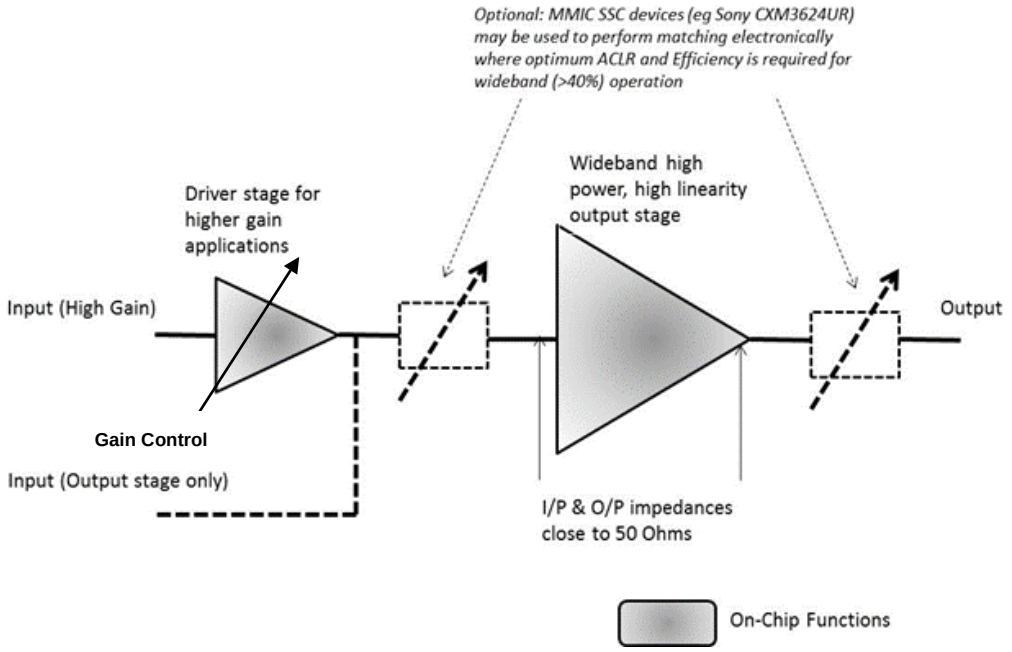
Output Power:
28-30dBm

Power added Efficiency:
45% (<2700MHz)
35% (>3000MHz)

Gain (Single Stage operation):
25dB (<1250MHz)
12dB min(3800MHz)

Gain (2 Stage operation):
28dB (<1250MHz)
20dB min (3800MHz)

Schematic



PIN-OUT & Package Dimensions

PIN	Description
1	Vd1 output stage (connect to supply via Ld1)
2, 6, 7, 10, 11, 13, 19, 20	GND
3	DC Ground 2 (ground via inductor LS2)
4	Vd2 output stage (connect to supply via Ld2)
5	DC Ground 3 (ground via inductor LS3)
8	RF Output (DC coupled). Vd3 output stage (connect to supply via Ld3)
9	Vg3 output stage
12	Driver RF Input
14	Vg driver
15	Vd driver (connect to supply via Ldriver)
16	Output Stage RF Input (connect pin 16 to pin 15 for 2 stage operation)
17	Vg2 output stage
18	Vg1 output stage