QuickFeather Low Power MCU Open Source Hardware Development Kit User Guide (Rev 1.2)

This document serves as a guide for the user to getting started with the QuickFeather revision 1.2 board.

This guide provides users with functional descriptions, configuration options for the QuickFeather Low Power MCU Open Source Hardware Development Kit Rev 1.2. It also serves as a "Getting Started" and "How To" guide.

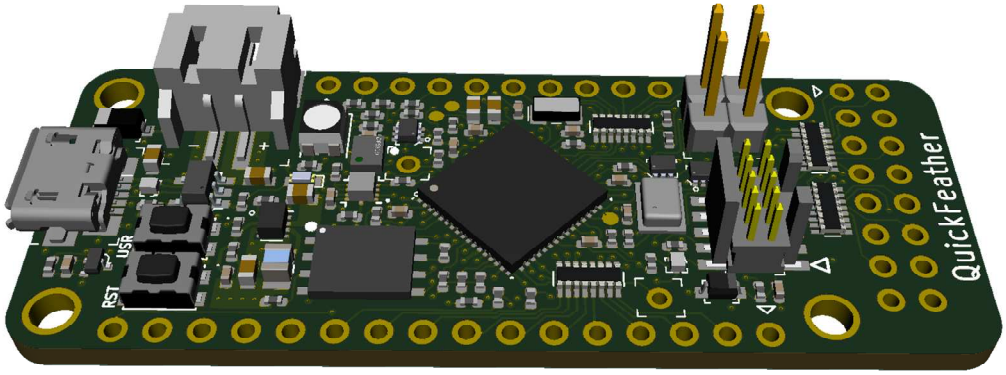

Figure 1: QuickFeather Low Power MCU Open Source Hardware Development Kit

QuickFeather Low Power MCU Open Source Hardware Development Kit Overview

The QuickFeather Low Power MCU Open Source Hardware Development Kit (HDK) is a small form factor system ideal for enabling the next generation of low-power Machine Learning (ML) capable IoT devices. Unlike other development kits which are based on proprietary hardware and software tools, QuickFeather is based on 100% open source hardware, compatible with the Adafruit Feather form factor, and is built around 100% open source software (including the Symbiflow FPGA Tools).

The QuickFeather HDK is powered by QuickLogic's EOS™ S3 (https://www.quicklogic.com/products/eos-s3/), the first eFPGA-enabled Arm Cortex®-M4F MCU to be fully supported with Zephyr RTOS and FreeRTOS. Other functionality includes:

- QuickLogic EOS S3 MCU Platform
- mCube MC3635 accelerometer
- Infineon DPS310 pressure sensor
- Infineon IM69D130 MEMS microphone
- 16Mbit of on-board flash memory
- User button and RGB LED
- Powered from USB or a single Li-Po battery

- Integrated battery charger
- USB data signals tied to programmable logic
- IO signals break-routed into general purpose pinheads
- Compatible with standard 0.1" breadboards

Benefits

- QuickFeather HDK is small, Feather compatible, inexpensive, and is 100% supported by open source tools.
- With a Cortex M4F MCU and integrated eFPGA, the EOS S3 lets you innovate with 100% open source hardware and software.

Applications

- Tiny ML applications (such as with SensiML's AI Software Platform and Google's TensorFlow Lite)
- General purpose MCU applications

Getting Started

What You Need

- 1 × QuickFeather HDK Rev 1.2 development board
- 1 x Micro-USB 2.0 cable[1], Type A to Micro B for Power
- Laptop (Win10 OS[2] or Linux OS) running terminal program (such as PuTTY[3] or any UART console application)

Note[1, 2]:

[1] you will need to provide your own USB cable

[2] Windows 7 and Windows 8 are not supported

[3] PuTTY download & installation: https://www.putty.org/

Running pre-loaded program from Flash

The purpose of the pre-loaded program is to make it very fast and straightforward for a new user to verify the board is functioning correctly. While we do production testing of every QuickFeather HDK before we ship, sometimes things happen during shipping or storage. Running this test takes less than a minute to do, requires no knowledge of the HDK, and will give you peace of mind the HDK is ready for you to start innovating freely.

1. Make sure there is no shunt installed at J7 and J1; if there are shunts installed, remove the shunts; save the shunts for future firmware development
2. Provide power to the QuickFeather HDK using the micro USB cable; the power source can be either a PC or wall adapter. When there is power applied to the board, the LED flashes “white” for a short duration
3. Press the “reset” button
4. The LED flashes blue color for 5 seconds and then turns off
5. Wait for 5 seconds
6. On Windows 10 machine, open Device Manager to check for the assign COM port

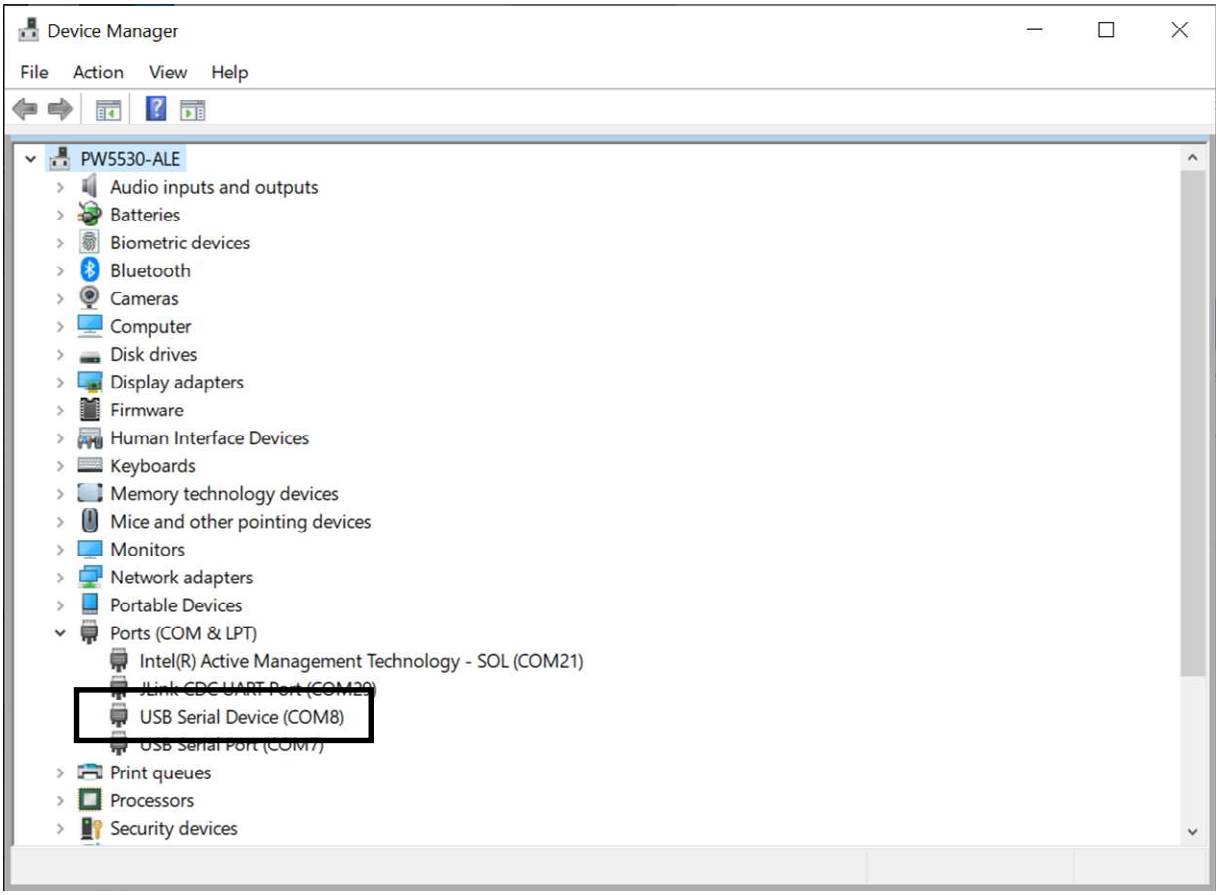

Figure 2: Checking COM Port with Device Manager

Note: for Win10 system, the system device manager may not fully configure QuickFeather as COM port when install for the first time, repeat step (3) to (6).

7. Launch PuTTY application and configure for Serial access and select “Open”

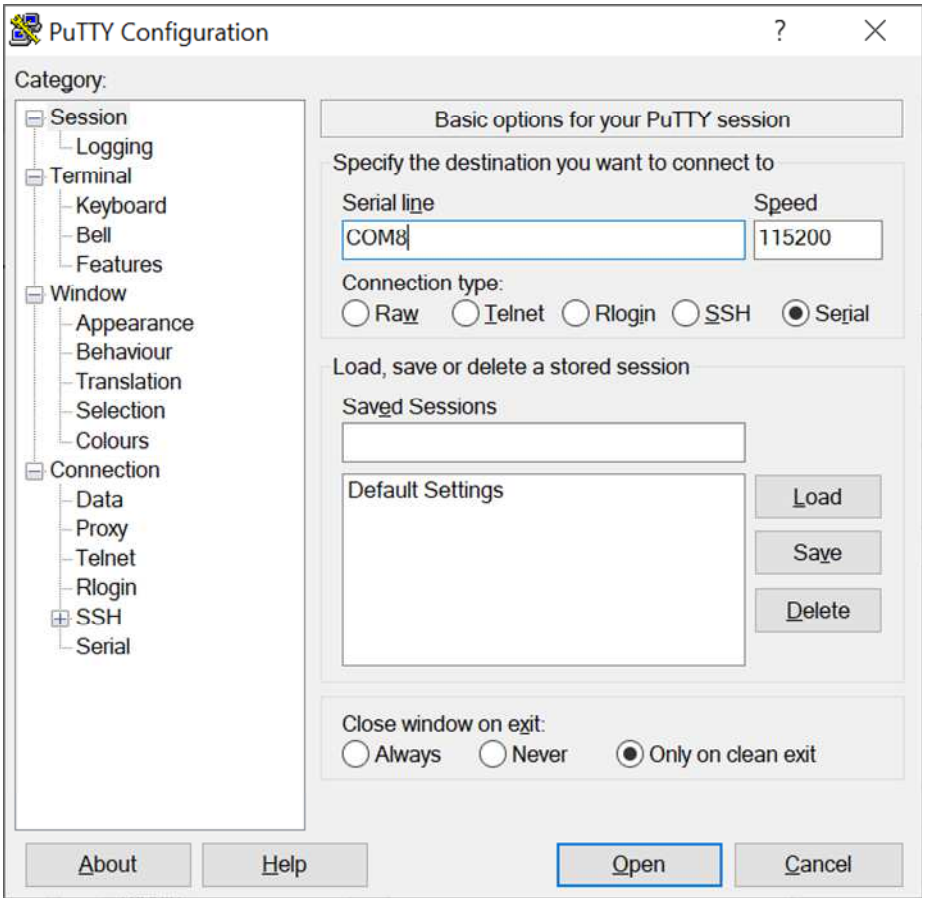

Figure 3: Checking COM Port with Device Manager

8. Perform the followings in the PuTTY terminal:

   a) Type: “diag” to bring up QuickFeather diagnostic menu
   b) Type: “help” to bring up the menu of commands
   c) Type: “red”; the command shows red color for LED
   d) Type: “red”; the LED turns off the LED
   e) Try “green” and “blue” command

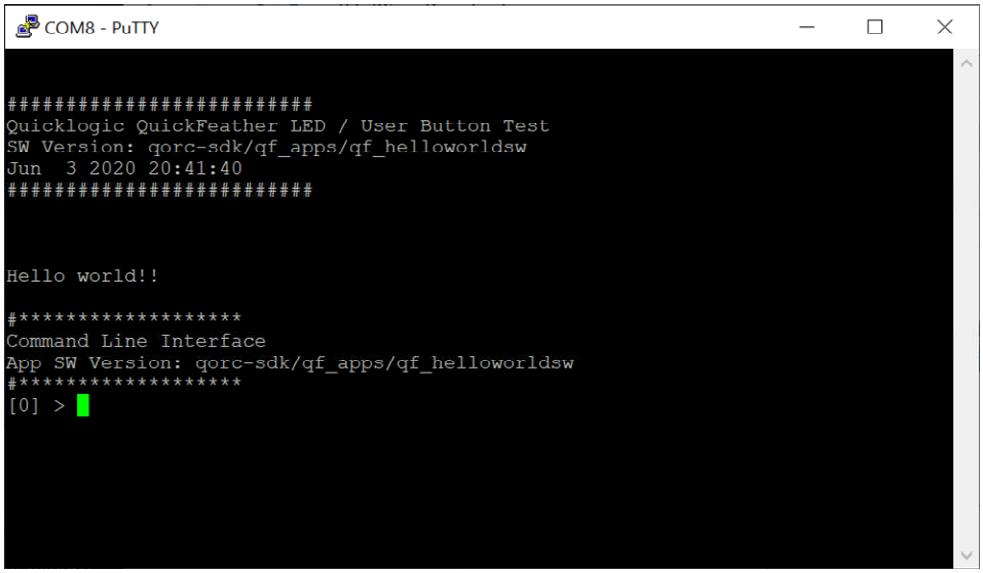

Figure 4: Example of Hello World application menu

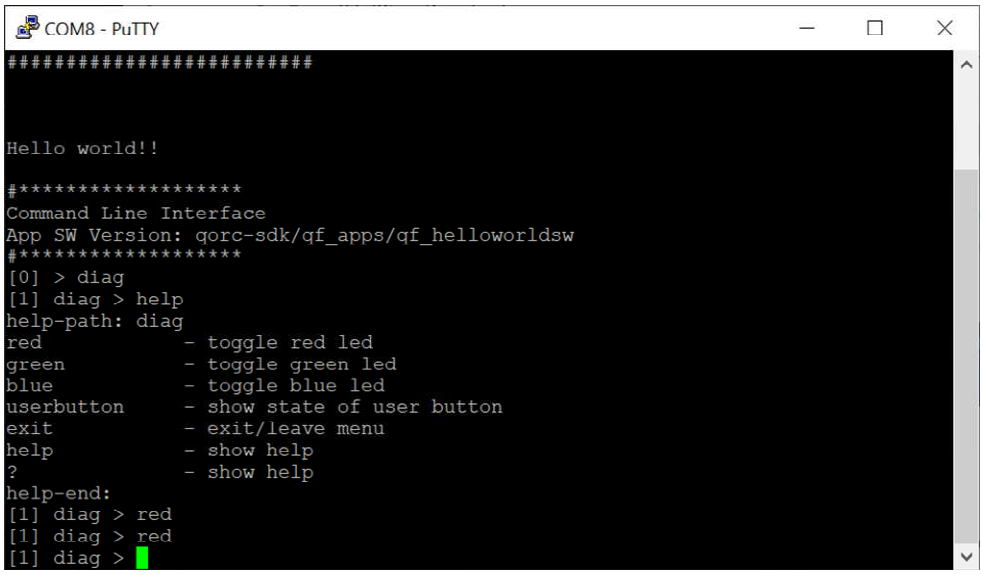

Figure 5: Example of diagnostic menu

Board Layout Overview

Components on the Board

- QuickLogic EOS S3 MCU Platform
- mCube MC3635 accelerometer
- Infineon DPS310 pressure sensor
- Infineon IM69D130 MEMS microphone
- 16Mbit of on-board flash memory
- User button and RGB LED
- Hardware Reset button
- Powered from USB or a single Li-Po battery
- Integrated battery charger
- USB data signals tied to programmable logic
- IO signals break-routed into general purpose pinheads

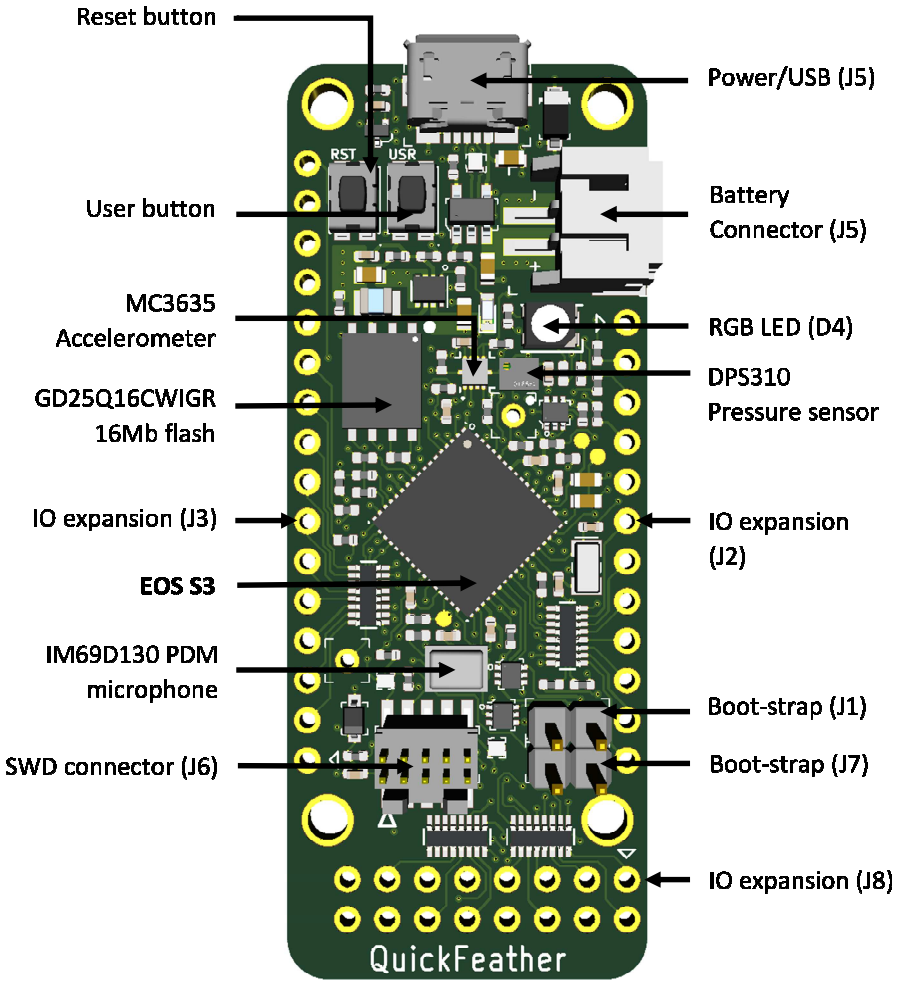

Figure 6: QuickFeather HDK Board Layout Overview

IO Expansion Connectors

EOS S3 MCU IO Map

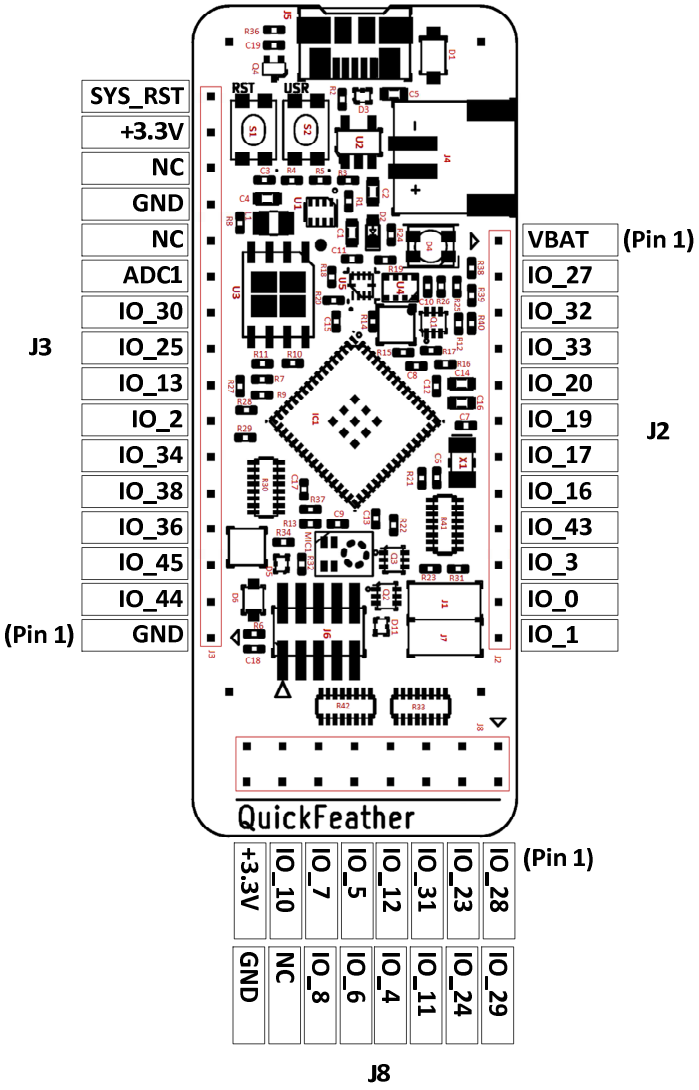

Figure 7: QuickFeather HDK IO Expansion connectors

EOS S3 MCU IO	*QuickFeather HDK Function*	*Additional Function*	*Expansion*
IO_0	I2C0 SCL		J2.11
IO_1	I2C0 SDA		J2.12
IO_2	IO		J3.7
IO_3	Accelerometer MC3635 interrupt		J2.10
IO_4	IO		J8.8
IO_5	IO		J8.9
IO_6	User Button input		J8.10
IO_7	IO		J8.11
IO_8	IO		J8.12
IO_10	IO		J8.13
IO_11	IO		J8.6
IO_12	IO		J8.7
IO_13	IO		J3.8
IO_14	Serial Wire Debug CLK		J6.4
IO_15	Serial Wire Debug DATA		J6.2
IO_16	IO	SPI Slave CLK	J2.8
IO_17	IO	SPI Slave MISO (input)	J2.7
IO_18	Blue LED		N/A
IO_19	IO	SPI Slave MOSI	J2.6
IO_20	IO	SPI Slave CSn	J2.5
IO_21	Green LED		N/A
IO_22	Red LED		N/A
IO_23	IO	I2S Slave WCLK (frame)	J8.3
IO_24	IO	I2S Slave DATA (dout)	J8.4
IO_25	IO		J3.9
IO_27	IO	SPI Master CS2	J2.2
IO_28	PDM Data; to isolate, remove R13		J8.1
IO_29	PDM CKO		J8.2
IO_30	IO		J3.10
IO_31	IO	I2S Slave CLK (input)	J8.5
IO_32	IO		J2.3
IO_33	IO		J2.4
IO_34	SPI Master CLK		J3.6
IO_36	SPI Master MISO		J3.4
IO_38	SPI Master MOSI (flash)		J3.5
IO_40	IO		N/A
IO_43	IO	Interrupt output to Host	J2.9
IO_44	IO	UART TX	J3.2
IO_45	IO	UART RX	J3.3

Connector J2

J2	EOS S3 MCU IO	QFN Pin#	Function
1			VBAT
2	IO_27	28	IO; SPI Master CS2n
3	IO_32	22	IO; I2C bus 1 SDA
4	IO_33	21	IO; I2C bus 1 SCL
5	IO_20	37	SPI Slave SSn input; EOS S3 boot-strap
6	IO_19	36	SPI Slave MOSI input; EOS S3 boot-strap
7	IO_17	42	SPI Slave MISO output
8	IO_16	40	SPI Slave CLK input
9	IO_43	7	EOS S3 Interrupt output
10	IO_3	2	MC3635 Interrupt input
11	IO_0	4	I2C0 SCL
12	IO_1	5	I2C0 SDA

Connector J3

J3	EOS S3 MCU IO	QFN Pin#	Function
1			Ground
2	IO_44	8	S3 UART TX
3	IO_45	9	S3 UART RX
4	IO_36	17	SPI Master MISO input
5	IO_38	16	SPI Master MOSI output
6	IO_34	20	SPI Master CLK output
7	IO_2	6	IO
8	IO_13	55	IO
9	IO_25	31	IO
10	IO_30	25	IO
11	ADC1	47	ADC1 input
12			No Connect
13			Ground
14			No Connect
15			+3.3V
16	SYS_RSTn	41	EOS S3 HW reset input

Connector J8

J8	*EOS S3 MCU IO*	*QFN Pin#*	*Function*
1	IO_28	27	PDM microphone Data
2	IO_29	26	PDM microphone CLK
3	IO_23	33	I2S Slave WCLK input
4	IO_24	32	I2S Slave DATA output
5	IO_31	23	I2S Slave CLK input
6	IO_11	57	IO
7	IO_12	56	IO
8	IO_4	3	IO
9	IO_5	64	IO
10	IO_6	62	User button input
11	IO_7	63	IO
12	IO_8	61	IO
13	IO_10	59	IO
14			No Connect
15			+3.3V
16			Ground

Development connector

EOS S3 MCU SWD connector

J6	*EOS S3 MCU IO*	*Function*
1		+3.3V
2	IO_15	SWD IO
3		Ground
4	IO_14	SWD CLK
5		Ground
6		No Connect
7		No Connect
8		No Connect
9		Ground
10	SYS_RSTn	Hardware Reset

Boot-strap IO_19 & IO_20

- Install both shunts to use SWD Debugger for development
- Remove both shunts for boot-from-flash

Note: QuickFeather HDK board flash device must contain valid boot image for successful boot from flash.

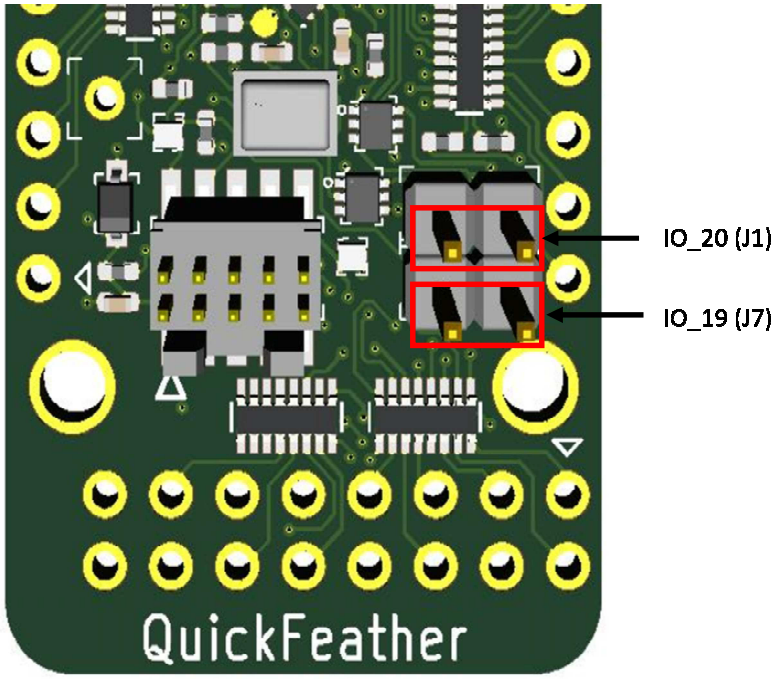

Figure 8: Boot strap J1 and J7

QuickFeather HDK power supplies

There are two ways to provide power to the QuickFeather HDK: USB connector (J5) or Battery connector (J4).

When both ports are connected at the same time, the USB power activates the battery charging circuit that provide charging current to the battery.

When using a rechargeable battery, the minimum input voltage will determine the maximum currents that the system needs to support. This is important when connecting additional peripherals to the QuickFeather HDK that also requires connection to +3.3V for supplies.

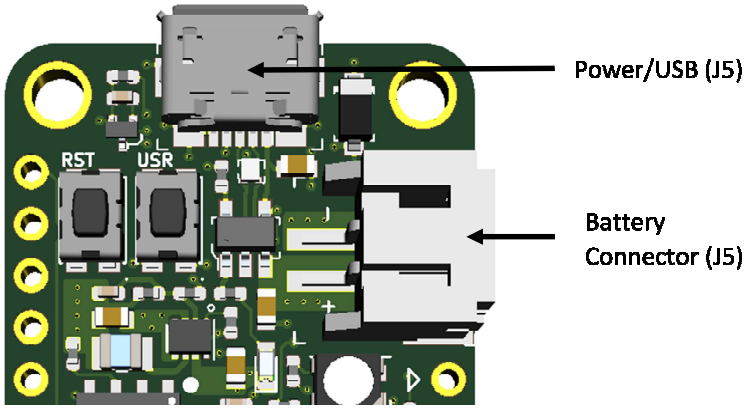

Figure 9: QuickFeather HDK Power inputs

Connecting additional Peripherals to the QuickFeather HDK

QuickLogic's QuickFeather supports direct connection to FeatherWing module (providing that the FeatherWing module has Stack Headers installed) via expansion connector J2 and J3. Refer to Adafruit web site for additional information on available FeatherWing modules.

Sensor with I2C port

QuickFeather board supports connecting to sensor module with I2C slave interface via expansion connectors J2. QuickFeather I2C supports I2C Standard mode (100KHz) and Fast mode (400KHz). There are two I2C buses available:

- I2C0 bus: J2 pin 12 (SDA) and J2 pin 11 (SCL); the signals (SCL and SDA) are connected to 4.7KΩ pull-up resistor. This bus is shared with onboard I2C sensors: Accelerometer MC3635 (address 0x44h) and Pressure DPS310 (address 0x77h).
- I2C1 bus: J2 pin 3 (SDA) and J2 pin 4 (SCL); there is no pull up resistor on the I2C1 bus.

Steps to connect external I2C sensors to QuickFeather board:

- Ground connection
- Power connection (+3.3V supplies); check supply voltage level meeting connecting module requirement
- Connect SCL and SDA signals; check IO level (> +3.0V IO only)
- Keep connecting wires as short as possible
- Configure the I2C address to avoid address 0x44h (on-board ACCEL MC3635) and address 0x77h (on-board Pressure sensor DPS310)
- Check SCL and SDA rise time (< 1000 ns for Standard mode and < 300 ns for Fast mode)

  Note: refer to I2C- bus specification for details (UM10204)

Sensor with SPI Slave port

QuickFeather board supports connecting to sensor module with SPI slave interface via expansion connectors J2 and J3: SPI MASTER CLK (J3 pin 6), SPI MASTER MISO (J3 pin 4), SPI MASTER MOSI (J3 pin 5) and SPI MASTER SS2 (J2 pin 2). The maximum supported SPI clock frequency is 10MHz.

Steps to connect external SPI sensor to QuickFeather board:

- Ground connection
- Power connection (+3.3V supplies check supply voltage level meeting connecting module requirement
- Connect SPI MASTER signals; check IO level (> +3.0V IO only)
- Keep connecting wires as short as possible
- Check signal quality using scope

PDM Microphones

Single PDM microphone

The on-board PDM microphone (Infineon IM69D130) is configured as left channel output (driving active data on falling edge of PDM CLK). QuickFeather supports external PDM microphone connection via expansion connector J8: PDM CLK (J8 pin 2) and PDM DATA (J8 pin 1).

Steps to connect one external PDM microphone to QuickFeather board:

- Ground connection
- Power connection (+3.3V supplies check supply voltage level meeting connecting module requirement
- Connect PDM CLK and PDM DATA signals; check IO level (> +3.0V IO only)
- Keep connecting wires as short as possible
- PDM microphone is configured as right channel microphone; the L/R signal or Channel signal is connected to VDD
- Check signal quality using scope

Two PDM microphones

To support two external PDM microphones configuration, it is required to disable the connection of the on-board PDM microphone.

QuickFeather supports external PDM microphone connection via expansion connector J8: PDM CLK (J8 pin 2) and PDM DATA (J8 pin 1).

Steps to connect two external PDM microphones to QuickFeather board:

- Ground connection
- Power connection (+3.3V supplies check supply voltage level meeting connecting module requirement
- **Remove R13 (100Ω resistor)**
- Connect PDM CLK and PDM DATA signals; check IO level (> +3.0V IO only)
- Keep connecting wires as short as possible; avoid star connection scheme (see figure below)
- Configure one PDM microphone as left channel and one PDM microphone as right channel
- Check signal quality using scope

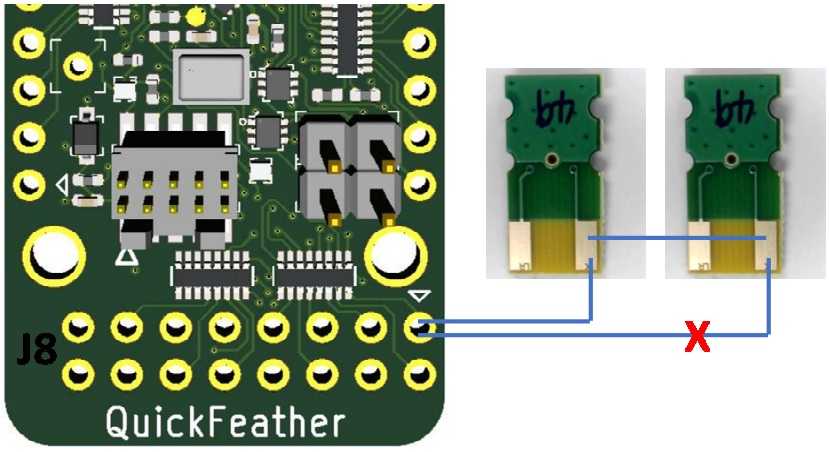

Figure 10: Microphones Wiring recommendation

Download Binaries using Jlink SWD

QuickFeather supports loading and testing stand-alone eFPGA design or eFPGA + M4 MCU design, using SWD standard tool such as Segger's Jlink SWD or OCD. Below are the instructions for system with Windows 10 OS with Segger Jlink pod

What you need

- Laptop or PC with Windows 10
- Segger Jlink pod and PC connecting USB cable
- Segger Jlink adapter to 10-pin connector and cable
- QuickFeather board and micro USB cable

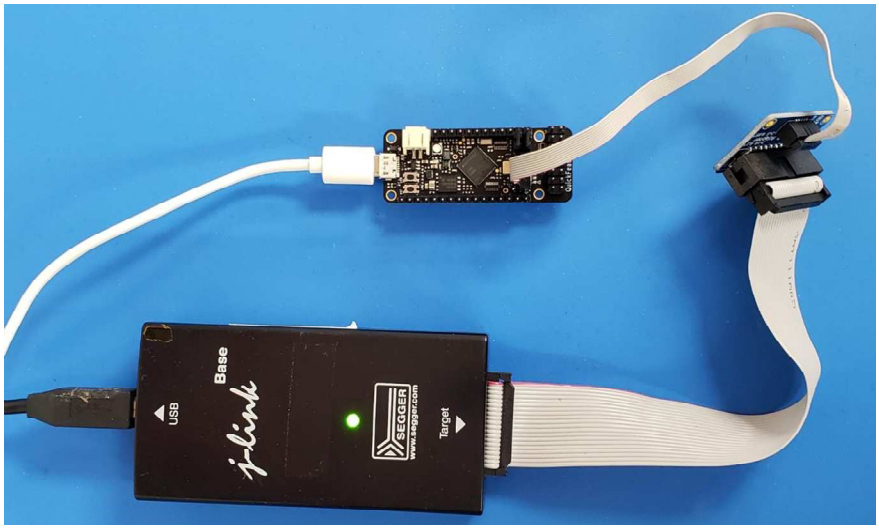

Figure 11: Jlink to QuickFeather connection

Download stand-alone FPGA binaries instructions

- Disconnect QuickFeather power; if USB-to-Serial cable connected to the board, remove the connection from PC
- Install shunts at QuickFeather J1 and J7
- Connect micro USB cable from QuickFeather to PC
- Connect 10-pin cable to QuickFeather connector J6; check connector key for correct alignment
- Press reset button
- Open CMD console
- Type: "Jlink.exe -device cortex-m4 -If SWD -speed 4000 -commandFile "Jlink script"

  Note:
  - Jlink.exe: Link commander – include reference to the location of executable
  - Jlink script: output file symbiflow for EOS S3 FPGA binaries
  - Refer to Jlink Commander for more additional information

Download FPGA binaries + M4 MCU binaries instructions

- Disconnect QuickFeather power; if USB-to-Serial cable connected to the board, remove the connection from PC

- Install shunts at QuickFeather J1 and J7
- Connect micro USB cable from QuickFeather to PC
- Connect 10-pin cable to QuickFeather connector J6; check connector key for correct alignment
- Press reset button
- Open CMD console (#1)
- Launch Jlink commander (i.e. type “Jlink.exe”) and follow the on-screen instructions to connect to QuickFeather M4 target
- Execute the followings in Link Commander console
    - Type: “r” to reset the EOS S3
    - Type: “loadbin m4_application.bin 0x0”
    - Type: “r”
- Open another CMD console (#2)
- Type: “Jlink.exe -device cortex-m4 -If SWD -speed 4000 -commandFile "Jlink script"
  Note:
    - Jlink.exe: Link commander – include reference to the location of executable
    - Jlink script: Symbiflow’s output for EOS S3 FPGA binaries
    - Refer to Jlink Commander for more additional information
- Return to console #1; type: “g”; the M4 binaries in M4 SRAM will start to run and the eFPGA is configured

Revision

Version	Date	Revision
1.0	June 2020	First release.
1.1	June 2020	Update with Hello World application figures
1.2	June 2020	Update with instruction to use Jlink to download: • FPGA binaries • FPGA + M4 binaries