DTP2 Milestone 2 Extension

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Signal Processing Block:

Configurable LPF/HPF for Digital Audio Signal

Integration in the Audio Synthesizer Project

Digital Filter type FIR

- Structure
- Design & Quantisation (w/ Matlab)
- HW Implementation (w/ FPGA)
- Simulation & Test

Phase-2 *Milestone-2*
Digital Audio-Loop Test

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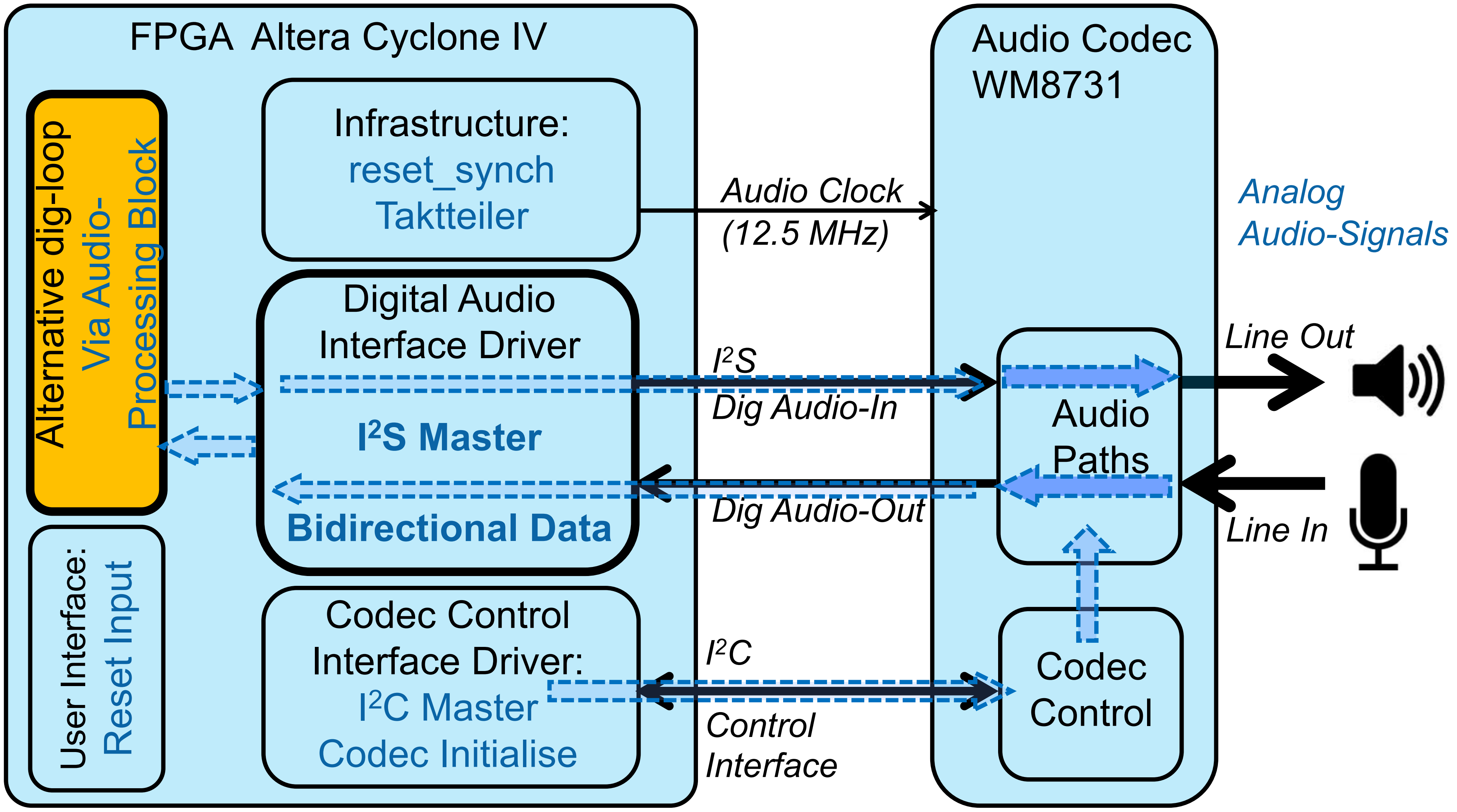

Objective: modify the digital audio signal with a filter

Digital Audio Interface Driver Blocks

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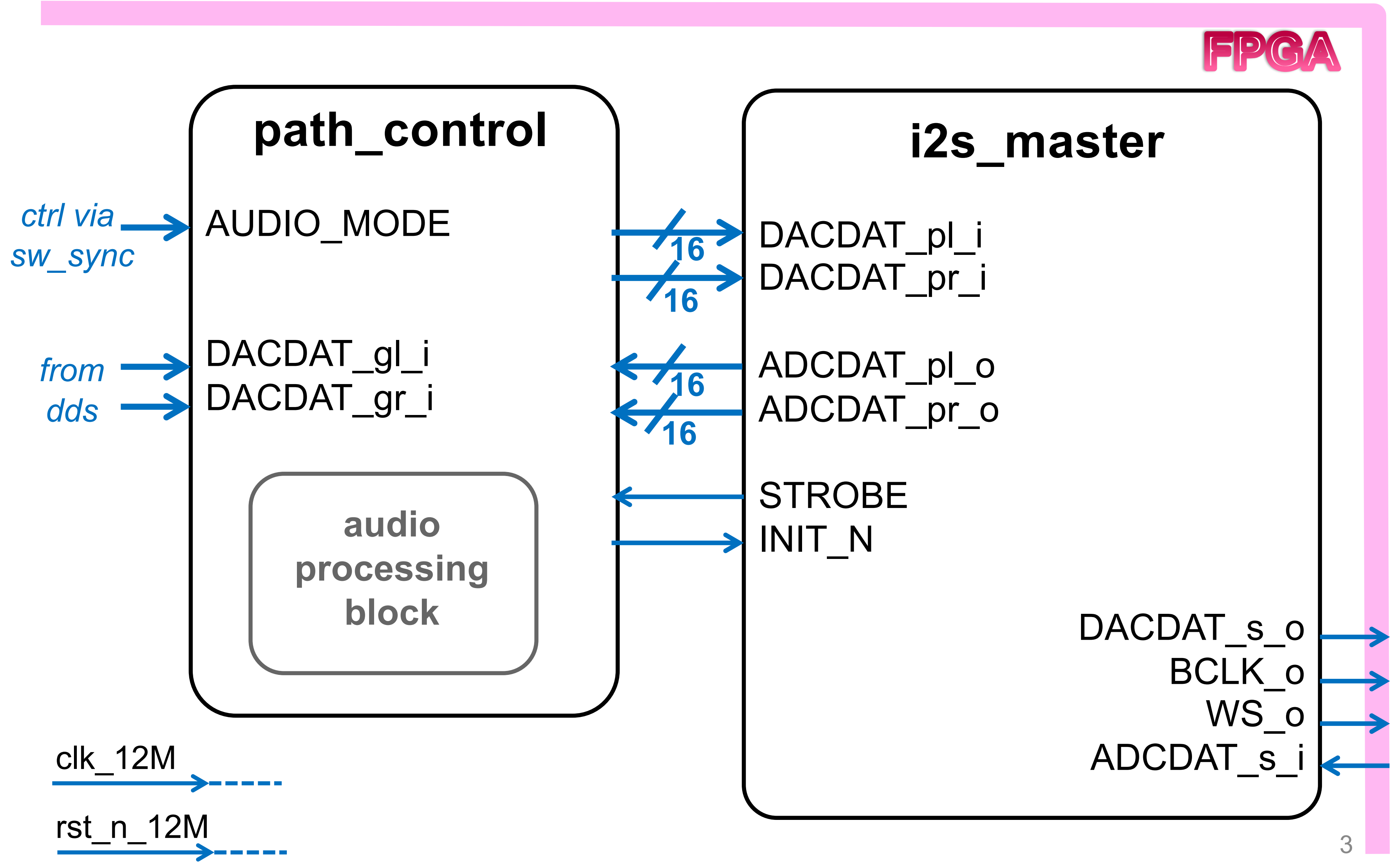

Digital Filter type FIR

FIR (finite impulse response)

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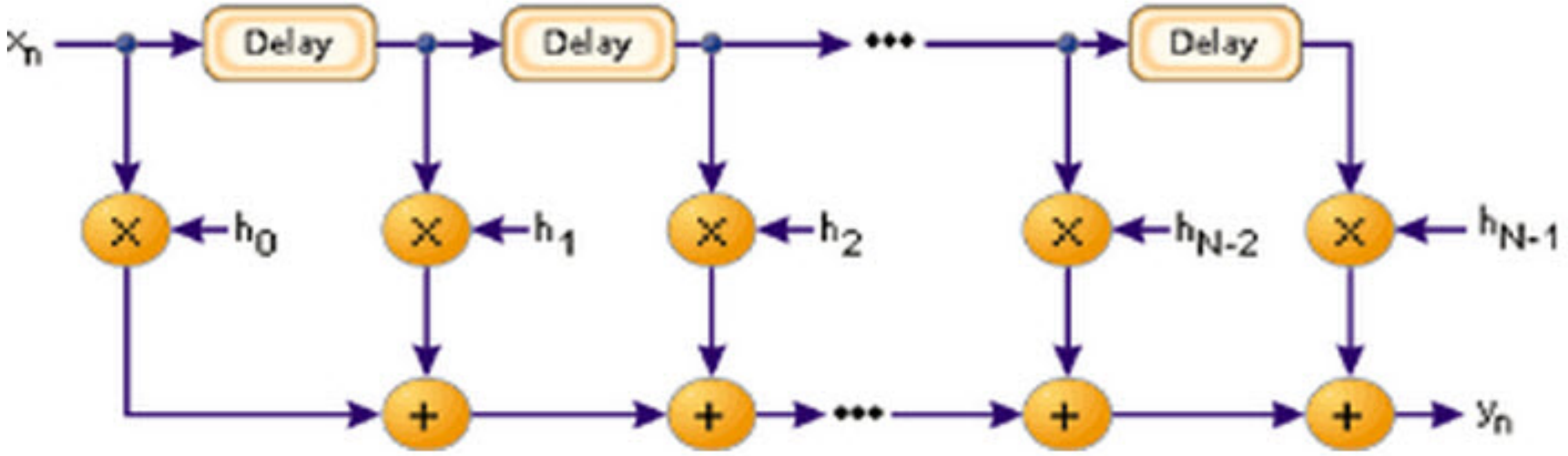
Principle:
Several input samples are multiplied with coefficients and added up.

Implementation Structure:
Need a delay line, multipliers and adders.



Source: https://www.elprocus.com/fir-filter-for-digital-signal-processing/

Digital Filter type FIR

FIR (finite impulse response)

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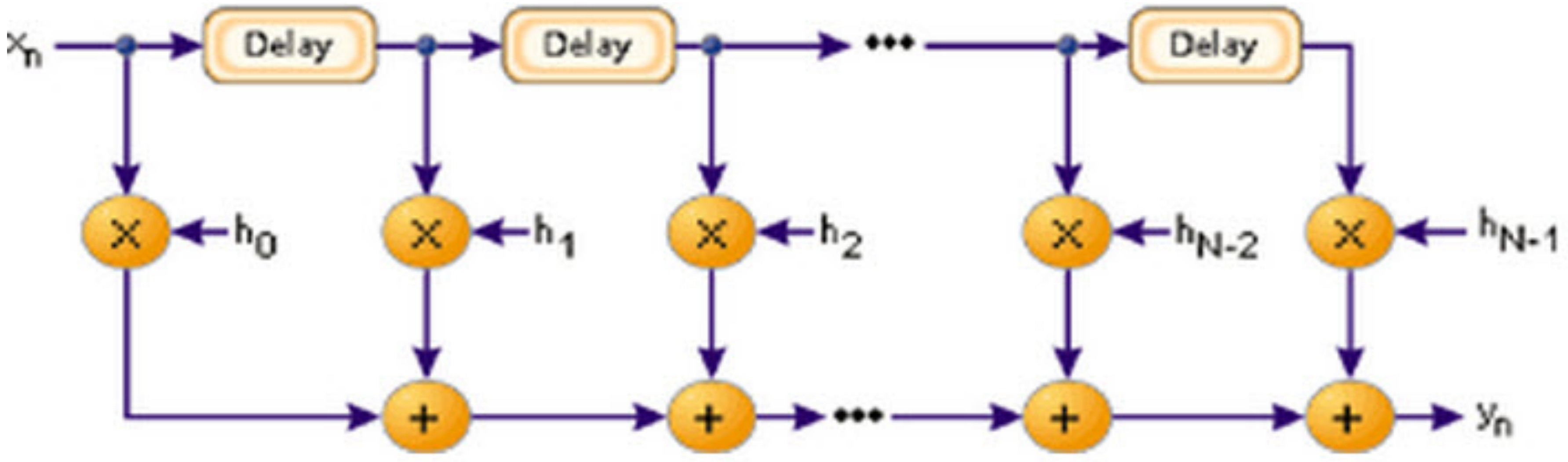
Digital Filter Design:
How many coefficients? How many bits pro coefficient (resolution)?
Can be calculated & simulated in Matlab, and it is topic for later semesters!

Implementation Details:
Delay line in FPGA => memory block
Multiplication block => not many available, solution: higher frequency and reuse



Source: https://www.elprocus.com/fir-filter-for-digital-signal-processing/

Digital Filter type FIR

HW Implementation

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FPGA Resources
what is new

→

Mem Blocks
for delay line

Multipliers
also called DSP-blocks

VHDL Description
what is new

Mem Blocks
use a separated block with
behavioural description of RAM blocks
which is supported by synthesizer
For Cyclone devices:
M4K Blocks, described in handbook
as embedded memory

Multipliers
use signals with defined resolution
consider increase of width on output

Field Programmable Gate Array (FPGA) Architecture (2/3)

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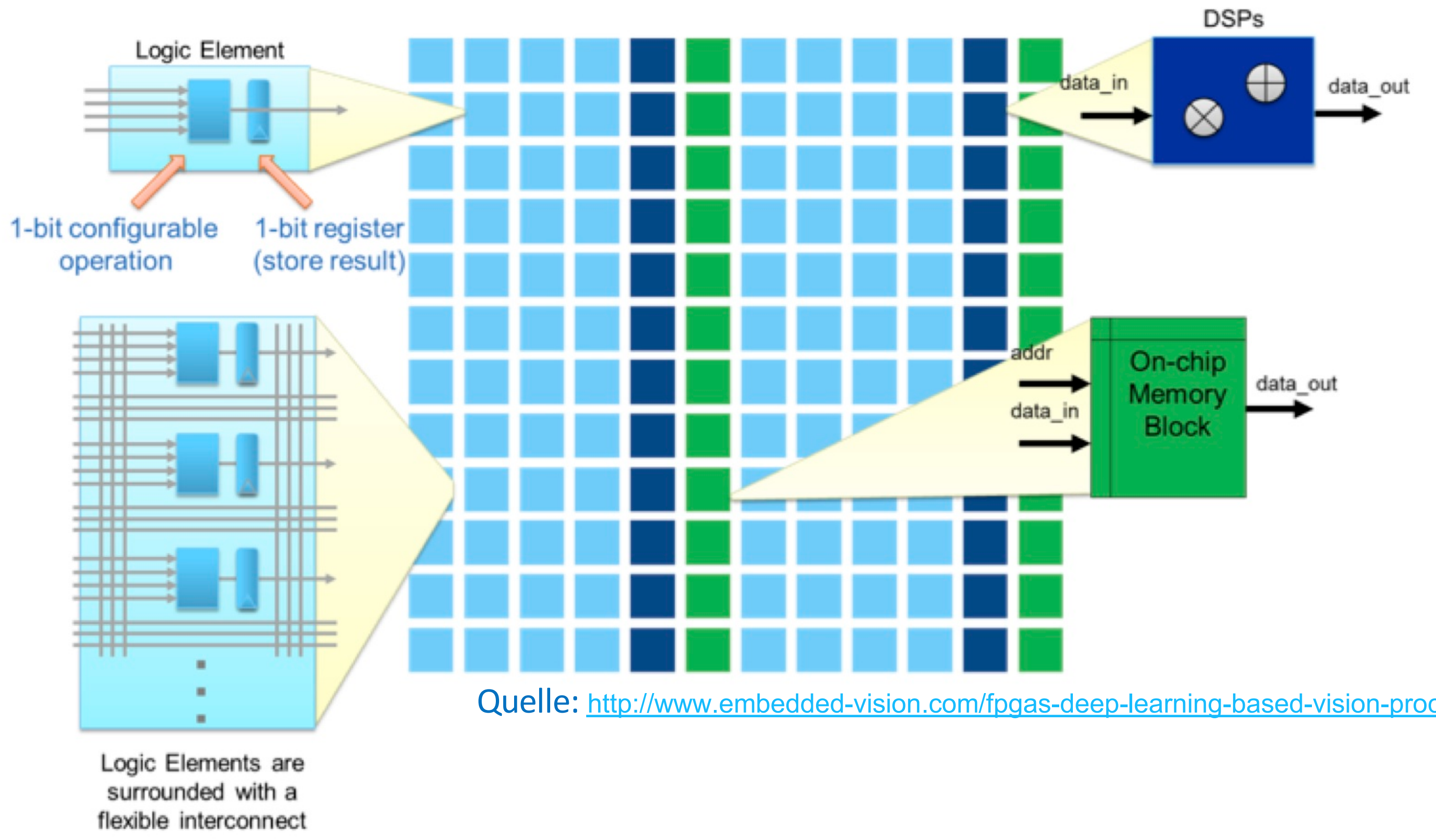
Plus Macrocells, like :

RAM blocks ; Multipliers and Adders (DSP blocks) ; PLLs (clock generation);
Clock networks (clock distribution) and Input/Output blocks


Logic Element
1-bit configurable operation
1-bit register (store result)
DSPs
data_in
data_out
addr
data_in
On-chip Memory Block
data_out
Logic Elements are surrounded with a flexible interconnect

Quelle: http://www.embedded-vision.com/fpgas-deep-learning-based-vision-processing

Digital Filter type FIR

HW Implementation

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VHDL Syntax
what is new → **Arrays**
For Look-Up-Table (LUT storing filter coefficients)

[extract from audio_filter_pkg.vhd]

```
constant N_LUT:                natural := 255;    -- length of LUT = 255
constant N_RESOL_COEFF:        natural := 16;     -- Attention: 1 bit reserved for sign

-- range : [-2^15; +(2^15)-1] = [-32768 ; +32767]
subtype  t_fir_range is integer range -(2**(N_RESOL_COEFF-1)) to
                                       (2**(N_RESOL_COEFF-1))-1;

type     t_lut_fir is array (0 to N_LUT-1) of t_fir_range;

constant LUT_FIR_LPF_200Hz : t_lut_fir :=(
         -14,-15,-19,-25,-34,-45,-58,-73,-90,-109,-129,-149,-170,-189,-208,
         …         );
```

Digital Filter type FIR

HW Implementation

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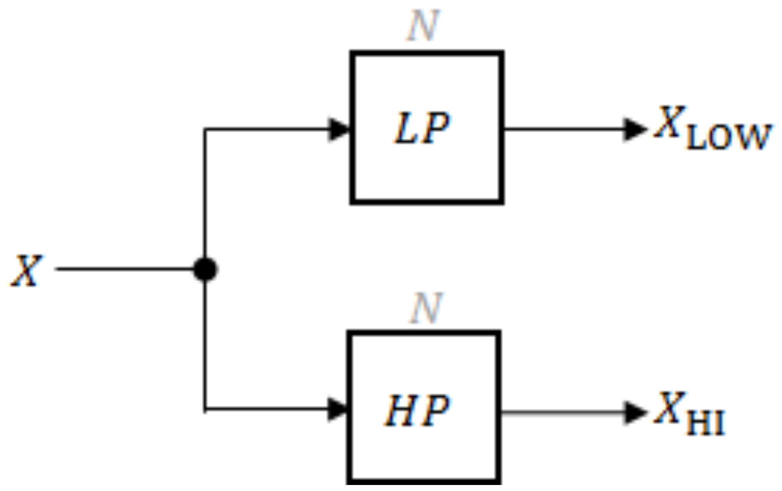
Low Pass Filter $\Rightarrow$ **Complementary High Pass Filter**



Based on the idea above
(that the input signal can be split into ist low-pass and high-pass frequency contents)

How would you calculate the output of the HPF based on the LPF?

Testbench for FIR-Core

Block Level TB around LPF

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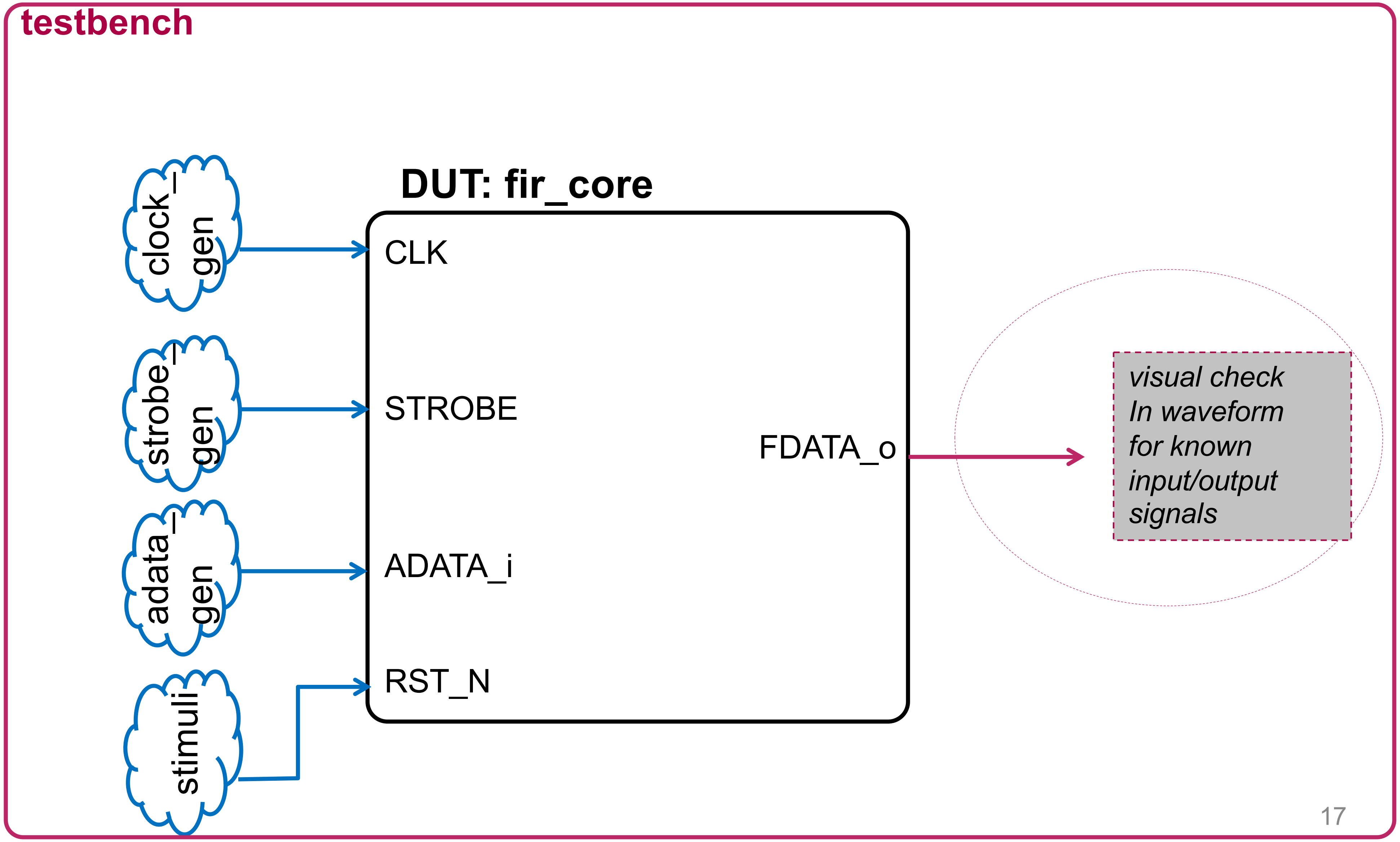

Testbench for FIR-Core

Block Level Simulation: Impulse & Square-Pulse Responses

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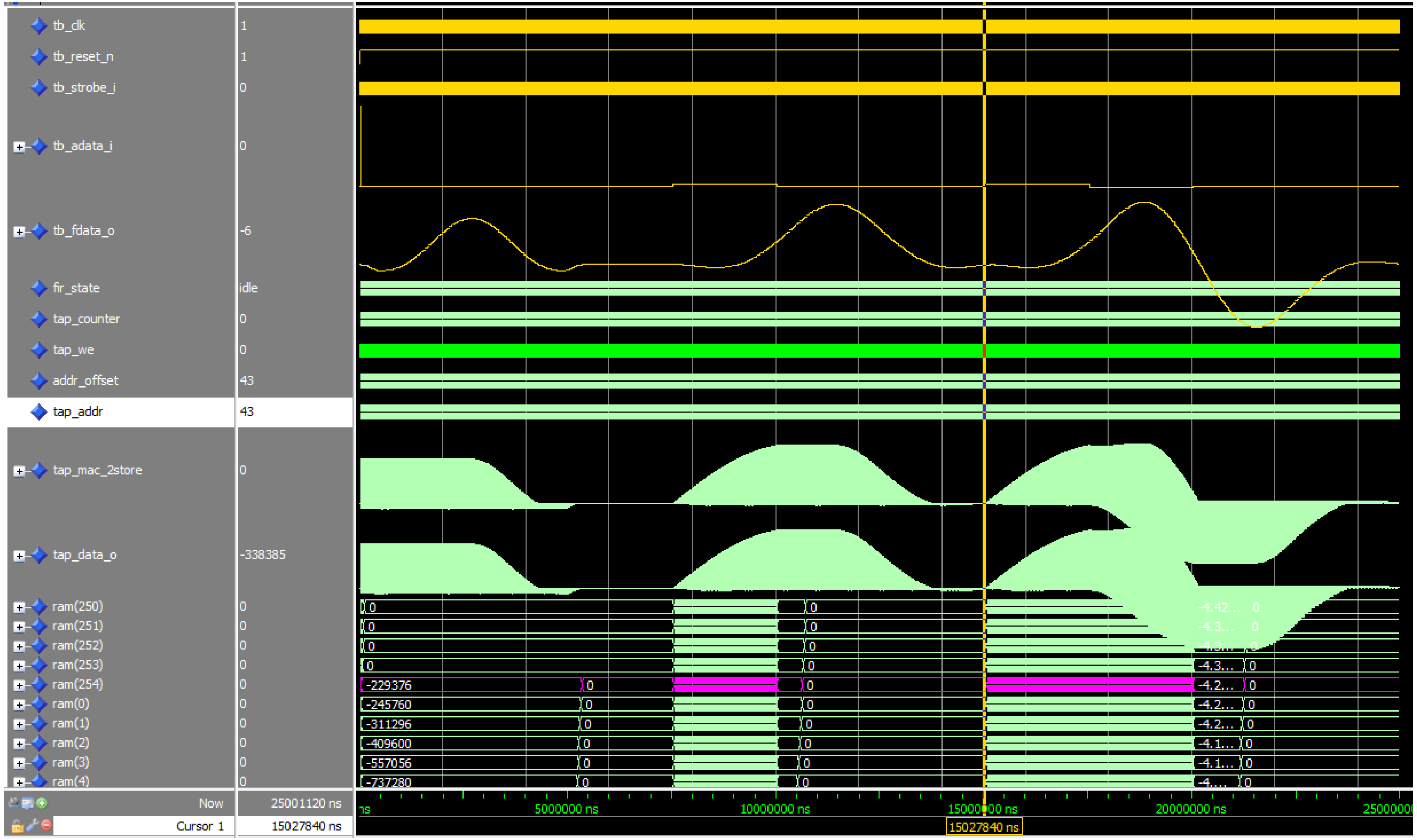

tb_clk	1
tb_reset_n	1
tb_strobe_i	0
tb_adata_i	0
tb_fdata_o	-6
fir_state	idle
tap_counter	0
tap_we	0
addr_offset	43
tap_addr	43
tap_mac_2store	0
tap_data_o	-338385
ram(250)	0
ram(251)	0
ram(252)	0
ram(253)	0
ram(254)	0
ram(0)	0
ram(1)	0
ram(2)	0
ram(3)	0
ram(4)	0
Now	25001120 ns
Cursor 1	15027840 ns