

REV	Description	DATE	BY
A4A	Initial Production Release.	11/19/2012	GC
A5	On the initial production release the processors were to be found incorrect as supplied by TI. Parts while marked AM3359 were actually AM3352. This revision uses the correct parts.	1/2/2013	GC
	1. Deleted R29-R44 from the LCD lines. 2. Added 47pf capacitors C156-C173 to LCD data lines to ground. 3. Changed schematic revision to A5A. 4. Changed a few footprints after PCB update for above changes. 5. Added access point for the battery function of the TPS65217C. 6. Added Ferrite beads in series with LED power and 5V power rail of the USB host connector. Required to pass FCC/CE testing due to noise emissions on that pin. 7. Added power button to enable sleep, wakeup, power down and power up features on the system. 8. Added Modification to add 100K ohm resistor to ground to prvent crosstalk when serial cable is not plugged in.	2/8/2013	GC
A5B	1. Added 100K pulldown on J1 pin 4 to prvent crosstalk when serial cable is not connected into PCB layout.	4/1/2013	

PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	POWER MANAGEMENT
3	PROCESSOR 1 OF 3, JTAG HEADER
4	PROCESSOR 2 OF 3, USB PORTS
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	DDR3 MEMORY
8	eMMC FLASH
9	10/100 ETHERNET
10	HDMI FRAMER
11	EXP CONN, uSD

NOTE: PCB Revision for this board is Rev B4.

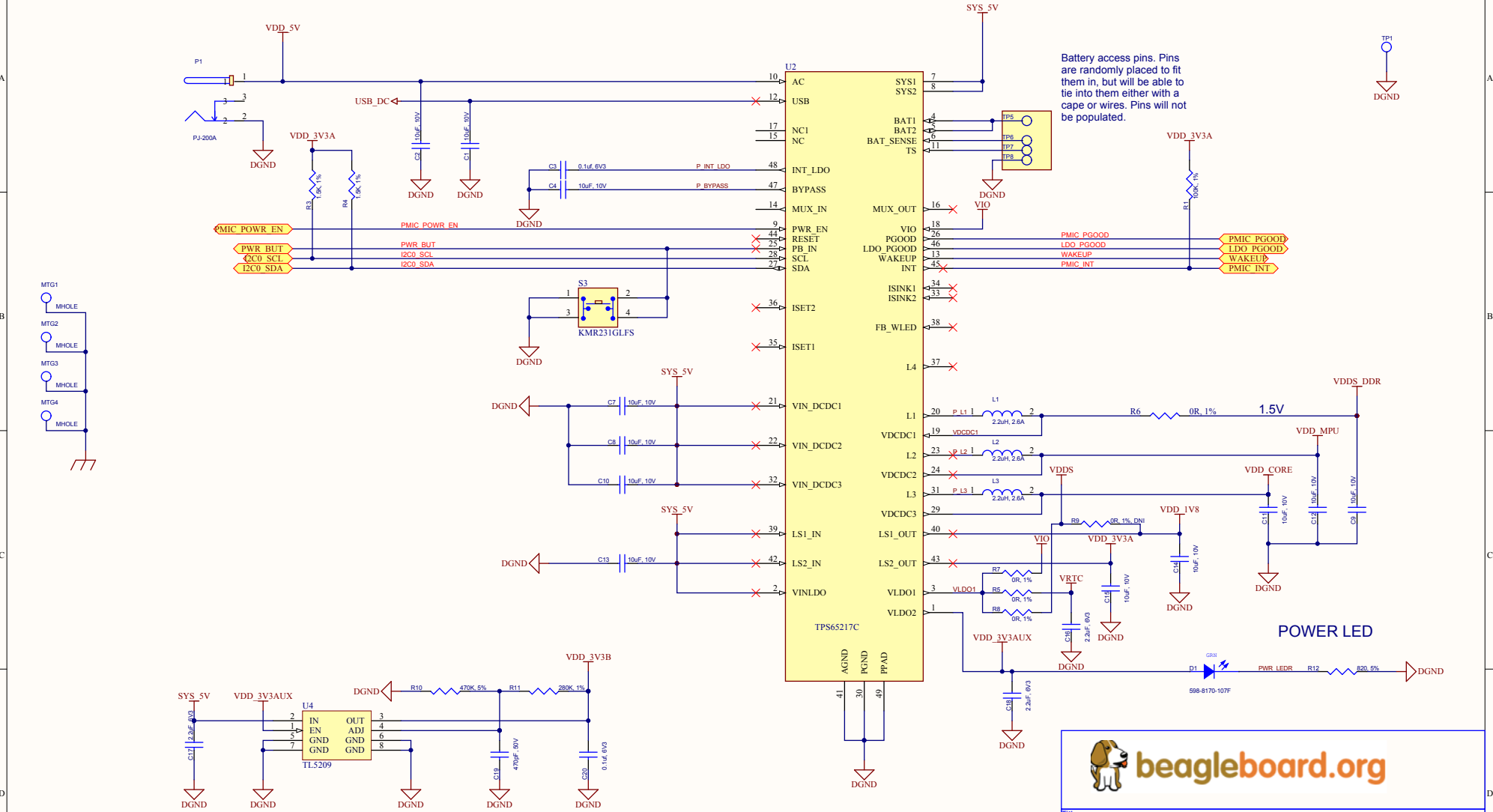
This schematic is \*NOT SUPPORTED\* and DOES NOT constitute a reference design. Only "community" support is allowed via resources at [BeagleBoard.org/discuss](http://BeagleBoard.org/discuss).

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Title BeagleBoneBlack Cover Page		
Size A	Document Number 450-5500-001	Rev A5B
Date: Monday, April 01, 2013	Sheet 1 of 11	

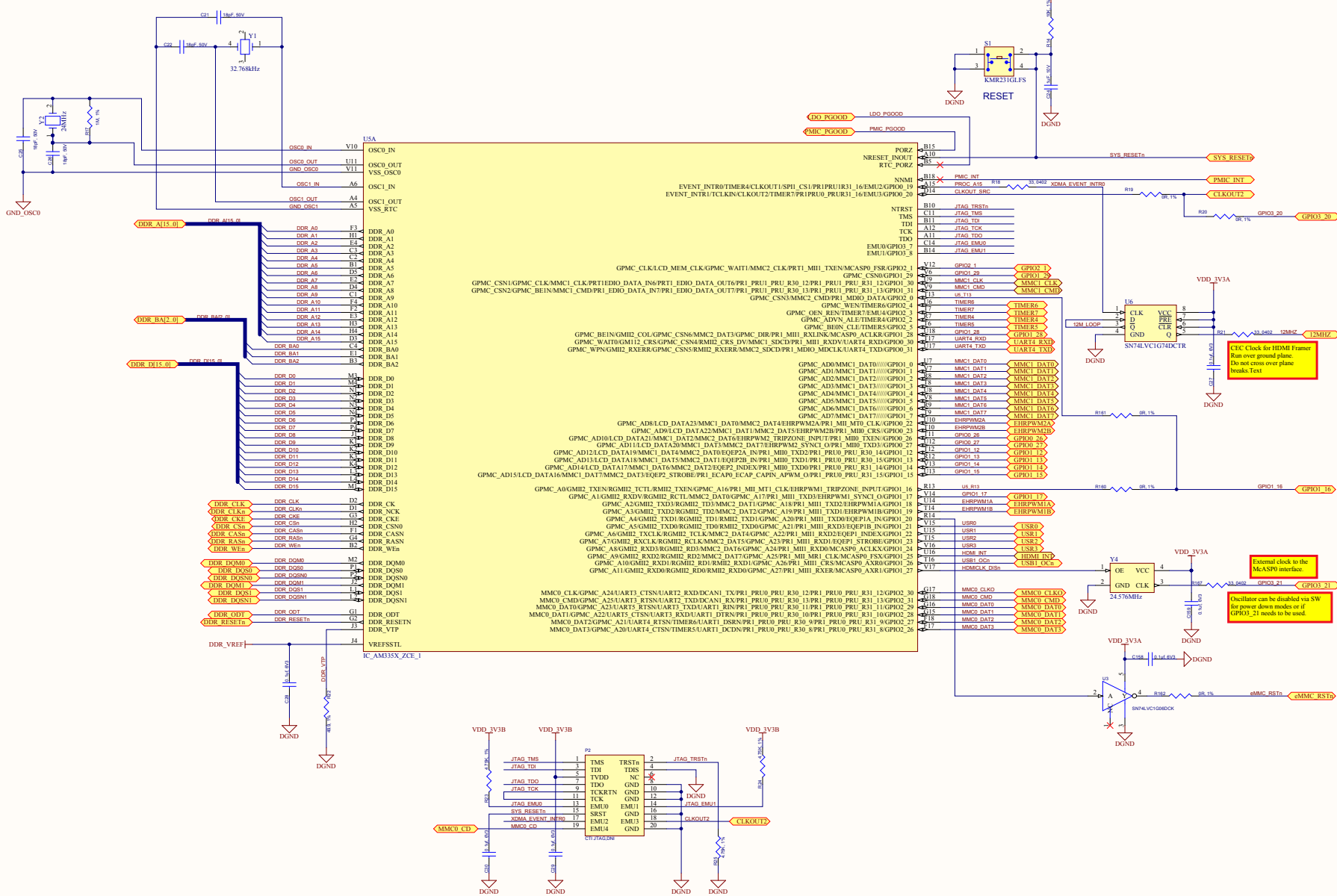
# 5V DC POWER

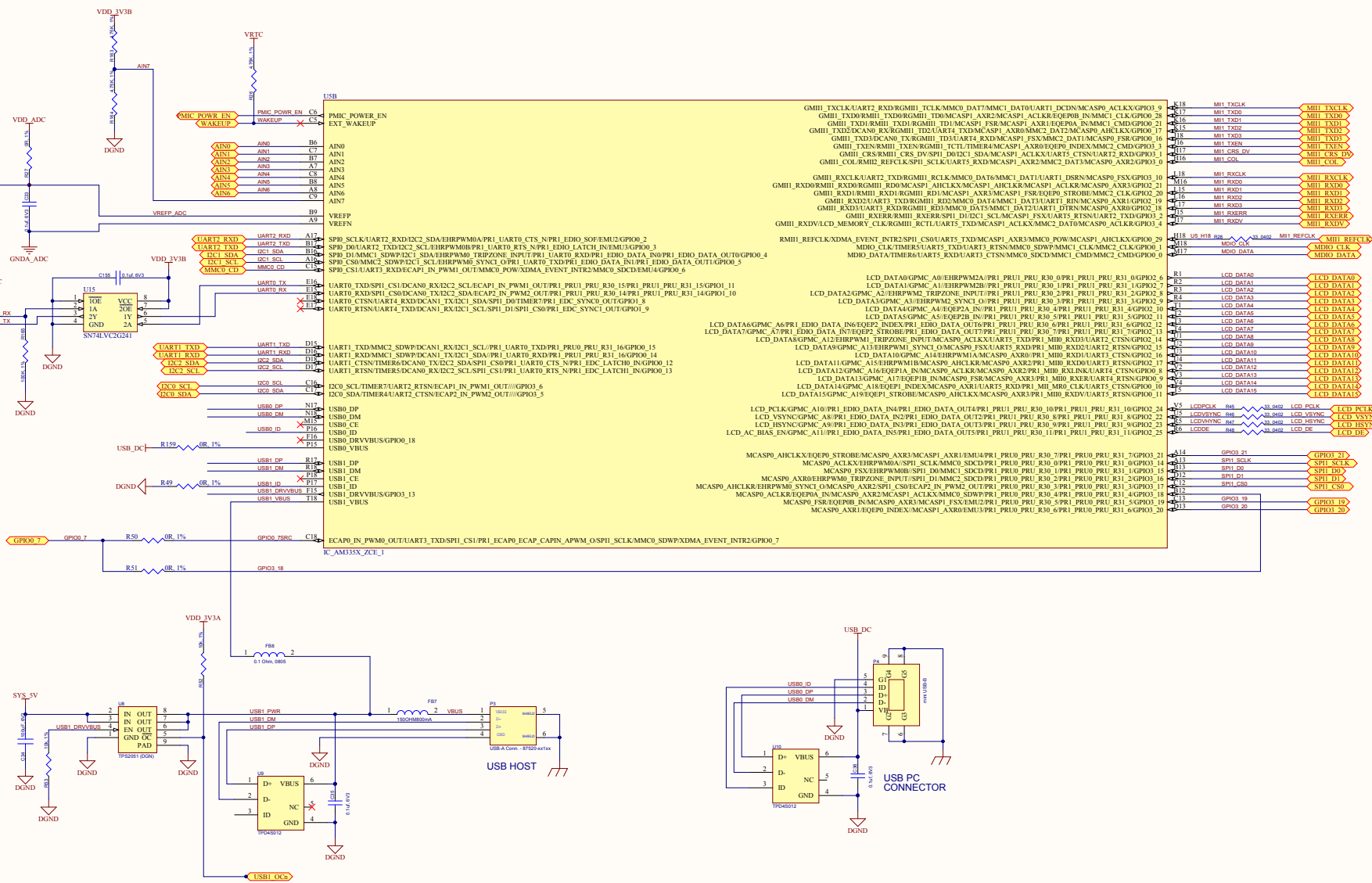


Battery access pins. Pins are randomly placed to fit them in, but will be able to tie into them either with a cape or wires. Pins will not be populated.

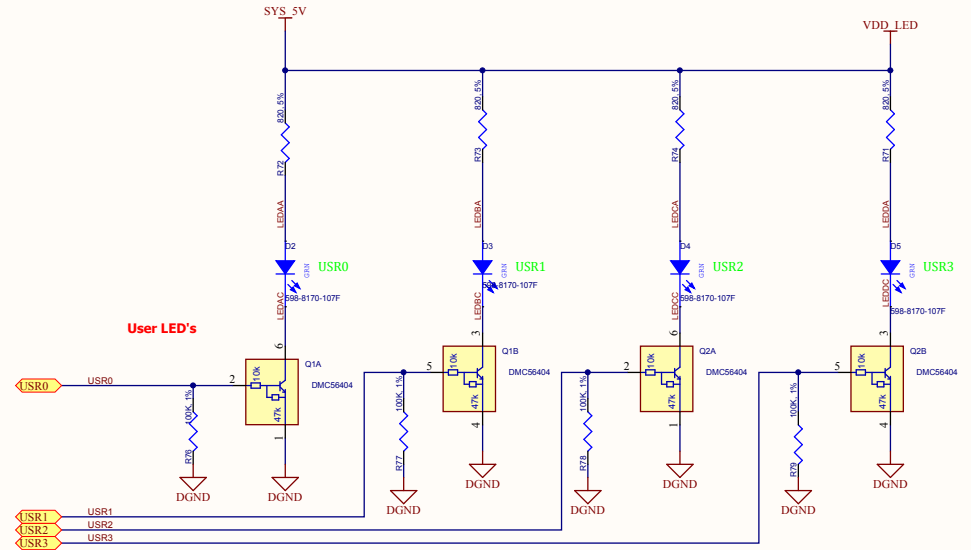
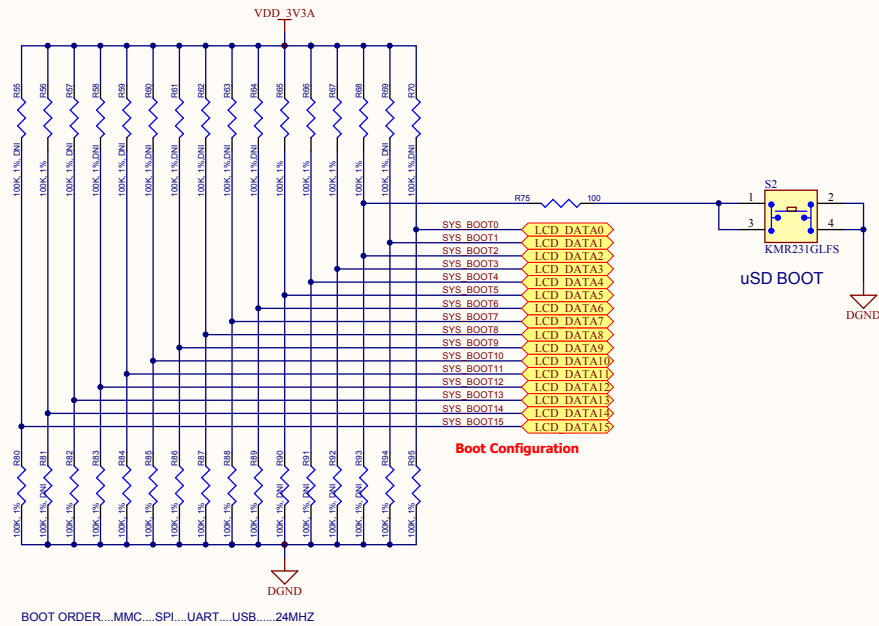
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Title BeagleBoneBlack Power Management		
Size A	Document Number 450-5500-001	Rev A5B
Date: Monday, April 01, 2013		Sheet 2 of 11









SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC1	MMC0	UART0	USB0[5]
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0	MMC0	USB0[5] 1	UART0



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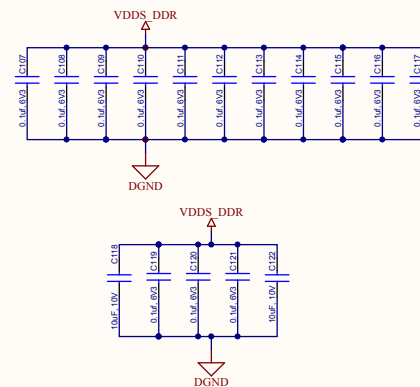
Title BeagleBoneBlack LED, Configuration, and Reset

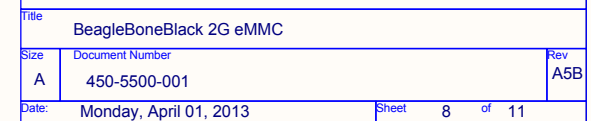
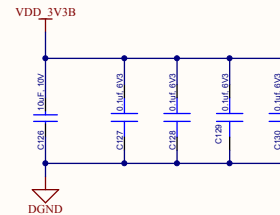
Size A Document Number 450-5500-001

Rev A5B

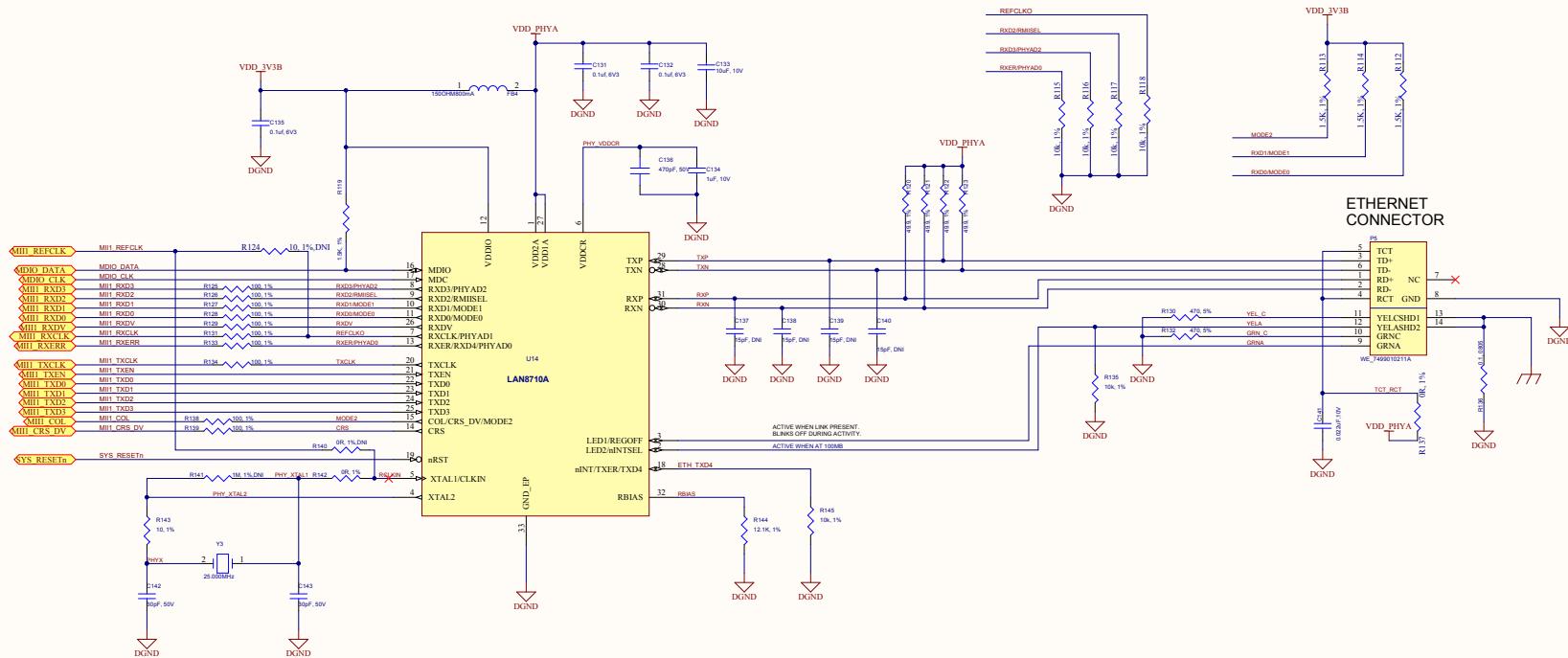
Date: Monday, April 01, 2013

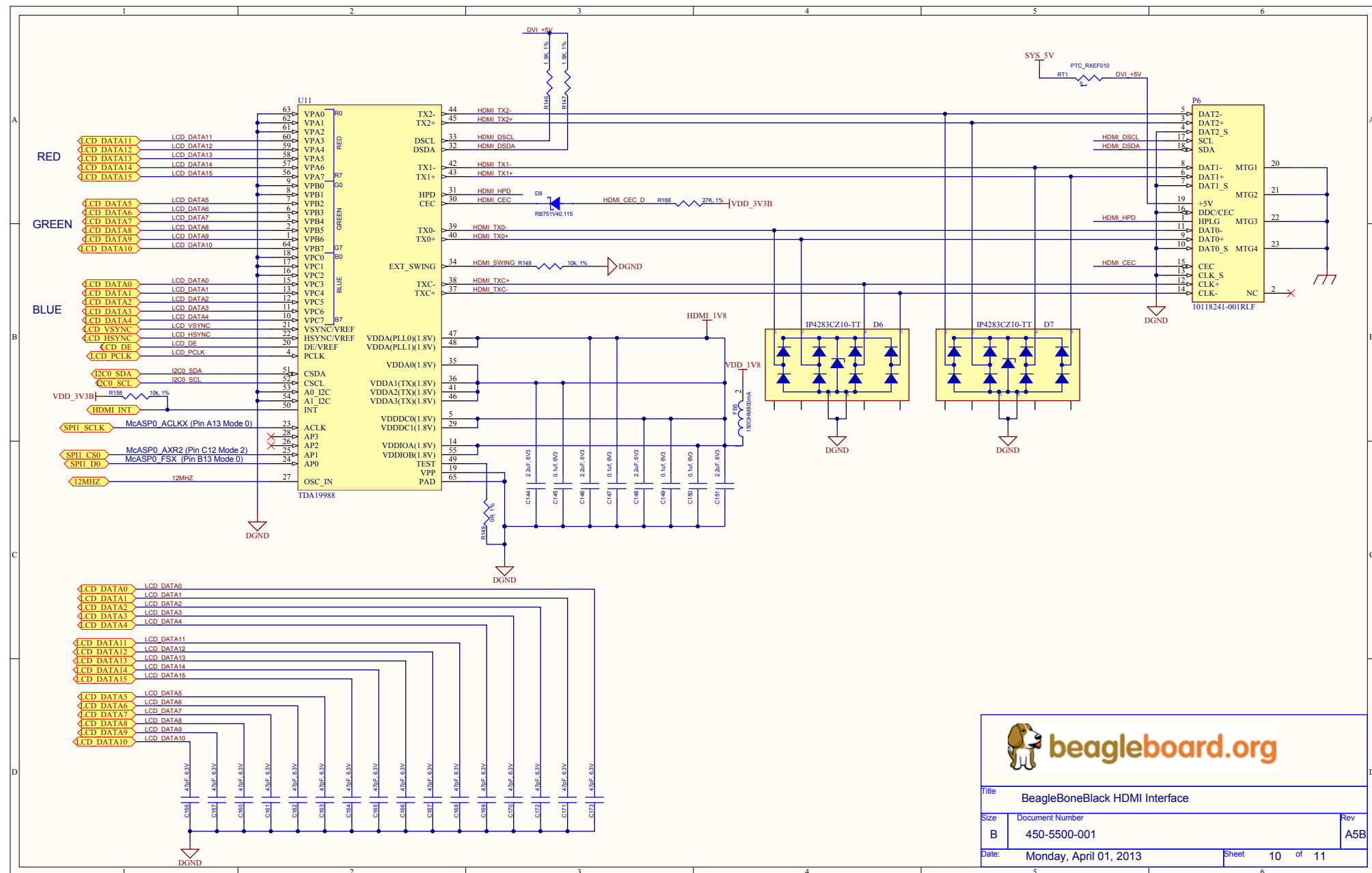
Sheet 6 of 11



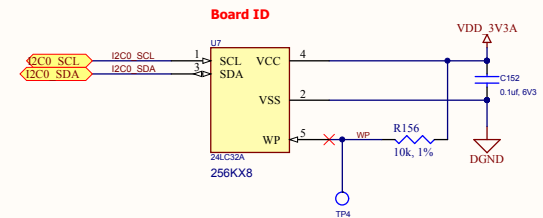
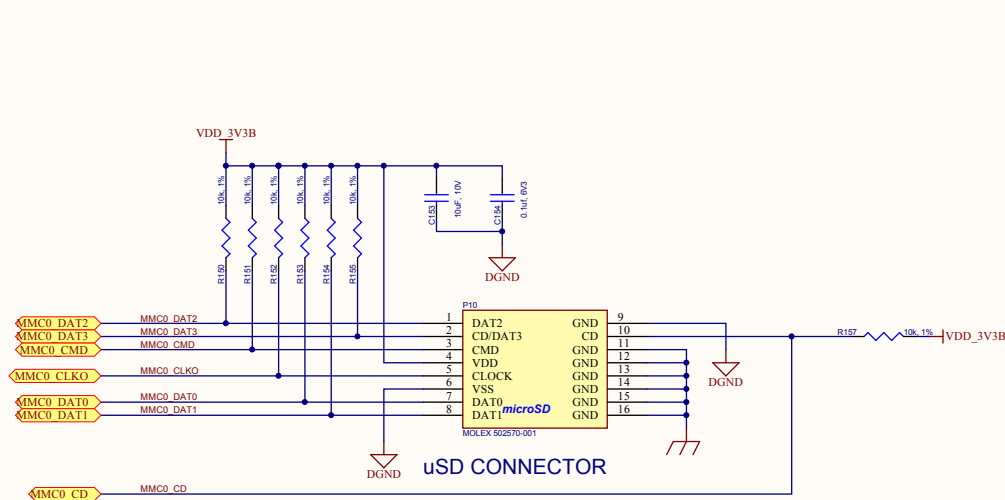
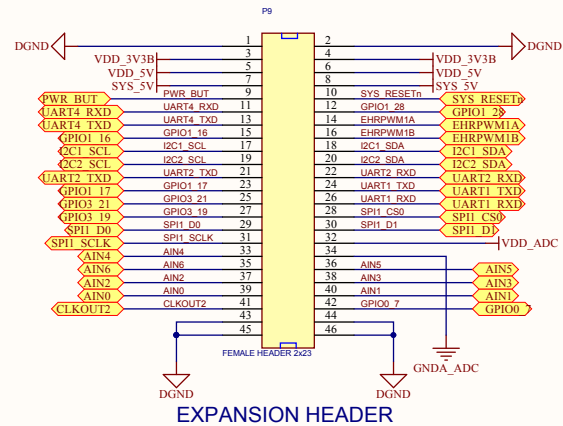
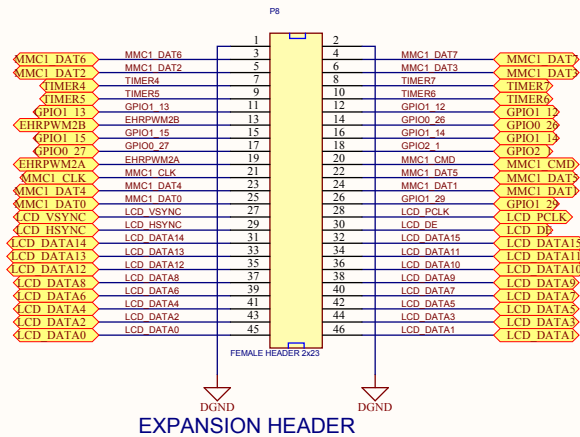






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Title				BeagleBoneBlack HDMI Interface			
Size	Document Number					Rev	
B	450-5500-001					A5B	
Date:	Monday, April 01, 2013			Sheet	10	of	11



Title: BeagleBoneBlack Expansion Headers, uSD and EEPROM

Size: A Document Number: 450-5500-001 Rev: A5B

Date: Monday, April 01, 2013 Sheet: 11 of 11

FAB NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE NOTED.
2. THE PWB SHALL BE FABRICATED TO IPC-6012, CLASS 2 AND WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2. CURRENT REVISIONS.
3. BOARD MATERIAL SHALL BE 180 Tg/350 Td ISOLA FR-370HR OR EQUIVALENT, ROHS COMPLIANT AND LEAD FREE ASSEMBLY CAPABLE. BOARD MATERIAL SHALL MEET OR EXCEED PC-4101B. COLOR: NATURAL.
4. BOARD MATERIAL & CONSTRUCTION TO BE ULL APPROVED AND MARKED ON THE FINISHED BOARD.
5. MINIMUM COPPER WALL THICKNESS OF PLATED-THRU HOLES TO BE .001 INCH, WITH A MINIMUM ANNULAR RING OF .002 INCH.
6. OVERALL BOARD THICKNESS TO BE .062 +/- .010 AND APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES, MEASURED FROM COPPER TO COPPER.
7. MAX. WARP & TWIST TO BE .0075 INCHES PER INCH.
8. BOARD MUST BE ELECTRICALLY TESTED USING SUPPLIED PC-D-356 NETLIST.
9. ALL WAS TO HAVE SOLDERMASK.

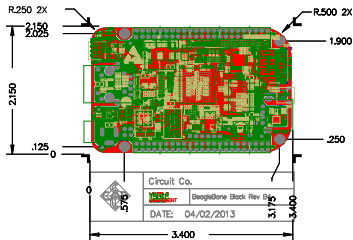
FINISHED AS SMOOTH WALL BY VENDOR.  
PROCESS NOTES:

1. PLATE ALL EXPOSED AREAS WITH ELECTROLESS IMMERSION GOLD, NICKEL 150 MICRONS THK MIN. GOLD 5-15 MICRONS THK MIN.
2. APPLY LP SOLDERMASK OVER BARE COPPER (SMBRC). COLOR: BLACK. SOLDERMASK SHALL CONFORM TO PC-SM-840, CLASS H, CURRENT REV.
3. SOLDERMASK ARTWORK HAS ZERO (0) OVERSIZED PADS. FABRICATION VENDOR IS ALLOWED TO ADJUST THE COMPONENT SOLDERMASK PADS TO MEET THEIR TOOLING REQUIREMENTS.
4. APPLY LP SILKSCREEN OR EQUIVALENT PER THE ARTWORK. COLOR: WHITE.

LAYER STACK-UP - ALL DIMENSIONS IN INCHES

LAYER#	COPPER WEIGHT REF	500um SINGLE ENDED IMPEDANCE CONTROL +/- .05%	500um DIFFERENTIAL IMPEDANCE CONTROL +/- .05%	1000um DIFFERENTIAL IMPEDANCE CONTROL +/- .10%
		TRACE WIDTH	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE
LAYER 1 - PRIMARY SDE - SIGNAL	HALF-PLATING	4.75	4.5/6.5	3.75/7.25
LAYER 2 - GROUND PLANE	1			
LAYER 3 - SIGNAL	1	5.25	5.0/7.0	4.00/8.00
LAYER 4 - SIGNAL	1	5.25	5.0/7.0	4.00/8.00
LAYER 5 - SPLIT POWER PLANE	1			
LAYER 6 - SECONDARY SDE - SIGNAL	HALF-PLATING	4.75	4.5/6.5	3.75/7.25

DRILL CHART: TOP to BOTTOM				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
*	6.0	+3.0/-3.0	PLATED	27
*	8.0	+3.0/-3.0	PLATED	794
*	12.0	+3.0/-3.0	PLATED	30
o	30.0	+3.0/-3.0	PLATED	96
o	40.0	+3.0/-3.0	PLATED	26
o	63.0	+3.0/-3.0	PLATED	2
o	125.0	+3.0/-3.0	PLATED	4
O	128.0	+5.0/-5.0	NON-PLATED	2
*	50.0x15.0	+3.0/-3.0	PLATED	2
x	95.0x40.0	+3.0/-3.0	PLATED	2
x	120.0x40.0	+3.0/-3.0	PLATED	1
x	120.0x40.0	+3.0/-3.0	PLATED	1
x	140.0x40.0	+3.0/-3.0	PLATED	1



DATE 04/02/13 DESIGN ENGR PROJECT ENGR ENGR MGR NEXT ASSEMBLY	APPROVED		CIRCUITCO.	
	CHECKED			
	DRAFTING	CoCad	FABRICATION DRAWING, BeagleBone Black	
	ENGR			
		TOLERANCES UNLESS OTHERWISE SPECIFIED		
		1/16" & 1/8" 1/16" & 1/8" 1/16" & 1/8"		
		DO NOT SCALE DRAWING		
		SCALE	NONE	
		SHEET	1 OF 1	
		PCB REV B4		
		SIZE		D

