REV	Description	DATE	BY
A3	Production release.	10/21/2011	GC
A3A	Updated in conjunction with the release of the SRM. Typos and naming changes. No change in design.	11/5/2011	GC
A4	1. Changed supplier for the SD card connector due to availability issue. Created a dual footprint for two differrent parts. SD connector is now reversed, so label down is the new orientation. 2. Changed R76 from a 50 ohm to 49.9 ohm. Smaller package and lower cost. Changed footprint to 0402. 3. Changed C99 termination to DGND. 4. Added 10K pulldown to fix link speed LED. 5. Changed C7 to a 0805 package in PCB layout.	12/1/2011	GC
A5	1. Changed R219 to DNI. It was causing issues with Ethernet DHCP IP address aquisition. Will be added back in on revision A6. 2. Removed VDD_CORE rail from VPP PIN. Ball on procesor was removed before assembly. PCB will be changed in Revision A6.	2/3/2012	GC

This schematic is *NOT SUPPORTED* and DOES NOT constitute a reference design. Only "community" support is allowed via resources at BeagleBoard.org/discuss.

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PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	POWER MANAGEMENT
3	PROCESSOR 1 OF 3
4	PROCESSOR 2 OF 3
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	MEMORY
8	ETHERNET AND USB HOST
9	USB CONCENTRATOR
10	SERIAL AND JTAG
11	EXP CONN, uSD, AND LDO

NOTE: PCB Revision for this board is Rev C1.

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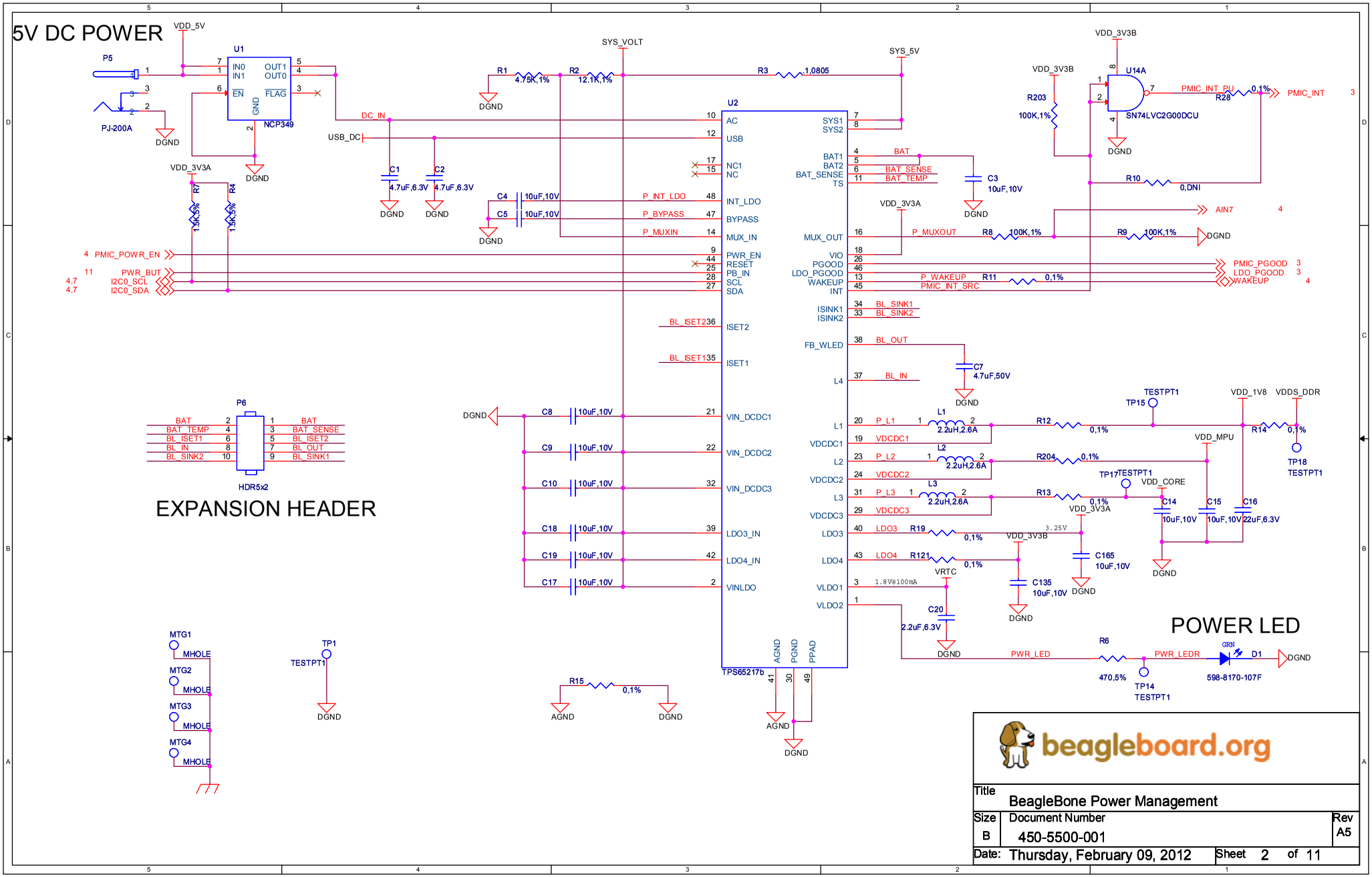
5V DC POWER
VDD_5V
P5
PJ-200A
U1
NCP349
IN0
IN1
OUT1
OUT0
EN
FLAG
GND
DGND
SYS_VOLT
R1
4.75K,1%
R2
12.1K,1%
R3
1,0805
SYS_5V
DC_IN
USB_DC
C1
4.7uF,6.3V
C2
4.7uF,6.3V
VDD_3V3A
R7
1.5K,5%
R4
1.5K,5%
U2
TPS65217b
AC
USB
NC1
NC
INT_LDO
BYPASS
MUX_IN
PWR_EN
RESET
PB_IN
SCL
SDA
SYS1
SYS2
BAT1
BAT2
BAT_SENSE
TS
MUX_OUT
VIO
PGOOD
LDO_PGOOD
WAKEUP
INT
ISINK1
ISINK2
ISET2
ISET1
FB_WLED
L4
L1
VDCDC1
L2
VDCDC2
L3
VDCDC3
LDO3
LDO4
VLDO1
VLDO2
VIN_DCDC1
VIN_DCDC2
VIN_DCDC3
LDO3_IN
LDO4_IN
VINLDO
AGND
PGND
PPAD
C3
10uF,10V
C4
10uF,10V
C5
10uF,10V
C7
4.7uF,50V
C8
10uF,10V
C9
10uF,10V
C10
10uF,10V
C18
10uF,10V
C19
10uF,10V
C17
10uF,10V
C20
2.2uF,6.3V
C135
10uF,10V
C165
10uF,10V
C14
10uF,10V
C15
10uF,10V
C16
22uF,6.3V
L1
2.2uH,2.6A
L2
2.2uH,2.6A
L3
2.2uH,2.6A
R8
100K,1%
R9
100K,1%
R10
0,DNI
R11
0,1%
R12
0,1%
R13
0,1%
R14
0,1%
R15
0,1%
R19
0,1%
R121
0,1%
R204
0,1%
R203
100K,1%
R28
0,1%
R6
470,5%
U14A
SN74LVC2G00DCU
PMIC_INT_PU
PMIC_INT
P_INT_LDO
P_BYPASS
P_MUXIN
P_MUXOUT
P_WAKEUP
PMIC_INT_SRC
BAT
BAT_SENSE
BAT_TEMP
BL_SINK1
BL_SINK2
BL_ISET2
BL_ISET1
BL_OUT
BL_IN
P_L1
P_L2
P_L3
LDO3
LDO4
VRTC
1.8V@100mA
3.25V
PWR_LED
PWR_LEDR
D1
GRN
598-8170-107F
AIN7
PMIC_PGOOD
LDO_PGOOD
WAKEUP
PMIC_POWR_EN
PWR_BUT
I2C0_SCL
I2C0_SDA
VDD_3V3B
VDD_1V8
VDDS_DDR
VDD_MPU
VDD_CORE
TESTPT1
TP15
TP17
TP18
TP14
TP1
P6
HDR5x2
BAT
BAT_TEMP
BL_ISET1
BL_IN
BL_SINK2
BL_SINK1
EXPANSION HEADER
POWER LED
MTG1
MTG2
MTG3
MTG4
MHOLE
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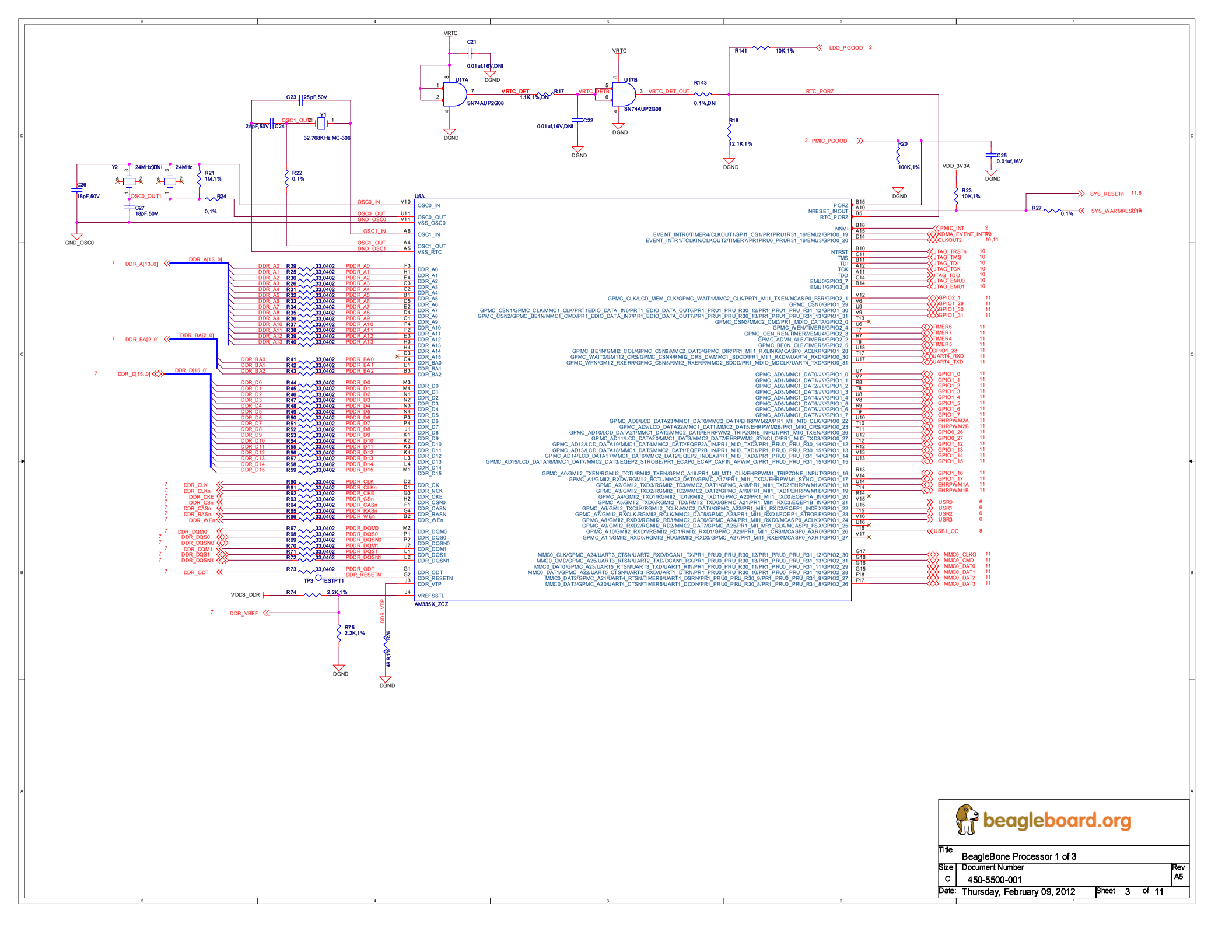
VRTC
C21
0.01 uf,16V,DNI
DGND
U17A
SN74AUP2G08
VRTC_DET
R17
1.1K,1%,DNI
U17B
VRTC_DETB
VRTC_DET_OUT
R143
0,1%,DNI
R141
10K,1%
LDO_PGOOD 2
RTC_PORZ
C22
0.01uf,16V,DNI
R18
12.1K,1%
2 PMIC_PGOOD
R20
100K,1%
C25
0.01uf,16V
VDD_3V3A
R23
10K,1%
SYS_RESETn 11,8
R27
0,1%
SYS_WARMRESETn 10
C23 25pF,50V
25pF,50V C24
OSC1_OUT
Y1
32.768KHz MC-306
Y2 24MHz,DNI
24MHz
R21
1M,1%
R22
0,1%
C26
18pF,50V
OSC0_OUT1
C27
18pF,50V
R24
0,1%
GND_OSC0
U5A
OSC0_IN
OSC0_OUT
GND_OSC0
OSC1_IN
OSC1_OUT
GND_OSC1
VSS_OSC0
VSS_RTC
AM335X_ZCZ
PORZ
NRESET_INOUT
RTC_PORZ
NMI
EVENT_INTR0/TIMER4/CLKOUT1/SPI1_CS1/PR1PRU1R31_16/EMU2/GPIO0_19
EVENT_INTR1/TCLKIN/CLKOUT2/TIMER7/PR1PRU0_PRUR31_16/EMU3/GPIO0_20
NTRST
TMS
TDI
TCK
TDO
EMU0/GPIO3_7
EMU1/GPIO3_8
GPMC_CLK/LCD_MEM_CLK/GPMC_WAIT1/MMC2_CLK/PRT1_MII1_TXEN/MCASP0_FSR/GPIO2_1
GPMC_CSN0/GPIO1_29
GPMC_CSN1/GPMC_CLK/MMC1_CLK/PRT1EDIO_DATA_IN6/PRT1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_12/PR1_PRU1_PRU_R31_12/GPIO1_30
GPMC_CSN2/GPMC_BE1N/MMC1_CMD/PR1_EDIO_DATA_IN7/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_13/PR1_PRU1_PRU_R31_13/GPIO1_31
GPMC_CSN3/MMC2_CMD/PR1_MDIO_DATA/GPIO2_0
GPMC_WEN/TIMER6/GPIO2_4
GPMC_OEN_REN/TIMER7/EMU4/GPIO2_3
GPMC_ADVN_ALE/TIMER4/GPIO2_2
GPMC_BE0N_CLE/TIMER5/GPIO2_5
GPMC_BE1N/GMII2_COL/GPMC_CSN6/MMC2_DAT3/GPMC_DIR/PR1_MII1_RXLINK/MCASP0_ACLKR/GPIO1_28
GPMC_WAIT0/GM112_CRS/GPMC_CSN4/RMII2_CRS_DV/MMC1_SDCD/PR1_MII1_RXDV/UART4_RXD/GPIO0_30
GPMC_WPN/GMII2_RXERR/GPMC_CSN5/RMII2_RXERR/MMC2_SDCD/PR1_MDIO_MDCLK/UART4_TXD/GPIO0_31
GPMC_AD0/MMC1_DAT0/////GPIO1_0
GPMC_AD1/MMC1_DAT1/////GPIO1_1
GPMC_AD2/MMC1_DAT2/////GPIO1_2
GPMC_AD3/MMC1_DAT3/////GPIO1_3
GPMC_AD4/MMC1_DAT4/////GPIO1_4
GPMC_AD5/MMC1_DAT5/////GPIO1_5
GPMC_AD6/MMC1_DAT6/////GPIO1_6
GPMC_AD7/MMC1_DAT7/////GPIO1_7
GPMC_AD8/LCD_DATA23/MMC1_DAT0/MMC2_DAT4/EHRPWM2A/PR1_MII_MT0_CLK/GPIO0_22
GPMC_AD9/LCD_DATA22/MMC1_DAT1/MMC2_DAT5/EHRPWM2B/PR1_MII0_CRS/GPIO0_23
GPMC_AD10/LCD_DATA21/MMC1_DAT2/MMC2_DAT6/EHRPWM2_TRIPZONE_INPUT/PR1_MII0_TXEN/GPIO0_26
GPMC_AD11/LCD_DATA20/MMC1_DAT3/MMC2_DAT7/EHRPWM2_SYNCI_O/PR1_MII0_TXD3/GPIO0_27
GPMC_AD12/LCD_DATA19/MMC1_DAT4/MMC2_DAT0/EQEP2A_IN/PR1_MII0_TXD2/PR1_PRU0_PRU_R30_14/GPIO1_12
GPMC_AD13/LCD_DATA18/MMC1_DAT5/MMC2_DAT1/EQEP2B_IN/PR1_MII0_TXD1/PR1_PRU0_PRU_R30_15/GPIO1_13
GPMC_AD14/LCD_DATA17/MMC1_DAT6/MMC2_DAT2/EQEP2_INDEX/PR1_MII0_TXD0/PR1_PRU0_PRU_R31_14/GPIO1_14
GPMC_AD15/LCD_DATA16/MMC1_DAT7/MMC2_DAT3/EQEP2_STROBE/PR1_ECAP0_ECAP_CAPIN_APWM_O/PR1_PRU0_PRU_R31_15/GPIO1_15
GPMC_A0/GMII2_TXEN/RGMII2_TCTL/RMII2_TXEN/GPMC_A16/PR1_MII_MT1_CLK/EHRPWM1_TRIPZONE_INPUT/GPIO1_16
GPMC_A1/GMII2_RXDV/RGMII2_RCTL/MMC2_DAT0/GPMC_A17/PR1_MII1_TXD3/EHRPWM1_SYNCI_O/GPIO1_17
GPMC_A2/GMII2_TXD3/RGMII2_TD3/MMC2_DAT1/GPMC_A18/PR1_MII1_TXD2/EHRPWM1A/GPIO1_18
GPMC_A3/GMII2_TXD2/RGMII2_TD2/MMC2_DAT2/GPMC_A19/PR1_MII1_TXD1/EHRPWM1B/GPIO1_19
GPMC_A4/GMII2_TXD1/RGMII2_TD1/RMII2_TXD1/GPMC_A20/PR1_MII1_TXD0/EQEP1A_IN/GPIO1_20
GPMC_A5/GMII2_TXD0/RGMII2_TD0/RMII2_TXD0/GPMC_A21/PR1_MII1_RXD3/EQEP1B_IN/GPIO1_21
GPMC_A6/GMII2_TXCLK/RGMII2_TCLK/MMC2_DAT4/GPMC_A22/PR1_MII1_RXD2/EQEP1_INDEX/GPIO1_22
GPMC_A7/GMII2_RXCLK/RGMII2_RCLK/MMC2_DAT5/GPMC_A23/PR1_MII1_RXD1/EQEP1_STROBE/GPIO1_23
GPMC_A8/GMII2_RXD3/RGMII2_RD3/MMC2_DAT6/GPMC_A24/PR1_MII1_RXD0/MCASP0_ACLKX/GPIO1_24
GPMC_A9/GMII2_RXD2/RGMII2_RD2/MMC2_DAT7/GPMC_A25/PR1_MII_MR1_CLK/MCASP0_FSX/GPIO1_25
GPMC_A10/GMII2_RXD1/RGMII2_RD1/RMII2_RXD1/GPMC_A26/PR1_MII1_CRS/MCASP0_AXR0/GPIO1_26
GPMC_A11/GMII2_RXD0/RGMII2_RD0/RMII2_RXD0/GPMC_A27/PR1_MII1_RXER/MCASP0_AXR1/GPIO1_27
MMC0_CLK/GPMC_A24/UART3_CTSN/UART2_RXD/DCAN1_TX/PR1_PRU0_PRU_R30_12/PR1_PRU0_PRU_R31_12/GPIO2_30
MMC0_CMD/GPMC_A25/UART3_RTSN/UART2_TXD/DCAN1_RX/PR1_PRU0_PRU_R30_13/PR1_PRU0_PRU_R31_13/GPIO2_31
MMC0_DAT0/GPMC_A23/UART5_RTSN/UART3_TXD/UART1_RIN/PR1_PRU0_PRU_R30_11/PR1_PRU0_PRU_R31_11/GPIO2_29
MMC0_DAT1/GPMC_A22/UART5_CTSN/UART3_RXD/UART1_DTRN/PR1_PRU0_PRU_R30_10/PR1_PRU0_PRU_R31_10/GPIO2_28
MMC0_DAT2/GPMC_A21/UART4_RTSN/TIMER6/UART1_DSRN/PR1_PRU0_PRU_R30_9/PR1_PRU0_PRU_R31_9/GPIO2_27
MMC0_DAT3/GPMC_A20/UART4_CTSN/TIMER5/UART1_DCDN/PR1_PRU0_PRU_R30_8/PR1_PRU0_PRU_R31_8/GPIO2_26
PMIC_INT
XDMA_EVENT_INTR0
CLKOUT2
JTAG_TRSTn
JTAG_TMS
JTAG_TDI
JTAG_TCK
JTAG_TDO
JTAG_EMU0
JTAG_EMU1
GPIO2_1
GPIO1_29
GPIO1_30
GPIO1_31
TIMER6
TIMER7
TIMER4
TIMER5
GPIO1_28
UART4_RXD
UART4_TXD
GPIO1_0
GPIO1_1
GPIO1_2
GPIO1_3
GPIO1_4
GPIO1_5
GPIO1_6
GPIO1_7
EHRPWM2A
EHRPWM2B
GPIO0_26
GPIO0_27
GPIO1_12
GPIO1_13
GPIO1_14
GPIO1_15
GPIO1_16
GPIO1_17
EHRPWM1A
EHRPWM1B
USR0
USR1
USR2
USR3
USB1_OC
MMC0_CLKO
MMC0_CMD
MMC0_DAT0
MMC0_DAT1
MMC0_DAT2
MMC0_DAT3
DDR_A[13..0]
DDR_BA[2..0]
DDR_D[15..0]
DDR_CLK
DDR_CLKn
DDR_CKE
DDR_CSn
DDR_CASn
DDR_RASn
DDR_WEn
DDR_DQM0
DDR_DQS0
DDR_DQSN0
DDR_DQM1
DDR_DQS1
DDR_DQSN1
DDR_ODT
DDR_RESETN
TP3
TESTPT1
VDDS_DDR
R74
2.2K,1%
DDR_VREF
R75
2.2K,1%
DDR_VTP
R76
49.9,1%
DGND
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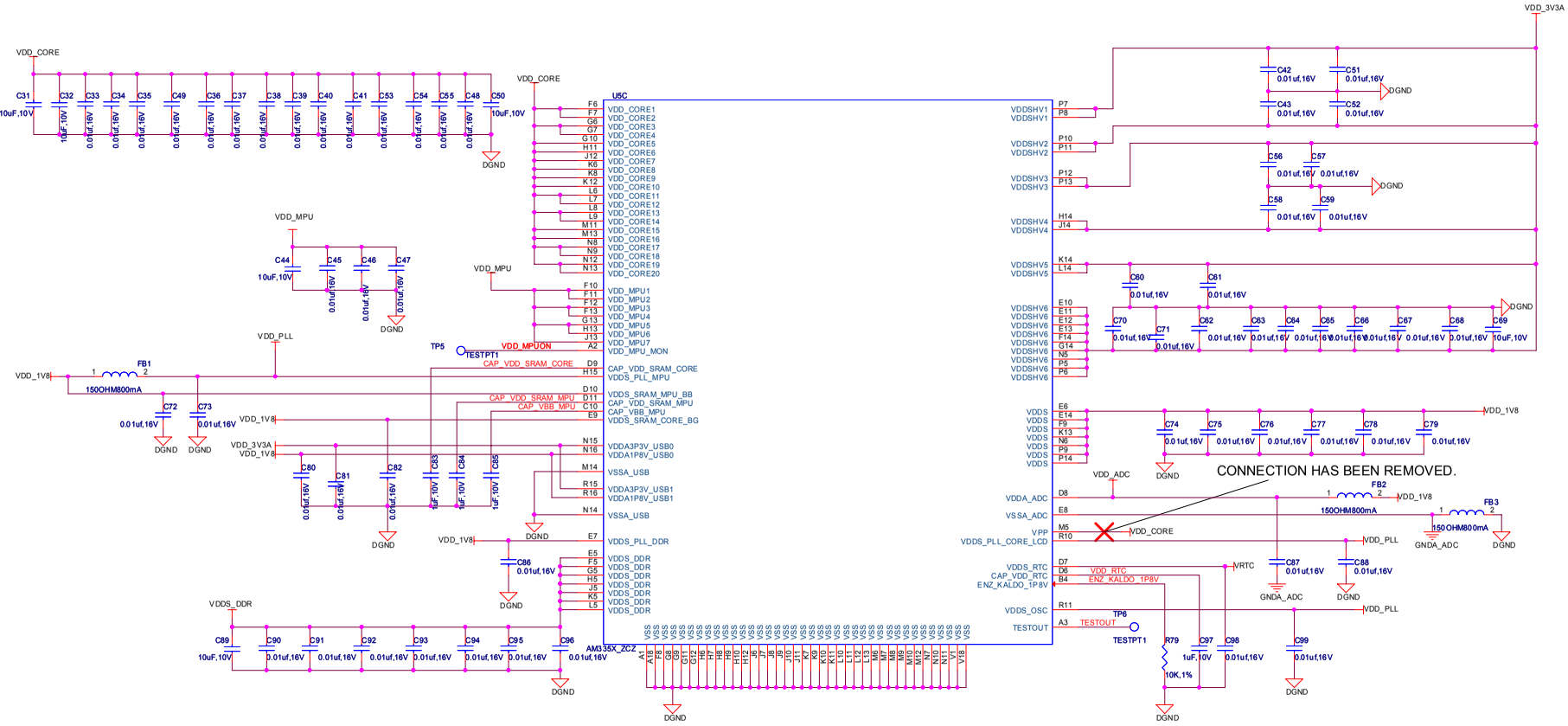

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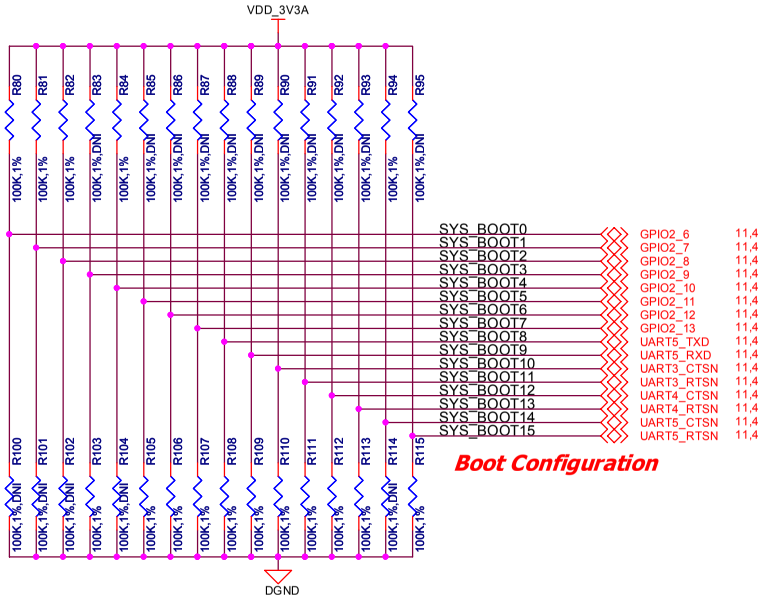
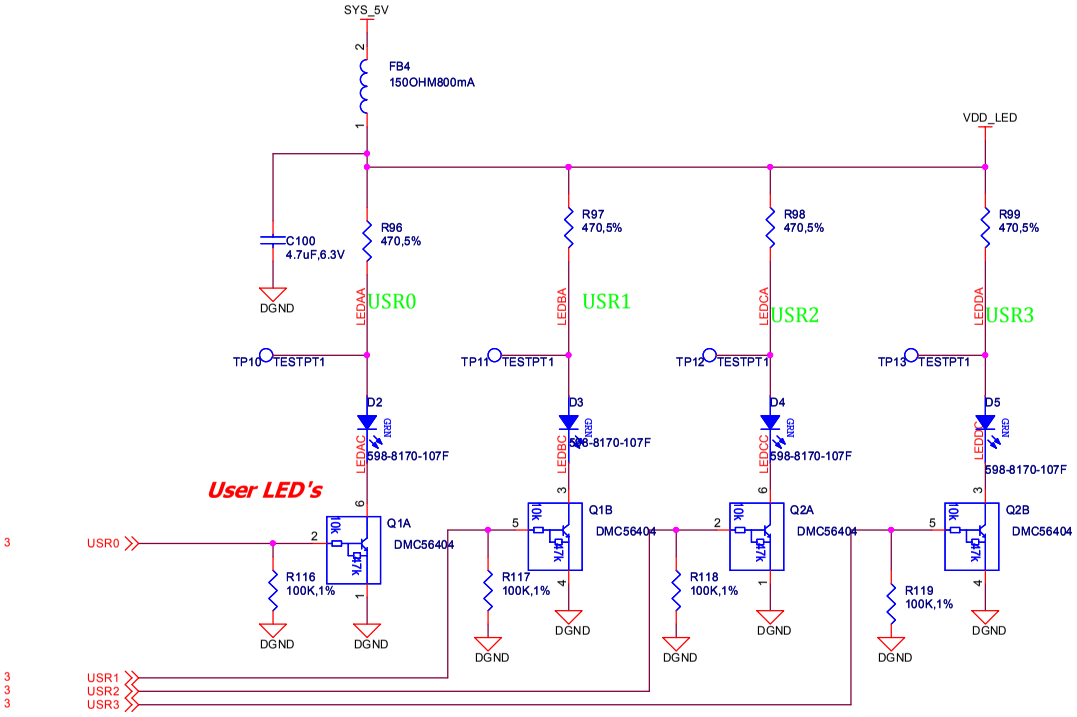
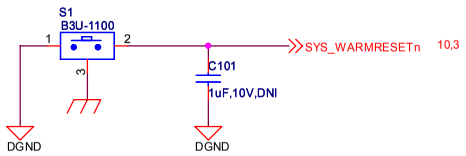


Boot Configuration

BOOT ORDER....MMC....SPI....UART....USB.....24MHZ



RESET BUTTON



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Title	BeagleBone LED, Configuration and Reset	
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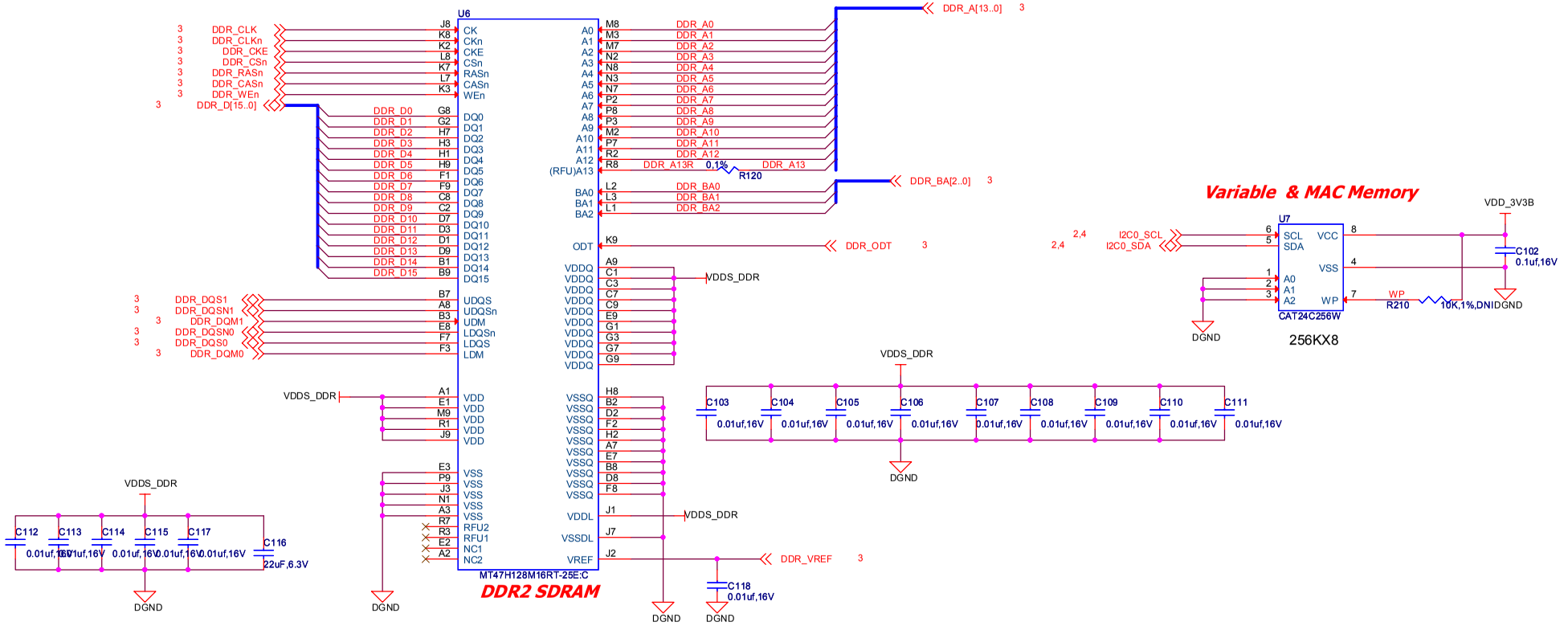

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Title	BeagleBone DDR2 Memory	
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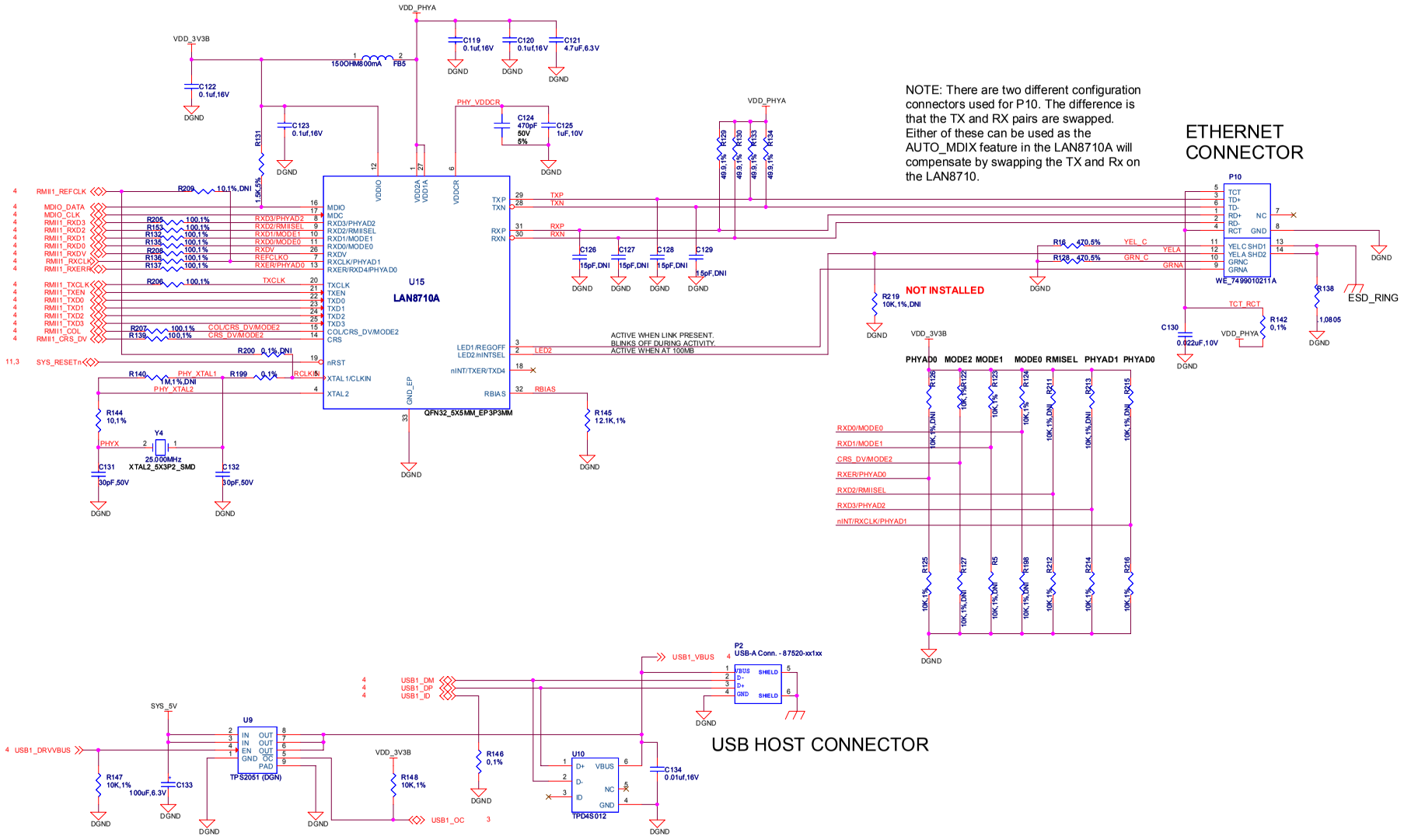

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Title	BeagleBone Ethernet and USB Host	
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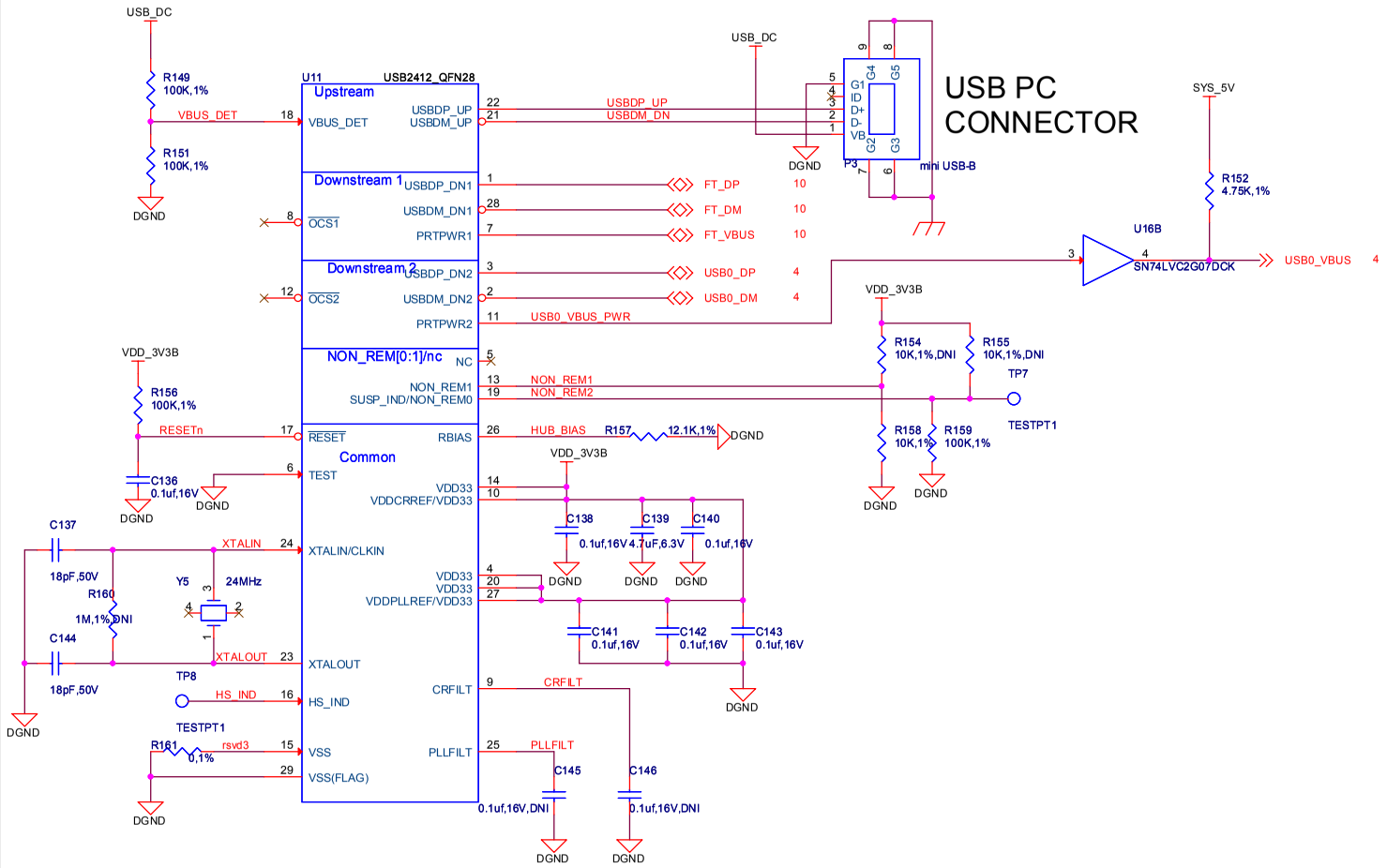

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Title	BeagleBone USB Concentrator	
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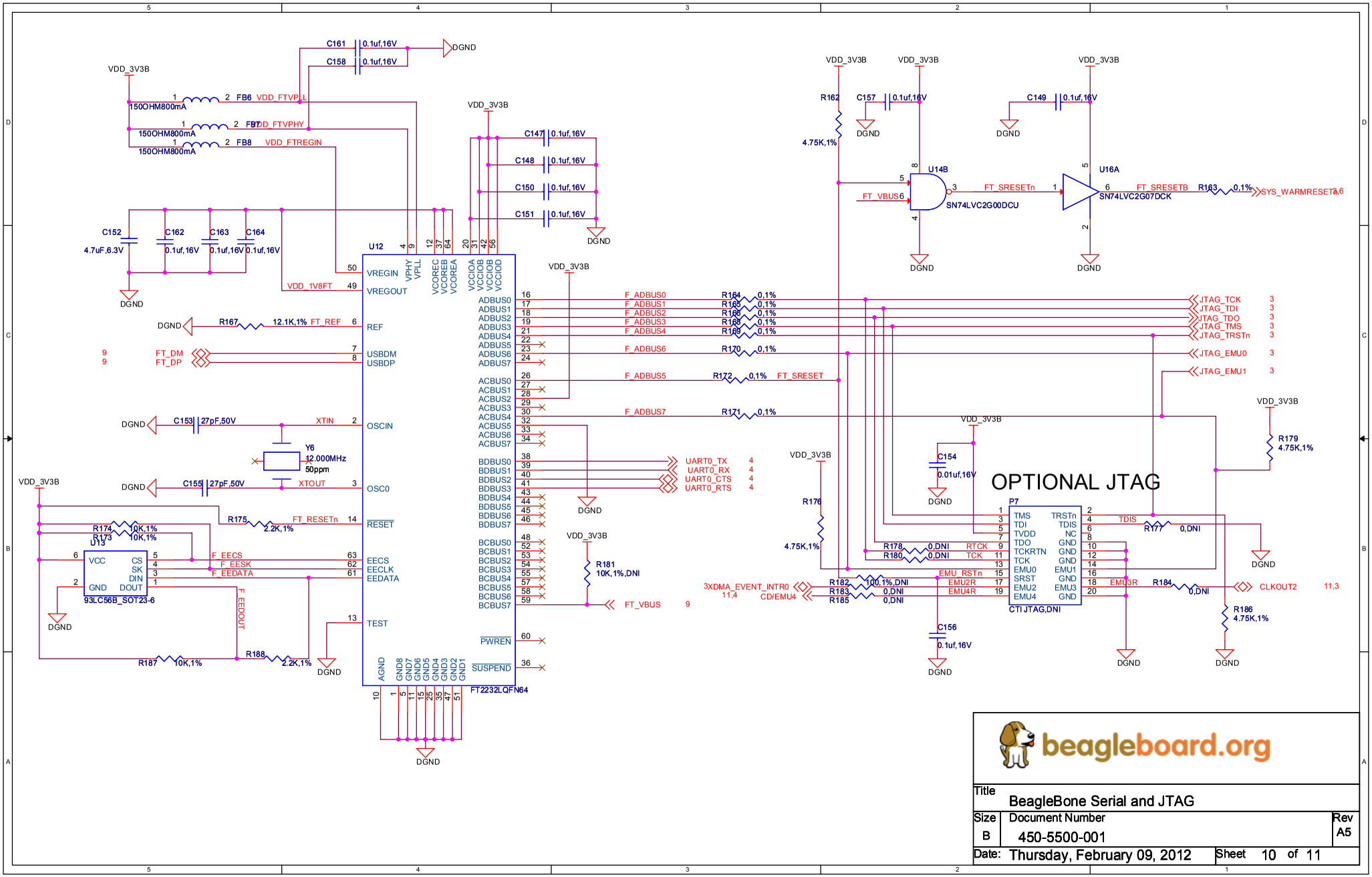

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Title	BeagleBone Serial and JTAG	
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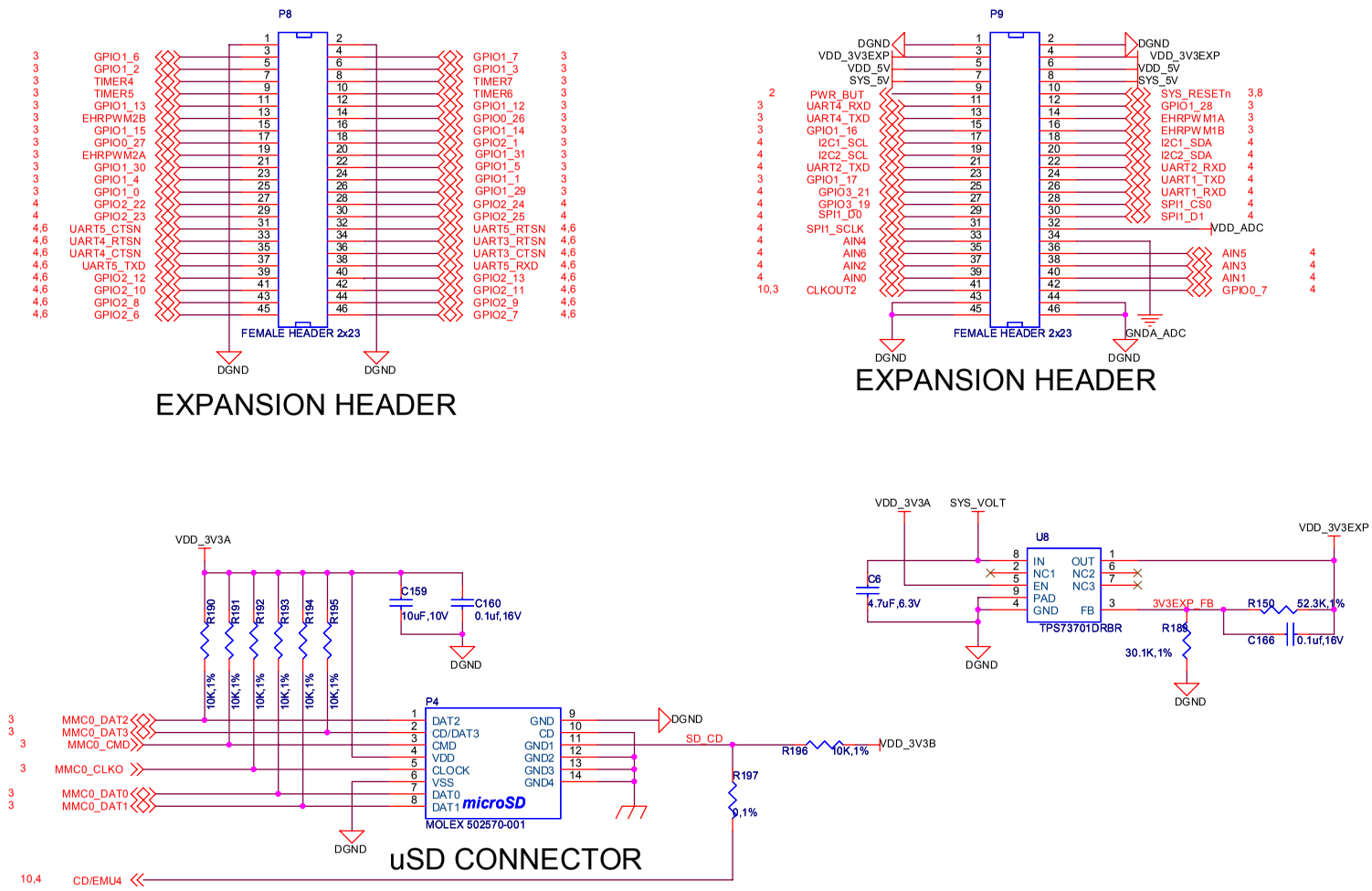

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Title	BeagleBone Expansion Headers, SD/MMC.and LDO	
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