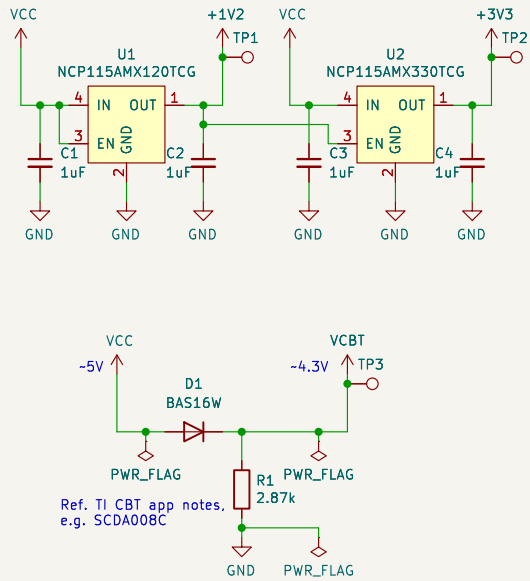
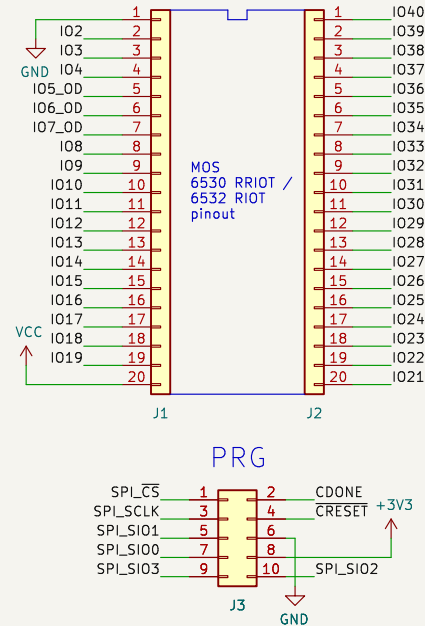


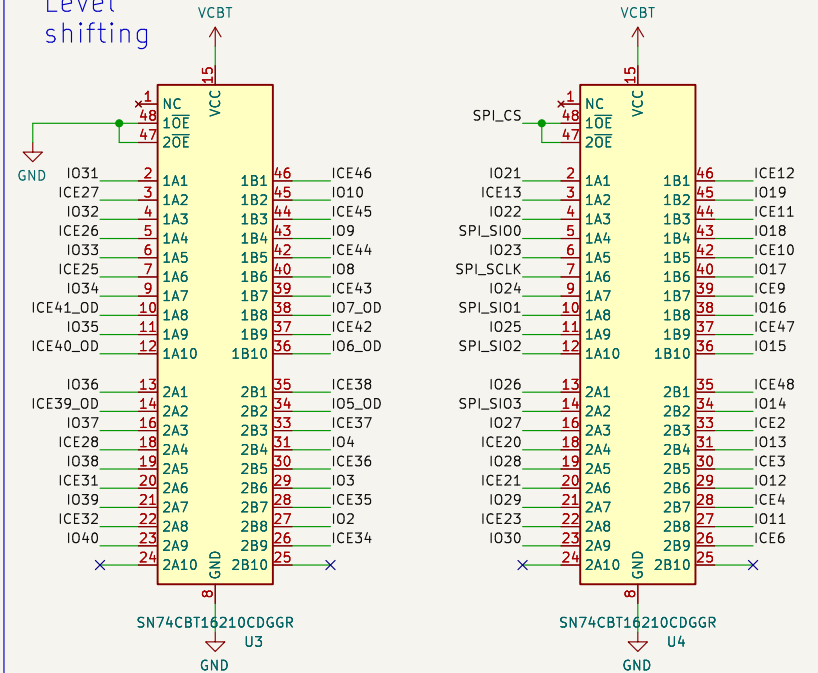
Power



I/O



Level shifting



FPGA

