CS35L36A Schematic and Layout Guidelines

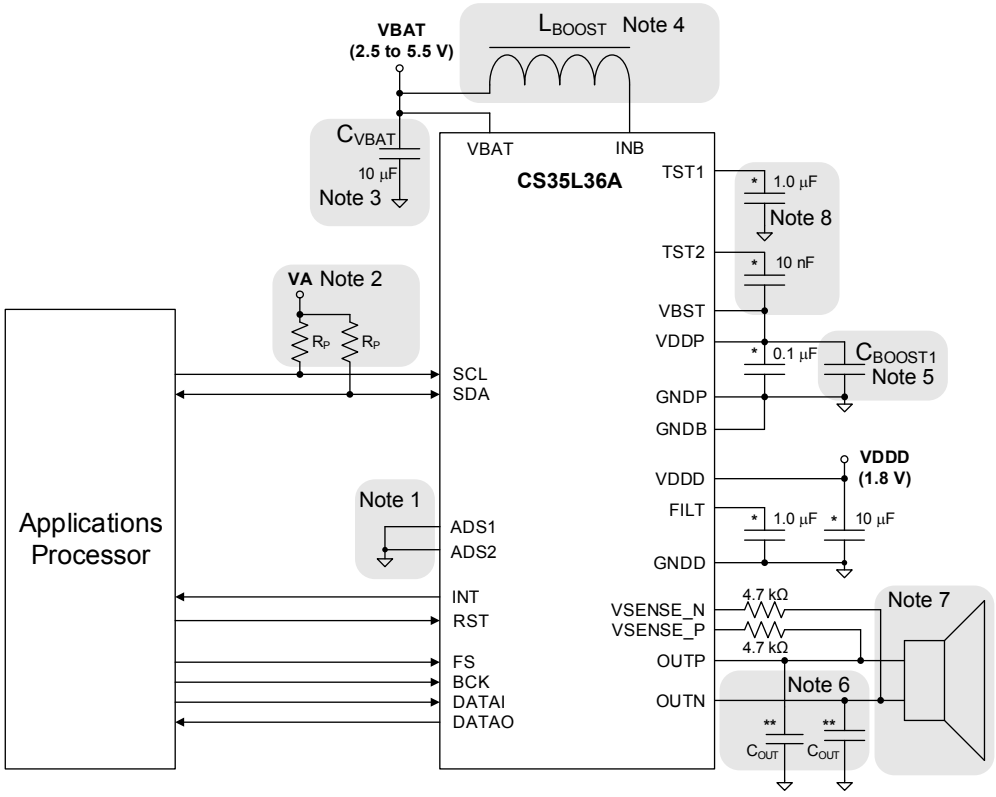
1 Introduction

This document describes the schematic and layout guidelines for the CS35L36A amplifier.

All layout recommendations are preliminary and may be updated in future revisions of this document.

2 Schematic Reference

The schematic below corresponds to a basic configuration for the amplifier.



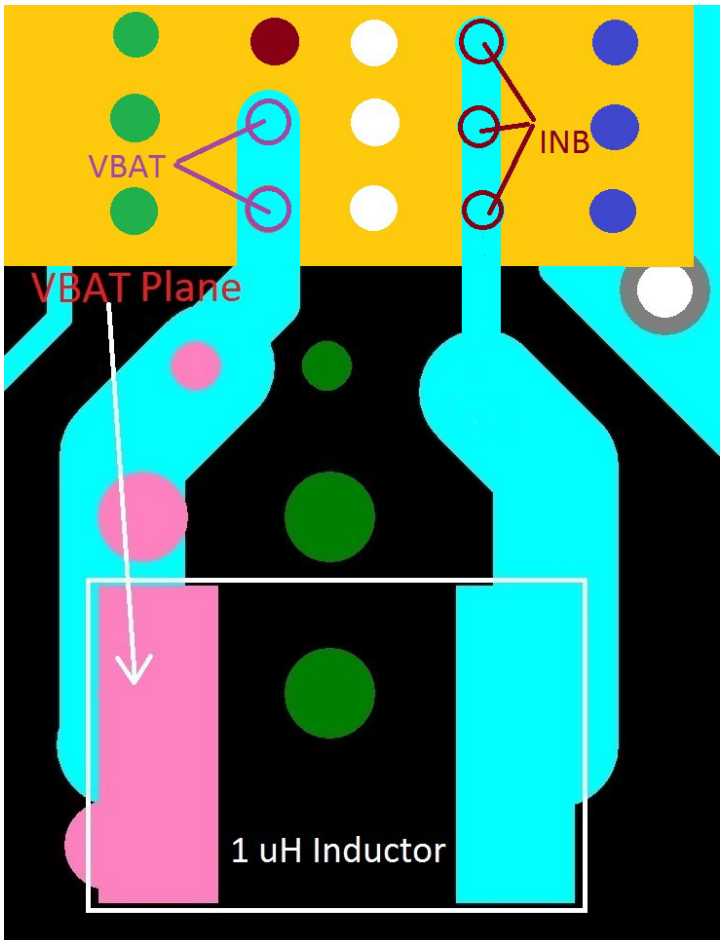
2.1 Schematic Suggestions - Component Selection

1. This shows one example of how to configure the 7-bit I²C address. The I²C address is set as 0x50 in this case.
2. Minimum R_P value is determined from the maximum VDDD level, the minimum sink current strength of their respective output, and the maximum low-level output voltage (V_{OL}). Maximum R_P values may be determined by how fast their associated signals must transition, taking into account load capacitance.
3. Place the 10-µF bulk capacitor close to the L_{BOOST} inductor.
4. Boost converter L_{BOOST} inductor values of 2.2 to 1.0 µH are supported for typical use operation. However, the selected L_{BOOST} inductor must not derate to a value of less than 0.7 µH during normal use to maintain proper loop stability.
5. The boost converter C_{BOOST} capacitors are recommended to have a maximum voltage rating of at least 10 V and must not derate to a combined capacitance value of less than 3.6 µF when 10.0 VDC is applied across the capacitors. Note that ceramic capacitors can derate considerably when a DC voltage is applied to them. The total derated C_{BOOST} capacitance at 10.0 VDC must not exceed 58 µF.
6. The C_{OUT} capacitors are optional EMI suppressors that are used depending on the application requirements. It is recommended that the value of these components not exceed 2 nF, as switching losses increase linearly with increases to these capacitances.
7. When using a simulated speaker load of 8 Ω + 33 µH, a Coilcraft DO5040H-333MLB inductor is used.
8. Presence of capacitors on TST1 and TST2 pins impart no functionality during normal operation. They may be omitted and are completely optional.

3 Layout Suggestions

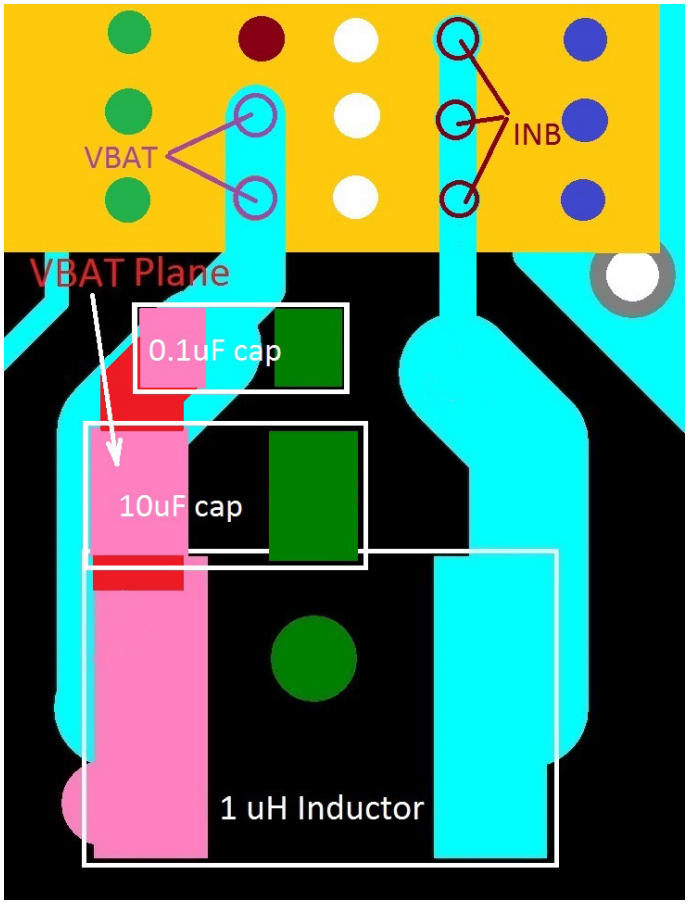
3.1 VBAT Routing

1. Use a power plane for VBAT delivery.
2. Connect VBAT to the inductor with multiple vias.
3. The VBAT pins (C1, C2) should drop down directly to the VBAT plane through vias.
4. Use wide (~25 mil) and as short as possible traces to connect the inductor to the INB node (E1, E2, E3).



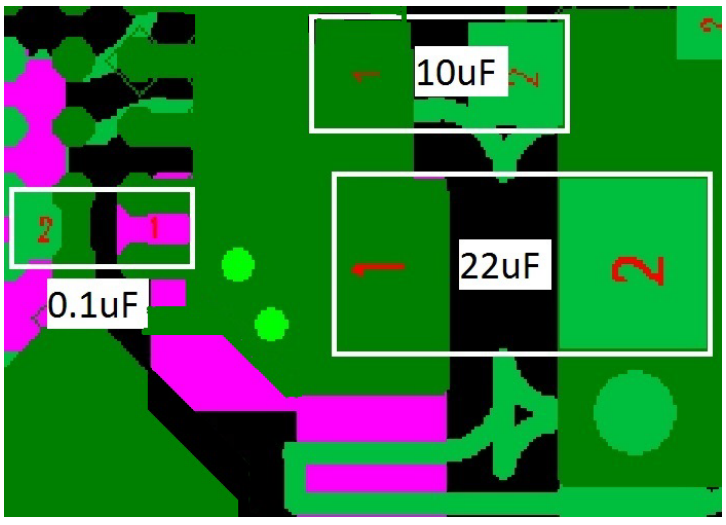
3.2 VBAT Decoupling

1. Place a 0.1 µF capacitor as close to the VBAT pins (C1, C2) as possible.
2. Place a 10 µF CVBAT capacitor as close to the inductor connection to the VBAT supply as possible. Depending on the available board space, it may be placed on either side of the board.



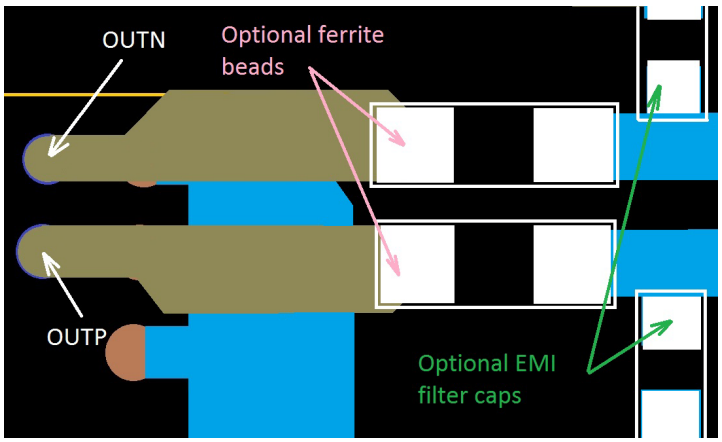
3.3 VBST Routing

1. Place a 0.1 µF CBOOST(OUT) bypass cap as close to the VBST pins (F1, F2, F3) as possible.
2. Place larger CBOOST(OUT) bypass caps (22 µF and 10 µF) close to VBST pads.
3. Tie all VBST/VDDP pins together (F1 through F6) by a 5 mil wide trace and come out to a wider ~25 mil trace for the large bypass caps.



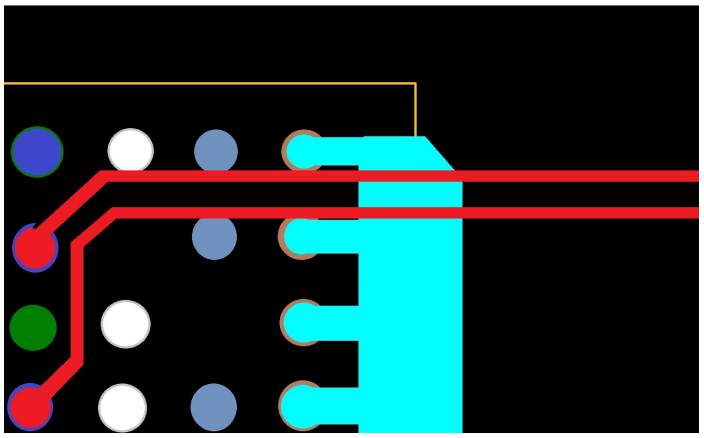
3.4 Speaker Routing

1. OUTP and OUTN traces should be as symmetrical as possible.
2. Bring out signals on inner layer and come up to top layer.
3. Maintain 30-40 mil trace width as traces go out to the SPKR pads.
4. Maintain distance from VBST/VDDP before bringing traces up to the top layer.
5. Have GND shield around output traces to avoid noise coupling.



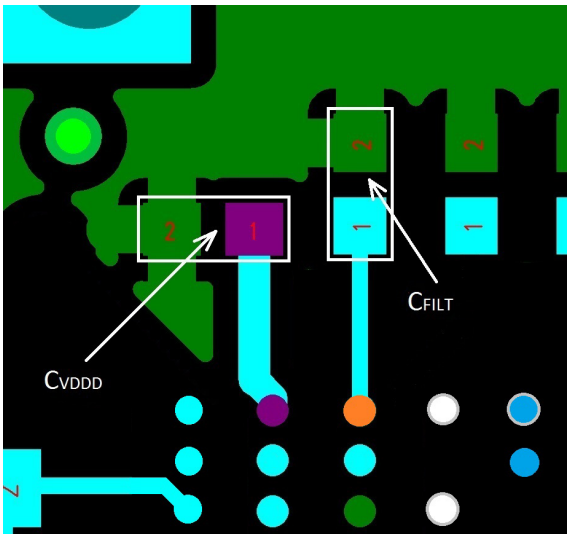
3.5 VSENSE Routing

1. Run 5 mil or wider VSENSE_P and VSENSE_N traces differentially between VSENSE_P, VSENSE_N pads and the output side of the EMI filter (speaker side).
2. Provide GND shielding around VSENSE_P and VSENSE_N traces to minimize noise coupling from the Class-D outputs.
3. An RC filter may be optionally added to the VSENSE_P and VSENSE_N lines for output EMI filtering.



3.6 Miscellaneous Routing

1. Place the FILT decoupling capacitor as close as possible to pad C6.
2. Place the VDDD decoupling capacitor as close as possible to pad B6.
3. All ground pins need to be connected to the same ground plane.



4 Revision History

Table 4-1. Revision History

Revision	Change
R1 SEP ‘17	Initial revision.

Important: Please check with your Cirrus sales representative to confirm that you are using the latest revision of this document.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.