

## Mono Class D Amplifier with Boost Converter and Monitoring

### Speaker Amplifier Features

- Digital input, advanced  $\Delta\Sigma$  closed-loop architecture
- 7.0 W @ 1% THD+N into 8  $\Omega$  (VBAT = 3.8 V)
- Programmable digital volume and amplifier gain
- Idle channel noise: 9  $\mu\text{Vrms}$  (A-weighted)
- Audio signal adaptive noise reduction
- Class D architecture with adaptive output stage reduces idle power consumption and switching losses

### Monitoring Features

- Battery supply (VBAT) and boost converter supply (VBST)
- Integrated amplifier output current (IMON) and dual voltage (VMON1 + VMON2)
- VMON-to-IMON ratio accuracy  $\leq \pm 0.4\%$
- VMON absolute accuracy variation  $\leq \pm 2\%$
- IMON absolute accuracy variation  $\leq \pm 2\%$
- Local generation of monitoring reference produces values independent of supply rails

### Boost Converter Features

- Adjustable bandwidth digital control loop
- Continuous Conduction Mode for high power delivery
- Discontinuous Conduction Mode for low idle power consumption
- Programmable boost voltages of up to 12 V
- Integrated boost and rectification FETs
- Integrated Class H tracking of audio signal

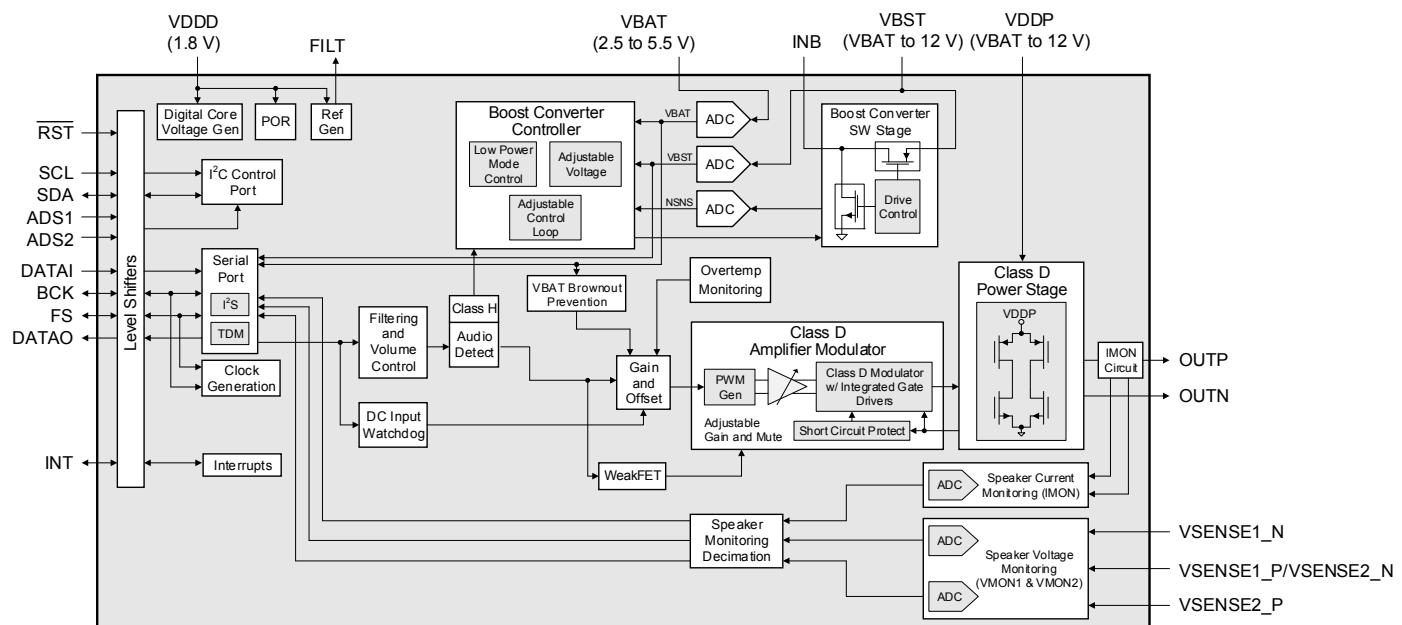
### Protection Features

- VBAT brownout prevention
- IC overtemperature foldback and protection
- Amplifier short-circuit protection
- DC input watchdog

### Clocking Features

- BCK or FS can be used as a reference clock
- No dedicated MCLK required
- Self clocking in low-power boost mode

(Features continue on p. 2)



## Serial Port Audio and Data Features

- Dual-mode serial port (SP)
  - Slave audio clock operation
  - Tightly controlled group delay variation
  - I<sup>2</sup>S and TDM modes
    - Configurable audio/data packet depths and locations
    - Tristateable DATA0 allows sharing of data bus

## System Features

- Wide range of sample rate support
  - 8–48, 88.2, 96, 176.4, 192 kHz
- I<sup>2</sup>C control port
  - Four selectable I<sup>2</sup>C device addresses
- Software reset
- Power up time (from release of RST): 3 ms
- Power down time: 1 ms
- Typical power consumption
  - Device reset: 5.0 µW
  - Idle power with Class H and all monitoring: 6.0 mW

## General Description

The CS35L38A integrates a wide-bandwidth boost converter with a digital-input, closed-loop Class D amplifier and monitoring. For easy system integration, the CS35L38A is highly programmable via the I<sup>2</sup>C control port interface.

The internal Class D amplifier features an advanced, low-noise, closed-loop architecture to provide a high power supply rejection ratio (PSRR) and a complementary output stage. The elevated VBST supply generated by the boost converter allows the CS35L38A to deliver 7.0 W to an 8 Ω speaker at 1% THD+N.

The digitally controlled boost converter boosts standard-voltage lithium-ion and lithium-polymer battery voltages to levels as high as 12 V. Low (idle) power consumption discontinuous conduction and high power delivery continuous conduction mode are available with the digital boost converter. The boost converter's output voltage supply is configurable in 50 mV steps.

The CS35L38A contains multiple integrated and configurable power management options: Class H automatically tracks the incoming audio signal and manages the VBST voltage to maximize power delivery efficiency; amplifier weak-FET drive allows for a reduction of power consumption during idle/low output power conditions.

The CS35L38A monitors several signals via the signal monitoring blocks. There are six monitoring ADCs. Two ADCs are used to monitor supply voltages: VBAT (battery) and VBST. A high-speed ADC is used to monitor the boost converter's inductor current when operating in CCM Mode. A further three ADCs, one monitoring current and two monitoring voltage delivered to the speaker by the amplifier, provide data to an upstream speaker-protection or enhancement algorithm.

Brownout prevention is available on the VBAT supply to allow the user to reduce the amplifier loading in the event of a weakened battery state or a low voltage supply condition. The brownout prevention quickly responds to a drop in the VBAT supply.

The CS35L38A includes a DC input watchdog which protects against corrupt data being sent from the host processor. This prevents a constant DC output being delivered to the speaker, protecting the transducer from damage.

Internal PLL clock generation and source selection allows for a variety of clock rates and configurations via the selectable input clock source.

The CS35L38A is available in a commercial-grade 34-ball WLCSP package for operation from –40°C to +85°C.

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## 1 Pin Assignments and Descriptions

### 1.1 WLCSP (Through-Package View)

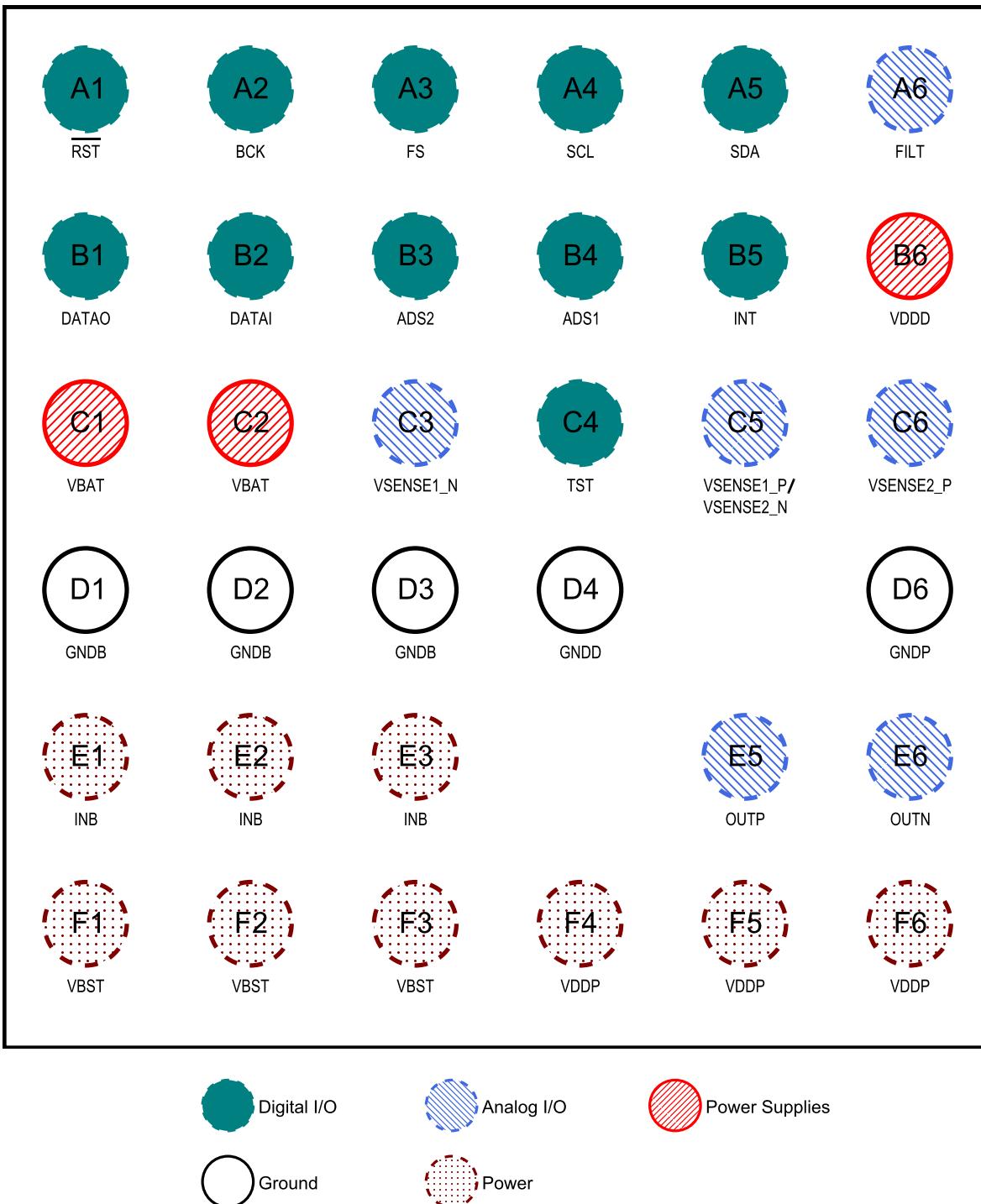


Figure 1-1. WLCSP Ball Assignments (Through-Package View)

## 1.2 WLCSP Pin Descriptions

**Table 1-1. WLCSP Pin Descriptions**

Ball Name	Ball #	Power Supply	I/O	Ball Description	Internal Connection	Digital I/O Driver	Digital I/O Receiver
RST	A1	VDDD	I	<b>Reset.</b> Driving this pin low places the device in hardware reset.	—	—	CMOS, with hysteresis
BCK	A2	VDDD	I/O	<b>Serial Clock.</b> Serial shift clock for the serial audio interface.	Weak pull-down	Tristateable CMOS	CMOS, with hysteresis
FS	A3	VDDD	I/O	<b>Left Right and Frame Sync Clock.</b> In I <sup>2</sup> S Mode, determines which channel, left or right, is active on the serial audio/data lines. In TDM Mode, indicates the start of a TDM frame.	Weak pull-down	Tristateable CMOS	CMOS, with hysteresis
SCL	A4	VDDD	I	<b>Serial Control-Port Clock.</b> Serial clock for the I <sup>2</sup> C serial control port.	—	—	CMOS, with hysteresis
SDA	A5	VDDD	I/O	<b>Serial Control-Port Data.</b> Serial data for the I <sup>2</sup> C serial control port.	—	CMOS/open drain	CMOS, with hysteresis
FILT	A6	VDDD	O	<b>Positive Voltage Reference.</b> Positive reference for the internal circuits.	—	—	—
DATAO	B1	VDDD	O	<b>Serial Audio/Data Output.</b> I <sup>2</sup> S/TDM serial data output used to monitor voltage and current delivered to the load via OUT signal, error volumes, and VBAT and VBST supply voltages.	Weak pull-down	Tristateable CMOS	—
DATAI	B2	VDDD	I	<b>Serial Audio/Data Input.</b> I <sup>2</sup> S/TDM serial audio data input.	Weak pull-down	—	CMOS, with hysteresis
ADS2 ADS1	B3 B4	VDDD	I	<b>Address Select Pins.</b> Selects the I <sup>2</sup> C slave address of the device.	—	—	—
INT	B5	VDDD	O	<b>Interrupt Output.</b> Programmable interrupt output when configured.	—	Tristateable CMOS	CMOS, with hysteresis
VDDD	B6	N/A	I	<b>Analog and Digital Power.</b> Power supply for internal analog and digital sections.	—	—	—
VBAT	C1, C2	N/A	I	<b>Boost Converter Power.</b> Power supply for the boost converter and portions of the Class D amplifier.	—	—	—
VSENSE1_N VSENSE1_P/ VSENSE2_N VSENSE2_P	C3 C5 C6	VDDP	I	<b>Voltage Sense Inputs.</b> Sense voltage for signal originating from OUTP/N	—	—	—
TST	C4	N/A	I	<b>Test Input.</b> Pin may remain floating or may optionally be connected to VBST through a capacitor.	Weak pull-down	—	—
GNDB	D1, D2, D3	N/A	I	<b>Power Ground—Boost.</b> Ground reference for the boost converter.  <b>Note:</b> All ground pins should be connected to the same ground plane as soon as possible.	—	—	—
GNDD	D4	N/A	I	<b>Analog and Digital Ground.</b> Ground reference for the analog and digital portions of the IC.  <b>Note:</b> All ground pins should be connected to the same ground plane as soon as possible.	—	—	—
GNDP	D6	N/A	I	<b>Power Ground—Amplifier.</b> Ground reference for the Class D amplifier's output stage.  <b>Note:</b> All ground pins should be connected to the same ground plane as soon as possible.	—	—	—
INB	E1, E2, E3	VBST	I	<b>Boost Switch.</b> Input to internal boost FETs. Connect to L <sub>BST</sub> inductor.	—	—	—
OUTP OUTN	E5 E6	VDDP	O	<b>Differential Audio Output.</b> Class D amplifier outputs.	—	—	—
VBST	F1, F2, F3	N/A	O	<b>Boosted Supply from Boost Converter.</b> Power supply for the Class D amplifier's output stage produced by the internal boost converter. VBST is connected to the VDDP pins to provide power to the amplifier.	—	—	—

**Table 1-1. WLCSP Pin Descriptions (Cont.)**

<b>Ball Name</b>	<b>Ball #</b>	<b>Power Supply</b>	<b>I/O</b>	<b>Ball Description</b>	<b>Internal Connection</b>	<b>Digital I/O Driver</b>	<b>Digital I/O Receiver</b>
VDDP	F4, F5, F6	N/A	I	<b>Amplifier Power.</b> Power supply for the Class D amplifier's output stage.	—	—	—

**Note:** Digital I/Os without an internal weak pull-down resistor must not be left floating.

### 1.3 Electrostatic Discharge (ESD) Protection Circuitry



ESD-sensitive device. The CS35L38A is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

## 2 Typical Connection Diagrams

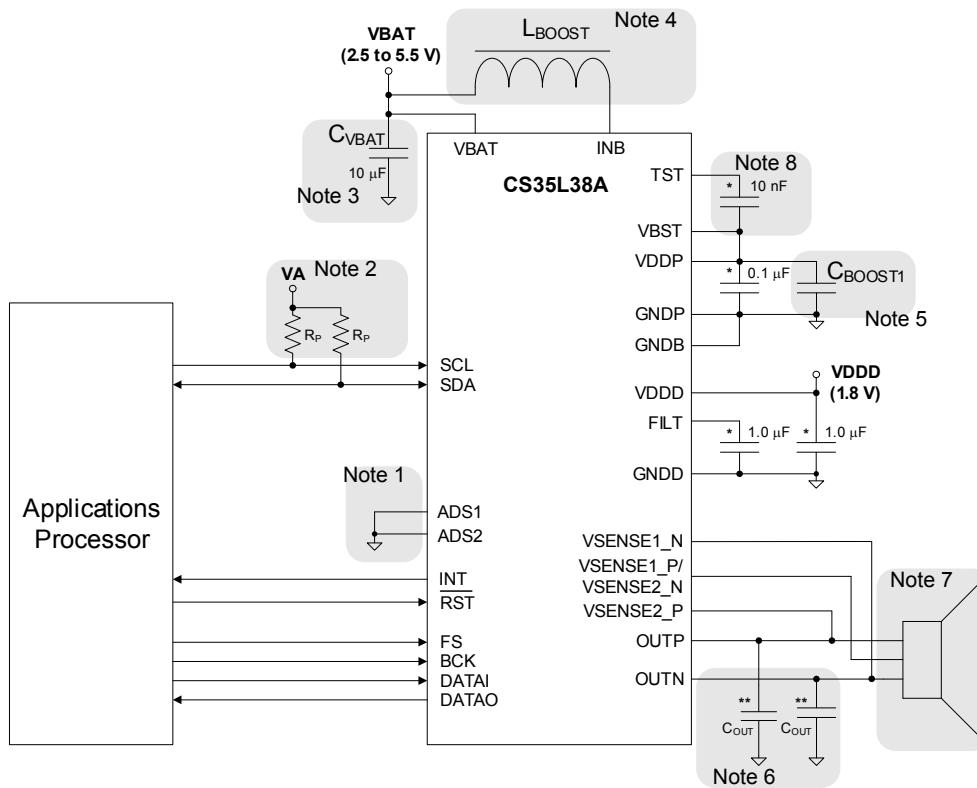


Figure 2-1. Typical Connection Diagram – Connection to 3-Terminal Speaker

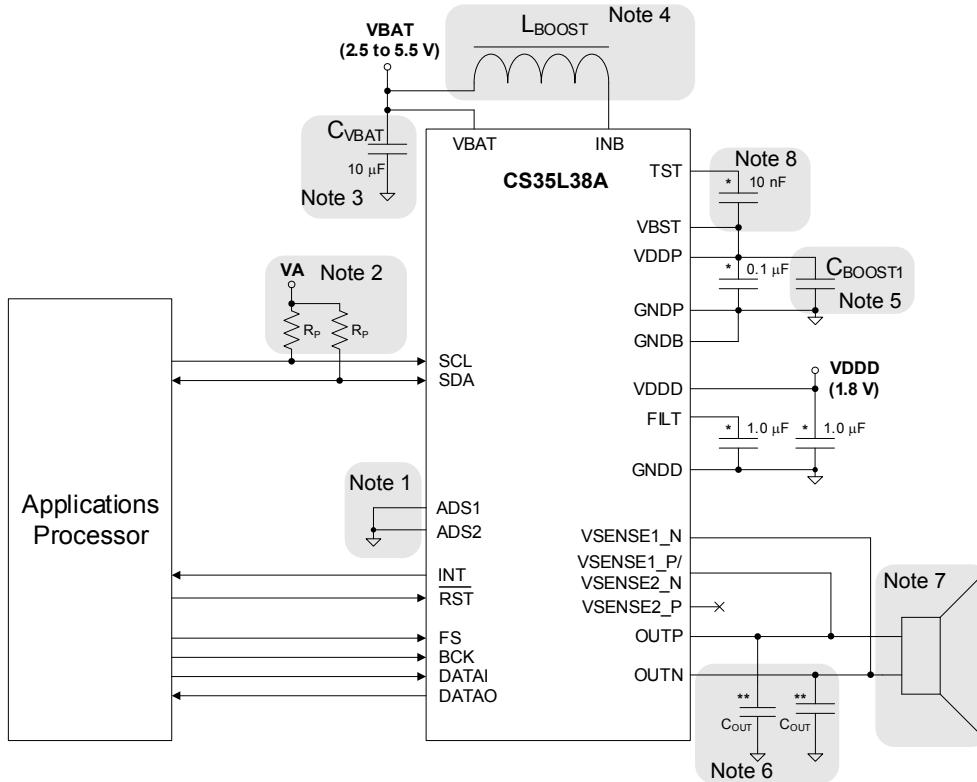


Figure 2-2. Typical Connection Diagram – Connection to 2-Terminal Speaker

**General Notes for Typical Connection Diagrams** (see [Table 2-1](#) for specific notes cross-referenced in the figure):

- [Fig. 2-1](#) is intended to provide a sample of possible connection schemes and does not encompass all variations.
- All external passive component values listed are nominal values.  
Key for capacitor types required:  
 \* Use low ESR, X7R/X5R capacitors.  
 \*\* Use low ESR, X7R/C0G capacitors.
- If no type symbol is shown next to a capacitor, any type may be used.

**Table 2-1. Typical Component Values and Types (Notes for [Fig. 2-1](#))**

Module	Description
Digital Input/ Output	1. This shows one example of how to configure the 7-bit I <sup>2</sup> C address. The I <sup>2</sup> C address is set as 0x50 in this case.
Analog Input	2. Minimum R <sub>P</sub> value is determined from the maximum VA level, the minimum sink current strength of their respective output, and the maximum low-level output voltage (V <sub>OL</sub> ). Maximum R <sub>P</sub> values may be determined by how fast their associated signals must transition, taking into account load capacitance.
Boost Converter	3. Place the 10 $\mu$ F bulk capacitor close to the L <sub>BOOST</sub> inductor. 4. Boost converter L <sub>BOOST</sub> inductor values of 2.2 to 1.0 $\mu$ H are supported for typical use operation. However, the selected L <sub>BOOST</sub> inductor must not derate to a value of less than 0.7 $\mu$ H during normal use to maintain proper loop stability. 5. The boost converter C <sub>BST</sub> capacitors are recommended to have a maximum voltage rating of at least 16 V and must not derate to a combined capacitance value of less than 3.6 $\mu$ F when 12 V <sub>DC</sub> is applied across the capacitors. Note that ceramic capacitors can derate considerably when a DC voltage is applied to them. The total derated C <sub>BST</sub> capacitance at 12 V <sub>DC</sub> must not exceed 58 $\mu$ F with the default BST_K1 and BST_K2 coefficients listed in <a href="#">Table 4-13</a> .
Amplifier	6. The C <sub>OUT</sub> capacitors are optional EMI suppressors that are used depending on the application requirements. It is recommended that the value of these components not exceed 2 nF, as switching losses increase linearly with increases to these capacitances.
Miscellaneous	7. When using a simulated speaker load of 8 $\Omega$ + 33 $\mu$ H, a Coilcraft DO5040H-333MLB inductor is used. 8. Presence of capacitors on these pins impart no functionality during normal operation. They may be omitted and are completely optional.

### 3 Characteristics and Specifications

**Table 3-1** defines in detail general parameters as they are characterized in this section.

**Table 3-1. Parameter Definitions**

Parameter	Definition
Dynamic range	The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a -60 dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Dynamic range is expressed in decibel units.
Frequency response	A measure of the amplitude response variation from 20 Hz to 20 kHz or 20 Hz to 40 kHz relative to the amplitude response at 1 kHz. Frequency response is expressed in dB.
IMD-ITU-R (CCIF)	A measure of the nonharmonic nonlinearities, using two equal amplitude (1:1), closely spaced, high frequency input tones (19 kHz/20 kHz) and looking for beat frequencies. The nonlinearities are found by subtracting the two input tones to find the location (1 kHz).
Output offset voltage	The DC offset voltage present at the amplifier's output when it is receiving muted audio from the source or when its volume is digitally muted.

**Table 3-2. Recommended Operating Conditions**

Test conditions (unless specified otherwise): GNDD = GNDP = 0 V, all voltages with respect to ground. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

**Table 3-1** describes some parameters in detail.

Parameters		Symbol	Minimum	Maximum	Units
DC power supply	Analog (and digital I/O and core) <sup>1</sup>	VDDD	1.66	1.94	V
	Battery <sup>2</sup>	VBAT	2.5	5.5	V
	Internally generated boost	VBST <sub>DC</sub>	VBAT	12.0	V
	Class D amplifier supply	VDDP	VBAT	12.0	V
External voltage applied to analog outputs		V <sub>INA0</sub>	-0.3	VDDP + 0.3	V
External voltage applied to digital inputs <sup>3</sup>		V <sub>INDI</sub>	-0.3	VDDD + 0.3	V
External voltage applied to digital outputs <sup>3</sup>		V <sub>INDO</sub>	-0.3	VDDD + 0.3	V
External voltage applied VSENSE_P/N pins		V <sub>IN-VMON</sub>	-0.3	VDDP + 0.3	V
Ambient temperature		T <sub>A</sub>	-40	+85	°C

1. A valid VBAT voltage must be present whenever a VDDD voltage is applied.

2. Device performance is specified with a VBAT down to 2.8 V. The CS35L38A continues to operate functionally down to 2.5 V, but may not meet all parametric specifications.

3. The maximum over/under voltage is limited by the input current.

**Table 3-3. Absolute Maximum Ratings**

Test conditions (unless specified otherwise): GNDD = GNDP = 0 V; all voltages with respect to ground. **Table 3-1** describes some parameters in detail.

Parameters		Symbol	Minimum	Maximum	Units
DC power supply	Analog	VDDD	-0.3	2.33	V
	Battery	VBAT	-0.3	6.6	V
	Internally-generated boost	VBST	VBAT-0.3	14.4	V
	Class D amplifier supply	VDDP	VBAT-0.3	14.4	V
Input current <sup>1</sup>		I <sub>in</sub>	—	±10	mA
Output load impedance		Z <sub>L</sub>	3.2	—	Ω
Ambient operating temperature (local to device, power applied)		T <sub>A</sub>	-50	+115	°C
Junction operating temperature (power applied)		T <sub>J</sub>	-40	+150	°C
Storage temperature		T <sub>STG</sub>	-65	+150	°C

**Caution:** Stresses beyond "Absolute Maximum Ratings" levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in **Table 3-2**, "Recommended Operating Conditions," is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins do not cause SCR latch up.

**Table 3-4. Class D Amplifier Load-Independent Output Characteristics**

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections to, and passive components used with, the CS35L38A; input test signal is a 24 bit full-scale 997 Hz sine wave with 1 LSB of triangular PDF dither applied; typical/min/max performance data taken with VDDD = 1.8 V, VBAT = 3.6 V T<sub>A</sub> = 25°C; VDDP is automatically adjusted between VBAT and 12.0 V by Class H based on signal level; GNDD = GNDB = GNDP = 0 V; AMP\_GAIN\_PCM = 19 dB; AMP\_VOL\_PCM = 0 dB; AMP\_RAMP\_PCM = 000; measurement bandwidth is 20 Hz to 20 kHz; Fs = 48 kHz; L<sub>BST</sub> = 1.0 μH; f<sub>PLL\_OUT</sub> = 192 MHz. Table 3-1 describes some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters	Symbol	Minimum	Typical	Maximum	Units
Amplifier analog gain	A <sub>V</sub>	-0.2 19.8 0.8	0 20.0 1.0	0.2 20.2 1.2	dB dB dB
Idle channel noise (A-weighted) <sup>1</sup> Dynamic range enhancement disabled Level-dependent muting disabled	ICN <sub>AW</sub>	— — —	9 10 27	— — —	μV <sub>RMS</sub> μV <sub>RMS</sub> μV <sub>RMS</sub>
Output switching frequency <sup>2</sup>	f <sub>AMP_SW</sub>	—	f <sub>MCLK_INT</sub> /28	—	Hz
Output offset voltage	V <sub>AMP_OFFSET</sub>	— — —	— — —	±1.0 ±1.0 ±1.0	mV mV mV
Output full-scale voltage <sup>3</sup> (VDDD = 1.8 V, VDDP = 12.0 V, no load, 0-dBFS input)	V <sub>AMP_FS</sub>	1.31 2.08 9.30 VDDP	1.38 2.19 9.79 VDDP	1.45 2.30 10.28 VDDP	V <sub>PK</sub> V <sub>PK</sub> V <sub>PK</sub> V <sub>PK</sub>
Power-up time – normal <sup>4, 5</sup>	t <sub>AMP_PUP</sub>	—	—	3	ms
Power-up time – fast <sup>4</sup>	t <sub>AMP_PUP_FAST</sub>	—	—	1	ms
Power-down response time <sup>6, 7</sup>	t <sub>AMP_PDN</sub>	—	—	1	ms
Audio group delay—I <sup>2</sup> S/TDM <sup>8</sup>	GD <sub>AMP</sub>	— — —	107 61 39	— — —	μs μs μs
Audio group delay between devices sharing same audio clocks (PCM) <sup>8</sup>	GD <sub>AMP-2-AMP</sub>	—	—	4	μs

1. Specified with an input signal of modulated digital zero and amplifier output nets driven. Typical performance is specified with Class H enabled.

2. Refer to Table 4-26 for a list of f<sub>MCLK\_INT</sub> values.

3. Refer to Table 4-5 for a full list of typical gain output full-scale voltages.

4. Power-up time, t<sub>AMP\_PUP</sub>, is the time required for device outputs to begin switching after the amplifier power-up command (AMP\_EN = 1) is issued.

Typical t<sub>AMP\_PUP</sub> is based on the digital volume soft ramp being disabled (AMP\_RAMP\_PCM = 000) and FILT being discharged. If FILT is charged by setting the FILT\_GLOBAL\_OVR at the time of amplifier power-up, the amplifier power-up time is reduced to t<sub>AMP\_PU\_FAST</sub>.

5. The soft-ramp rate configuration (AMP\_RAMP\_PCM), the digital volume configuration, and the f<sub>PLL\_OUT</sub> frequency affect the amplifier maximum power-up time.

6. Amplifier power-down, t<sub>AMP\_PDN</sub>, is the time required for the switching on the outputs to stop once the power-down command is given by setting AMP\_EN = 0 in the control port. The typical t<sub>AMP\_PDN</sub> time is based on the digital volume soft ramp being disabled (AMP\_RAMP\_PCM = 000).

7. The soft-ramp rate configuration (AMP\_RAMP\_PCM), the digital volume configuration, and the f<sub>PLL\_OUT</sub> frequency affect the amplifier maximum power-down time.

8. Group delay is the time required for the effect of a sample presented at the DATA1 pin for a of the device to appear on the output pins of the amplifier when Class H is disabled. Time is measured from the start of the audio frame containing the data (MSB of the left channel in I<sup>2</sup>S Mode or MSB of slot 0 in TDM Mode) to when it is output via the Class D amplifier.

**Table 3-5. Class D Amplifier Load-Dependent Output Characteristics**

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections to, and passive components used with, the CS35L38A; input test signal is a 24 bit full-scale 997 Hz sine wave with 1 LSB of triangular PDF dither applied; typical/min/max performance data taken with VDDD = 1.8 V, VBAT = 3.6 V, VDDP = VBST = 12.0 V; GNDD = GNDB = GNDP = 0 V; T<sub>A</sub> typ/min/max = 25°C; AMP\_GAIN\_PCM = 19 dB; AMP\_VOL\_PCM = 0 dB; AMP\_RAMP\_PCM = 000; BST\_IPK = BST\_IPKCTL-MAX; measurement bandwidth is 20 Hz–20 kHz AES-17; Fs = 48.0 kHz; L<sub>BST</sub> = 1.0 μH; f<sub>PLL\_OUT</sub> = 192 MHz; simulated speaker load = 8 Ω + 33 μH. Table 3-1 describes some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters	Symbol	Minimum	Typical	Maximum	Units
Power delivered to load VBAT = 3.8 V @ 1% THD+N (continuous average) <sup>1</sup>	P <sub>O@1%</sub>	— —	7.00 1.70	— —	W W
Power delivered to load VBAT = 3.6 V @ 1% THD+N (continuous average) <sup>1</sup>	P <sub>O@1%</sub>	— — —	4.65 4.68 4.65	— — —	W W W
Power delivered to load VBAT = 4.3 V @ 1% THD+N (continuous average) <sup>1</sup>	P <sub>O@1%</sub>	— — —	5.40 5.60 5.60	— — —	W W W

**Table 3-5. Class D Amplifier Load-Dependent Output Characteristics (Cont.)**

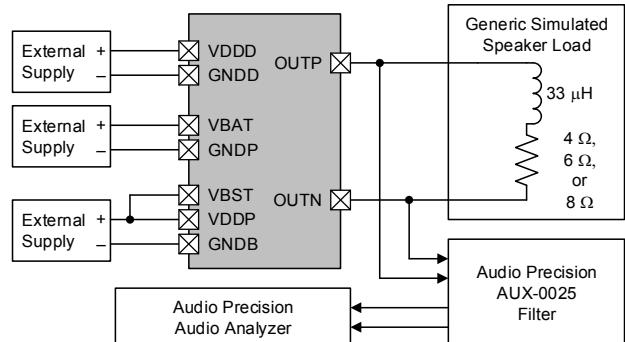
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Parameters	Symbol	Minimum	Typical	Maximum	Units
Power delivered to load VBAT = 3.6 V VDDP = 9.3 V <sub>DC</sub> @ 10% THD+N (continuous average) <sup>1</sup>	PO@10%	—	5.50	—	W
VDDP = 8.2 V <sub>DC</sub>			5.60	—	W
VDDP = 7.0 V <sub>DC</sub>			5.40	—	W
Amplifier operating efficiency VBAT = 3.6 V VDDP = 10.0 V <sub>DC</sub> @ 10% THD+N <sup>2</sup>	ηA	89	90	—	%
VDDP = 8.2 V <sub>DC</sub>		—	88	—	%
VDDP = 7.0 V <sub>DC</sub>		—	87	—	%
Total harmonic distortion + noise PO = 1.0 W	THD+N	—	-80	—	dB
VDDP = 10.0 V <sub>DC</sub>			-78	—	dB
VDDP = 8.2 V <sub>DC</sub>			-77	—	dB
Intermodulation distortion 8 Ω load	IMD	—	—	-88	dB
Power-supply intermodulation distortion 8 Ω load	PSIMD	—	—	-69	dB
Noise injection on VDDP: 217 Hz, 100-mVpp Input signal: 1 kHz, 400 mW				—	dB
Frequency response 8 Ω load	FRAMP	-0.1	0	0.1	dB
20 Hz to 20 kHz 20 Hz to 40 kHz (Fs = 96 kHz)		-0.8	0	0.8	dB
Turn on/off pop/click (A-weighted) <sup>3,4</sup>	CPAMP	—	-66	-64	dBV
8 Ω load			—	-66	dBV
6 Ω load			—	-64	dBV
4 Ω load			—	-64	dBV

1. The amplifier's maximum output power may be limited by the boost converter's maximum load current, I<sub>BST\_OUT\_MAX</sub>; see Table 3-6.

2. Amplifier efficiency specified in this table assumes the amplifier output stage is

powered from an external voltage supply (on VDDP) instead of the onboard boost converter. This encompasses the power consumption of the amplifier from VDDP as well as the overhead of the IC from VDDD and VBAT. See Table 3-9 for the combined efficiency of the entire device, where the amplifier (VDDP) is supplied by the boost converter's output (VBST). Tests for this specification were performed with the generic simulated speaker load shown here:



3. This spec applies to both power up and power down of the device under any condition in which the amplifier is turned on or off via one of the various control port options available, or the output stage switching is halted due to a mute or level-dependent muting, and is applicable for both weak-FET and normal operation modes. When measurement is taken, to best mimic customer use case, VDDP varies between VBAT and 10.0 V as a function of Class H.

4. AMP\_GAIN\_PCM = 0 dB

**Table 3-6. Boost Converter Characteristics**

Test conditions (unless specified otherwise): Fig. 2-1 shows connections to, and passive components used with, the CS35L38A; typical/min/max performance data taken with VDDD = 1.8 V, VBAT = 3.6 V, VDDP = VBST = 12.0 V; GNDD = GNDB = GNDP = 0 V; TA = 25°C; LBST = 1.0 μH; fPLL\_OUT = 192 MHz. Table 3-1 describes some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters	Symbol	Minimum	Typical	Maximum	Units
Boost output voltage <sup>1</sup> VBST_CTL-MIN VBST_CTL-MAX <sup>2</sup> ΔVBST_CTL	VBST	—	VBAT	—	V
			12.0	—	V
			50	—	mV
VBST overvoltage protection <sup>3</sup> VBST_PROT-MIN VBST_PROT-MAX ΔVBST_PROT	VBST_PROT	—	10.0000	—	V
			13.9375	—	V
			62.5	—	mV
High VBST shutdown error threshold <sup>4</sup>	VBST_ERR	13.5	14.5	15.5	V
LBST shorts inductance threshold	L <sub>BST_ERR</sub>	—	—	0.16	μH
Load regulation 2.8 V < VBAT < 5.5 V; 0 A < Load < I <sub>BST_OUT_MAX</sub>	V <sub>BST_LOAD</sub>	—	100	—	mV/A
Line regulation 2.8 V < VBAT < 5.5 V; I <sub>BST_OUT</sub> = 0 A, 500 mA	V <sub>BST_LINE</sub>	—	100	—	mV/V

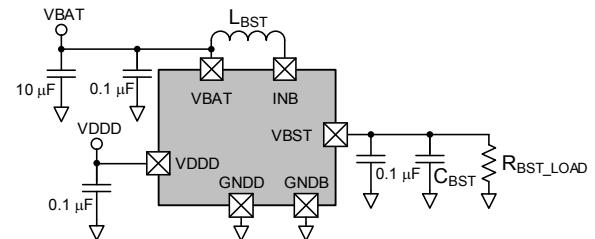
**Table 3-6. Boost Converter Characteristics (Cont.)**

Test conditions (unless specified otherwise): Fig. 2-1 shows connections to, and passive components used with, the CS35L38A; typical/min/max performance data taken with VDDD = 1.8 V, VBAT = 3.6 V, VDDP = VBST = 12.0 V; GNDD = GNDB = GNDP = 0 V; TA = 25°C; L<sub>BST</sub> = 1.0 μH; f<sub>PLL\_OUT</sub> = 192 MHz. Table 3-1 describes some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters	Symbol	Minimum	Typical	Maximum	Units
Boost FET peak-current limit BST_IPK <sub>CTL-MIN</sub> BST_IPK <sub>CTL-MAX</sub> ΔBST_IPK <sub>CTL</sub>	I <sub>BST_L</sub>	—	1.6	—	A
		—	6.5	—	A
		—	100	—	mA
I <sub>BST_L</sub> set-point variation 1.6 < I <sub>BST_L</sub> ≤ 3.0 3.0 < I <sub>BST_L</sub> ≤ 4.5	ΔI <sub>BST_L</sub>	-120 -190	—	120 190	mA
Power-up time <sup>5</sup> From BST_EN = 00 → 10 (GLOBAL_EN = 1) From GLOBAL_EN = 0 → 1 (BST_EN = 10)	t <sub>BST_PUP</sub>	— —	1 3	— —	ms ms
Power-down time <sup>6</sup>	t <sub>BST_PDN</sub>	—	0.5	—	ms
Boost FET ON resistance I <sub>BST_OUT</sub> = 500 mA	R <sub>DSON-B</sub>	—	80	—	mΩ
Rectification FET ON resistance I <sub>BST_OUT</sub> = 500 mA	R <sub>DSON-R</sub>	—	100	—	mΩ
Operating efficiency <sup>7</sup> VBST = 12.0 V; VBAT = 4.3 V; I <sub>BST_OUT</sub> = 500 mA; L <sub>BST</sub> = 1.0 μH	η <sub>B</sub>	—	85	—	%

**CAUTION:** The maximum allowable discharge depth of the batteries specified by the battery manufacturer must not be exceeded.

- The VBST output level is manually configured via BST\_CTL via the control port or automatically via the Class H algorithm. However, if BST\_CTL is configured to generate a VBST output level lower than VBST<sub>MIN</sub>, the VBST level is limited to VBST<sub>MIN</sub>.
- VBST<sub>CTL-MAX</sub> 12 V requires that VBAT > 3 V due to duty cycle limitations.
- This is the VBST voltage in which an additional control loop engages in order to actively restrict peak voltage transients.
- The VBSTERR shutdown voltage is referenced relative to GND and is intended to protect the CS35L38A and external components from being damaged during corner case use conditions.
- t<sub>BST\_PUP</sub> is the time the boost converter takes to reach VBST<sub>MIN</sub> after BST\_EN, BST\_GLOBAL\_OVR, or the GLOBAL\_EN have been programmed to power up the boost converter. This specification is valid for the passive components shown in Fig. 2-1. If the L<sub>BST</sub> or C<sub>BST</sub> value is increased, this value may increase. The f<sub>PLL\_OUT</sub> frequency, BST\_SFT\_RAMP, and external components (L<sub>BST</sub> and C<sub>BST</sub>) can affect boost-converter power-up time or time to a target VBST voltage.
- Power-down time t<sub>BST\_PDN</sub> refers to the time required for the switching on the INB net to stop once the boost converter been transitioned from its powered-up state to a powered-down state via the BST\_EN or GLOBAL\_EN controls.
- Efficiency specified in this table assumes that the boost converter is driving an external resistive load via the VBST pin, instead of the onboard Class D amplifier. Losses from the boost-converter inductor (L<sub>BST</sub>) are included in the calculation and are based on the load described in Note 1 in Table 3-8. R<sub>BST\_LOAD</sub> is selected to produce the specified value of I<sub>OUT(B)</sub>. For the combined efficiency of the entire device, where the boost converter load is provided by the internal Class D amplifier driving a simulated speaker load attached to the OUTP/N nets; see Table 3-9.


**Table 3-7. Device Power Consumption Specifications—Low Power Modes**

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; GND = GNDD = GNDB = GNDP = 0 V; all voltages are with respect to GND; VDDD = 1.8 V, VBAT = VDDP = VBST = 3.60 V; TA typ = 25°C; RST deasserted; PLL\_REFCLK\_EN = 1; control port inactive. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Use Configuration	Typical		
	I <sub>VDDD</sub> (μA)	I <sub>VBAT</sub> (μA)	P <sub>TOTAL</sub> (μW)
RST pin = LOW, VDDD = 0 V	Serial port clocks not active	0	0.55
RSTpin = LOW	Serial port clocks not active	1.7	0.55
	Serial port clocks active 1	1.7	0.55
Power down (GLOBAL_EN = 0, x_GLOBAL_OVR = 0)	Serial port clocks not active	66	8.0
	Serial port clocks active 1	94	8.0
			147
			198

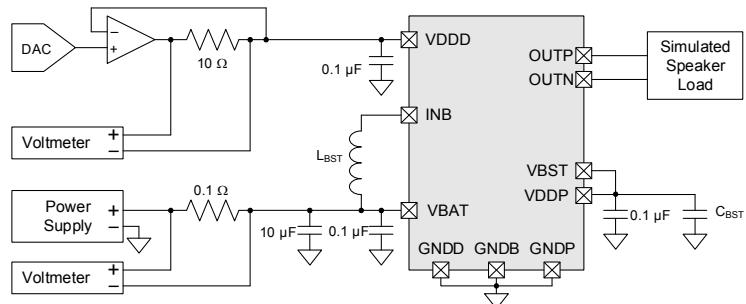
1. BCK = 6 MHz and FS = 48 kHz

**Table 3-8. Idle Channel Device Power Consumption— $L_{BST} = 1.0 \mu\text{H}$  (Simulated Speaker Load)**

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections to, and passive components used with, the CS35L38A; typical/min/max performance data taken with VDDD = 1.8 V, VBAT = 3.6 V, VDDP = VBST; TA typ = 25°C; GNDD = GNDB = GNDP = 0 V; AMP\_GAIN\_PCM = 19 dB; AMP\_VOL\_PCM = 0 dB; AMP\_RAMP\_PCM = 000; Fs = 48 kHz; L<sub>BST</sub> = 1.0 μH; f<sub>PLL\_OUT</sub> = 192 MHz; BST\_DCM\_FREQ = 50 kHz; DATAO\_CLOAD = 20 pF; ASP in TDM Slave Mode (ASP\_FMT = 000) with Fs = 48.0 kHz, BCK = 6 MHz. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Use Configuration 1, 2		Typical			
		I <sub>VDDD</sub> (mA)	I <sub>VBAT</sub> (mA)	I <sub>VDDP</sub> (mA)	P <sub>TOT</sub> (mW)
Boost Only	VBST = VBAT	0.28	0.01	—	0.54
	VBST = 12 V <sup>3</sup>	2.11	0.20	—	4.52
Amp Only Boost in bypass mode	VBST = VDDP = VBAT	4.23	3.34	—	18.20
		2.23	0.02	—	4.86
Amp + Boost + VMON1/2 + IMON+ Class H <sup>4</sup>	VBST = VDDP = VBAT	6.00	3.40	—	23.04
		3.19	0.07	—	5.40

1. Simulated speaker load is a 33 μH inductor in series with an 8-Ω resistor. Specified testing components are as follows:  
 L<sub>BST</sub> (Wurth 74438336010)



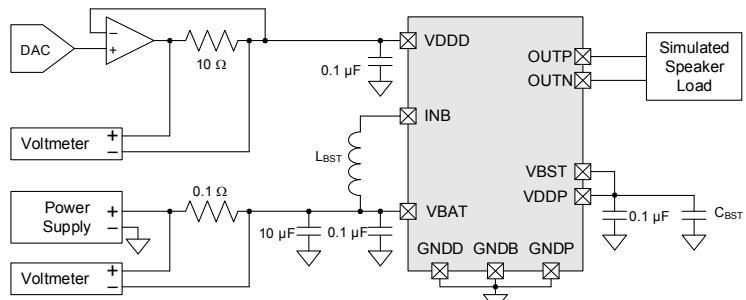
2. Boost converter DCM mode auto detection and amplifier weak-FET automatic detection enabled for all test conditions.  
 3. BST\_CTL = 0x96, BST\_EN = 10, BST\_CTL\_SEL = 0, BST\_AUTO\_DCM\_EN = 1  
 4. When Weak-FET Mode is enabled and level-dependent muting is disabled, Weak-FET Mode is automatically entered during idle to reduce amplifier power consumption

**Table 3-9. Device Efficiency (Simulated Speaker Load)**

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; GND = GNDD = GNDB = GNDP = 0 V; all voltages are with respect to GND; VDDD = 1.8 V, VBAT = 3.6 V; TA = 25°C; RST inactive; f<sub>PLL\_OUT</sub> = 192 MHz; AMP\_GAIN\_PCM = 19 dB; ASP is in Slave Mode with Fs = 48 kHz; input test signal is a 24 bit 997 Hz sine wave with 1 LSB of triangular PDF dither applied. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Use Configuration 1		Minimum	Typical	Maximum	Units
P <sub>OUT</sub> = 500 mW	VBAT = 3.8 V	—	83	—	%
P <sub>OUT</sub> = 1.0 W	VBST = Class H <sup>2</sup>	—	83	—	%
P <sub>OUT</sub> @ 10% THD+N	VBAT = 3.6 V, VBST = VBAT	—	90	—	%
	VBAT = 3.6 V, VBST = VBST <sub>MIN</sub>	—	87	—	%

1. Tests were performed with the simulated speaker load (33 μH in series with an 8-Ω resistor). Specified testing components are as follows:  
 L<sub>BST</sub> (Wurth 74438336010).



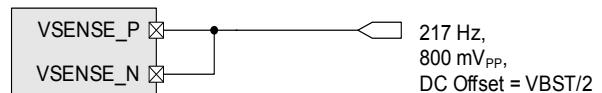
2. Class H is configured as follows: CLASSH\_EN = 1; all other Class H configurations are default.

**Table 3-10. Signal Monitoring Characteristics**

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; inputs to VSENSE\_P/N are 997 Hz sine waves supplied by the CS35L38A's Class D amplifier; GND = GNDD = GNDB = GNPD = 0 V; all voltages are with respect to GND; typical performance data taken with VDDD = 1.8 V, VBAT = 3.6 V, VDDP = VBST = 12.0 V, AMP\_GAIN\_PCM = 19 dB, AMP\_VOL\_PCM = 0 dB; min/max performance data taken with VDDD = 1.8 V, VBAT = 3.6 V, VDDP = VBST = 12.0 V; TA typ/min/max = 25°C; LBST = 1.0  $\mu$ H; fPLL\_OUT = 192 MHz; measurement bandwidth is 20 Hz to 20 kHz; Fs = 48.0 kHz; simulated speaker load = 8  $\Omega$  + 33  $\mu$ H. Table 3-1 defines some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters <sup>1</sup>		Minimum	Typical	Maximum	Units	
Characteristics for all ADCs	Power-up time <sup>2</sup> From GLOBAL_EN = 0 → 1	—	—	3	ms	
	Group delay—VMON1/2, IMON <sup>3</sup> Fs = 48 kHz Fs = 96 kHz Fs = 192 kHz	— — —	103 75 35	— — —	$\mu$ s $\mu$ s $\mu$ s	
VBATMON characteristics	Voltage resolution	—	5.94	—	mV	
	Nominal 3.6 V voltage measurement	3.54	3.60	3.66	V	
	Input voltage for 0-dBFS output	—	6.087	—	V	
VBSTMON characteristics <sup>4</sup>	Voltage resolution	—	13.67	—	mV	
	Nominal 12.0 V voltage measurement	11.76	12.00	12.24	V	
	Input voltage for 0-dBFS output	—	14.00	—	V	
VMON1 and VMON2 characteristics	Dynamic range (unweighted), VSENSE_P/N = $\pm 8.0$ V (16 V <sub>PP</sub> )	74	82	—	dB	
	Total harmonic distortion + noise	8 Vpk	—	-73.5	-67.5	dB
	Nominal 12.0 V voltage measurement	11.76	12.00	12.24	V	
	Analog full-scale input signal capability <sup>5, 6</sup>	—	12.60	—	V	
	Input voltage for 0-dBFS output <sup>7</sup>	—	12.30	—	V	
	Common mode rejection ratio (217 Hz @ 800 mV <sub>PP</sub> ) <sup>8</sup>	50	60	—	dB	
	Single-ended input impedance	—	500	—	k $\Omega$	
	DC offset error	-10	—	10	mV	
IMON characteristics	Dynamic range (unweighted), $\pm 1.0$ A (2 A <sub>PP</sub> )	66	74	—	dB	
	Total harmonic distortion + noise <sup>9</sup>	1 Apk	—	-66	-60	dB
	Nominal 1.00 A current measurement	0.98	1.00	1.02	A	
	Analog full-scale input signal capability <sup>5</sup>	2	—	—	A	
	Input current for 0-dBFS output <sup>7</sup>	—	2.1	—	A	
	DC offset error	-4	0	4	mA	
	Voltage-to-current isolation	—	55	—	dB	
	VMON/IMON gain ratio variance	-0.40	—	0.40	%	

1. Measurements reported in dB are shown relative to the corresponding input voltage or current. Applies to all THD+N and resolution values in the table.
2. The amount of time measured from the completion (or ACK) of the control port write (GLOBAL\_EN = 1) to the time at which the first valid data word is present on the serial port output. GLOBAL\_EN = 0 represents a full power-down, where VDDD is present, and RST is not asserted.
3. xMON group delay is measured from the time a signal is presented on the respective input pins (VBAT, VBST, OUTP, or VSENSE\_P/N) until the start of the frame where the digitized data is output via the serial port. Simulated speaker load equivalent to 8- $\Omega$ .
4. VBST measurements conducted with BST\_EN = 00 and specified voltage range applied to the VBST/VDDP pins.
5. The point at which analog clipping occurs, producing a 3 dB reduction in linearity.
6. This must track the maximum signal swing that the amplifier is capable of reproducing with the maximum effective AMP\_GAIN\_PCM configuration.
7. The full-scale (maximum code) signal refers to the 16 bit or 24 bit scaled xMON D<sub>OUT</sub>. For more information on the D<sub>OUT</sub> to xMON current conversion, refer to Section 4.5.2 and Section 4.5.3.
8. CMRR test setup for VSENSE\_P/N.



9. The total harmonic distortion of IMON is measured using the CS35L38A Class D amplifier as the audio source, which is connected to an 8- $\Omega$  + 33  $\mu$ H speaker load, operating under the typical performance test conditions to produce a large, unclipped audio signal.

**Table 3-11. PSRR Characteristics**

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; GNDD = GNDB = GNDP = 0 V; VDDD = 1.8 V; VBAT = 3.6 V, VDDP = VBST; LBST = 1.0  $\mu$ H; fPLL\_OUT = 192 MHz; unless indicated otherwise, voltages are with respect to ground. TA = 25°C. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters	Noise Injected Into	Noise Measured On	Noise Amplitude (mVpk)	Noise Frequency (Hz)	Minimum	Typical	Maximum	Units
Class D amplifier PSRR AMP_GAIN_PCM = 4 dB	VBAT	OUTP/N	100	217	—	74	—	dB
				1k	—	74	—	dB
				20k	—	50	—	dB
Class D amplifier PSRR AMP_GAIN_PCM = 19 dB	VDDD	OUTP/N	100	217	—	80	—	dB
				1k	—	80	—	dB
				20k	—	60	—	dB
Boost + amplifier PSRR 2 AMP_GAIN_x = 19 dB	VBAT	OUTP/N	100	217	—	74	—	dB
				1k	—	74	—	dB
				20k	—	50	—	dB
VMON1/2 PSRR 3	VDDD	DATAO	100	217	—	45	—	dB
				1k	—	45	—	dB
				20k	—	43	—	dB

1. When the noise source is injected into VDDP, VDDP is driven externally.

2. This test measures PSRR when the boost converter is providing the amplifier with a 12 V supply from VBST to VDDP.

3. To isolate VMON and IMON VDDD PSRR from the audio path while maintaining a connected and sourced operational state, the amplifier signal source is muted (AMP\_MUTE = 1).

**Table 3-12. VBAT Brownout Prevention Monitoring Characteristics**

Test conditions (unless specified otherwise): Fig. 2-1 shows connections to, and passive components used with, the CS35L38A; typical/min/max performance data taken with VDDD = 1.8 V, VBAT = 3.6 V, VDDP = VBST = 12.0 V; GNDD = GNDB = GNDP = 0 V; TA typ/min/max = 25°C; LBST = 1.0  $\mu$ H; fPLL\_OUT = 192 MHz. Table 3-1 describes some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters 1	Symbol	Minimum	Typical	Maximum	Units
Initial VBAT brownout response voltage threshold VBAT <sub>BR1-MIN</sub> VBAT <sub>BR1-MAX</sub> $\Delta$ VBAT <sub>BR1</sub>	VBAT <sub>BR_1</sub>	—	2.497	—	V
		—	3.874	—	V
		—	0.048	—	V
Initial VBAT brownout threshold set point variation	$\Delta$ VBATBR <sub>BR1-VAR</sub>	-60	—	+60	mV
Second VBAT brownout threshold relative to initial threshold	VBAT <sub>BR_1</sub> – VBAT <sub>BR_2</sub>	20	50	80	mV
Third VBAT brownout threshold relative to second threshold	VBAT <sub>BR_2</sub> – VBAT <sub>BR_3</sub>	20	50	80	mV
Initial brownout response time 2	t <sub>VBATBR_INIT</sub>	—	—	10	$\mu$ s
Attenuation release volume step	VOL <sub>VBATBR_REL</sub>	—	0.0625	—	dB
Attenuation attack volume step 3 VBAT <sub>BR_1</sub> triggered VBAT <sub>BR_2</sub> triggered VBAT <sub>BR_3</sub> triggered	VOL <sub>VBATBR_ATK</sub>	0.125	—	1.250	dB
		0.250	—	2.500	dB
		0.500	—	5.000	dB
Maximum volume attenuation limit VBATBR <sub>ATT-LIM-MIN</sub> VBATBR <sub>ATT-LIM-MAX</sub> $\Delta$ VBATBR <sub>ATT-LIM</sub>	VBATBR <sub>ATT-LIM</sub>	—	0	—	dB
		—	15	—	dB
		—	1	—	dB

**Table 3-12. VBAT Brownout Prevention Monitoring Characteristics (Cont.)**

Test conditions (unless specified otherwise): Fig. 2-1 shows connections to, and passive components used with, the CS35L38A; typical/min/max performance data taken with VDDD = 1.8 V, VBAT = 3.6 V, VDDP = VBST = 12.0 V; GNDD = GNDB = GNDP = 0 V; TA typ/min/max = 25°C; LBST = 1.0 µH; fPLL\_OUT = 192 MHz. Table 3-1 describes some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters 1	Symbol	Minimum	Typical	Maximum	Units	
Attenuation attack rate 4	VBATBR_ATK_RATE = 000 VBATBR_ATK_RATE = 001 VBATBR_ATK_RATE = 010 VBATBR_ATK_RATE = 011 VBATBR_ATK_RATE = 100 VBATBR_ATK_RATE = 101 VBATBR_ATK_RATE = 110 VBATBR_ATK_RATE = 111	tVBATBR_ATK	1.5 4 9 24 49 99 249 499	2.5 5 10 25 50 100 250 500	3.5 6 11 26 51 101 251 501	µs/step µs/step µs/step µs/step µs/step µs/step µs/step µs/step
Error cleared wait period 5	VBATBR_WAIT = 00 VBATBR_WAIT = 01 VBATBR_WAIT = 10 VBATBR_WAIT = 11	tVBATBR_WAIT	9 99 249 499	10 100 250 500	11 101 251 501	ms ms ms ms
Attenuation release rate 6	VBATBR_REL_RATE = 000 VBATBR_REL_RATE = 001 VBATBR_REL_RATE = 010 VBATBR_REL_RATE = 011 VBATBR_REL_RATE = 100 VBATBR_REL_RATE = 101 VBATBR_REL_RATE = 110 VBATBR_REL_RATE = 111	tVBATBR_REL	4 9 24 49 99 249 499 999	5 10 25 50 100 250 500 1000	6 11 26 51 101 251 501 1001	ms/step ms/step ms/step ms/step ms/step ms/step ms/step ms/step

1. All timings are referenced with fPLL\_OUT = 192 MHz. When using a fPLL\_OUT other than 192 MHz, all timings scale by 192 MHz/fPLL\_OUT.

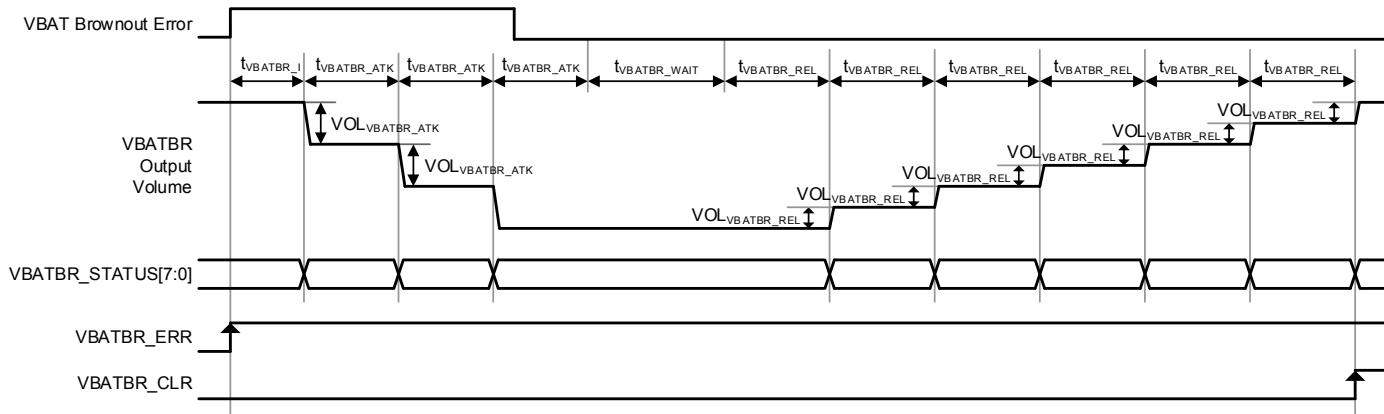
2. tVBATBR\_INIT is the time required for the system to detect the initial VBAT brownout condition, modify the device's operational state, and allow for the initial change in attenuation propagate through the amplifier.

3. The attenuation volume step varies based on the current VBAT voltage threshold range. The specified minimum/maximum range is based on the available user configurations. For more information on the multiple VBAT voltage thresholds, refer to Section 4.6.2.

4. tVBATBR\_ATK is the time required to attenuate an additional volume adjustment step after the initial response a prior attacking state has been implemented.

5. tVBATBR\_WAIT is the time the VBAT brownout prevention state machine waits after an error condition has cleared before proceeding to a release state.

6. tVBATBR\_REL is the time required to release a volume attenuation adjustment after the wait period has cleared or between consecutive gain attenuation release adjustments.


**Figure 3-1. VBATBR Error, Volume Attenuation, Status Reporting, and Interrupts**
**Table 3-13. Device Temperature Monitoring and Protection Characteristics**

Test conditions (unless specified otherwise): Fig. 2-1 shows connections to, and passive components used with, the CS35L38A; typical/min/max performance data taken with VDDD = 1.8 V, VBAT = 3.6 V, VDDP = VBST = 12.0 V; GNDD = GNDB = GNDP = 0 V; TA typ/min/max = 25°C. Table 3-1 describes some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters	Minimum	Typical	Maximum	Units	
Overtemperature warning threshold	AMP_OTW_THLD = 00 AMP_OTW_THLD = 01 AMP_OTW_THLD = 10 AMP_OTW_THLD = 11	— — — —	105 115 125 135	— — — —	°C
Overtemperature error threshold 1	—	150	—	—	°C

1. The same internal temperature-measuring circuitry is used to create both the overtemperature warning and error signals. Overtemperature warning/error threshold deviation is applied equally to both thresholds, which results in the individual thresholds being inaccurate to the same degree and of the same polarity as all other values. For example, if the overtemperature warning threshold is 10°C below the AMP\_OTW\_THLD setting, the overtemperature error threshold is also 10°C below its specified threshold.

**Table 3-14. Digital Interface Specifications and Characteristics**

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; VDDD = 1.8 V, VBAT = 3.6 V, VBST = 12 V; GNDD = GNDB = GNDP = 0 V; TA typ/min/max = 25°C. Table 3-1 describes some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters		Symbol	Minimum	Maximum	Units
Digital I/O hysteresis		—	75	—	mV
Input leakage current (per pin) <sup>1,2</sup>	BCK, FS, DATAI, DATAO All other digital pins	I <sub>IN</sub>	— —	±4000 ±100	nA nA
Internal weak pull-down	BCK, FS, DATAI, DATAO	—	550	2450	kΩ
Input capacitance (per pin)		—	—	10	pF
SDA pull-up resistance <sup>3</sup>	R <sub>P</sub>	500	—	—	Ω
VDDD logic input: RST	High-level input voltage	V <sub>IH</sub>	1.20	—	V
	Low-level input voltage	V <sub>IL</sub>	—	0.40	V
VDDD logic I/Os	High-level output voltage	I <sub>OH</sub> = -100 μA	V <sub>OH</sub>	VDDD-0.2	—
	Low-level output voltage	All outputs, I <sub>OL</sub> = 100 μA SDA, I <sub>OL</sub> as per R <sub>P(min)</sub> <sup>3</sup>	V <sub>OL</sub>	— —	0.20 0.20•VDDD
	High-level input voltage	V <sub>IH</sub>	0.70•VDDD	—	V
	Low-level input voltage	V <sub>IL</sub>	—	0.30•VDDD	V

1. Specification includes current through internal pull up/down resistors, where applicable (as defined in Section 1).

2. Leakage current is measured with VDDD = 1.80 V, VBAT = 3.60 V, VBST = 3.60 V, and RST asserted. Each pin is tested while being driven high and low.

3. Minimum R<sub>P</sub> values (shown in Fig. 2-1 and specified in Table 3-14) are determined from the maximum VDDD level, the minimum sink current strength of their respective output, and the maximum low-level output voltage (V<sub>OL</sub>). Maximum R<sub>P</sub> values may be determined by how fast their associated signals must transition (e.g., the lower the R<sub>P</sub> value, the faster the I<sup>2</sup>C bus can operate for a given bus load capacitance).

**Table 3-15. DC Characteristics**

Test conditions (unless specified otherwise): Fig. 2-1 shows connections to, and passive components used with, the CS35L38A; typical/min/max performance data taken with VDDD = 1.8 V, VBAT = 3.6 V, VDDP = VBST = 12.0 V; GNDD = GNDB = GNDP = 0 V; TA typ/min/max = 25°C. Table 3-1 describes some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

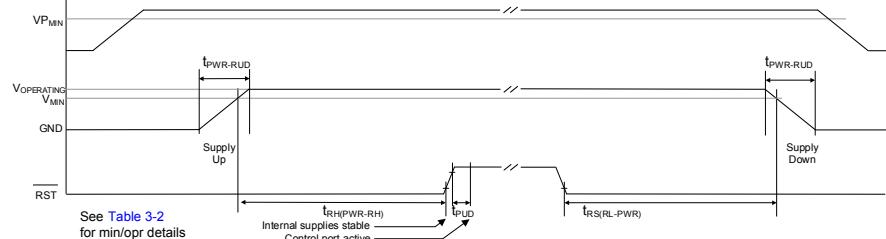
Parameters		Minimum	Typical	Maximum	Units
FILT voltage	DISCHG_FILT = 0	—	1.45	—	V
VDDD power-on reset (POR) threshold (V <sub>POR</sub> )	Up Down	— —	1.2 0.9	— —	V

**Table 3-16. Switching Specifications—Power, Reset, Master Clock References**

Test conditions (unless specified otherwise): Fig. 2-1 shows connections to, and passive components used with, the CS35L38A; typical/min/max performance data taken with VDDD = 1.8 V, VBAT = 3.6 V, VDDP = VBST = 12.0 V; GNDD = GNDB = GNDP = 0 V; TA typ/min/max = 25°C. Table 3-1 describes some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters 1		Symbol	Minimum	Typical	Maximum	Units
Reset <sup>2</sup>	RST low (logic 0) pulse width	t <sub>RLPW</sub>	1	—	—	ms
Power supplies <sup>2</sup>	Power-supply ramp up/down	t <sub>PWR-RUD</sub>	—	—	100	ms
Digital PLL – REFCLK input	Nominal REFCLK input reference frequency <sup>3</sup>	BCK FS <sup>4</sup>	f <sub>BCK</sub> f <sub>FS</sub>	0.128 8.0	— —	24.576 192.0
	REFCLK input phase jitter (100 Hz to REFCLK/2)	j <sub>REFCLK-PH</sub>	—	—	300	psRMS
	REFCLK input source duty cycle	D <sub>REFCLK</sub>	45	—	55	%

1. Power and reset sequencing



2. See Section 5.1 for example power-up and power-down sequences.

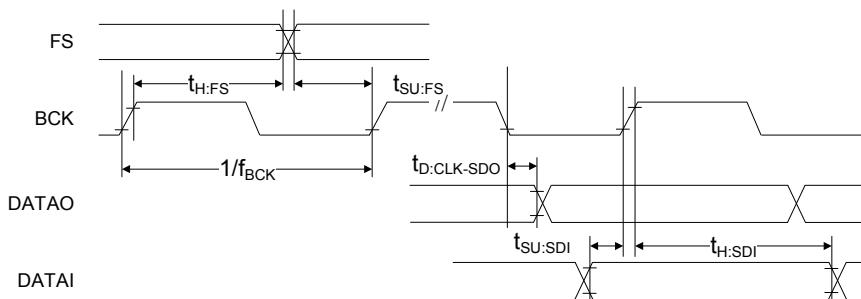
3. Input reference clocks slower than 1 MHz are supported as an input reference clock, but may produce a reduced amplifier and monitoring performance and may vary based on the performance of the slower reference clock.  
 4. FS duty cycle must comply with DREFCLK requirement.

**Table 3-17. Switching Specifications—Audio Serial Port (ASP)**

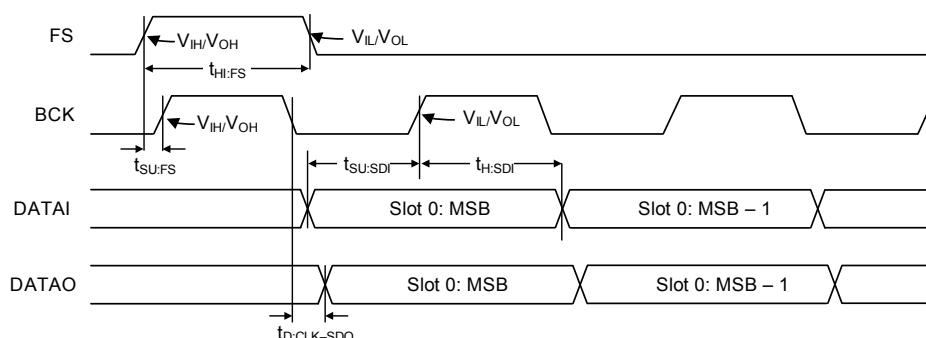
Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; Inputs: Logic 0 = GNDD = GNDB = GNDP = 0 V, VDDD = 1.8 V, VBAT = 3.6 V, VBST = 12.0 V, Logic 1 = VDDD; DATAO C<sub>LOAD</sub> = 20 pF; output timings are measured at V<sub>OL</sub> and V<sub>OH</sub> thresholds for VDDD logic (as specified in Table 3-14); T<sub>A</sub> typ/min/max = 25°C. Table 3-1 describes some parameters in detail. Specifications are valid following the completion of the device initialization sequence defined in Section 4.1.3.

Parameters 1,2,3,4		Symbol	Minimum	Maximum	Units
Slave Mode	Nominal FS input sample/frame rate <sup>5</sup>	Fs	8	192	kHz
	FS duty cycle	I <sup>2</sup> S D <sub>FS</sub>	45	55	%
	FS high period <sup>6</sup>	TDM t <sub>H:FS</sub>	1/f <sub>BCK</sub>	(n-1)/f <sub>BCK</sub>	s
	BCK frequency	f <sub>BCK</sub>	16•Fs	24.576	MHz
	BCK duty cycle	D <sub>BCK</sub>	45	55	%
	FS setup time before BCK latching edge	t <sub>SU:FS</sub>	10	—	ns
	FS hold time after BCK launching edge	I <sup>2</sup> S t <sub>H:FS</sub>	5	—	ns
	DATAI setup time before BCK latching edge	t <sub>SU:SDI</sub>	10	—	ns
	DATAI hold time after BCK latching	t <sub>H:SDI</sub>	5	—	ns
	DATAO delay time after BCK launching edge	t <sub>D:CLK-SDO</sub>	—	15	ns
	DATAO Hi-Z delay time after BCK latching edge	t <sub>DLY:HIZ</sub>	3	20	ns

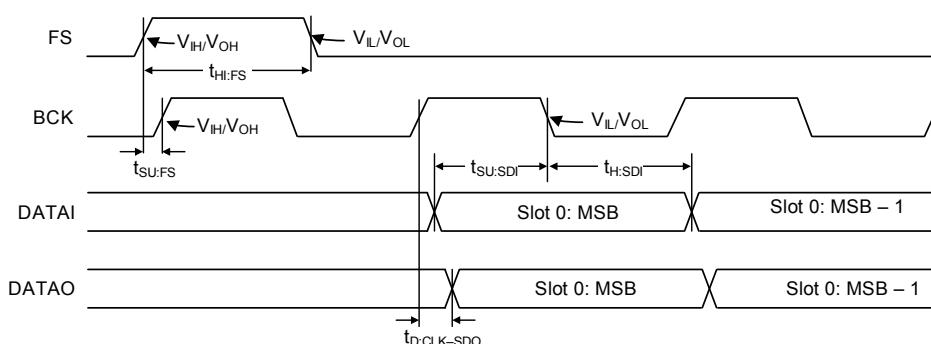
1. ASP timing in I<sup>2</sup>S Mode  
 (ASP\_FMT = 010)



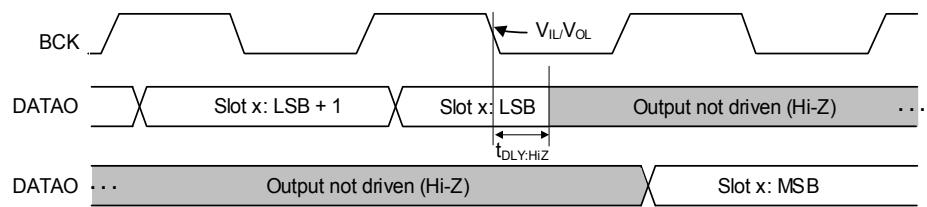
2. ASP timing in TDM 1 Mode  
 (ASP\_FMT = 000) (see Section 4.11.1.3)



3. ASP timing in TDM 1.5 Mode  
 (ASP\_FMT = 100) (see Section 4.11.1.3)



4. ASP DATA0 hand-off timing for sharing the audio serial port bus



5. Sample rates available are based on a combination of the REFCLK frequency provided and the  $f_{PLL\_OUT}$  frequency. The REFCLK to  $f_{PLL\_OUT}$  relationship is shown in [Table 4-25](#) in [Section 4.9.1.5](#), and the available sample rates for each  $f_{PLL\_OUT}$  are shown in [Table 4-26](#) in [Section 4.9.2.1](#).  
6. "n" refers to the total number of BCKs in a given FS frame.

**Table 3-18. Switching Specifications—I<sup>2</sup>C Control Port**

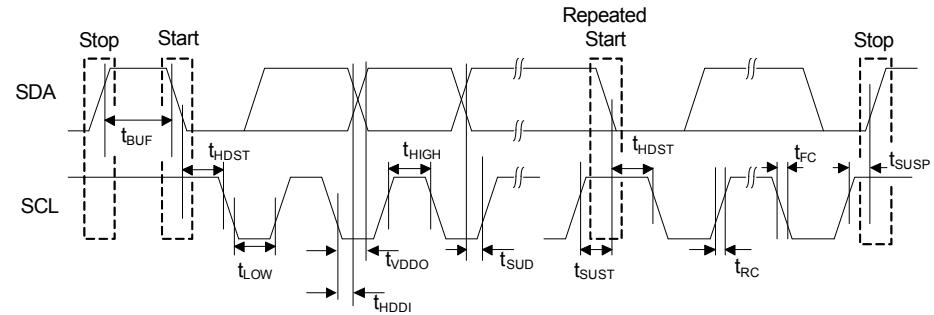
Test conditions (unless specified otherwise): [Fig. 2-1](#) shows typical connections; GND = GNDD = GNDB = GNDP = 0 V; all voltages with respect to GND; VDDD = 1.8 V; inputs: Logic 0 = GNDD = 0 V, Logic 1 = VDDD;  $T_A$  typ/min/max = 25°C; SDA load capacitance equal to maximum value of  $C_B$  = 400 pF; minimum SDA pull-up resistance,  $R_P(\min)$ .<sup>1</sup> [Table 3-1](#) describes some parameters in detail. All specifications are valid for the signals at the pins of the CS35L38A with the specified load capacitance. Specifications are valid following the completion of the device initialization sequence defined in [Section 4.1.3](#).

Parameter 2	Symbol 3	Minimum	Maximum	Units
SCL clock frequency	$f_{SCL}$	—	1000	kHz
Clock low time	$t_{LOW}$	500	—	ns
Clock high time	$t_{HIGH}$	260	—	ns
Start condition hold time (before first clock pulse)	$t_{HDST}$	260	—	ns
Setup time for repeated start	$t_{SUST}$	260	—	ns
Rise time of SCL and SDA	$t_{RC}$	—	1000 300 120	ns ns ns
Fall time of SCL and SDA	$t_{FC}$	—	300 300 120	ns ns ns
Setup time for stop condition	$t_{SUSP}$	260	—	ns
SDA setup time to SCL rising	$t_{SUD}$	50	—	ns
SDA input hold time from SCL falling <sup>4</sup>	$t_{HDDI}$	0	—	ns
Output data valid (Data/Ack) <sup>5</sup>	$t_{VDDO}$	—	3450 900 450	ns ns ns
Bus free time between transmissions	$t_{BUF}$	500	—	ns
SDA bus capacitance	$C_B$	—	400	pF
SCL/SDA pull-up resistance <sup>1</sup>	$R_P$	500	—	Ω
Pulse width of spikes to be suppressed	$t_{ps}$	0	50	ns
Power-up delay (Delay before I <sup>2</sup> C can communicate after POR or RST deassertion)	$t_{PUD}$	—	500	μs

1. The minimum  $R_P$  value (resistor shown in [Fig. 2-1](#)) is determined by using the maximum level of VDDD, the minimum sink current strength of its respective output, and the maximum low-level output voltage  $V_{OL}$ . The maximum  $R_P$  value may be determined by how fast its associated signal must transition (e.g., the lower the value of  $R_P$ , the faster the I<sup>2</sup>C bus is able to operate for a given bus load capacitance). See I<sup>2</sup>C bus specification referenced in [Section 12](#).

2. All timing is relative to thresholds specified in [Table 3-14](#),  $V_{IL}$  and  $V_{IH}$  for input signals, and  $V_{OL}$  and  $V_{OH}$  for output signals.

3. I<sup>2</sup>C control-port timing.



4. Data must be held long enough to bridge the transition time,  $t_{FC}$ , of SCL.

5. Time from falling edge of SCL until data output is valid.

## 4 Functional Description

The functional descriptions of the CS35L38A blocks are listed

- Operational State Control ([Section 4.1](#))
- Class D Amplifier ([Section 4.2](#))
- Digital Boost Converter ([Section 4.3](#))
- Device Power Management ([Section 4.4](#))
  - Class H Tracking ([Section 4.4.1](#))
  - Weak-FET Amplifier Drive Strength Control ([Section 4.4.2](#))
  - Device Level-dependent Muting ([Section 4.4.3](#))
- Signal Monitoring ([Section 4.5](#))
- VBAT Brownout Prevention ([Section 4.6](#))
- Device- and System-Level Error Protection ([Section 4.7](#))
  - Amplifier DC Input Watchdog Protection ([Section 4.7.1](#))
  - Die Temperature Monitoring ([Section 4.7.2](#))
- Dynamic Range Enhancement (DRE) ([Section 4.8](#))
- Device Clocking and Reference Clock Configurations ([Section 4.9](#))
- PCM Audio and Monitoring Data Packets and Routing ([Section 4.10](#))
- Audio Serial Port Data Interface ([Section 4.11](#))
- Interrupt Reporting ([Section 4.12](#))
- I2C Control Port ([Section 4.13](#))

### 4.1 Operational State Control

The CS35L38A offers a flexible array of controls that can manipulate the device's operational state. Each control is described in the sections that follow.

#### 4.1.1 Hardware Reset

Asserting the  $\overline{\text{RST}}$  input places the device in a hardware reset state. Holding the device in hardware reset returns all internal state machines to their initial states and halts all functionality entirely. The control port remains inaccessible through I<sup>2</sup>C during the hardware reset state, which represents the lowest possible power consumption condition.

Deasserting the  $\overline{\text{RST}}$  input promotes the CS35L38A to a low-power standby state. After exiting hardware reset, the device resolves the AD[1:0] fields of the I<sup>2</sup>C slave address based on ADS1 and ADS2. Each address is determined by the connection of ADS2 and ADS1 according to [Table 4-1](#).

**Table 4-1. ADS1/ADS2 Decode**

ADS2 Connection	ADS1 Connection	AD1	AD0
GNDD	GNDD	0	0
GNDD	VDDD	0	1
VDDD	GNDD	1	0
VDDD	VDDD	1	1

The usage of the AD[1:0] fields as they apply to the I<sup>2</sup>C slave address is further detailed in [Section 4.13.1](#).

#### 4.1.2 Momentary Reset

The applications processor can issue a momentary reset by way of register control. These reset sources do not force the device to revisit the state of the ADS1 and ADS2 pins.

- **Control-Port Soft Reset**—resets all registers. This momentary reset is triggered by writing a specific value to the [SFT\\_RST\\_DEVID1](#) control (see p. 88). After a control-port soft reset is issued, the device initialization sequence defined in [Section 4.1.3](#) must be performed immediately following the power-up delay specified in [Table 3-17](#).

### 4.1.3 Device Initialization Sequence

The register addresses in the following sequence must be written in the order shown following the deassertion of the RST input or the completion of a control-port soft reset, described in [Section 4.1.1](#) and [Section 4.1.2](#) respectively. In both cases, the power-up delay specified in [Table 3-17](#) must be observed.

After reset, the user is required to perform chip initialization before any other operation. The user should perform this process every time after performing a hard or soft reset. This can be performed through the I<sup>2</sup>C interface.

Step	Action	I <sup>2</sup> C Address	Data
1	Poll until data equals:	0x000002030	Bit[7] = b1
2	Poll until data equals:	0x000000510	Bit[25] = b1
3	Write:	0x000000020	0x00005555
4	Write:	0x000000020	0x0000AAAA
5	Write:	0x00D0004C	0x00FEFFFF
6	Write:	0x00002400	0x00000039
7	Write:	0x00000C00	0x00000000
8	Write:	0x00000C08	0x00000001
9	Write:	0x00E02800	0x00DD0102
10	Write:	0x00000C08	0x00000000
11	Write:	0x00000C00	0x00000001
12	Wait until the INT pin (configured as the interrupt) is set to logic low.		
13	Write:	0x00D0004C	0x00FFFFFF
14	Read 1:	0x00002828	Bit[2] = b0 Bit[1] = b1 Bit[0] = b1
15	Write:	0x00D0000C	0x00010000
16	Write:	0x00002400	0x00000038
17	Write:	0x00000C00	0x00000000
18	Write:	0x00000020	0x0000CCCC
19	Write:	0x00000020	0x00003333

1. If data differs from the listed bit sequence, the device has not initialized successfully and must not be enabled (GLOBAL\_EN = 1).

### 4.1.4 Global Enable, Functional Block Enables

Clearing the [GLOBAL\\_EN](#) control (see p. 88) places the CS35L38A in a low-power standby state by collectively disabling all functional blocks throughout the device with the exception of the I<sup>2</sup>C control port (if selected as described in [Section 4.1.1](#)).

All other functional blocks are equipped with their own enable control, which can be freely set or cleared during standby. The device is rendered operational by setting GLOBAL\_EN, at which time any functional blocks that were armed in standby are powered up.

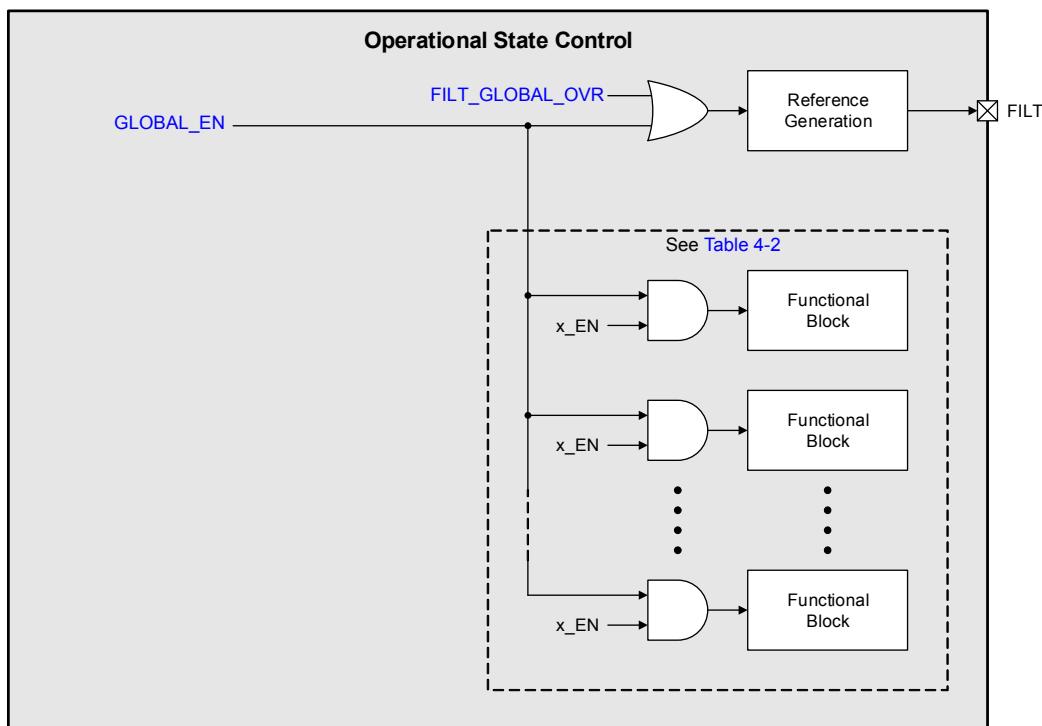
Each defeatable functional block and its associated override control are shown in [Table 4-2](#). Functional blocks advertised as having an override control can remain enabled during standby. If a functional block's override control is set, its corresponding enable control is not gated by GLOBAL\_EN.

**Table 4-2. Functional Block Enable and Override Controls**

Functional Block		Enable Control	Override Control	Reference
Playback	Class D Amplifier and Modulator	<a href="#">AMP_EN</a>	—	<a href="#">Section 4.2</a>
	Dynamic Range Enhancement	<a href="#">AMP_DRE_EN</a>	—	<a href="#">Section 4.8</a>
Power Delivery	Digital Boost Converter	<a href="#">BST_EN</a>	<a href="#">BST_GLOBAL_OVR</a>	<a href="#">Section 4.3</a>
Device Power Management	Class H Tracking	<a href="#">CLASSH_EN</a>	—	<a href="#">Section 4.4.1</a>
	Weak-FET Control	<a href="#">WKFET_AMP_EN</a>	—	<a href="#">Section 4.4.2</a>

**Table 4-2. Functional Block Enable and Override Controls**

Functional Block		Enable Control	Override Control	Reference
Monitoring	Voltage Monitoring (VMON1)	VMON_EN	—	Section 4.5
	Voltage Monitoring (VMON2)	VMON_EN	—	
	Current Monitoring	IMON_EN	—	
	VBAT Monitoring	VBATMON_EN	—	
	VBST Monitoring	VBSTMON_EN	—	
Protection	VBAT Brownout Prevention	VBATBR_EN	—	Section 4.6 Section 4.7.1 Section 4.7.2
	DC Input Watchdog	DCIN_WD_EN	—	
	Die Temperature Monitoring	TEMPMON_EN	TEMPMON_GLOBAL_OVR	
Communication and Control	Audio Serial Port Receiver CH1	ASP_RX1_EN	—	Section 4.11
	Audio Serial Port Transmitter CH1	ASP_TX1_EN	—	
	Audio Serial Port Transmitter CH2	ASP_TX2_EN	—	
	Audio Serial Port Transmitter CH3	ASP_TX3_EN	—	
	Audio Serial Port Transmitter CH4	ASP_TX4_EN	—	
	Audio Serial Port Transmitter CH5	ASP_TX5_EN	—	
	Audio Serial Port Transmitter CH6	ASP_TX6_EN	—	


**Figure 4-1. Operational State Control Logic**

#### 4.1.4.1 Changing Global Enable

Clearing and setting GLOBAL\_EN must be performed in a prescribed manner. Depending on the system and device configuration, use one of three methods.

1. If interrupts from the device are processed by an external Application Processor:
  - The device can be placed into low-power standby state by performing the following register writes.

Register	Address	Value
GLOBAL_ENABLES	0x0000_2014	0x0000_0000
N/A	N/A	Wait for: GLOBAL_PDN_DONE_EINT == 1
—	0x0000_5C00	0x0000_0000
INT_EINT_4	0x00D0_000C	Reset: GLOBAL_PDN_DONE_EINT == 0

- The device can be placed in active state by performing the following register writes.

Register	Address	Value
—	0x0000_5C00	0x0000_8000
GLOBAL_ENABLES	0x0000_2014	0x0000_0001

2. If interrupts from the device are not processed, and the device digital volume soft-ramp AMP\_RAMP\_PCM is disabled (device default):
  - The device can be placed into low-power standby state by performing the following register writes.

Register	Address	Value
GLOBAL_ENABLES	0x0000_2014	0x0000_0000
—	0x0000_5C00	0x0000_0000
Do not change device state to active for at least 1.0ms.		

- After the device has been in low-power standby state for at least 1.0ms, it can be placed in active state by performing the following register writes.

Register	Address	Value
—	0x0000_5C00	0x0000_8000
GLOBAL_ENABLES	0x0000_2014	0x0000_0001

3. If interrupts from the device are not processed, and the device digital volume soft-ramp AMP\_RAMP\_PCM is enabled:
  - The device can be placed into low-power standby state by performing the following register writes.

Register	Address	Value
GLOBAL_ENABLES	0x0000_2014	0x0000_0000
—	—	WAIT x ms based on AMP_RAMP_PCM. <sup>1</sup>
—	0x0000_5C00	0x0000_0000

<sup>1</sup>.Depending on the value of AMP\_RAMP\_PCM, the above wait time must be at least the time indicated in [Table 4-3](#).

**Table 4-3. Delay Values**

AMP_RAMP_PCM Value (binary)	Delay Before State Change (ms)
001	12
010	25
011	50
100	90
101	200
110	350
111	750

- The device can be placed in active state by performing the following register writes.

Register	Address	Value
—	0x0000_5C00	0x0000_8000
GLOBAL_ENABLES	0x0000_2014	0x0000_0001

#### 4.1.5 Reference Generation Precharge

The CS35L38A generates a voltage reference used by the playback path and exposes that reference to the FILT pin, which must be decoupled to ground with a 1.0- $\mu$ F capacitor. When GLOBAL\_EN is changed from zero to one, the reference is enabled and the FILT capacitor begins to charge—the delay of which directly impacts amplifier power-up time. Once GLOBAL\_EN is cleared again, the reference is disabled and the FILT capacitor gradually discharges.

Alternatively, the FILT reference can be maintained while GLOBAL\_EN = 0 if the FILT\_GLOBAL\_OVR control (see p. 90) is set. Holding the FILT reference while the device rests in standby can expedite subsequent amplifier power-up cycles at the expense of added standby power consumption. If FILT\_GLOBAL\_OVR = AMP\_EN = 1 while GLOBAL\_EN = 0, amplifier power-up time is reduced from  $t_{AMP\_PUP}$  to  $t_{AMP\_PUP\_FAST}$  (both specified in Table 3-4) during subsequent assertions of GLOBAL\_EN.

#### 4.1.6 Interrupt Status Fields

Table 4-4 describes the interrupt status fields associated with the operational state of the CS35L38A.

**Table 4-4. Operational State Interrupt Status Fields**

Raw Status Flag	Cause	Rising-Edge Flag	Interrupt Mask
GLOBAL_EN_ASSERT_STS	A power-up request was initiated by the device's own GLOBAL_EN control.	GLOBAL_EN_ASSERT_EINT	GLOBAL_EN_ASSERT_MASK
GLOBAL_PUP_DONE_STS	All enabled functional blocks have been rendered operational following the assertion of GLOBAL_EN.	GLOBAL_PUP_DONE_EINT	GLOBAL_PUP_DONE_MASK
GLOBAL_PDN_DONE_STS	All functional blocks have been disabled and the device rests in standby.	GLOBAL_PDN_DONE_EINT	GLOBAL_PDN_DONE_MASK

## 4.2 Class D Amplifier

The CS35L38A comprises a high-performance digital PWM generator feeding into a closed-loop Class D modulator. The amplifier receives digital audio via the Serial Port input which supports a wide range of PCM audio sample rates (see [Section 4.9.2](#)). The amplifier's audio path includes a fully functional volume control and wide range of analog gains to support various use cases.

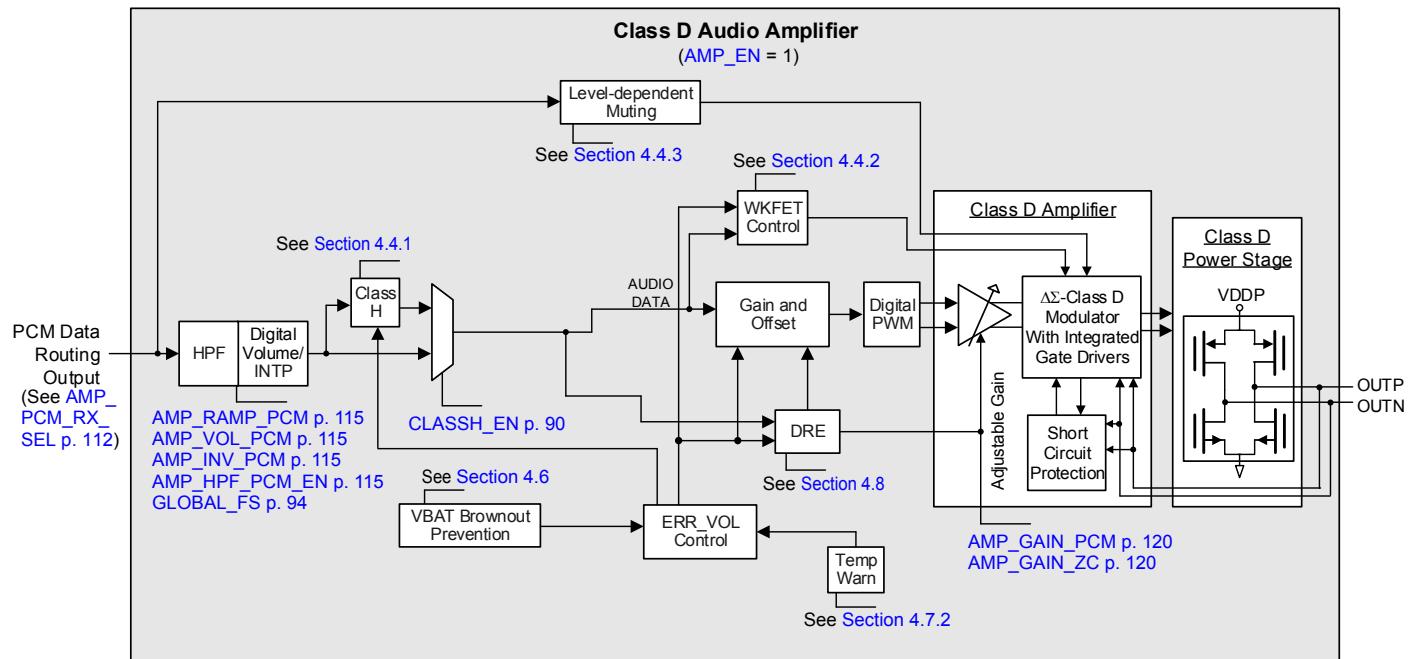


Figure 4-2. Class D Audio Amplifier Block Diagram

### 4.2.1 Power-Up and Power-Down Bits (AMP\_EN)

Power control of the Class D amplifier is provided via [AMP\\_EN](#) (see [p. 89](#)).

### 4.2.2 PCM Volume Control (AMP\_VOL\_PCM)

The digital volume control, [AMP\\_VOL\\_PCM](#) (see [p. 115](#)), in the amplifier audio data path, sets the digital attenuation or the gain applied to the signal and can be adjusted from -102 to +12 dB in 0.125 dB steps.

The [AMP\\_VOL\\_PCM](#) configuration controls the volume of the serial port PCM audio inputs.

**Note:** The [AMP\\_VOM\\_PCM](#) gain should not be set to a value higher than +3.5 dB if dynamic range enhancement is enabled ([AMP\\_DRE\\_EN=1](#)), see [Section 4.8.1](#).

#### 4.2.2.1 PCM Muting via the Digital Volume Control

In addition to the -102 dB to +12 dB volume adjustment, mute settings are encoded in the volume control. By setting [AMP\\_VOL\\_PCM](#) to any value from 0x400 to 0x4CF, the digital audio path is muted. This mutes the audio provided to the input of the analog Class D amplifier. The Class D amplifier outputs a modulated zero signal. This signal, when averaged differentially across the load, produces an output of approximately 0 Vrms.

Unlike the analog mute, when the digital mute is applied, the OUTP/N pins continue to toggle unless the amplifier level-dependent muting function is enabled as described in [Section 4.4.3](#).

#### 4.2.2.2 PCM Digital Soft Ramping (AMP\_RAMP\_PCM)

By setting [AMP\\_RAMP\\_PCM](#) (see p. 115), volume-control updates written to AMP\_VOL\_PCM are applied slowly by stepping through each volume-control setting with a delay between volume step adjustments configured by AMP\_RAMP\_PCM. The soft ramp is disabled by setting AMP\_RAMP\_PCM = 000.

When enabled, the amount of delay between steps is set via the digital soft-ramp rate bits and can vary from 0.5 ms/6 dB to 30 ms/6 dB. Individual adjustments occur in 0.125 dB volume steps.

When the soft ramp is enabled and the AMP\_VOL\_PCM is changed from a muted value to a non-muted value, the soft ramp steps through any muted codes prior to stepping through any unmuted codes. Any soft-ramp timing calculations when coming out of mute must include these additional steps.

#### 4.2.3 PCM Amplifier Audio Inversion (AMP\_INV\_PCM)

[AMP\\_INV\\_PCM](#) (see p. 115), inverts the polarity of the PCM audio provided to the Class D amplifier. This inversion is performed digitally by inverting the PCM audio provided to the Class D amplifier.

#### 4.2.4 PCM Amplifier High Pass Filter Enable (AMP\_HPF\_PCM\_EN)

The PCM path high pass filter is enabled and disabled via the [AMP\\_HPF\\_PCM\\_EN](#) (see p. 115).

For normal use, it is recommended to leave the high pass filter enabled, as any DC offset produced by the PCM audio source can directly impact amplifier pop/click performance during power up/down.

#### 4.2.5 Amplifier Analog Gain Control

The analog gain between the output of the digital PWM modulator and the input of the closed-loop Class D amplifier is configurable from 0 to 20.0 dB.

[Table 4-5](#) shows example outputs for a full-scale input signal, assuming AMP\_VOL\_PCM = 0 dB for all input sources.

**Table 4-5. Amplifier Gain Peak Output Voltage with 0 dB Digital Input Signal—All Inputs**

AMP_GAIN_PCM	Gain (dB)	Unloaded Full-Scale Peak Output Voltage (V <sub>PK</sub> ) <sup>1</sup>	AMP_GAIN_PCM	Gain (dB)	Unloaded Full-Scale Peak Output Voltage (V <sub>PK</sub> ) <sup>1</sup>
00000	0	1.38	01011	11	4.90
00001	1	1.55	01100	12	5.50
00010	2	1.74	01101	13	6.17
00011	3	1.95	01110	14	6.93
00100	4	2.19	01111	15	7.77
00101	5	2.46	10000	16	8.72
00110	6	2.76	10001	17	9.79
00111	7	3.09	10010	18	10.98
01000	8	3.47	10011	19	12.17
01001	9	3.90	10100	20	13.82
01010	10	4.37	10101-11111	—	Reserved

1. Actual peak amplifier output voltages are limited by the VDDP voltage provided to the amplifier. Amplifier output voltages larger than VDDP are clipped by the VDDP voltage.

##### 4.2.5.1 Analog Gain Control—Serial Port Input (AMP\_GAIN\_PCM)

When the amplifier is configured to use a PCM audio source, the [AMP\\_GAIN\\_PCM](#) (see p. 120) configures the analog gain applied to the input of the Class D amplifier.

##### 4.2.5.2 Analog Gain Change Zero Cross (AMP\_GAIN\_ZC)

To reduce the risk of producing audio artifacts, [AMP\\_GAIN\\_ZC](#) (see p. 120) controls whether any user-controlled amplifier gain change occurs on an audio zero-crossing point. If no zero-crossing point occurs, the detection times out after a period of 50 ms, allowing a gain change to occur.

If AMP\_GAIN\_ZC = 0 (disabled), amplifier gain changes occur immediately when the update is received, increasing the likelihood of audio artifacts.

Setting AMP\_GAIN\_ZC = 1 enables the functionality when the Serial Port PCM input is selected as the audio source.

#### 4.2.6 OUTP/N Shorts Detection

To determine whether the OUTP or OUTN pins are shorted together, to GND or to VDDP, a comparison of the expected PWM output is made versus the actual OUTP/N output. When a large enough difference is detected, an AMP\_SHORT error ([AMP\\_SHORT\\_ERR\\_EINT](#) (see p. 123) and/or BST\_SHORT error ([BST\\_SHORT\\_ERR\\_EINT](#) (see p. 122) is reported and Speaker-Safe Mode is entered (as described in [Section 4.2.8](#)), to prevent damage to the device or system. For an OUTP/N short to GND or short to VDDP condition, no audio output signal is required. However, for an OUTP to OUTN shorts condition to be observed, a large enough, nonzero audio signal must be applied to produce a measurable difference on the PWM outputs.

If one of these short conditions occur, the AMP\_SHORT\_ERR\_STS and/or the BST\_SHORT\_ERR\_STS bit is set, and if AMP\_SHORT\_ERR\_MASK = 0 and BST\_SHORT\_ERR\_MASK = 0, the interrupt pin is asserted. Additionally, the device enters Speaker-Safe Mode, which is described in [Section 4.2.8](#).

In order to exit an AMP\_SHORT error condition, the hardware error must first be resolved via the release sequence. Powering down and up the digital blocks using GLOBAL\_EN or AMP\_EN does not clear the AMP\_SHORT or BST\_SHORT error condition. Once the shorts condition is no longer present, the [AMP\\_SHORT\\_ERR\\_RLS](#) (see p. 92) or BST\_SHORT\_ERR\_RLS (see p. 92) can be sequenced to exit Speaker-Safe Mode.

It is recommended, when powering up the CS35L38A for the first time on an assembled PCB, that the output stage is not configured to start up in a Weak-FET Mode ([WKFET\\_AMP\\_FRC](#) = 1) to immediately detect any shorts. When operating in Weak-FET Mode, there is limited ability to detect an amplifier shorts condition. Refer to [Section 4.4.2](#) for more information on weak-FET operation.

#### 4.2.7 Class D Audio Amplifier Fault/Error Conditions

[Table 4-6](#) describes the interrupt associated with components shown in [Fig. 4-2](#).

**Table 4-6. Class D Audio Amplifier Error Status Fields**

Raw Status Flag	Cause	Rising-Edge Flag	Interrupt Mask
<a href="#">AMP_SHORT_ERR_STS</a>	The device has determined that OUTP or OUTN have shorted to one another, GND, or VDDP.	<a href="#">AMP_SHORT_ERR_EINT</a>	<a href="#">AMP_SHORT_ERR_MASK</a>

#### 4.2.8 Speaker-Safe Mode Errors and Release Behavior

When a specific set of errors occurs, the CS35L38A enters a Speaker-Safe Mode of operation to protect the device and any surrounding components (e.g. a speaker load, boost converter inductor, etc.) from the potential of physical damage. When a speaker-safe error condition occurs, the CS35L38A shuts down the boost converter and audio amplifier with the outputs in a Hi-Z state, and the user has triggered a manual release via the corresponding release register field.

The errors listed in [Table 4-7](#) summarize the conditions that cause the CS35L38A to enter Speaker-Safe Mode, and their corresponding status and release registers.

**Table 4-7. Speaker-Safe Mode Error Conditions**

Error	Cross-Reference to Description	Error Description Section
Amplifier short error	<a href="#">AMP_SHORT_ERR_EINT p. 123</a>	<a href="#">Section 4.2.6</a>
Amplifier short error mask	<a href="#">AMP_SHORT_ERR_MASK p. 129</a>	
Amplifier short error release	<a href="#">AMP_SHORT_ERR_RLS p. 92</a>	
Boost converter inductor short error	<a href="#">BST_SHORT_ERR_EINT p. 122</a>	<a href="#">Section 4.3.6.2</a>
Boost converter inductor short error mask	<a href="#">BST_SHORT_ERR_MASK p. 128</a>	
Boost converter inductor short error release	<a href="#">BST_SHORT_ERR_RLS p. 92</a>	
Boost converter over voltage error	<a href="#">BST_OVP_ERR_EINT p. 122</a>	<a href="#">Section 4.3.5.3</a>
Boost converter over voltage error mask	<a href="#">BST_OVP_ERR_MASK p. 128</a>	
Boost converter over voltage error release	<a href="#">BST_OVP_ERR_RLS p. 91</a>	
Boost converter under voltage error	<a href="#">BST_DCM_UVP_ERR_EINT p. 122</a>	<a href="#">Section 4.3.5.4</a>
Boost converter under voltage error mask	<a href="#">BST_DCM_UVP_ERR_MASK p. 128</a>	
Boost converter under voltage error release	<a href="#">BST_UVP_ERR_RLS p. 91</a>	
Overtemperature error	<a href="#">TEMP_ERR_EINT p. 122</a>	<a href="#">Section 4.7.2.3</a>
Overtemperature error mask	<a href="#">TEMP_ERR_MASK p. 128</a>	
Overtemperature error release	<a href="#">TEMP_ERR_RLS p. 91</a>	
Clocking error	<a href="#">PLL_UNLOCK_EINT p. 124</a>	<a href="#">Section 4.9.1.4</a>
Clocking error mask	<a href="#">PLL_UNLOCK_MASK p. 130</a>	

In order to clear Speaker-Safe Mode, the offending condition must first be corrected. Then the associated release registers (RLS\_x) can be sequenced by writing 0, 1, then 0 to initiate a release of the speaker-safe mode error condition handling.

Alternatively, asserting RST or removing the VDDD supply, triggering the POR will clear a speaker-safe operational state.

## 4.3 Digital Boost Converter

The digital boost converter consists of three ADCs and two digital control loops. The three ADCs measure the VBAT voltage, VBST voltage, and inductor current through the boost converter's N-FET. This digitized voltage and current information is then provided to the digital boost converter's controller for processing.

This converter uses a digitized control loop based on a current-controlled synchronous boost converter architecture that continually monitors the L<sub>BST</sub> inductor current during boosted operation. The outer control loop takes the digitized VBST voltage and the digitized current information provided by the inner loop to regulate the boosted voltage to the desired level between VBST<sub>MIN</sub> and VBST<sub>MAX</sub> (see [Table 3-6](#)). The VBST voltage level can be either automatically controlled by the internal Class H algorithm or manually controlled by the user

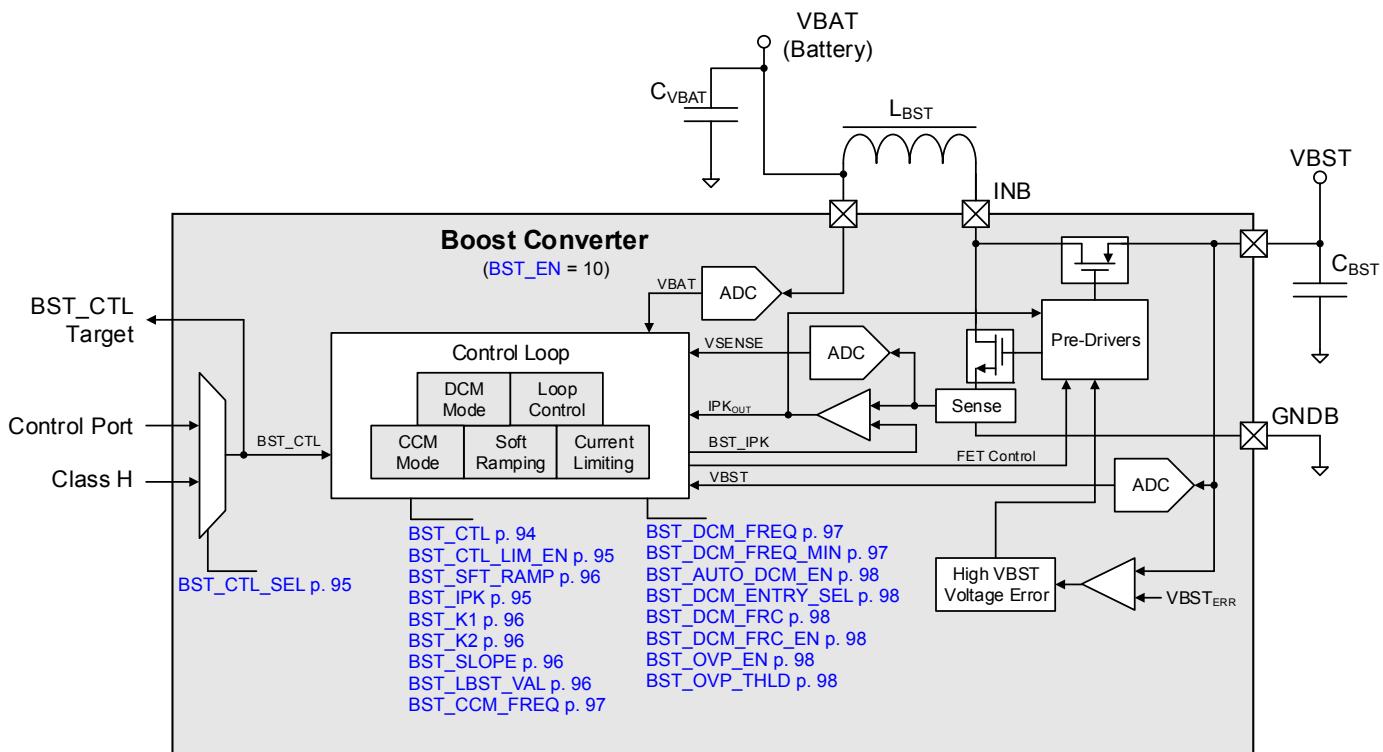


Figure 4-3. Digital Boost Converter Block Diagram

#### 4.3.1 Boost Converter Enable/Power-Up Control (BST\_EN)

The boost converter enable/power-up register field, **BST\_EN** (see p. 89), controls whether the boost converter is powered up and in which operating state. Table 4-8 provides more details on the different power-up and power-down configuration of the digital boost converter.

Enabling the digital boost converter **BST\_EN** = 10 automatically enables the **VBATMON** and **VBSTMON** supply monitoring ADCs (see Section 4.5.4 and Section 4.5.5).

Table 4-8. Mode Descriptions—**BST\_EN** Settings

<b>BST_EN</b>	<b>GLOBAL_EN<sup>1</sup></b>	<b>RST</b>	<b>Description</b>
XX	X	Low	IC is held in a reset state. The boost converter is powered down and the rectification FET is disabled (diode conduction only).
XX	0	High	The boost converter is powered down and is turned off. VBAT and VBST are only connected through an intrinsic diode which is in parallel with the rectification FET.
00	1	High	Reserved
01 (Boost disabled—rectification FET on)	1	High	Used when the boost converter control block is to be powered down with the rectification FET turned on, connecting VBST to VBAT. This is similar to setting <b>BST_EN</b> = 10 and <b>BST_CTL</b> = 0x00, except that the control block is powered down. This is the lowest power mode for operating the device when VBST = VBAT and no boost converter functionality is required.
10 (Boost enabled)	1	High	The boost converter is powered up and operational. In this mode, <b>BST_CTL</b> settings set the boost converter output to the level described in Section 4.3.2.
11	1	High	Reserved.

<sup>1</sup>The control of **GLOBAL\_EN** can be overridden using the **BST\_GLOBAL\_OVR** control. See Section 4.1.4.

#### 4.3.2 VBST Voltage Control

The CS35L38A's boost converter VBST voltage is capable of being managed in multiple ways for purposes of both flexibility and efficiency. The control source, VBST range, limiting, and voltage soft-ramping of the VBST supply generated by the digital boost converter are all flexible and configurable in order to support a wide range of use cases.

#### 4.3.2.1 VBST Voltage Control Source Selection (BST\_CTL\_SEL)

There are multiple sources which can control the VBST target voltage, and the control source is selectable via the [BST\\_CTL\\_SEL](#) configuration (see [p. 95](#)).

- Manual VBST voltage target from control port—[Section 4.3.2.3](#)
- Automatic VBST voltage target from Class H tracking—[Section 4.4.1](#)

The Class H tracking is only available as an audio source when a PCM audio source is selected.

#### 4.3.2.2 VBST Voltage Control Limiting (BST\_CTL\_LIM\_EN)

When the BST\_CTL\_SEL is configured to use Class H tracking, the boost converter's voltage can be optionally limited by the control port BST\_CTL configuration.

Setting the [BST\\_CTL\\_LIM\\_EN](#) configuration (see [p. 95](#)) enables the boost converter's maximum boost voltage to be limited by the BST\_CTL setting, even if there is a Class H tracking request to make the target voltage larger than BST\_CTL.

#### 4.3.2.3 VBST Voltage Control (BST\_CTL)

When selected as the VBST target source, the VBST voltage can be manually programmed via the control port using the [BST\\_CTL](#) configuration (see [p. 94](#)). This configuration determines the digital boost converter's output voltage (VBST), as shown in [Table 4-9](#).

**Table 4-9. Using BST\_CTL to Manually Control the VBST Voltage**

BST_CTL	VBST Target Voltage	Notes
0000 0000	VBAT	Internal rectification FET is turned on and boost FET does not switch.
0000 0001	2.55	If the target VBST voltage is less than VBAT, the boost converter remains in Bypass Mode
0000 0010	2.60	If the target VBST voltage is less than VBAT, the boost converter remains in Bypass Mode
...	...	—
1011 1100	11.90	—
1011 1101	11.95	—
1011 1110	12.00	VBST level is limited to 12.0 VDC. Any setting above this code is held at 12.0 VDC.

#### 4.3.2.4 VBST Voltage Soft Ramping (BST\_SFT\_RAMP)

The CS35L38A's digital boost converter uses soft ramping to minimize current loading transients during normal operation. The soft ramping reduces the instantaneous load changes that can occur when the VBST voltage is increasing or decreasing, which is intended to minimize both inrush and backpowering from the digital boost converter to the VBAT supply. The rate of the soft ramping is controlled by the [BST\\_SFT\\_RAMP](#) configuration (see [p. 96](#)).

When a change in the target VBST configuration occurs, the digital boost converter restricts immediate large VBST voltage changes, converting them to a series of sequential steps until reaching the configured boost voltage. For example, if the user changes the configuration of BST\_CTL from 4.2 V to 8.0 V, the boost voltage is stepped up in a series of 50 mV increments from 4.2 V until reaching 8.0 V to minimize loading transients.

A virtual RC filter is applied to each of the 50 mV steps to further reduce inrush current produced by the change in voltage. The response of this virtual RC filter changes along with BST\_SFT\_RAMP to respond appropriately to the longer or shorter time periods in between each 50 mV step.

When the VBST target voltage is increased, the rate of increase is centered around the BST\_SFT\_RAMP configuration. However, when the VBST target is decreased, depending on the operating conditions (e.g., C<sub>BST</sub>, change in VBST, boost loading, etc.), the actual ramp down time may be larger than the BST\_SFT\_RAMP target. This minimizes the potential of backpowering the charge from C<sub>BST</sub> capacitor on to the VBAT supply when the load resistance is not low enough to naturally discharge the C<sub>BST</sub> capacitor.

In addition, when transitioning between different VBST voltages, care must be taken to not produce large amounts of inrush current (when increasing VBST) or to back-power VBAT (when decreasing VBST). The CS35L38A's digital boost converter applies a soft ramp to all of the changes in VBST voltage to reduce inrush current when increasing VBST and the back-powering of the VBAT supply when decreasing the VBST voltage.

**Fig. 4-4** illustrates a boost converter without soft-ramping along with the associated inrush and backpowering on VBAT. **Fig. 4-5** illustrates shows how the inrush and backpowering are significantly reduced on with the `BST_SFT_RAMP` functionality of the CS35L38A's digital boost converter.

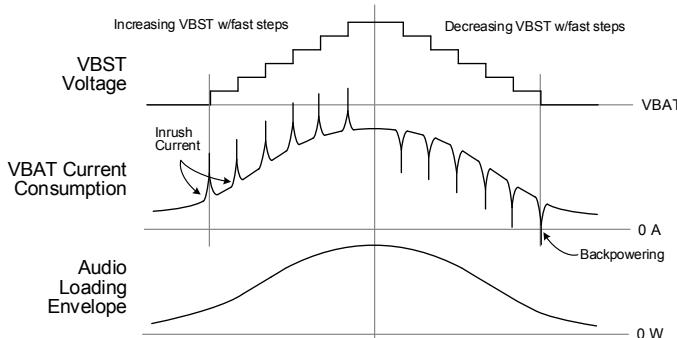


Figure 4-4. Fast Voltage Step Boost Converter

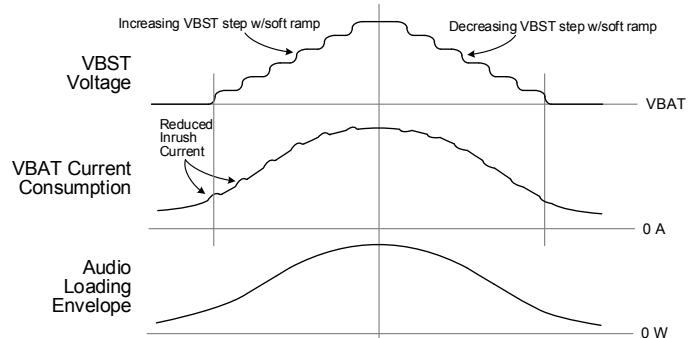


Figure 4-5. CS35L38A's Boost Converter with Soft Ramping

### 4.3.3 Boost Converter Switching Modes

The digital boost converter has two primary modes of operation to support different use cases: Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM). The modes, along with the details of their intended operational use, are listed in [Table 4-10](#).

Table 4-10. Boost Converter DCM and CCM Modes

Boost Switching Mode	VBST Power Delivery	Class H Support	Low Power VBST Voltage Maintenance	Configurable Switching Frequency Range <sup>1</sup>	Rectification FET Operation
DCM	Very low VBST loading only	N	Y	90 Hz–2.00 MHz <sup>2</sup>	Diode conduction only
CCM	Capable of idle to VBST max power delivery	Y	N	889 kHz–2.00 MHz <sup>3</sup>	Active and synchronous to boost FET

1. Frequencies listed are with a  $f_{PLL\_OUT}$  of 192 MHz.

2. The absolute minimum DCM switching frequency is bounded by  $[24 \text{ MHz} / (12 + BST\_DCM\_FREQ)] / BST\_DCM\_FREQ\_MIN$ . See [Section 4.3.3.5](#).

3. The switching frequency range in CCM Mode is based on the `BST_CCM_FREQ` configuration. See [Section 4.3.6](#).

DCM Mode is intended to maintain the VBST voltage on the  $C_{BST}$  capacitor when the rest of the CS35L38A is operating in a low power or idle power mode. It is not intended to support power delivery from the VBST to the VDDP of the amplifier. Along with level-dependent muting, it allows the CS35L38A to enter a very low power operational state for use cases in which Class H is not being used to automatically manage the VBST voltage based on the audio signal.

CCM Mode is intended to be the boost converter's operational mode for power delivery to the amplifier or an external loading source. When operating with Class H tracking enabled, there is not a need to enter a DCM mode of operation, as when the audio signal is low enough the boost converter is automatically disabled and put into Bypass Mode ( $VBST = VBAT$ ) in order to minimize power consumption and maximize efficiency.

#### 4.3.3.1 Boost Converter DCM Mode Enable (`BST_AUTO_DCM_EN`)

The `BST_AUTO_DCM_EN` configuration (see [p. 98](#)) enables the DCM Mode control and automatic transitioning between DCM Mode and CCM Mode. The transitioning between DCM Mode and CCM Mode is automatically controlled by an input audio signal via the level-dependent muting control.

#### 4.3.3.2 Boost Converter DCM Mode Entry Control (BST\_DCM\_ENTRY\_SEL)

The [BST\\_DCM\\_ENTRY\\_SEL](#) configuration (see [p. 98](#)) configures the boost converter to select the source of the automatic CCM to DCM entry to be from the audio path level-dependent muting, or disable the automatic detection functionality, requiring the boost converter to manually be put into DCM Mode via the [BST\\_DCM\\_FRC](#) and [BST\\_DCM\\_FRC\\_EN](#) controls.

#### 4.3.3.3 Boost Converter DCM Mode Exit Control (BST\_DCM\_EXIT\_SEL)

The [BST\\_DCM\\_EXIT\\_SEL](#) configuration (see [p. 97](#)) configures the boost converter to select the source of the automatic DCM exit to be the audio path level-dependent muting or to disable the automatic detection functionality, which requires the boost converter to manually be put into DCM Mode via the [BST\\_DCM\\_FRC](#) and [BST\\_DCM\\_FRC\\_EN](#) controls.

#### 4.3.3.4 Boost Converter Force DCM Mode (BST\_DCM\_FRC and BST\_DCM\_FRC\_EN)

[BST\\_DCM\\_FRC](#) (see [p. 98](#)) and [BST\\_DCM\\_FRC\\_EN](#) (see [p. 98](#)) allow the boost converter to be manually forced into DCM Mode, regardless of the state of [BST\\_AUTO\\_DCM\\_EN](#). When manually forced into DCM Mode, the automatic DCM to CCM and CCM to DCM detections are overridden and the boost converter remains in DCM Mode.

When enabled by the [BST\\_DCM\\_FRC\\_EN](#), the [BST\\_DCM\\_FRC](#) action occurs on either the transition from 0 to 1 or vice versa. If the [BST\\_AUTO\\_DCM\\_EN](#) is enabled, it can override the [BST\\_DCM\\_FRC](#) as shown in [Table 4-11](#).

**Table 4-11. Boost Converter DCM Mode Force**

BST_AUTO_DCM_EN	BST_DCM_FRC_EN	BST_DCM_FRC <sup>1</sup>	Automatic DCM ↔ CCM Control	DCM Mode Entry	DCM Mode Exit <sup>2</sup>
0	0	x	Disabled	CCM Mode operation only	
0	1	0		Force into DCM Mode	—
0	1	0→1		—	Force to CCM Mode
0	1	1→0		Remains in DCM if no error condition occurs	Exits DCM if <a href="#">VBST_DCM_UVP_ERR</a> occurs
0	1	1			
1	0	x	Enabled	Automatic CCM ↔ DCM control	
1	1	0		Force into DCM Mode <sup>3</sup>	—
1	1	0→1		—	Force to CCM Mode <sup>3</sup>
1	1	1→0			
1	1	1	Enabled	Automatic CCM ↔ DCM control	

1. [BST\\_DCM\\_FRC](#) cannot be set when boost converter is brought up with [GLOBAL\\_EN](#).

2. [VBST\\_DCM\\_UVP\\_ERR](#) can force a DCM Mode exit under any condition. Refer to [Section 4.3.5.4](#).

3. May automatically transition to DCM or CCM Mode based on operational conditions after the manual force has completed when [BST\\_AUTO\\_DCM\\_EN](#) = 1.

When manually configured into DCM Mode, the boost converter is intended to only be supporting VBST voltage maintenance of the  $C_{BST}$  capacitor, the idle power consumption of the CS35L38A, plus any leakage present on the VBST net. If a large enough external loading event pulls down the VBST voltage to the VBAT supply voltage, the boost converter will disable itself, flag an error, and enter Bypass Mode (see [Section 4.3.5.4](#)).

The DCM Mode force must only be enabled after the boost converter has been powered up and has ramped to the desired voltage.

#### 4.3.3.5 Boost Converter DCM Mode Switching Frequency (BST\_DCM\_FREQ)

The [BST\\_DCM\\_FREQ](#) (see [p. 97](#)) configures the boost converter's base rate switching frequency when operating in DCM Mode.

The [BST\\_DCM\\_FREQ](#) sets the primary switching frequency when operating in DCM Mode ( $f_{BST\_SW\_DCM}$ ). The DCM switching frequency configuration ([BST\\_DCM\\_FREQ](#)) is only applicable when operating in DCM Mode. [Eq. 4-1](#) shows how to calculate the DCM switching frequency base rate. Where the [BST\\_DCM\\_FREQ](#) is based on decimal value configuration of the register.

For example setting `BST_DCM_FREQ = 00 0000 0010` means that for [Eq. 4-1](#) the `BST_DCM_FREQ` is a decimal value of 2.

$$f_{BST\_DCM\_SW} = \left( \frac{f_{PLL\_OUT}}{8 \times (12 + BST\_DCM\_FREQ)} \right)$$

**Equation 4-1. Boost Converter DCM Switching Frequency**

Refer to [Section 4.3.6.1](#) for information on adjusting the boost converter switching frequency when in CCM Mode and [Section 4.9.1.5](#) on the  $f_{PLL\_OUT}$  frequency.

The `BST_DCM_FREQ` must be configured to support the expected output loading of the system from the VBST supply. The switching frequency impacts the effective maximum duty cycle of the boost converter when operating in DCM Mode. As the `BST_DCM_FREQ` is reduced, the amount of boost FET on time, relative to a fixed period off time is also reduced.

#### 4.3.3.6 Boost Converter DCM Mode Minimum Switching Frequency (`BST_DCM_FREQ_MIN`)

Configuring the `BST_DCM_FREQ_MIN` (see [p. 97](#)) to a non-zero value allows the boost converter's switching frequency to be further reduced when operating in DCM Mode. If there is very little or no loading on the VBST supply when operating in DCM Mode, the boost converter has the option to skip `BST_DCM_FREQ` switching periods and slow down its effective switching frequency to further reduce its power consumption. This allows the CS35L38A to operate in a very low power state while maintaining a boosted VBST supply voltage.

To disable the boost converter from skipping switching periods while operating in DCM Mode pulse skipping, set `BST_DCM_FREQ_MIN = 0`.

#### 4.3.4 Inductor Current Limiting

The boost FET peak-current limit governs the peak current that is allowed to flow through the inductor during each on cycle of the boost FET. The boost FET is turned off either when the ON time of the boost FET reaches the ON time required by the controller or when it hits the boost peak-current limit. This boost current is quantized and sent to the digital boost converter control block for processing.

##### 4.3.4.1 Peak Current Limiter (`BST_IPK` and `BST_IPK_EINT`)

The boost-peak current threshold is controlled by `BST_IPK` (see [p. 95](#)). If the current demands on the output net of the boost converter (VBST) force the inductor current to reach the configured limit ( $I_{BST\_L}$ ), the boost converter limits the current through the  $L_{BST}$  inductor. If the loading on VBST remains while the current is being limited, the boost converter's output voltage may droop below its configured voltage.

The `BST_IPK_EINT` bit (see [p. 122](#)) is set when the inductor current limit is in effect.

#### 4.3.5 VBST Overvoltage and Undervoltage Protection and Errors

The digital boost converter contains integrated monitoring and protection for high VBST voltage conditions. This protects against damage of both the CS35L38A and its surrounding components.

##### 4.3.5.1 VBST Overvoltage Protection Threshold (`BST_OVP_THLD` and `BST_OVP_EINT`)

If a change in configuration, the system environment, or loading transient causes the VBST voltage to rapidly increase, a safety response is triggered and the controller actively limits the maximum VBST voltage (VBSTPROT) as configured by the `BST_OVP_THLD` (see [p. 98](#)). After the VBST voltage is reduced back to its configured VBST voltage the digital boost converter returns to normal operation.

When the high voltage is actively limiting, `BST_OVP_EINT` (see [p. 122](#)) is set.

#### 4.3.5.2 VBST Overvoltage Protection Enable (BST\_OVP\_EN)

The overvoltage protection may be disabled with the [BST\\_OVP\\_EN](#) (see p. 98). For most operational conditions, it is recommended that the VBST overvoltage protection is enabled in order to help protect external components such as the  $C_{BST}$  capacitor.

#### 4.3.5.3 VBST Overvoltage Error (BST\_OVP\_ERR\_EINT)

In the event of a device or other hardware failure creates a high VBST voltage error condition above the  $V_{BSTM}$  voltage, a secondary level of protection is triggered. This VBST high voltage error ( $V_{BSTM}$ ) protection exists outside of the main digital boost converter control loop. When this VBST high voltage error condition occurs, the digital boost converter is disabled, a weak discharge path is turned on to bleed off the VBST voltage, the CS35L38A is put into Speaker-Safe Mode, and [BST\\_OVP\\_ERR\\_EINT](#) (see p. 122) is set. This error can only be cleared by cycling either [GLOBAL\\_EN](#) or [BST\\_EN](#) in order to power down and then power back up the boost converter. To return the boost to normal operation, [BST\\_OVP\\_ERR\\_RLS](#) must be set and cleared.

#### 4.3.5.4 VBST DCM Mode Undervoltage Error (BST\_DCM\_UVP\_ERR\_EINT)

In the event that the VBST voltage is pulled down to VBAT voltage during DCM Mode operation, [BST\\_DCM\\_UVP\\_ERR\\_EINT](#) (see p. 122) is triggered and the device enters Speaker-Safe Mode. In order to exit this error condition, the VBST load must be removed, and this error can only be cleared by cycling either [GLOBAL\\_EN](#) or [BST\\_EN](#) in order to power down and then power back up the boost converter. To return the boost to normal operation, [BST\\_UVP\\_ERR\\_RLS](#) must be set and cleared.

### 4.3.6 $L_{BST}$ Selection and Boost Converter Configuration

The CS35L38A allows the flexibility of using of an  $L_{BST}$  inductance of 2.2  $\mu$ H to 1.0  $\mu$ H. Note that the selected  $L_{BST}$  inductor must not derate to a value of less than 0.7  $\mu$ H under any condition. Depending on the manufacturer, load rating, parasitics, and type of inductor, the derating characteristics of a specific inductor can vary widely. If a given  $L_{BST}$  inductor can derate to 0.7  $\mu$ H or below, it is not considered to be fully compatible with the CS35L38A.

The digital boost converter contains controls to allow the user to configure the digital boost converter's control loop for different boost converter external component configurations ( $L_{BST}$  and  $C_{BST}$ ) or system-level requirements. These configurations are listed in [Table 4-12](#).

**Table 4-12. Boost Converter  $L_{BST}$  Inductor Configuration Bits**

Name	Register Cross-Reference	Field Description
Boost converter coefficient 1	<a href="#">BST_K1 p. 96</a>	BST_K1 and BST_K2 are used to adjust the boost converter's feedback loop to compensate for the changes produced by using a different $L_{BST}$ inductance or different system requirements.
Boost converter coefficient 2	<a href="#">BST_K2 p. 96</a>	<b>Note:</b> Adjusting for a lower inductance reduces the loop bandwidth.
Boost converter slope compensation	<a href="#">BST_SLOPE p. 96</a>	BST_SLOPE allows for adjustment of the boost converter's internal ramp-gen slope to compensate for the changes produced by a using a different $L_{BST}$ inductance.
Boost converter target inductance value	<a href="#">BST_LBST_VAL p. 96</a>	BST_LBST_VAL seeds the digital boost converter's inductor estimation block with an initial seeded reference value.
Boost converter switching frequency	<a href="#">BST_CCM_FREQ p. 97</a>	BST_CCM_FREQ controls the fundamental output switching frequency of the digital boost converter's INB net.

The recommended configurations for example  $L_{BST}$  inductor values are listed in [Table 4-13](#). All configurations assume a maximum of 30% derating below the typical value under all operating conditions.

**Table 4-13. Recommended Configurations for Common  $L_{BST}$  Values**

Typical $L_{BST}$ ( $\mu$ H)	Derated $C_{BST}$ ( $\mu$ F)	<b>BST_K1</b>	<b>BST_K2</b>	<b>BST_SLOPE</b>	<b>BST_CCM_FREQ</b>	<b>BST_LBST_VAL</b>
1.0	22	0x3C	0x3C	0x75	0x0	0x0
1.2	22	0x3C	0x3C	0x6B	0x0	0x1

#### 4.3.6.1 Boost Converter Switching Frequency (BST\_CCM\_FREQ)

The boost converter switching frequency is adjusted using [BST\\_CCM\\_FREQ](#) (see p. 97) and allows the user to adjust the output switching frequency of the boost and rectification FETs.

[Eq. 4-2](#) provides a formula for calculating the  $f_{\text{BST\_SW\_FREQ}}$ . The output switching frequencies will scale with an increased or decreased  $f_{\text{PLL\_OUT}}$ . For most operating conditions it is recommended to leave [BST\\_CCM\\_FREQ](#) at its default configuration.

$$f_{\text{BST\_SW\_FREQ}} = \left( \frac{f_{\text{PLL\_OUT}}}{8 \times (12 + \text{BST\_CCM\_FREQ})} \right)$$

**Equation 4-2. Boost Converter CCM Switching Frequency**

#### 4.3.6.2 $L_{\text{BST}}$ Inductance/Shorts Error Protection (BST\_SHORT\_ERR\_EINT)

If there is a significant issue with the  $L_{\text{BST}}$  inductor or hardware and the measured  $L_{\text{BST}}$  inductance falls below the threshold value of  $L_{\text{BST\_ERR}}$  (see [Table 3-6](#)), the boost converter is automatically disabled and the CS35L38A is put into Speaker-Safe Mode to protect the CS35L38A, the inductor, other external components, the PCB, and the battery. When this low inductance error condition is detected, [BST\\_SHORT\\_ERR\\_EINT](#) (see p. 122) is set.

**Note:** The  $L_{\text{BST}}$  inductance is monitored only when the boost converter is generating a boosted supply with  $\text{VBST}/\text{VBAT}$  ratio  $> 1.8$  and not when in Bypass Mode ( $\text{VBST} = \text{VBAT}$ ).

The  $L_{\text{BST}}$  inductance error is intended to flag hardware problems such as an assembly issue or failure of the inductor, while reducing the risk of potential damage to the CS35L38A and its surrounding hardware. This error can only be cleared by cycling either [GLOBAL\\_EN](#) or [BST\\_EN](#) in order to power down and then power back up the boost converter. To return the boost to normal operation, [BST\\_SHORT\\_ERR\\_RLS](#) must be set and cleared.

#### 4.3.7 Digital Boost Converter Fault/Error Conditions

[Table 4-14](#) describes the errors related to the digital boost converter.

**Table 4-14. Digital Boost Converter Error Status Fields**

Raw Status Flag	Cause	Rising-Edge Flag	Interrupt Mask
<a href="#">BST_IPK_STS</a>	Indicates that the inductor current limiting is active.	<a href="#">BST_IPK_EINT</a>	<a href="#">BST_IPK_MASK</a>
<a href="#">BST_OVP_STS</a>	VBST voltage is rapidly rising; the controller is actively attempting to limit VBST voltage to $\text{VBST-PROT}$ as configured.	<a href="#">BST_OVP_EINT</a>	<a href="#">BST_OVP_MASK</a>
<a href="#">BST_OVP_ERR_STS</a>	VBST voltage is over the $\text{VBST}_{\text{ERR}}$ voltage.	<a href="#">BST_OVP_ERR_EINT</a>	<a href="#">BST_OVP_ERR_MASK</a>
<a href="#">BST_DCM_UVP_ERR_STS</a>	VBST voltage is pulled under the VBAT voltage during DCM Mode operation.	<a href="#">BST_DCM_UVP_ERR_EINT</a>	<a href="#">BST_DCM_UVP_ERR_MASK</a>
<a href="#">BST_SHORT_ERR_STS</a>	The measured $L_{\text{BST}}$ inductance has fallen below approximately $0.2\mu\text{H}$ .	<a href="#">BST_SHORT_ERR_EINT</a>	<a href="#">BST_SHORT_ERR_MASK</a>

### 4.4 Device Power Management

The CS35L38A offers three different types of power management control subsystems which monitor the incoming audio data in order to minimize device power consumption while maximizing efficiency:

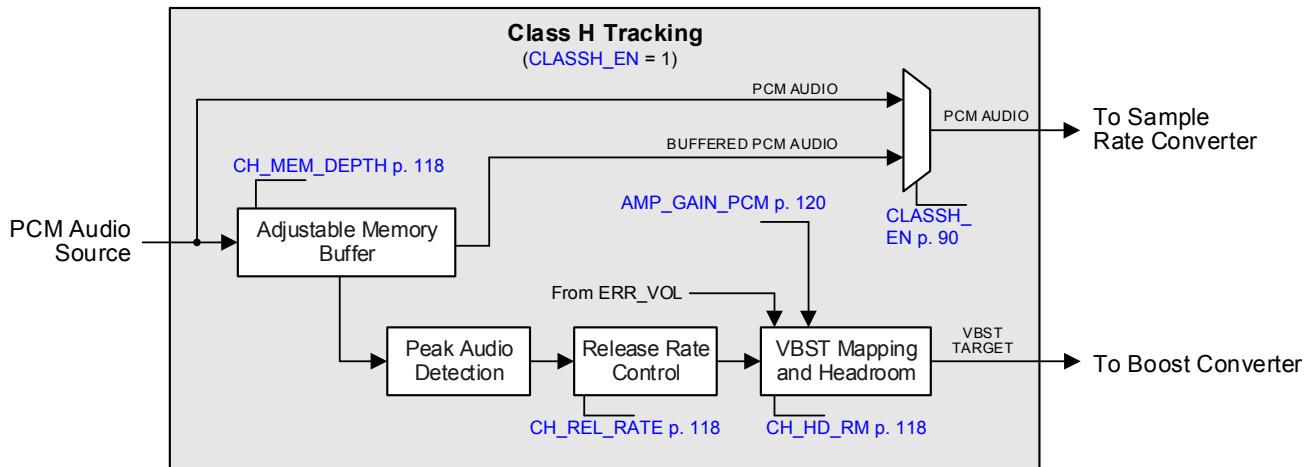
- Class H tracking—Manages VBST supply voltage generation (see [Section 4.4.1](#))
- Amplifier weak-FET drive—Manages amplifier drive strength (see [Section 4.4.2](#))
- Level-dependent muting—Manages power state of multiple functional blocks (see [Section 4.4.3](#))

#### 4.4.1 Class H Tracking

The internal Class H tracking can be used to automatically configure the boost converter's generated VBST voltage (described in [Section 4.3](#)) based on the requirements of the audio signal and device configurations. The Class H analyzes the audio data in its buffer memory, predicts the amplifier's audio output amplitude signal, adds a user configured headroom, and produces a VBST target for the digital boost converter to generate.

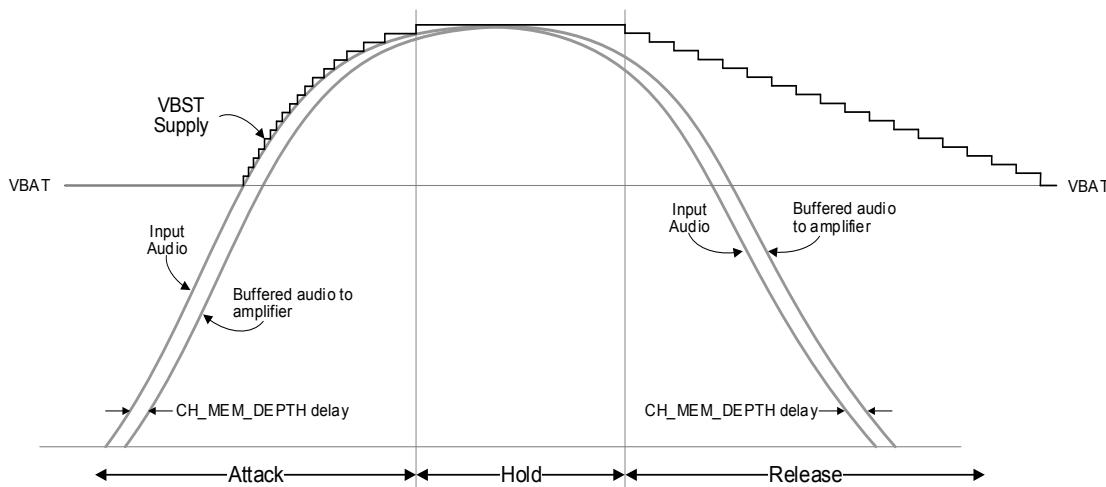
The Class H takes into account the gain configurations of the amplifier audio path (see [Section 4.2.2](#) and [Section 4.2.5](#)) as well as the ERR\_VOL attenuation applied from a VBAT brownout prevention error (see [Section 4.6](#)) or overtemperature warning (see [Section 4.7.2](#)). This enables the Class H to minimize the requested boost voltage under various conditions, decreasing device power consumption, and maximizing efficiency.

[Fig. 4-6](#) shows the audio and data flow through the Class H.



**Figure 4-6. Class H Tracking**

[Fig. 4-7](#) shows the relationship between the audio envelope and the buffered audio signal presented to the Class D amplifier. A programmable delay is created by the Class H's memory buffer and is configured via the [CH\\_MEM\\_DEPTH](#) field, described in [Section 4.4.1.2](#).



**Figure 4-7. Class H Audio Envelope—Attack, Hold, and Release**

The three conditions of the cycle are described as follows:

**Attack.** An attacking condition occurs when the input audio signal update shows an increase in amplitude, in response to which the target VBST supply voltage is increased. To prevent clipping the audio output, an attacking condition responds immediately to a change in audio signal by increasing the VBST supply. Otherwise, the Class D amplifier could attempt to produce an output signal larger than what the VBST supply voltage could support without clipping.

**Hold.** A hold condition is reached when the audio envelope amplitude changes by less than  $\Delta V_{BST\_CTL}$  relative to the current value and can be treated as approximately flat. The hold condition continues until the internal Class H algorithm detects the audio envelope changing by at least  $\Delta V_{BST\_CTL}$ .

- If the change is an increase by more than  $\Delta V_{BST\_CTL}$ , the algorithm returns immediately into the attack condition and the boost voltage is determined by the audio input signal.

**Release.** A release condition exists when the amplitude of the audio envelope is falling, during which the target  $V_{BST}$  supply voltage can be reduced in response. During a release condition, the internal Class H algorithm follows the audio envelope in 50 mV steps (i.e.,  $\Delta V_{BST\_CTL}$ ).  $CH\_REL\_RATE$  determines the time period between consecutive release steps.

#### 4.4.1.1 Power-Up and Power-Down Bits (CLASSH\_EN)

The Class H algorithm is enabled or disabled by using [CLASSH\\_EN](#) (see p. 90). If the Class H tracking is enabled ( $CLASSH\_EN = 1$ ), the audio sent to the amplifier's audio path is buffered in the Class H's memory, and a target  $V_{BST}$  voltage is sent to the digital boost converter. The boost converter must be configured to select the Class H as the reference input in order for the supply to track the Class H target.

As shown in [Table 4-15](#), the Class H's target  $V_{BST}$  can be bypassed even if Class H is enabled. However, the memory buffer is always enabled whenever Class H is enabled. The  $BST\_CTL\_SEL$  is described in [Section 4.3.2.1](#).

**Table 4-15. Class H and Boost Converter Control**

CLASSH_EN	BST_CTL_SEL	Class H Memory Buffer – Amplifier Audio	VBST Target Voltage Source
0	0	Bypassed	Control Port – $BST\_CTL$
	1		$V_{BST} = V_{BAT}$ (Bypass Mode)
1	0	Buffer Utilized	Control Port – $BST\_CTL$
	1		Class H Controlled

To prevent audio artifacts, the amplifier must be powered down (see [Section 4.2.1](#)) whenever the state of the  $CLASSH\_EN$  is changed.

#### 4.4.1.2 Class H Memory Depth Control (CH\_MEM\_DEPTH)

The memory buffer in the Class H tracking is intended to buffer the audio for enough time to allow the Class H to process the audio signal, update the target  $V_{BST}$  voltage to the boost converter, and allow the boost converter to respond prior to the audio being output from the Class D amplifier. The Class H memory buffer allows the Class H algorithm to effectively “look ahead” and prepare for the audio signal that the Class D amplifier has not yet produced.

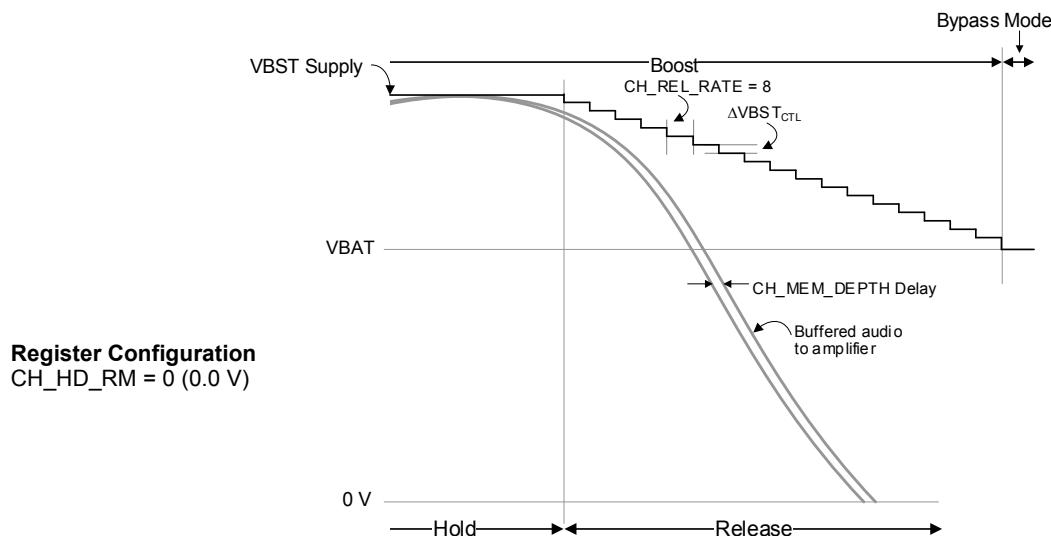
The Class H memory buffer depth is controlled using [CH\\_MEM\\_DEPTH](#) (see p. 118). The internal memory is dynamically managed based on the internally generated sample rate in order to keep the delay period similar between different sample rates.

The  $CH\_MEM\_DEPTH$  configuration must only be changed only if the Class H tracking is disabled ( $CLASSH\_EN = 0$ ).

#### 4.4.1.3 Class H Release-Rate Control (CH\_REL\_RATE)

[Fig. 4-8](#) shows the effect of the [CH\\_REL\\_RATE](#) bits (see p. 118), which configure the amount of time between consecutive release updates to the boost converter. In the release condition, if the configured release-rate requirements have not been met, the most recently updated boost converter configuration is held until the release-rate requirements are met, or if the boost converter configuration is updated based on changes in the audio envelope. For example, if there are a number of consecutive release conditions and the release rate is set to 50  $\mu s$ , the release condition updates the  $V_{BST}$  target voltage sent to the boost converter at a rate of 1 step per 50  $\mu s$ , effectively slowing down the decrease of the  $V_{BST}$  supply. If the max detection path determines that a larger  $V_{BST}$  voltage is needed to support the incoming audio signal, the release condition is no longer valid and the Class H algorithm immediately enters an attacking condition state.

**CH\_REL\_RATE = 8**—Update time based on consecutive release periods



**Figure 4-8. The Effect of the CH\_REL RATE on the Descent of the Supply Voltage**

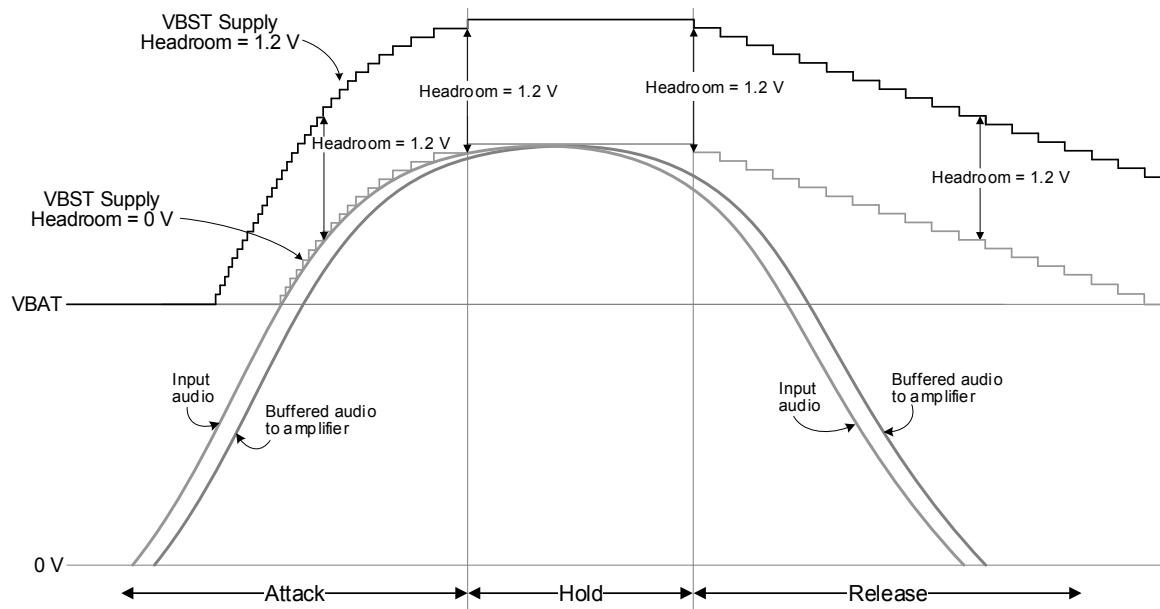
As Fig. 4-8 shows, the Class H release steps always occur in 50 mV increments between  $\text{VBST}_{\text{MIN}}$  and  $\text{VBST}_{\text{CTL-MAX}}$ . A larger step amplitude occurs when transitioning between  $\text{VBST}_{\text{MIN}}$  and  $\text{VBAT}$ , determined by the minimum boost level. After reaching  $\text{VBST}_{\text{MIN}}$  in a continually releasing condition, the  $\text{BST}_{\text{CTL}}$  word continues to be reduced by the Class H algorithm. However, once it reaches  $\text{VBST}_{\text{MIN}}$ , it is automatically limited by the boost converter until reaching  $\text{VBAT}$ . It must be noted that when the Class H algorithm is in a continually releasing state there are conditions where the actual generated VBST voltage may remain the same for two consecutive CH\_REL\_RATE periods. This can occur due to the conversion of the audio envelope to a BST\_CTL configuration.

#### 4.4.1.4 Class H Headroom Control (CH\_HD\_RM)

The **CH\_HD\_RM** (see p. 118), allow the Class H tracking to generate a voltage guard-band between the audio output amplitude and the VBST supply target voltage to be generated by the boost converter.

Fig. 4-9 shows the VBST supply for two values of CH\_HD\_RM for the same audio input signal; one has a headroom of  $\text{CH}_\text{HD}_\text{RM} = 0 \text{ V}$  and the other has a headroom of  $\text{CH}_\text{HD}_\text{RM} = 1.2 \text{ V}$ .

Due to efficiency losses in the system, to produce an unclipped audio signal with a specific output amplitude, the amplifier's supply voltage actually must be higher than the audio signal output amplitude. The magnitude of the voltage supply headroom is specific to the system configuration, taking into account losses in external components, Class D amplifier  $\text{RDS}_{\text{ON}}$ , boost converter configuration, and losses in the signal path to the speaker load.

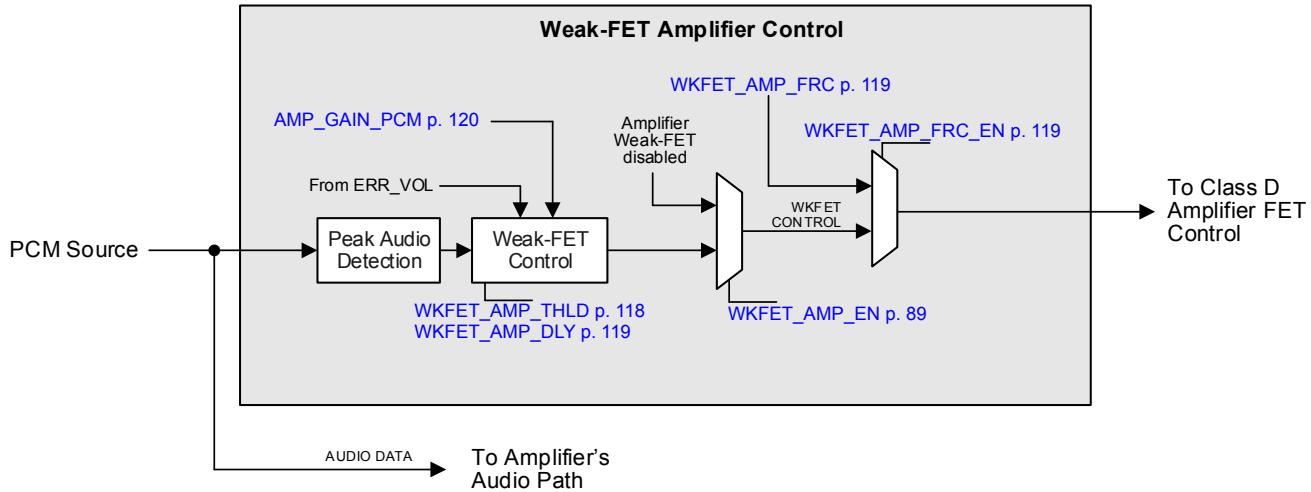


**Figure 4-9. Headroom Control**

#### 4.4.2 Weak-FET Amplifier Drive Strength Control

The CS35L38A's amplifier can monitor the PCM audio stream and dynamically adapt the operational state of its output switching FETs. This is done in order to minimize power consumption and can be utilized when operating in an idle or low loading condition. The strength of the output drivers is reduced when operating in a Weak-FET Drive Mode and must not be used to drive a large load.

Fig. 4-6 shows the audio and data flow through the weak-FET control.



**Figure 4-10. Weak-FET Drive Control Block Diagram**

##### 4.4.2.1 Automatic Weak-FET Drive Enable (WKFET\_AMP\_EN)

**WKFET\_AMP\_EN** (see p. 89) determines whether the weak-FET functionality of the Class D amplifier is automatically managed based on the weak-FET detection path. When the audio signal is below the configured weak-FET threshold (see Section 4.4.2.2), the amplifier automatically configures itself to run in Weak-FET Mode in order to reduce the amplifier's power consumption.

When **WKFET\_AMP\_FRC\_EN** is set, the automatic control is not available (see Section 4.4.2.4).

#### 4.4.2.2 Weak-FET Drive Threshold (WKFET\_AMP\_THLD)

[WKFET\\_AMP\\_THLD](#) (see p. 118) determines the voltage threshold at which the weak-FET operation is entered based on the amplitude of the rectified buffered audio signal when the automatic weak-FET drive is enabled (WKFET\_AMP\_EN = 1). If the audio amplitude is below the user-configurable weak-FET threshold for a long enough period of time, the amplifier enters a state of weak-FET drive operation. Otherwise, the Class D amplifier continues to operate using full-drive strength.

If the audio exceeds the configured WKFET\_AMP\_THLD the amplifier immediately exits weak-FET drive operation in order to support the larger output power delivery to the load.

#### 4.4.2.3 Weak-FET Drive Entry Delay (WKFET\_AMP\_DLY)

[WKFET\\_AMP\\_DLY](#) (see p. 119) controls the delay (in ms) before the amplifier switches to the weak-FET drive (after the audio envelope falls and remains below the amplitude specified in WKFET\_AMP\_THLD). Note that WKFET\_AMP\_DLY timings are quantized using a 1-ms clock, which can result in the actual timing being off from the configured timing by 1 ms.

The WKFET\_AMP\_DLY can be configured to produce a timing requirement (up to 1000 ms) to allow the user to avoid continual transitions in and out of weak-drive operation when around a zero crossing points of content within the audio band, while still taking advantage of the power savings of weak-drive operation during quiet audio passages.

#### 4.4.2.4 Manual Weak-FET Drive Force (WKFET\_AMP\_FRC and WKFET\_AMP\_FRC\_EN)

The Class D amplifier's switching output stage can be manually forced into a weak-drive operation for low power or idle operation by using [WKFET\\_AMP\\_FRC](#) (see p. 119) and [WKFET\\_AMP\\_FRC\\_EN](#) (see p. 119). Under normal operation, when weak-FET drive is enabled, any transitions in and out of weak-drive control are handled automatically, based on the audio signal (see [Section 4.4.1](#)).

If WKFET\_AMP\_FRC\_EN is set, the manual control functionality of the WKFET\_AMP\_FRC control is enabled. When enabled, the WKFET\_AMP\_FRC control configures whether the amplifier's power FETs are operating in Weak-FET Mode or normal operation. The Weak-FET Force Mode is intended for purposes of debugging and under most circumstances must be managed by the automatic detection.

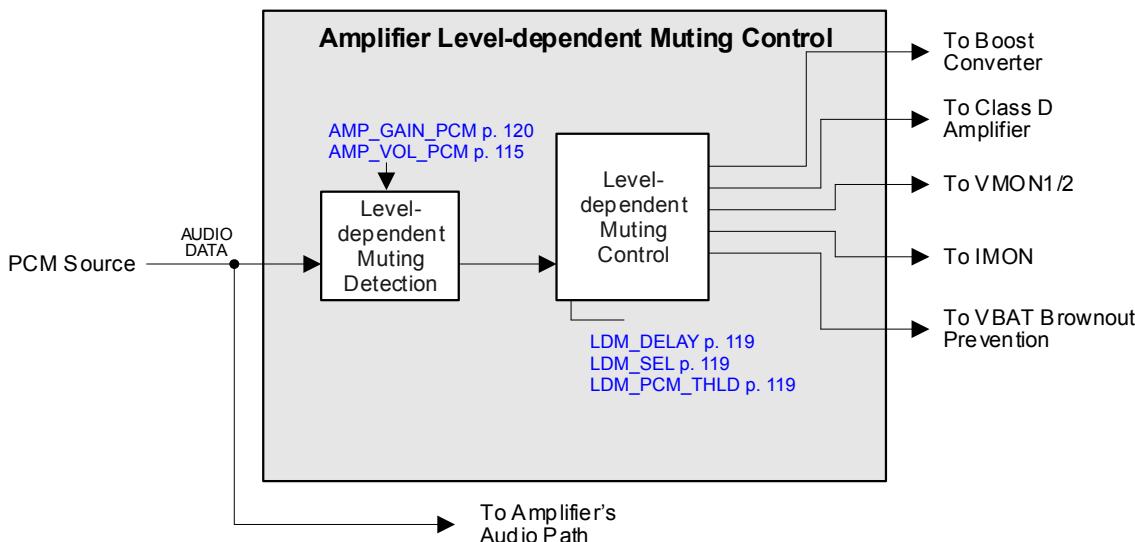
### 4.4.3 Device Level-dependent Muting

The level-dependent muting functionality allows the amplifier to stop switching as well as configure other blocks on the CS35L38A into a low power state in order to reduce power consumption during passages of very low or idle input audio.

LDM\_SEL (see [Section 4.4.3.2](#)) configures whether the level-dependent muting functionality is enabled for any or all of the available functional blocks, including the amplifier. The more functional blocks that are capable of being power-managed by the level-dependent muting, the greater the reduction in device power consumption during idle passages.

The PCM path uses an amplifier output referred amplitude detect source.

Fig. 4-11 shows the audio and data flow through the level-dependent muting control.



**Figure 4-11. Level-dependent Muting Block Diagram**

#### 4.4.3.1 Level-dependent Muting Mode Delay (LDM\_DELAY)

**LDM\_DELAY** (see p. 119) configures the amount of time that the audio signal must be below the LDM\_x\_THLD prior to entering a valid level-dependent muted state. The exit of a level-dependent muted state is immediate upon the detection of an audio signal larger than the LDM\_x\_THLD.

#### 4.4.3.2 Level-dependent Muting Mode/Enable Select (LDM\_SEL)

**LDM\_SEL** (see p. 119) configures which functional blocks are able to be put into a low power operational state when the incoming audio is below the level-dependent muting threshold level for a period of time defined by LDM\_DELAY (see Section 4.4.3.1).

For enabling level-dependent muting on PCM path, level-dependent muting is enabled by setting **LDM\_PCM\_THLD** with the proper value.

When enabled, if the audio is below the LDM\_x\_THLD (see Section 4.4.2.2), the amplifier's outputs stop switching in order to reduce idle channel noise and amplifier power consumption. When the audio is above the LDM\_x\_THLD with an additional 1dB of hysteresis, the amplifier's output will resume switching.

A description of the noise-gating functions controlled by LDM\_SEL are listed in Table 4-16. Amplifier will be level-dependent muted if any other LDM\_SEL bit is set, even if LDM\_SEL = xxxx0. For example, if LDM\_SEL = 001100 when the level-dependent muting condition happens, the VMON1, VMON2 and IMON together with the amplifier will be level-dependent muted to conserve power. Other components will not enter the level-dependent muted state for further power savings.

**Table 4-16. Amplifier Level-dependent Muting Behavior**

<b>LDM_SEL</b>	<b>Level-dependent Muting Control</b>	<b>Behavior Description</b>
000000	Level-dependent muting disabled	All level-dependent muting functionality is disabled. No level-dependent muting behavior occurs.
xxxx1	Amplifier level-dependent muted	When in a valid level-dependent muted state, the amplifier's output (OUTP/N) switching is disabled and the outputs are tied to GND when in a low power state. This eliminates the power consumption of the output switching, produces a state of very low idle channel noise, and a very high PSRR. When the level-dependent muting condition is exited, the amplifier immediately resumes normal OUTP/N operation.

**Table 4-16. Amplifier Level-dependent Muting Behavior (Cont.)**

<b>LDM_SEL</b>	<b>Level-dependent Muting Control</b>	<b>Behavior Description</b>
xxxx1x	Boost converter DCM Mode	When in a valid level-dependent muting condition, the boost converter uses the level-dependent muting signal to trigger entry into a low power DCM Mode of operation. The boost converter uses the exit of a level-dependent muted condition to trigger the boost converter from exiting its low power DCM mode of operation.
xxx1xx	VMON1/2 Low Power Mode	When in a valid level-dependent muted state, the VMON1/2 circuit is put into a low power operational state and the VMON1/2 packet available on the serial port is zero-filled. When the level-dependent muted state is exited, VMON1/2 returns to normal operation.
xx1xxx	IMON Low Power Mode	When in a valid level-dependent muted state, the IMON circuit is put into a low power operational state and the IMON packet available on the serial port is zero-filled. When the level-dependent muted state is exited, IMON returns to normal operation.
x1xxxx	VBAT brownout prevention gating	When in a valid level-dependent muted state the VBAT brownout prevention functionality is disabled. This disables any audio attenuation from occurring when operating in a level-dependent muted state and enables VBATMON ADC to enter a low power state if it is not being used by another functional block (e.g., the boost converter). When the VBAT brownout prevention is disabled by the level-dependent muting it gracefully releases the attenuation as if it were disabled by the user.
111111	All listed blocks level-dependent muted and put in a Low Power Mode	All level-dependent muted power reduction functionality is enabled

#### 4.4.3.3 Level-dependent Muting Interrupt Conditions

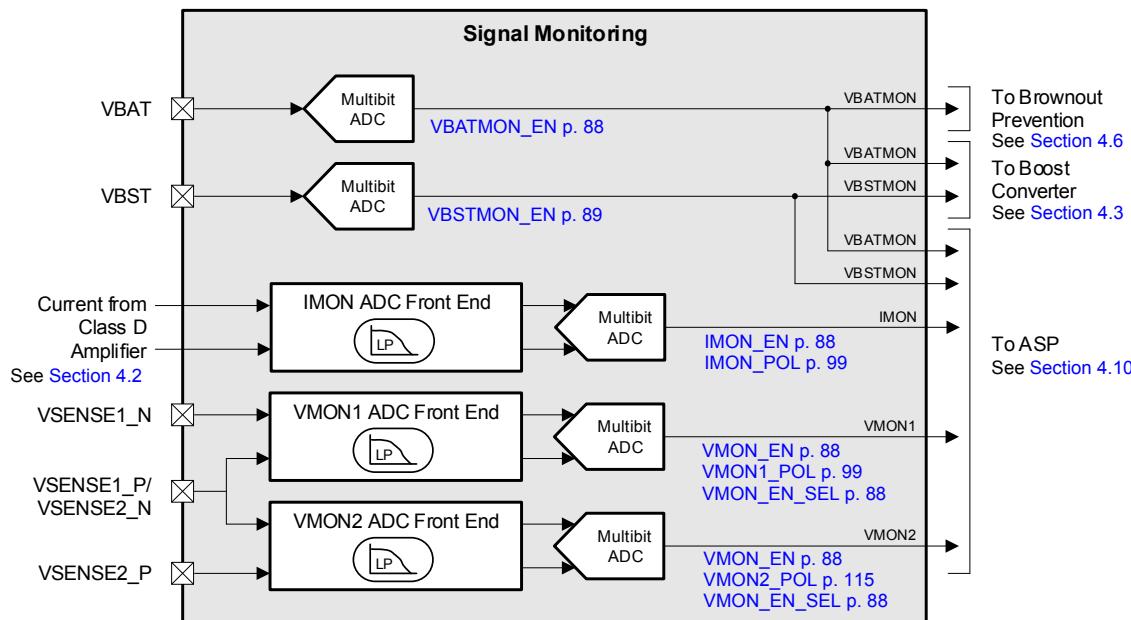
Table 4-17 describes the interrupt status fields that notify the entry and exit of level-dependent muting condition in PCM mode.

**Table 4-17. Level-dependent Muting Interrupt Status Fields**

<b>Cause</b>	<b>Rising-Edge Flag</b>	<b>Interrupt Mask</b>
Notifies when level-dependent muting has been entered. Only valid for PCM audio sources.	<a href="#">LDM_PCM_ON_RISE_EINT</a>	<a href="#">LDM_PCM_ON_RISE_MASK</a>
Notifies when level-dependent muting has been exited. Only valid for PCM audio sources.	<a href="#">LDM_PCM_ON_FALL_EINT</a>	<a href="#">LDM_PCM_ON_FALL_MASK</a>

## 4.5 Signal Monitoring

Signal-monitoring ADCs, shown in [Fig. 4-12](#), give upstream system processors access to important signals entering and exiting the device.



**Figure 4-12. Signal Monitoring Block Diagram**

The signal and supply monitoring is as follows:

- **VBATMON**—Monitors the voltage on the VBAT pin, which is most commonly the battery for the system.
- **VBSTMON**—Monitors the voltage on the VBST pin, which provides the power supply for the high-power output stage of the Class D amplifier.
- **VMON1** and **VMON2**—Monitors the output voltage of the Class D amplifier via the VSENSE1\_N, VSENSE1\_P/ VSENSE2\_N and VSENSE2\_P pins.
- **IMON**—Monitors the current that flows into the load being driven by the Class D amplifier.

An integrated ADC digitizes each of these analog signals, at which point, they can be sent to the system processor using the serial port.

### 4.5.1 Monitoring ADCs Power-Up and Power-Down Bits (xMON\_EN)

The VMON1 and VMON2 ADCs can be powered down by a combination of [VMON\\_EN](#) and [VMON\\_EN\\_SEL](#). Table 4-18 describes how these bits interact.

**Table 4-18. Enable Control for VMON1 and VMON2**

VMON_EN	VMON_EN_SEL	Function
0	x	VMON1 and VMON2 disabled
1	0	VMON1 enabled, VMON2 disabled
1	1	VMON1 and VMON2 enabled

The IMON ADC can be powered down by the [IMON\\_EN](#) bit (see [p. 88](#)). IMON\_EN is also dependent on [AMP\\_EN](#) being set.

The VBATMON and VBSTMON ADCs are required for operation of the VBAT brownout prevention, the digital boost converter, and external supply monitoring via the audio serial port (ASP). When VBAT brownouts are enabled, the VBATMON block is automatically powered up to support device operation and needs to be manually configured for usage.

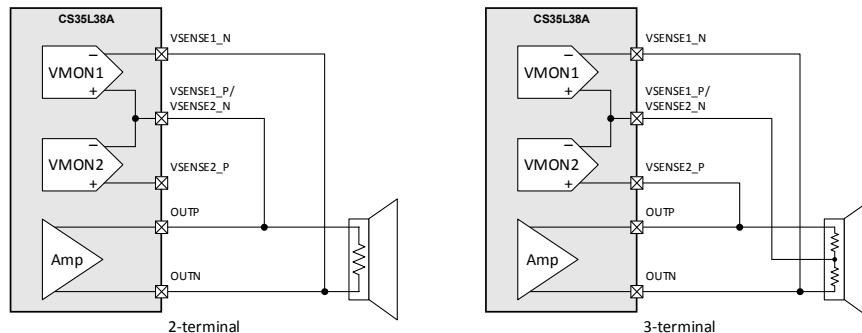
Setting the **VBATMON\_EN** and **VBSTMON\_EN** bits (see p. 89) ensures that they are powered up for purposes of serial port monitoring when no other subblock is requesting their use. Clearing **VBATMON\_EN** and **VBSTMON\_EN** does not ensure that the blocks are powered down. Other functionality on the CS35L38A may require these blocks to remain powered up and operational. For example, operation of the brownout prevention blocks may require that one or both of the supply monitoring ADCs be powered up.

The **VBATMON** and **VBSTMON** will be powered up automatically by function blocks that require them to be activated. Setting **VBATMON\_EN**, **VBATBR\_EN**, or **BST\_EN = 10** will power up **VBATMON** automatically. Setting **VBSTMON\_EN**, **BST\_EN**, or **AMP\_EN** will power up **VBSTMON** automatically.

#### 4.5.2 Monitoring Voltage across the Load—VMON1 and VMON2

As shown in Fig. 4-12, VMON1 monitoring is accomplished via the **VSENSE1\_P/VSENSE2\_N** and **VSENSE1\_N** pins, while VMON2 monitoring is accomplished via the **VSENSE2\_P** and **VSENSE1\_P/VSENSE2\_N** pins. For proper monitoring of the voltage across the load, the sense lines must be connected as close to the load as possible and with as little impedance between the load and the connection point as possible to reduce stray signals from coupling on to the traces. The operating and performance specifications for these ADC paths are given in Table 3-10.

The VMON1 and VMON2 ADCs can be used to measure the voltage across a standard 2-terminal speaker, or a 3-terminal speaker with the center tap. The enable controls for the VMON1 and VMON2 ADCs are described in Section 4.5.1, and the VMON1 and VMON2 outputs can be transmitted from the ASP using the PCM Transmit controls described in Section 4.10.2. The required connections to both types of load are shown in Fig. 4-13.



**Figure 4-13. Recommended connections – 2 and 3 terminal speakers**

When using 12 bits of VMON data, use Eq. 4-3 to convert  $D_{OUT}$  to voltage (in Volts), where  $D_{OUT}$  is the 12-bit digital output monitoring word in two's complement binary format (-2048 to +2047).

$$VMON = \left( \frac{D_{OUT}}{2^{11} - 1} \right) \times 12.3$$

**Equation 4-3. VMON Voltage Calculation—12 Bits**

When using 16 bits of VMON data, use Eq. 4-4 to convert  $D_{OUT}$  to voltage (in Volts), where  $D_{OUT}$  is the 16 bit digital output monitoring word in two's complement binary format (-32,768 to +32,767).

$$VMON = \left( \frac{D_{OUT}}{2^{15} - 1} \right) \times 12.3$$

**Equation 4-4. VMON Voltage Calculation—16 Bits**

When using 24 bits of VMON data, use Eq. 4-5 to convert  $D_{OUT}$  to voltage (in Volts), where  $D_{OUT}$  is the 24 bit digital output monitoring word in two's complement binary format (-8,388,608 to +8,388,607).

$$VMON = \left( \frac{D_{OUT}}{2^{23} - 1} \right) \times 12.3$$

**Equation 4-5. VMON Voltage Calculation—24 Bits**

Relative to VSENSE\_1P or VSENSE2\_P, negative D<sub>OUT</sub> values equate to a negative load voltage and positive D<sub>OUT</sub> values equate to a positive load voltage (assuming VMON\_POL = 1, which is default).

#### 4.5.3 Monitoring Current through the Load—IMON

The IMON load current monitoring circuitry on the CS35L38A is integrated on the IC. The operating and performance specifications for this ADC path are given in [Table 3-10](#).

When using 12 bits of IMON data, use [Eq. 4-7](#) to convert D<sub>OUT</sub> to current (in Amps), where D<sub>OUT</sub> is the 12-bit digital output monitoring word in two's complement binary format (-2048 to +2047).

$$\text{IMON} = \left( \frac{D_{\text{OUT}}}{2^{11} - 1} \right) \times 2.1$$

**Equation 4-6. IMON Current Calculation—12 Bits**

When using 16 bits of IMON data, use [Eq. 4-7](#) to convert D<sub>OUT</sub> to current (in Amps), where D<sub>OUT</sub> is the 16-bit digital output monitoring word in two's complement binary format (-32,768 to +32,767).

$$\text{IMON} = \left( \frac{D_{\text{OUT}}}{2^{15} - 1} \right) \times 2.1$$

**Equation 4-7. IMON Current Calculation—16 Bits**

When using 24 bits of IMON data, use [Eq. 4-8](#) to convert D<sub>OUT</sub> to current (in Amps), where D<sub>OUT</sub> is the 24 bit digital output monitoring word in two's complement binary format (-8,388,608 to +8,388,607).

$$\text{IMON} = \left( \frac{D_{\text{OUT}}}{2^{23} - 1} \right) \times 2.1$$

**Equation 4-8. IMON Current Calculation—24 Bits**

Relative to IMON, negative D<sub>OUT</sub> values equate to a negative current and positive D<sub>OUT</sub> values equate to a positive current (assuming IMON\_POL = 1, which is default).

#### 4.5.4 Monitoring Voltage on the VBAT Pin—VBATMON

Monitoring of the voltage present on the VBAT pin is integrated internally to the CS35L38A. The operating specifications for this ADC path are given in [Table 3-10](#).

Use [Eq. 4-9](#) to convert D<sub>OUT</sub> to VBAT voltage (in Volts), where D<sub>OUT</sub> is the 10-bit digital output monitoring word in unsigned decimal format (0 to 1023).

$$\text{VBAT} = \frac{D_{\text{OUT}} \times 6.087}{1024}$$

**Equation 4-9. VBAT Voltage Calculation**

#### 4.5.5 Monitoring Voltage on the VBST Pin—VBSTMON

Monitoring of the voltage present on the VBST pin is integrated internally to the CS35L38A. The operating specifications for this ADC path are given in [Table 3-10](#).

Use [Eq. 4-10](#) to convert D<sub>OUT</sub> to VBST voltage (in Volts), where D<sub>OUT</sub> is the 10-bit digital output monitoring word in unsigned decimal format (0 to 1023).

$$\text{VBST} = \frac{D_{\text{OUT}} \times 14.00}{1024}$$

**Equation 4-10. VBST Voltage Calculation**

#### 4.5.6 Data Transmission out of the CS35L38A

All of the signals that are monitored in the CS35L38A can be transmitted to the system processor via the serial port. The serial port transmit is described in [Section 4.10.1](#). The data is presented on these outputs simultaneously.

#### 4.5.7 Speaker Monitoring Polarity (xMON\_POL)

The [VMON1\\_POL](#), [IMON\\_POL](#) (see [p. 99](#)) and [VMON2\\_POL](#) (see [p. 115](#)) bits allow the user to change the polarity of the speaker monitoring data relative to the amplifier's output signal and relative to each other. VMON1\_POL and VMON2\_POL should be set to the same value when using both VMON1 and VMON2 (i.e. when monitoring a 3-terminal speaker).

#### 4.5.8 Signal Monitoring Fault/Error Conditions

The CS35L38A monitors each monitoring ADC for overflow conditions. If any of the monitoring signals overflows (see [p. 123](#)) is set, and, if the respective mask bit is cleared, an interrupt occurs. The error condition is exited when the signal is no longer overflowing.

[Table 4-19](#) describes the signal monitoring error conditions.

**Table 4-19. Signal Monitoring Error Status Fields**

Raw Status Flag	Cause	Rising-Edge Flag	Interrupt Mask
<a href="#">VMON_CLIP_STS</a>	The VMON1 ADC has overflowed.	<a href="#">VMON_CLIP_EINT</a>	<a href="#">VMON_CLIP_MASK</a>
<a href="#">VMON2_CLIP_STS</a>	The VMON2 ADC has overflowed.	<a href="#">VMON2_CLIP_EINT</a>	<a href="#">VMON2_CLIP_MASK</a>
<a href="#">IMON_CLIP_STS</a>	The IMON ADC has overflowed.	<a href="#">IMON_CLIP_EINT</a>	<a href="#">IMON_CLIP_MASK</a>
<a href="#">VBATMON_CLIP_STS</a>	The VBATMON ADC has overflowed.	<a href="#">VBATMON_CLIP_EINT</a>	<a href="#">VBATMON_CLIP_MASK</a>
<a href="#">VBSTMON_CLIP_STS</a>	The VBSTMON ADC has overflowed.	<a href="#">VBSTMON_CLIP_EINT</a>	<a href="#">VBSTMON_CLIP_MASK</a>

##### 4.5.8.1 Overflow for the Monitoring Signals

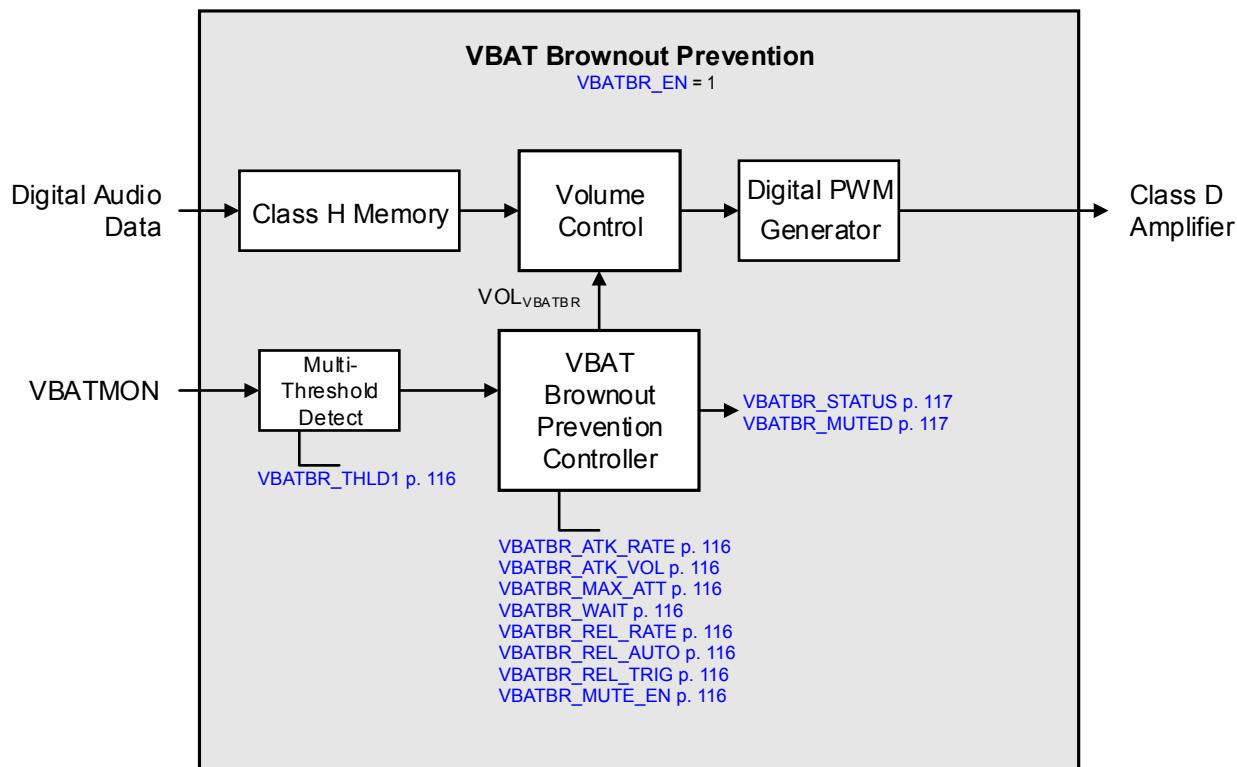
Due to the analog prescaling applied to the analog input signals, an overflow condition is unlikely to occur on these ADCs. This is because the operating specifications for maximum and minimum voltage constrain the voltage on these pins to a level far below what would be required to make the ADC overflow.

Before using VBATMON or VBSTMON status registers properly, it is possible that a spurious overflow error can occur when the block is taken out of power down. For this reason it is advised to clear the error status registers after xMON\_EN and GLOBAL\_EN have been set in order to clear any spurious errors from the status registers.

### 4.6 VBAT Brownout Prevention

The VBAT brownout prevention block is used to prevent the battery (VBAT) supply from drooping to a dangerously low level by rapidly reducing the amplifier loading from the system when an error occurs. The amplifier loading is decreased by lowering the audio amplitude. This reduces the demands on the VBAT to minimize the risk of brownout the system when the battery is in a weakened condition.

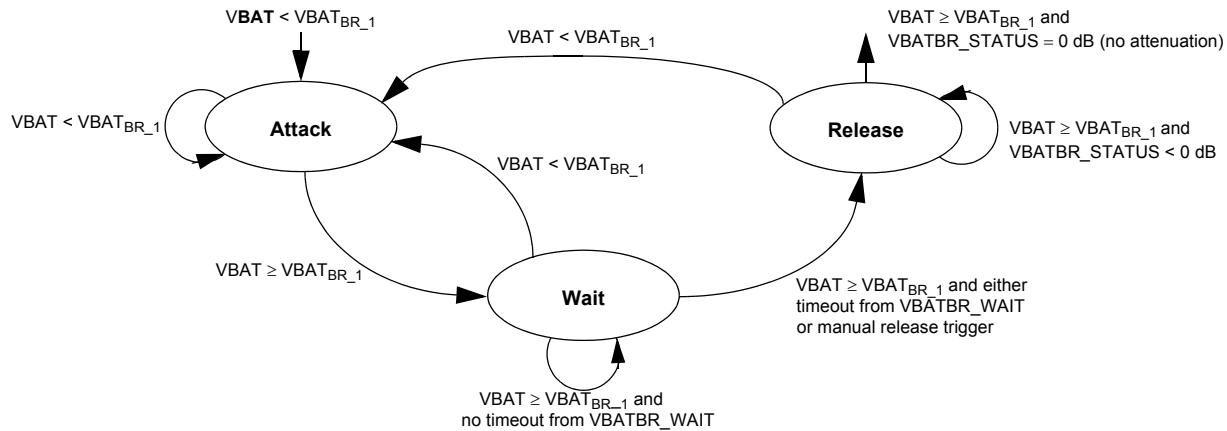
The VBAT brownout prevention, shown in [Fig. 4-14](#) monitors VBAT supply voltage, and if it drops below an initial user-configured threshold, a response is triggered to attenuate the audio signal. The purpose of this block is to rapidly reduce the loading on the VBAT supply when the voltage drops to a low enough level, where it is at risk for a brownout condition.



**Figure 4-14. VBAT Brownout Prevention Overview**

The VBAT brownout prevention continually monitors the VBAT voltage through the VBATMON supply monitoring (Section 4.5.4) block.

There are three main states to the VBAT brownout prevention block: attack, wait, and release. Fig. 4-15 provides a state diagram for the VBAT brownout prevention.

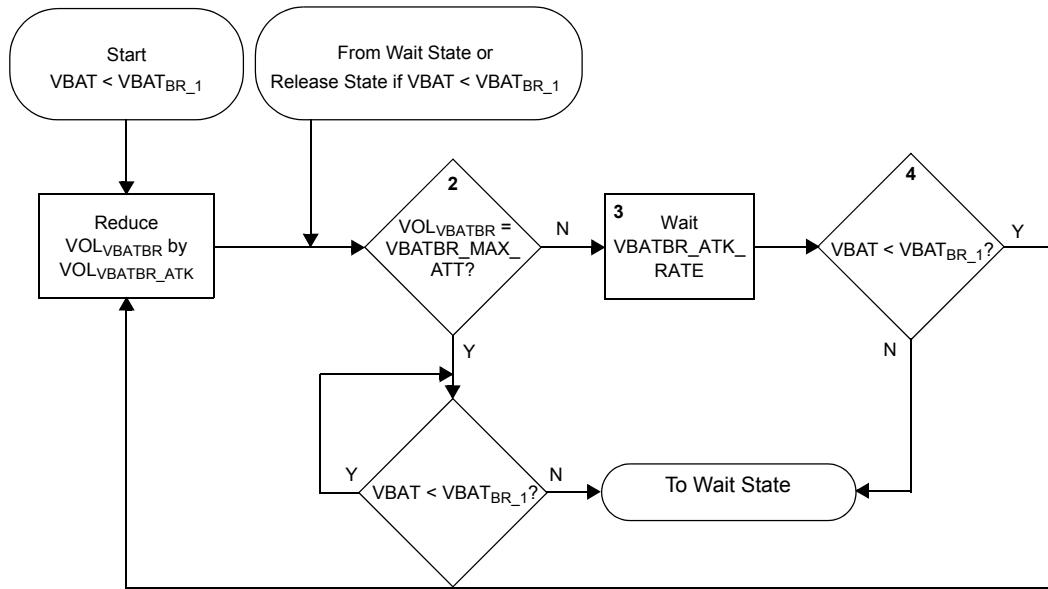


**Figure 4-15. VBAT Brownout Prevention State Diagram**

The attack state is when the measured VBAT voltage has violated the initial threshold voltage ( $VBAT_{BR\_1}$ ). This triggers an error condition (VBATBR\_EINT, see p. 122) and the audio volume is digitally attenuated to rapidly reduce the device power consumption due to the audio loading. The initial threshold voltage is set using VBATBR\_THLD1 (see p. 116). The VBAT threshold is described in more detail in Section 4.6.2.1.

If the VBAT supply voltage remains below  $VBAT_{BR\_1}$ , the digital volume is continually reduced by a volume step size of  $VOL_{VBATBR\_ATK}$  at a time rate of  $t_{VBATBR\_ATK}$  until reaching the attenuation limit, as configured by  $VBATBR\_MAX\_ATT$ . If the VBAT voltage continues to fall below  $VBAT_{BR\_2}$  or  $VBAT_{BR\_3}$ , justifying a more aggressive response, the  $VOL_{VBATBR\_ATK}$  volume step size is automatically increased, as described in [Section 4.6.2.2](#).

A flowchart of the brownout prevention attack state and a description of its stages are shown in [Fig. 4-16](#).



**Figure 4-16. Attack State Flowchart**

If the brownout prevention error condition clears, the wait state is entered. The wait state allows the supply voltage to settle and possibly recover after the reduction in audio loading that was produced by reducing the volume during the attack state. If the error remains cleared for a time,  $t_{VBATBR\_WAIT}$ , the controller exits the wait state and enters the release state. If at any time the brownout prevention error returns, the controller exits the wait state and returns to the attack state.

#### 4.6.1 VBAT Brownout Prevention Enable (VBATBR\_EN)

The VBAT brownout prevention block can be enabled using the [VBATBR\\_EN](#) bit (see [p. 89](#)). The brownout block must be enabled for action to be taken when either of the supplies' voltage falls below the user configured threshold.

If [VBATBR\\_EN](#) is cleared to disable the functionality while attenuation is being applied, the attenuation is first completely released prior to the VBATBR functionality being disabled. When disabled, the attenuation is automatically released back to 0 dB at the configured release rate ([VBATBR\\_REL\\_RATE](#)). The attenuation release on power-down occurs independent of the [VBATBR\\_REL\\_AUTO](#) configuration (see [Section 4.6.2.8](#)).

Enabling the VBAT brownout prevention automatically enables the VBATMON ADC.

#### 4.6.2 VBAT Brownout Prevention Voltage Thresholds

The VBAT brownout prevention threshold configuration is determined by monitoring the absolute VBAT supply voltage relative to the audio signal. This brownout prevention block utilizes a multi-threshold approach in order to minimize the over-attenuation which can often occur with a single threshold response.

The initial response thresholds  $VBAT_{BR\_1}$  are configured by the user (see [Section 4.6.2.1](#)). The second and third brownout thresholds are based on deltas from the user configured VBAT thresholds (refer to [Table 3-12](#)). As the voltage drop from the initial threshold becomes larger, so does the attenuation step size response.

No brownout settings should be changed while in error conditions and audio attenuation is present or the signal is being muted.

#### 4.6.2.1 VBAT Brownout Prevention Initial Voltage Threshold (VBATBR\_THLD1)

The VBAT brownout prevention initial voltage threshold, [VBATBR\\_THLD1](#) (see p. 116), configures the VBAT supply voltage at which the VBAT brownout initially starts responding ( $V_{BATBR\_1}$ ). If the VBAT supply voltage falls below the configurable threshold, an error condition is triggered and the VBAT brownout responds by entering an attacking state.

#### 4.6.2.2 Brownout Prevention Attack Volume/Gain (VBATBR\_ATK\_VOL)

The VBAT brownout prevention attack volume step sizes are configurable via [VBATBR\\_ATK\\_VOL](#) (see p. 116).

The  $VOL_{VBATBR\_ATK}$  responses are listed for each of the voltage thresholds in the [Table 4-20](#).

The VBATBR\_ATK\_VOL configures the amplitude of the attenuation step for each of the three VBAT voltage thresholds. During an attacking phase, the reactive VBAT brownout's volume response per step period is controlled by the configurable VBATBR\_THLD1 and two other preconfigured threshold ranges. This multithreshold approach allows the attenuation response to scale with how far below that user-configurable threshold the VBAT voltage has dropped.

The multithreshold approach has advantages over a single threshold approach. It reduces the overcorrection that can occur with a larger fixed-amplitude response when triggered by a marginal condition, while still allowing for a more aggressive response when the voltage supply conditions dictate it to be necessary. If the VBAT voltage is right at the VBATBR\_THLD1 voltage and the brownout prevention response triggers a drop in power consumption, the supply voltage can quickly recover, potentially creating a situation where the volume transitions back and forth between an error and non error conditions with a larger corrective step. The multithreshold approach is designed to reduce this repetitive pumping pattern of attacking and releasing which can occur with single threshold solutions.

**Table 4-20. Volume Attack Step Size**

VBATBR_ATK_VOL	VOL <sub>VBATBR_1</sub> Attack Attenuation (dB/step)	VOL <sub>VBATBR_2</sub> Attenuation (dB/step)	VOL <sub>VBATBR_3</sub> Attenuation (dB/step)
000	0.0625	0.125	0.250
001	0.125	0.250	0.500
010	0.250	0.500	1.000
011	0.500	1.000	2.000
100	0.750	1.500	3.000
101	1.000	2.000	4.000
110	1.250	2.500	5.000
111	1.500	3.000	6.000

#### 4.6.2.3 Brownout Prevention Attack Rates (VBATBR\_ATK\_RATE)

The attack rate register field, [VBATBR\\_ATK\\_RATE](#) (see p. 116), configures the time between consecutive VBAT brownout prevention volume attenuation adjustments when an error condition remains present. The attack rate control does not affect the timing of the initial attacking response ( $t_{VBATBR\_1}$ ) when a VBAT brownout prevention error first occurs, only the time between consecutive attacking volume attenuation adjustments ( $t_{VBATBR\_ATK}$ ).

The typical VBATBR\_ATK\_RATE times are based on  $f_{PLL\_OUT} = 192$  MHz. The VBATBR\_ATK\_RATE configurations can have a  $\pm 1\ \mu s$  time period error per step relative to their typical configured value. When using an  $f_{PLL\_OUT}$  other than 192 MHz, the step timings scale by 192 MHz/ $f_{PLL\_OUT}$ . For more information on the different  $f_{PLL\_OUT}$  frequencies, refer to [Section 4.9](#).

The VBATBR\_ATK\_RATE, when combined with the dynamic nature of the Digital Mode's multithreshold VOL<sub>VBATBR\_ATK</sub> response, allows the VBAT brownout prevention response to be easily tuned for a variety of reactions based on the power supply characteristics of the end system.

#### 4.6.2.4 Brownout Prevention Max Attenuation (VBATBR\_MAX\_ATT)

The VBAT brownout prevention maximum attenuation allows the user to control the maximum attenuation that the VBAT brownout can apply to the audio signal. Even if an error condition remains present, the brownout prevention only attenuates the audio signal up to the limit configured by VBATBR\_MAX\_ATT. The [VBATBR\\_MAX\\_ATT](#) attenuation (see p. 116) limit is configurable in increments of 1 dB, from 1 dB up to 15 dB.

#### 4.6.2.5 Brownout Prevention Mute Enable (VBATBR\_MUTE\_EN)

During the attack state, if the error volume attenuation has reached VBATBR\_MAX\_ATT with the error condition still present, the audio is muted if the [VBATBR\\_MUTE\\_EN](#) bit (see [p. 116](#)). The audio remains muted until the error condition has cleared and the brownout prevention enters a releasing state.

The VBATBR\_MUTE\_EN must not be changed after an error condition has occurred and audio attenuation is present or the signal is being muted.

#### 4.6.2.6 Brownout Prevention Release Volume Steps (VOL<sub>VBATBR\_REL</sub>)

The digital volume attenuation produced from a reactive VBAT brownout prevention error condition is released at a step size of 0.0625 dB/period (VOL<sub>VBATBR\_REL</sub>). The small steps minimize any audio pumping effects or audio transients that can occur with larger volume step sizes.

#### 4.6.2.7 Brownout Prevention Release Rates (VBATBR\_REL\_RATE)

[VBATBR\\_REL\\_RATE](#) (see [p. 116](#)) configures the time between consecutive VBAT brownout prevention volume attenuation adjustments ( $t_{VBATBR\_REL}$ ) while in the release state and when no error conditions are present for each block.

The typical VBATBR\_REL\_RATE times are based on  $f_{PLL\_OUT} = 192$  MHz. The VBATBR\_REL\_RATE configurations can have a  $\pm 1$  ms time period error per step relative to their typical configured value. When using an  $f_{PLL\_OUT}$  other than 192 MHz, the step timings scale by 192 MHz/ $f_{PLL\_OUT}$ . For more information on the different  $f_{PLL\_OUT}$  frequencies, refer to [Section 4.9](#).

#### 4.6.2.8 Brownout Prevention Automatic Release (VBATBR\_REL\_AUTO)

[VBATBR\\_REL\\_AUTO](#) (see [p. 116](#)) configures whether the VBAT brownout prevention enters a configurable wait state with an automatic release when no error conditions are present or require the user to manually trigger the respective block's release.

When configured for an automatic release (VBATBR\_REL\_AUTO = 1), the VBATBR\_WAIT period (see [Section 4.6.2.8](#)) is used to determine the amount of time the brownout prevention remains in the wait state before releasing. Otherwise, when configured for a manual release (VBATBR\_REL\_AUTO = 0), the brownout prevention remains in the wait state until the VBATBR\_REL\_TRIG is triggered (see [Section 4.6.2.10](#)).

If a VBAT brownout error condition re-occurs while in the wait state, the brownout prevention returns back to the attack state.

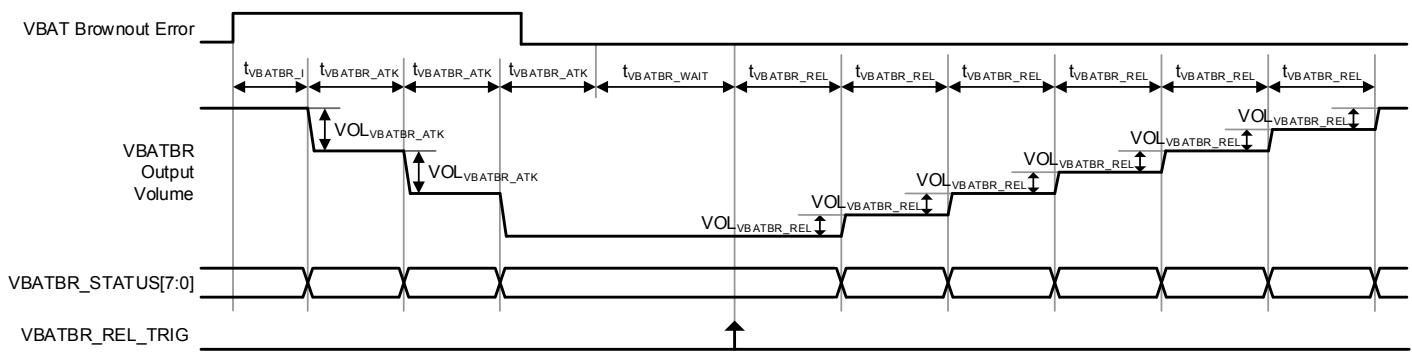
#### 4.6.2.9 Brownout Prevention Automatic Wait (VBATBR\_WAIT)

[VBATBR\\_WAIT](#) (see [p. 116](#)) configures the time ( $t_{VBATBR_WAIT}$ ) after the brownout prevention exits the attack state and no error conditions are present, before automatically proceeding to the release state.

The typical VBATBR\_WAIT times are based on  $f_{PLL\_OUT} = 192$  MHz. The VBATBR\_WAIT configurations can have a  $\pm 1$  ms time period error relative to their typical configured value. When using an  $f_{PLL\_OUT}$  other than 192 MHz, the step timings scale by 192 MHz/ $f_{PLL\_OUT}$ . For more information on the different  $f_{PLL\_OUT}$  frequencies, refer to [Section 4.9](#).

#### 4.6.2.10 Brownout Prevention Manual Release Trigger (VBATBR\_REL\_TRIG)

When the VBAT brownout prevention is configured for a manual release (VBATBR\_REL\_AUTO = 0), the [VBATBR\\_REL\\_TRIG](#) (see [p. 116](#)) is used to exit the wait state and enter the release state. If the manual release is not triggered and no brownout prevention error is present, the brownout prevention will remain in the wait state as long as it is powered up.



**Figure 4-17. VBAT Brownout Prevention Manual Release**

#### 4.6.2.11 Brownout Prevention Attenuation Status (VBATBR\_STATUS)

**VBATBR\_STATUS** (see p. 117) is a read-only register field that reports how much (if any) attenuation is applied to the audio signal by the VBAT brownout prevention control. The applied attenuation (VOL<sub>VBATBR</sub>) value is rounded up to the nearest 0.0625 dB increments when reported by the VBATBR\_STATUS register field. It reports 0 dB attenuation when no audio attenuation is being applied by the brownout prevention.

#### 4.6.2.12 Brownout Prevention Mute Status (VBATBR\_MUTE\_STATUS)

If the VBATBR\_MUTE\_EN option (Section 4.6.2.5) is enabled and the VBAT brownout prevention has muted the audio, the **VBATBR\_MUTED** (see p. 117) is set, indicating that the audio has muted.

#### 4.6.2.13 Brownout Prevention Error Conditions and Attenuation Clear

If a VBAT brownout prevention error occurs, the **VBATBR\_EINT** (on p. 122) flag is set. Once the error condition has cleared and any attenuation that has been applied has cleared and returned to 0 dB, the **VBATBR\_ATT\_CLR\_EINT** (see p. 122) flag is set indicating that attenuation is no longer being applied to the amplifier's audio.

Alternatively, the total attenuation being applied can be streamed out of the system by monitoring the **ERR\_VOL** from the serial port. The **ERR\_VOL** reports the combination of the attenuation from either and/or both blocks being applied to the audio stream.

### 4.6.3 VBAT Brownout Prevention Fault/Error Conditions

Table 4-21 describes the available errors for the VBAT brownout prevention.

**Table 4-21. VBAT Brownout Prevention Error Status Fields**

Raw Status Flag	Cause	Rising-Edge Flag	Interrupt Mask
<b>VBATBR_STS</b>	VBAT voltage has fallen below the brownout threshold and triggered a VBAT brownout response.	<b>VBATBR_EINT</b>	<b>VBATBR_MASK</b>
<b>VBATBR_ATT_CLR_STS</b>	Any attenuation applied due to a VBAT brownout event has been removed.	<b>VBATBR_ATT_CLR_EINT</b>	<b>VBATBR_ATT_CLR_MASK</b>

## 4.7 Device- and System-Level Error Protection

In addition to the block-level error protections (such as short detection, over/under voltage, or clocking protection), the CS35L38A contains a (system-level) input signal-based watchdog and die temperature protection.

The DC input watchdog monitors the incoming PCM input signal to determine if the input has been “stuck” above an amplitude threshold, effectively creating a DC output to the load for an extended period of time. The DC output error protection is described further in Section 4.7.1.

Die temperature monitoring prevents the CS35L38A from overheating by optionally reducing output power. If the die temperature exceeds the maximum operational range (as specified in [Table 3-3](#) and [Table 3-13](#)), operation of the device is shutdown to protect itself from physical damage. The overtemperature warning and error protections are described further in [Section 4.7.2](#).

## 4.7.1 Amplifier DC Input Watchdog Protection

The CS35L38A contains an input signal-monitoring watchdog that, when enabled, triggers an error condition if the incoming signal has remained above a user-configurable threshold for a duration of time. This indicates to the CS35L38A that the input source has become “stuck” and a DC signal has been applied to the load for an extended period of time, potentially posing a risk to the load itself. If an error condition is triggered, an interrupt is reported (see [Section 4.7.1.5](#)) and the response of the CS35L38A hardware is configurable (see [Section 4.7.1.4](#)).

### 4.7.1.1 DC Input Watchdog Enable (DCIN\_WD\_EN)

The DC input watchdog enable [DCIN\\_WD\\_EN](#) (see [p. 121](#)) configures if the watchdog is enabled and actively monitoring input audio signal. While [DCIN\\_WD\\_EN](#) is set and the watchdog is enabled, if the digital input signal provided to the amplifier exceeds [DCIN\\_WD\\_THLD](#) (see [Section 4.7.1.2](#)) for a duration of time [DCIN\\_WD\\_DUR](#) (see [Section 4.7.1.3](#)), a DC input watchdog error occurs and the CS35L38A responds as configured by [WD\\_MODE](#) (see [Section 4.7.1.4](#)).

The DC input watchdog detection monitors the signal prior to any high-pass filtering within the CS35L38A and is not impacted by the configuration of [AMP\\_HPF\\_PCM\\_EN](#) (see [Section 4.2.4](#)).

If the [DCIN\\_WD\\_EN](#) is cleared while an error event occurs, disabling the watchdog, any behavior applied by the DC-input watchdog is also cleared and the CS35L38A resumes normal operation.

### 4.7.1.2 DC Input Threshold (DCIN\_WD\_THLD)

[DCIN\\_WD\\_THLD](#) (see [p. 121](#)) configures the amplitude of the digital input signal that must be maintained for a configurable duration of time (see [Section 4.7.1.3](#)).

[DCIN\\_WD\\_THLD](#) is configured relative to the full-scale digital input signal in from 0.025•FS to 1•FS in 0.025•FS steps. To convert this to an output-referred DC voltage, the unloaded full-scale output voltage (defined by [AMP\\_GAIN\\_PCM](#), see [Table 4-5](#)) should be scaled by the threshold set by [DCIN\\_WD\\_THLD](#). Any digital volume control applied by [AMP\\_VOL\\_PCM](#) should also be taken into account.

**Example:**

- [AMP\\_GAIN\\_PCM](#) = +18 dB → [Table 4-5](#) provides an unloaded full-scale output of 10.98Vpk.
- [AMP\\_VOL\\_PCM](#) = -0.25 dB → can be expressed as a ratio:  $10^{(-0.25/20)} = 0.9716$
- If [DCIN\\_WD\\_THLD](#) is set for a threshold of 0.05•FS, the output-referred threshold is calculated as:

$$0.05 \cdot 0.9716 \cdot 10.98 = 0.5334 \text{ Vdc}$$

### 4.7.1.3 DC Input Signal Duration (DCIN\_WD\_DUR)

[DCIN\\_WD\\_DUR](#) (see [p. 121](#)) configures the time duration that the amplifier’s selected input signal must violate the [DCIN\\_WD\\_THLD](#) prior to triggering an error condition. [DCIN\\_WD\\_DUR](#) must not be changed while [DCIN](#) watchdog is enabled and has been triggered.

The signal magnitude must remain above [DCIN\\_WD\\_THLD](#) for the configured time duration. If the signal falls below the [DCIN\\_WD\\_THLD](#) or changes polarity, the duration timer is reset.

### 4.7.1.4 DC Input Watchdog Response Mode (WD\_MODE)

When a DC input watchdog error occurs, an interrupt is reported and the CS35L38A responds based on the configuration of the [WD\\_MODE](#), described in [Table 4-22](#).

**Table 4-22. Watchdog Response Modes**

WD_MODE	Amplifier Operational State	Interrupts
00	Amplifier continues normal operation regardless of error state.	
01 or 10	Reserved.	
11	A digital PCM volume mute is applied (see <a href="#">Section 4.2.2.1</a> ). Any soft ramping into or out of the digital PCM volume mute is governed by the configuration of AMP_RAMP_PCM (see <a href="#">Section 4.2.2.2</a> )	DCIN_ERR_EINT triggered on error (if unmasked)

The operational states of the signal and supply monitoring (see [Section 4.5](#)) are not impacted by the DC input watchdog and will continue to report what is being measured to the ASP (see [Section 4.11](#)) during an error condition.

#### 4.7.1.5 DC Input Watchdog Fault/Error Conditions

[Table 4-23](#) describes the available errors for the DC input watchdog.

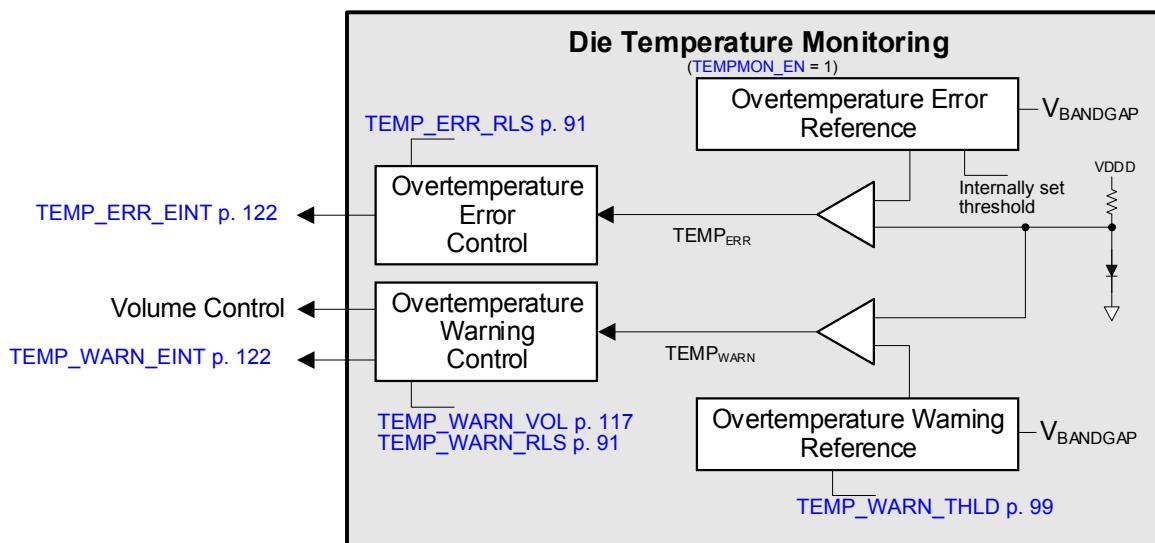
**Table 4-23. DC Input Watchdog Status Fields**

Cause	Raw Status Flag	Rising-Edge Flag	Interrupt Mask
DCIN_ERR_STS	The DC input watchdog has detected an error.	DCIN_ERR_EINT	DCIN_ERR_MASK

#### 4.7.2 Die Temperature Monitoring

Onboard monitoring of the die temperature is integrated to prevent the CS35L38A from reaching a temperature that would compromise reliability or functionality. The CS35L38A incorporates a two-threshold thermal-monitoring system. When die temperature exceeds the lower threshold, an overtemperature warning event occurs (see [Section 4.7.2.2](#)); if it exceeds the second threshold, an overtemperature error condition occurs (see [Section 4.7.2.3](#)).

The controls for the temperature monitoring are shown in [Fig. 4-18](#).


**Figure 4-18. Die Temperature Monitoring Block**

##### 4.7.2.1 Temperature Monitoring Enable (TEMPMON\_EN)

The CS35L38A supports independently enabling or disabling the temperature monitoring via [TEMPMON\\_EN](#) (see p. 89). The temperature monitoring can be enabled when operating in a low power mode. However, whenever the boost converter, amplifier, or IMON signal monitoring are enabled and operating the temperature monitoring is automatically enabled for purposes of thermal protection. The boost converter and amplifier contain large FETs to various supplies and GND. If the die is operating outside of the specified operational temperature (see [Table 3-3](#)) and in a thermal error condition, the boost converter and amplifier are not allowed to become active for purposes of device and system level protection.

#### 4.7.2.2 Die Temperature Overtemperature Warning

An overtemperature warning event occurs when the die temperature exceeds the threshold set by [TEMP\\_WARN\\_THLD](#) (see p. 99). The programmable die temperature thresholds are described in [Table 3-13](#). When the die temperature exceeds the programmed threshold, an TEMP\_WARN event is registered in the interrupt status and, if TEMP\_WARN\_MASK = 0, INT is asserted.

In addition to TEMP\_WARN being set and the interrupt pin being asserted (if the error is not masked), additional protection attempts to limit further increases in die temperature. This is done by applying a programmable attenuation to the program material being amplified. [TEMP\\_WARN\\_VOL](#) (see p. 117) is provided to program how much attenuation is applied to the signal. The amplifier's audio attenuation is applied in accordance with the AMP\_RAMP\_PCM when operating in PCM mode.

There are two ways to remove the attenuation applied during an overtemperature warning event. One is for the temperature to drop below the level set by TEMP\_WARN\_THLD with a 10°C hysteresis margin and to toggle [TEMP\\_WARN\\_RLS](#) (see p. 91). The other is to clear TEMP\_WARN\_VOL.

To exit the error condition, the die temperature must drop below the threshold set by TEMP\_WARN\_THLD with a 10°C hysteresis margin and the release bit, TEMP\_WARN\_RLS, must be sequenced.

#### 4.7.2.3 Die Temperature Overtemperature Error

An overtemperature error event occurs when the CS35L38A die temperature exceeds the error threshold shown in [Table 3-13](#). If the die temperature exceeds this threshold, an TEMP\_ERR event is registered in the interrupt status register and, if TEMP\_ERR\_MASK = 0, INT is asserted.

On an overtemperature error event, the CS35L38A enters Speaker-Safe Mode, described in [Section 4.2.8](#).

To exit the error condition, the die temperature must drop 10°C below the value in [Table 3-13](#) and the release bit, TEMP\_ERR\_RLS (see p. 91), must be toggled.

#### 4.7.2.4 Die Temperature Monitoring Fault/Error Conditions

[Table 4-24](#) describes the error status fields associated with components shown in [Fig. 4-18](#). The overtemperature error and warning fault conditions are described in more detail in the previous sections.

**Table 4-24. Die Temperature Monitoring Error Fields**

Raw Status Flag	Cause	Rising-Edge Flag	Interrupt Mask
<a href="#">TEMP_WARN_STS</a>	The CS35L38A die temperature has exceeded the warning threshold set by <a href="#">TEMP_WARN_THLD</a> .	<a href="#">TEMP_WARN_EINT</a>	<a href="#">TEMP_WARN_MASK</a>
<a href="#">TEMP_ERR_STS</a>	The CS35L38A die temperature has exceeded the error threshold.	<a href="#">TEMP_ERR_EINT</a>	<a href="#">TEMP_ERR_MASK</a>

### 4.8 Dynamic Range Enhancement (DRE)

The CS35L38A features dynamic range enhancement (DRE), adjusting the digital volume and analog amplifier gain in order optimize dynamic range performance on the Class D amplifier in PCM Mode.

If AMP\_DRE\_EN is cleared, the DRE is disabled and the CS35L38A is operating with a fixed analog gain and a fixed noise floor as described in [Section 4.2.5](#).

When the AMP\_DRE\_EN is set and the DRE is enabled, the analog gain and digital volume compensation are automatically managed. The configuration of the AMP\_GAIN\_PCM determines the maximum full-scale amplifier output voltage ( $V_{AMP\_FS}$ ), not the actual analog gain. When disabled, the AMP\_GAIN\_PCM configures the actual analog gain.

The goal of the DRE is to maintain as low of an analog gain as possible in order to always operate in a state with the lowest achievable noise floor, based on the audio signal to be output from the amplifier. The digital volume is synchronously adjusted to compensate for a change in analog gain so that the total audio path amplification remains constant.

#### 4.8.1 Dynamic Range Enhancement Enable (AMP\_DRE\_EN)

The Dynamic Range Enhancement (DRE) is enabled using the [AMP\\_DRE\\_EN](#) (see p. 89). When enabled, the analog gain and digital volume compensation are automatically managed.

**Note:** PCM digital volume gain AMP\_VOL\_PCM (see [Section 4.2.2](#)) should not be set to a value higher than +3.5 dB when DRE is enabled.

The DRE uses the AMP\_GAIN\_PCM (see [Section 4.2.5.1](#)) to determine the maximum allowable analog gain for the DRE. This allows the user to limit the maximum output signal in hardware. Turning on and off the DRE does not change the maximum output signal produced by the amplifier, it only manages the noise. Turning off the DRE always returns to operating with a fixed gain as determined by the AMP\_GAIN\_PCM.

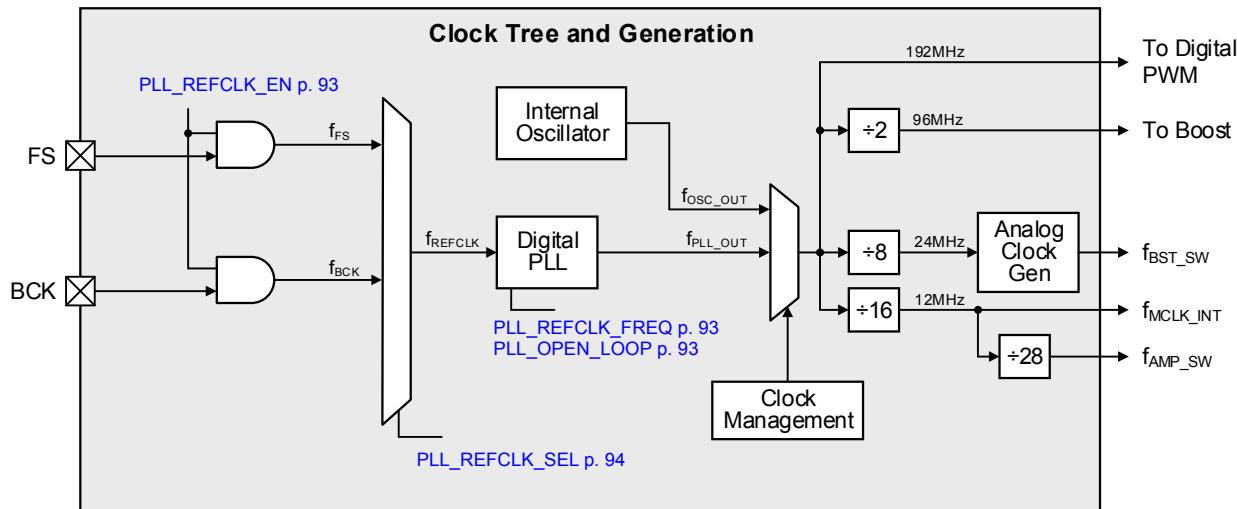
When enabled, the minimum analog gain is determined based on the incoming audio signal and the available amplifier gain range ( $A_{V\text{-MIN}}$ ) as specified in [Table 3-4](#).

### 4.9 Device Clocking and Reference Clock Configurations

The CS35L38A allows the user to select from the audio serial port clocks (BCK, FS), an input reference clock. This input reference clock is presented to the input of a digital PLL where it is then up-converted for use throughout the device.

#### 4.9.1 Input Reference Clock

The CS35L38A requires an input reference clock when outputting audio. As shown in [Fig. 4-19](#), the reference clock can be selected from one of multiple input audio source clocks.



**Figure 4-19. Digital PLL and Clocking Tree**

##### 4.9.1.1 Input Reference Clock Selection (PLL\_REFCLK\_SEL)

The [PLL\\_REFCLK\\_SEL](#) (see p. 94) selects the input reference clock from which the digital PLL generates its output frequency. This input reference clock can be from the serial port's FS or BCK when operating in Slave Mode.

##### 4.9.1.2 Input Reference Clock Enable (PLL\_REFCLK\_EN)

When cleared, the [PLL\\_REFCLK\\_EN](#) (see p. 93) disables some of the input reference clocks from being clocked into the PLL. This allows the user to reduce the power consumption of the device when a clock is present on the system, but the CS35L38A is not being used and is intended to be in a low power state when RST is not asserted.

For example, if a TDM serial port bus is shared between multiple devices, the BCK and FS may be present while the CS35L38A is powered down. Clearing the [PLL\\_REFCLK\\_EN](#) minimizes the amount of logic being toggled by the activity on the data bus.

#### 4.9.1.3 PLL Operational Mode (PLL\_OPEN\_LOOP)

The [PLL\\_OPEN\\_LOOP](#) (see p. 93) configures whether the PLL is running open-loop or closed-loop. The PLL must be configured to operate in open loop whenever the REFCLK input source is changing, the REFCLK frequency is changing, or a REFCLK is not available. If it detects that the REFCLK is not available, the PLL will automatically operate in open loop mode.

Operating in open loop is not recommended when any audio is being played through the amplifier.

#### 4.9.1.4 PLL Unlock Flag (PLL\_UNLOCK\_EINT)

The [PLL\\_UNLOCK\\_EINT](#) (see p. 124) indicates that the PLL has transitioned from locked to unlocked. Once initial lock has been achieved, this flag is set when the user manually configures the PLL to operate in open loop mode (see [Section 4.9.1.3](#)) or if the REFCLK input is removed.

#### 4.9.1.5 PLL Input Reference Clock Frequency (PLL\_REFCLK\_FREQ)

The [PLL\\_REFCLK\\_FREQ](#) (see p. 93) must be configured to match the input frequency present at the selected REFCLK source to the CS35L38A (see [Section 4.9.1.1](#) for REFCLK input selection).

[Table 4-25](#) lists the supported REFCLK input frequencies and the associated PLL\_REFCLK\_FREQ configurations available on the CS35L38A. Although functionally supported, the use of some REFCLK frequencies will operate at a reduced audio output performance. These reduced performance REFCLK rates are also included in [Table 4-25](#).

**Table 4-25. Input Reference Clock (REFCLK) Configurations and  $f_{PLL\_OUT}$  Frequency**

PLL_REFCLK_FREQ	REFCLK Input Frequency (kHz) <sup>1</sup>	Generated $f_{PLL\_OUT}$ (MHz)	PLL_REFCLK_FREQ	REFCLK Input Frequency (kHz)	Generated $f_{PLL\_OUT}$ (MHz)
000000	32.768	196.6080	...	100000	3000
000001	8	196.6080	...	100001	3072
000010	11.025	180.6336	...	100010	3200
000011	12	196.6080	...	100011	4000
000100	16	196.6080	...	100100	4096
000101	22.05	180.6336	...	100101	4800
000110	24	196.6080	...	100110	5644.8
000111	32	196.6080	...	100111	6000
001000	44.1	180.6336	...	101000	6144
001001	48	196.6080	...	101001	6250
001010	88.2	180.6336	...	101010	6400
001011	96	196.6080	...	101011	6500
001100	128	196.6080	...	101100	6750
001101	176.4	180.6336	...	101101	7526.4
001110	192	196.6080	...	101110	8000
001111	256	196.6080	...	101111	8192
010000	352.8	180.6336	...	110000	9600
010001	384	196.6080	...	110001	11289.6
010010	512	196.6080	...	110010	12000
010011	705.6	180.6336	...	110011	12288
010100	750	192.0000	...	110100	12500
010101	768	196.6080	...	110101	12800
010110	1000	192.0000	...	110110	13000
010111	1024	196.6080	...	110111	13500
011000	1200	192.0000	...	111000	19200
011001	1411.2	180.6336	...	111001	22579.2
011010	1500	192.0000	...	111010	24000
011011	1536	196.6080	...	111011	24576
011100	2000	192.0000	...	111100	25000
011101	2048	196.6080	...	111101	25600
011110	2400	192.0000	...	111110	26000
011111	2822.4	180.6336	...	111111	27000

1. REFCLK input frequencies between 8 kHz and 768 kHz and at 6.25 MHz, 6.5 MHz, 6.75 MHz, and 12.5 MHz are functionally supported, but will operate at a reduced audio performance. Full operational performance as is specified in [Table 3-4](#) and [Table 3-5](#).

[Table 4-25](#) shows the relationship between  $f_{PLL\_OUT}$  and the amplifier's output switching frequency ( $f_{AMP\_SW}$ ), boost converter's output switching frequency ( $f_{BST\_SW}$ ), and internal MCLK frequency ( $f_{MCLK\_INT}$ ). All register configurable timings which are based in  $\mu$ s or ms are relative  $f_{PLL\_OUT} = 192.0$  MHz and scale as indicated by the time period scalar.

**Table 4-26.  $f_{PLL\_OUT}$  to Amplifier, Boost Converter, and Internal MCLK Clocking Conversions**

Configured $f_{PLL\_OUT}$ (MHz)	Amplifier $f_{AMP\_SW}$ (kHz)	Boost Converter $f_{BST\_SW}$ (MHz)	Internal MCLK $f_{MCLK\_INT}$ (MHz)	Time period scalar
180.6336	403.2	1.882	11.2896	1.063
192.0000	428.6	2.000	12.000	1.000
196.6080	438.9	2.048	12.288	0.977

## 4.9.2 Device Global Sample Rate (GLOBAL\_FS)

The device level sample rate is configured using the [GLOBAL\\_FS](#) (see p. 94) control. Internally, the amplifier's audio data path and monitoring data path share a common sample rate. Externally, the CS35L38A supports a single sample rate for the audio serial port interface (see [Section 4.11](#)). The [GLOBAL\\_FS](#) configures the common sample rate at which these data paths and interfaces operate.

When changing [GLOBAL\\_FS](#) rates with the amplifier powered up, the [AMP\\_MUTE](#) must be set and volume must be cleared prior to changing [GLOBAL\\_FS](#) in order to prevent audio transients while transitioning between different reference clock frequencies.

### 4.9.2.1 Supported PCM Sample Rates and PLL Clocking Configurations

[Table 4-27](#) lists the supported sample rate configurations based on the PLL output frequency ( $f_{PLL\_OUT}$ ). For certain  $f_{PLL\_OUT}$  frequencies there is a subset of supported PCM sample rates available. More information on the PLL output frequency and how it relates to a REFCLK input is in [Section 4.9.1.5](#).

**Table 4-27. Supported Clocking Configurations and Sample Rates**

$f_{PLL\_OUT}$ (MHz)	Sample Rate (kHz)	GLOBAL_FS
180.6336	11.025	01001
	22.050	01010
	44.100	01011
	88.200	01100
	176.400	01101
192.0000	12.000	00001
	24.000	00010
	48.000	00011
	96.000	00100
	192.000	00101
	11.025	01001
	22.050	01010
	44.100	01011
	8.000	10001
	16.000	10010
	32.000	10011

**Table 4-27. Supported Clocking Configurations and Sample Rates (Cont.)**

fPLL_OUT (MHz)	Sample Rate (kHz)	GLOBAL_FS
196.6080	12.000	00001
	24.000	00010
	48.000	00011
	96.000	00100
	192.000	00101
	11.025	01001
	22.050	01010
	44.100	01011
	88.200	01100
	176.400	01101
	8.000	10001
	16.000	10010
	32.000	10011

#### 4.9.2.2 Monitoring Path Sample Rate Reference (SPKMON\_FS\_SEL)

The [SPKMON\\_FS\\_SEL](#) (see p. 94) allows the group delay of the monitoring path to be referenced relative to the audio serial port sample rate. This allows for a deterministic group delay relative to each interface port.

Alternatively, the SPKMON\_FS\_SEL may be configured to reference the audio serial port's sample rate clock or operate in a free-running state.

#### 4.9.3 Clocking Based Fault/Error Conditions

[Table 4-28](#) describes the available errors for the clocking sub-system.

**Table 4-28. Clocking Based Status Fields**

Raw Status Flag	Cause	Rising-Edge Flag	Interrupt Mask
<a href="#">PLL_UNLOCK_STS</a>	The PLL is not locked.	<a href="#">PLL_UNLOCK_EINT</a>	<a href="#">PLL_UNLOCK_MASK</a>

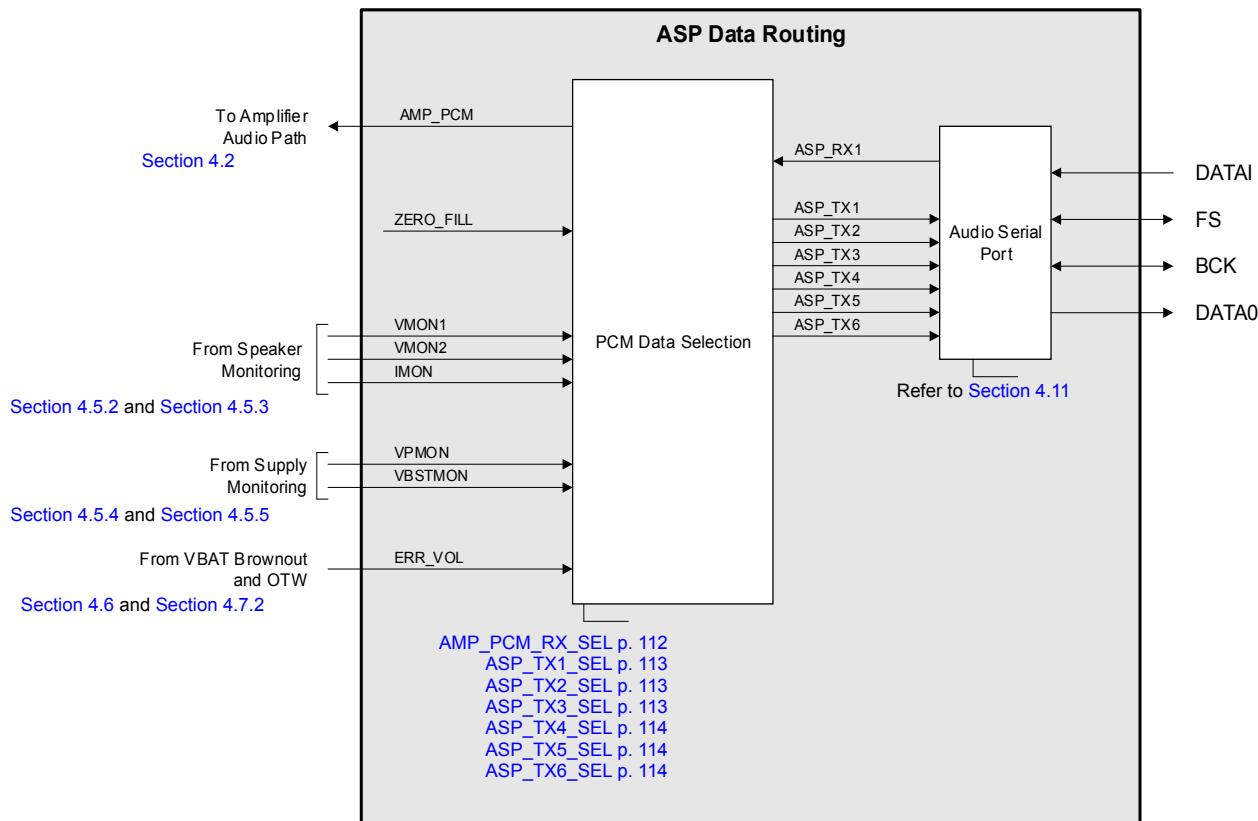
## 4.10 PCM Audio and Monitoring Data Packets and Routing

The CS35L38A contains a PCM data router which allows the user to select how the available PCM based audio and monitoring packets are routed to and from the audio serial port (see [Section 4.11](#)).

[Fig. 4-20](#) shows the PCM routing and selection block. Data to the routing and selection block is provided by the integrated monitoring and the audio serial port RX interface. Data is output from the routing and selection block to the internal amplifier PCM audio path and the audio serial port TX interface.

The available PCM RX data packets which can be provided to the amplifier's PCM path are described in [Section 4.10.1](#).

The available PCM TX data packets which can be provided to the audio serial port described in [Section 4.10.2](#).



**Figure 4-20. Data Selection and Routing Block Diagram**

#### 4.10.1 PCM Receive Data and Routing

The PCM receive path selects from the available PCM audio sources and provides this to the input of the audio amplifier datapath (see [Section 4.2](#)). When the amplifier's audio path is configured to operate in PCM mode, the PCM data selected from the data routing is output from the amplifier.

[Table 4-29](#) lists the available PCM data input sources for the PCM receive path.

**Table 4-29. PCM Receive Data Routing Sources**

Data Input Packet Name	Data Input Source Description	Description Section
ZERO_FILL	Zero fill data	<a href="#">Section 4.10.3</a>
ASP_RX1	Audio Serial Port RX1 channel	<a href="#">Section 4.10.1</a>

[Table 4-30](#) lists the PCM receive path routing control and its default configuration. In addition, the selected receive source must be configured to be active in order to produce an output signal on the amplifier.

**Table 4-30. PCM Receive Data Routing Controls**

Data Output Packet Name	Routing Control	Default Data Packet	Data Source Description
AMP_PCM	<a href="#">AMP_PCM_RX_SEL</a>	ASP_RX1	Up to 24 bits of PCM audio data

#### 4.10.2 PCM Transmit Data and Routing

The CS35L38A is capable of transmitting several different monitoring and status data packets via audio serial port in a PCM format for access by other devices in the system. These data packets are shown in [Table 4-31](#).

The VMON1, VMON2, and IMON packet depths are natively 24 bits wide. Scaling on the serial port allows these to be transmitted at a reduced bit depth (12 or 16-bit). However, at 12-bit performance may be reduced due to data being truncated by the reduced digital data packet depth. This reduction in speaker monitoring performance may be acceptable for some applications, but not for others, requiring an increased data packet depth.

**Table 4-31. PCM Transmit Routing Data**

Data Input Packet Name	Data Input Source Description	Data Section
ZERO_FILL	Zero fill data	<a href="#">Section 4.10.3</a>
VMON1 + VMON2	Amplifier output voltage monitoring	<a href="#">Section 4.5.2</a>
IMON	Amplifier load current monitoring	<a href="#">Section 4.5.3</a>
VBATMON	VBAT supply monitoring	<a href="#">Section 4.5.4</a>
VBSTMON	VBST supply monitoring	<a href="#">Section 4.5.5</a>
ERR_VOL	Combined error volume applied from VBATBR and a thermal warning	—

Under most circumstances the routing configuration of the transmit data packets does not need to be changed from the default selection. The audio serial port provides transmit channel and data packet location flexibility relative to its respective data frames. It is recommended to move transmit packet data around using the respective communication ports.

[Table 4-32](#) lists the available data selection routing controls and defaults for the audio serial port. Although up to 24 bits of data are available for each data packet, not all packets contain 24 bits of active data. For these data packets, the LSBs are zero-filled.

**Table 4-32. PCM Transmit Routing Control—Audio Serial Port**

ASP TX Packet Name	Routing Control	Default Data Packet	Data Source Formatting
ASP_TX1	<a href="#">ASP_TX1_SEL</a>	VMON1	24 bits of data available (see <a href="#">Section 4.5.2</a> and <a href="#">Section 4.5.3</a> )
ASP_TX2	<a href="#">ASP_TX2_SEL</a>	IMON	
ASP_TX3	<a href="#">ASP_TX3_SEL</a>	VBATMON	10-bits of data + LSB zero fill (see <a href="#">Section 4.5.4</a> and <a href="#">Section 4.5.5</a> )
ASP_TX4	<a href="#">ASP_TX4_SEL</a>	VBSTMON	
ASP_TX5	<a href="#">ASP_TX5_SEL</a>	ERR_VOL	
ASP_TX6	<a href="#">ASP_TX6_SEL</a>	ZERO_FILL	All zeros (no dither)

#### 4.10.3 Zero Fill Data Packets

The data router is capable of producing a zero-fill packet which can be provided to both the PCM RX path or the PCM TX path. All 24 bits of the PCM path are zero when in this configuration.

For the receive path, this allows an alternative to the digital mute.

For the transmit path, this allows zeros to be driven for the designated transmit channels for purposes of actively driving DATAO for the selective slot locations as an alternative to operating in a Hi-Z state.

An example of this would be two separate CS35L38A sharing a common DATAO when operating in I<sup>2</sup>S mode where the left channel and right channel are not completely filled with data. This would allow each CS35L38A to maintain zero-fill, maintaining active control of DATAO during its transmit half of the FS period while still allowing the other device's side to operate in a Hi-Z state.

#### 4.11 Audio Serial Port Data Interface

The CS35L38A provides an audio serial port interface (ASP), which receives the serial audio data and transmits multiple channels to monitor device status data. The audio serial port can be configured to operate in either I<sup>2</sup>S or TDM Modes (see [Section 4.11.1](#)). Flexible packet width and slot locations are available in both I<sup>2</sup>S or TDM Modes, as well as serial port bus sharing to support more than two devices on a single serial port bus.

The audio interface data packets can be reconfigured while enabled, including changes to the FS frame length and the data packet slot location configurations. The amplifier must be muted in order to prevent pop and click during the transition and care is required to ensure that any on-the-fly reconfiguration does not cause corruption to the active signal paths. The audio input channel must be disabled (see [Section 4.11.3](#)) prior to changing the serial port format, packing configuration, inversion, or FS frame length.

The serial port interface uses four pins:

- DATAO: serial data output (transmit)
- DATAI: serial data input (receive)
- BCK: serial data bit clock, for synchronization
- FS: left/right or frame synchronization alignment clock

The DATAI and DATAO are a part of a single serial port, sharing the BCK and FS, meaning the DATAI and DATAO always operate at the same bit clock and sample clock rate. The BCK and FS are configurable to operate in Slave Clocking Mode.

The CS35L38A's serial port supports one input receive path (see [Table 4-30](#) in [Section 4.10.1](#)) and eight output transmit paths (see [Table 4-32](#) in [Section 4.10.2](#)). Each input and output signal can be independently enabled or disabled (see [Section 4.11.3](#)). The digital audio interfaces can be configured as slave interfaces

The audio interface formats are described in [Section 4.11.1.1](#). The bit order is MSB-first in each case. Refer to [Table 3-17](#) for signal timing information.

The serial port bus can be shared with other devices capable of supporting a shared I<sup>2</sup>S/TDM bus in any of the ASP\_FMT configurations (see [Section 4.11.1](#)). The options for multichannel operation are described in [Section 4.11.3.1](#).

The serial port provides flexibility to support multiple slots of audio data within each FS sample frame. This flexibility allows multiple audio channels to be supported within a single FS sample frame as described in [Section 4.11.2](#).

Each audio and monitoring/data channel can be enabled or disabled independently using the transmit (TX) and receive (RX) signal paths. For each enabled channel, the PCM data is assigned to one time slot within the FS frame as described in [Section 4.11.2](#) and [Section 4.11.3](#).

The CS35L38A's internal data path is designed to operate with up to 24 bits of receive or transmit audio/data. The serial port is capable of transmitting and receiving up to 24 bits of available data or a reduced number of bits to support lower bandwidth systems (see [Section 4.11.5](#)).

The serial port receives the audio to the amplifier via DATAI on the AMP\_PCM\_RX data packet. This receive data is shown in [Table 4-30](#). The audio input AMP\_PCM\_RX input data packet is available in both I<sup>2</sup>S and TDM Modes. Although the CS35L38A supports audio data packets smaller than 24 bits, audio performance may be reduced due to a reduced quality of digital signal that occurs with the smaller digital audio packet.

Fig. 4-21 shows the block diagram and the configuration controls of the serial port.

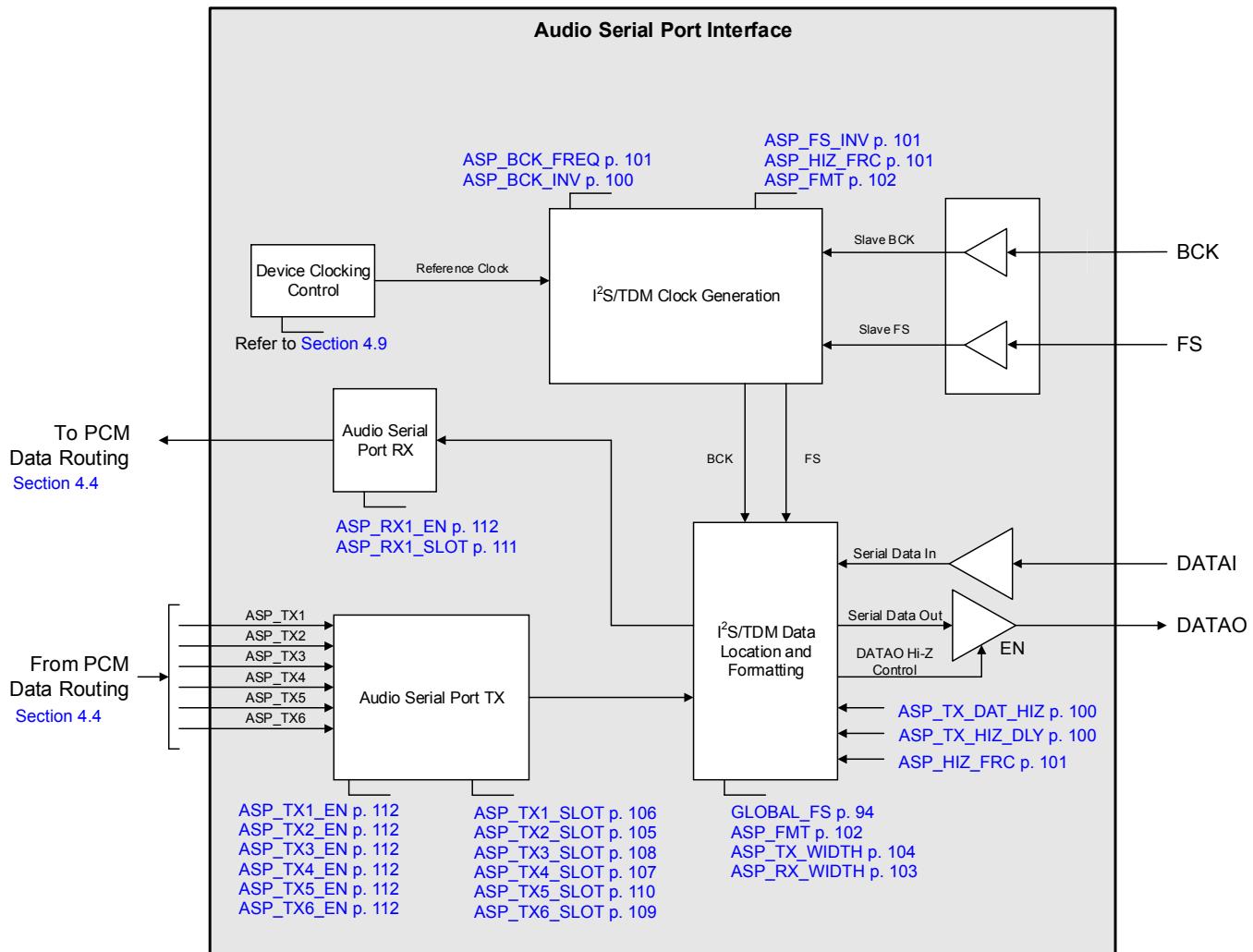


Figure 4-21. Serial Port Block Diagram and Configurations

#### 4.11.1 Audio Serial Port Mode Control and Formatting

The CS35L38A provides a serial port interface, which is capable of receiving the serial audio data and transmitting multiple channels of monitoring and device status data. The data sources for the serial port receive (RX) and transmit (TX) paths can be selected from the available data packets in [Table 4-31](#) in [Section 4.10.2](#).

The following interface format modes are supported on the serial port:

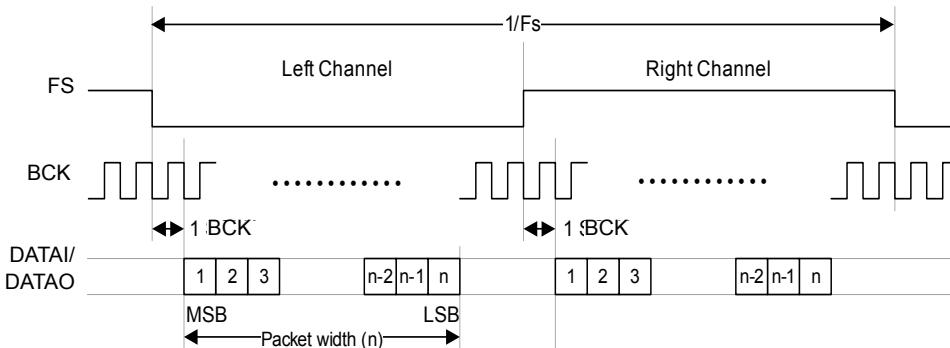
- I<sup>2</sup>S Mode
- TDM 1 Mode
- TDM 1.5 Mode

##### 4.11.1.1 Audio Serial Port Formatting Control (ASP\_FMT)

The serial port formatting mode is configured via **ASP\_FMT** (see [p. 102](#)). The **ASP\_FMT** allows the user to select from I<sup>2</sup>S Mode, TDM 1 Mode, and TDM 1.5 Mode. The difference between TDM Mode 1 and TDM Mode 1.5 is where the MSB data is launched on DATAO and considered valid on DATAI relative to the start of the sample period.

#### 4.11.1.2 Audio Serial Port I<sup>2</sup>S Mode Formatting

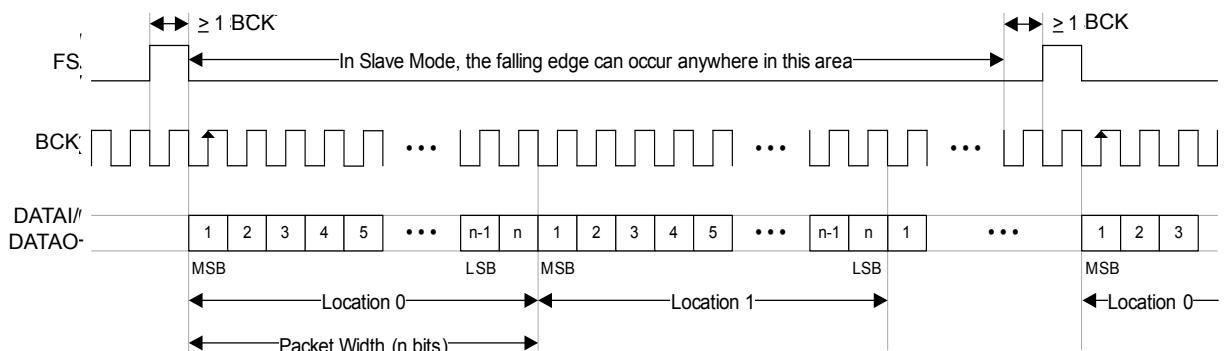
In I<sup>2</sup>S Mode (ASP\_FMT = 010), the MSB is considered valid on the second rising edge of BCK following a FS transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCK frequency, and sample rate, there may be unused BCK cycles between the LSB of one sample and the MSB of the next. I<sup>2</sup>S format is shown in [Fig. 4-22](#). When FS is low, it is considered to be the left channel, and when FS is high, it is considered to be the right channel in I<sup>2</sup>S Mode.



**Figure 4-22. I<sup>2</sup>S Format**

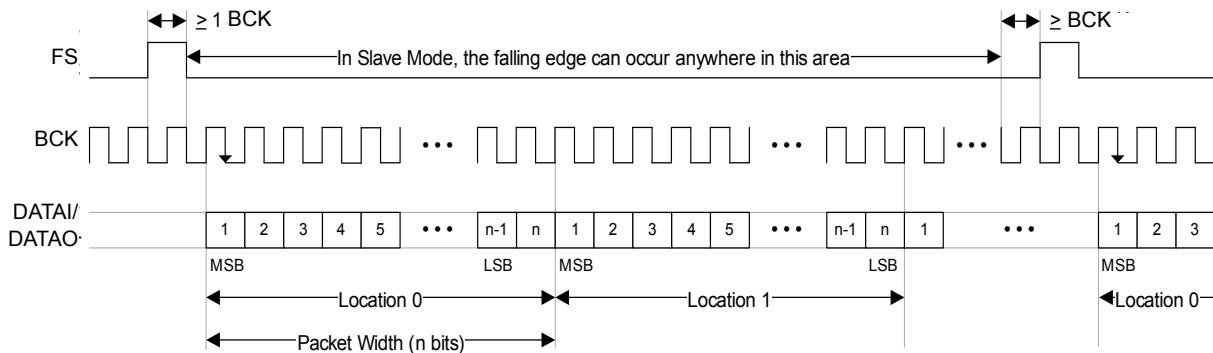
#### 4.11.1.3 Audio Serial Port TDM 1 and 1.5 Mode Formatting

The start of the TDM frame is the first rising edge of BCK after the rising edge of the frame synchronization (FS) pulse. When operating in TDM 1 Mode (ASP\_FMT = 000), the MSB of the first packet for both DATAI and DATAO is valid 1 full BCK period after the start of the frame, as shown in [Fig. 4-23](#). When operating in TDM 1.5 Mode (ASP\_FMT = 100), the MSB of the first packet for both DATAI and DATAO is valid 1.5 BCK periods after the start of the frame, as shown in [Fig. 4-24](#).



**Figure 4-23. TDM 1 Mode Formatting**

In TDM 1.5 Mode ( $\text{ASP\_FMT} = 100$ ), the TDM format with the MSB of DATAI and DATAO valid at 1.5 BCK periods relative to FS is shown in [Fig. 4-24](#). If  $\text{ASP\_BCK\_INV}$  is cleared, the BCK must be inverted relative to [Fig. 4-24](#) when operating in TDM 1.5 Mode operation.



**Figure 4-24. TDM 1.5 Mode Formatting**

In Slave Mode, it is possible to use any length of frame pulse less than  $1/F_s$ , providing the falling edge of the frame pulse occurs at least one BCK period before the rising edge of the next frame pulse.

#### 4.11.2 Audio Serial Port Slot Locations (ASP\_RX1\_SLOT and ASP\_TXn\_SLOT)

The slot locations of the receive and transmit data packets are configurable using the `ASP_RX1_SLOT` and `ASP_TXn_SLOT` registers (see [p. 106](#)). A slot location register is available for each data packet to provide flexible operation in a variety of systems with different communications requirements. A full list of the receive and transmit slot location configurations are available in [Table 4-30](#) and [Table 4-31](#) along with their corresponding data packets and enables.

The orientation of the slot locations varies slightly between I<sup>2</sup>S and TDM Modes of operation and are described further in [Section 4.11.2.1](#) and [Section 4.11.2.2](#).

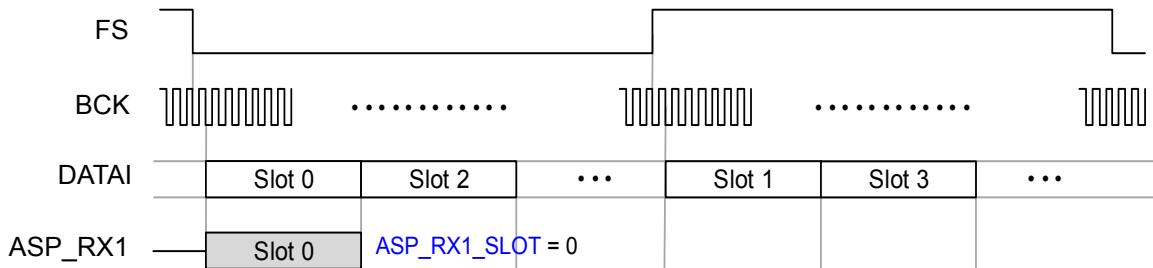
The time slots are assigned independently for the receive (DATAI) and transmit (DATAO) signal paths. There is no requirement to assign every available time slot to an audio sample and slots may be left unused. However, only 1 data packet can be assigned to each slot location and slot locations cannot be assigned to values that are out of bounds based on the number of BCKs per frame.

The number of BCK cycles within a slot is configurable. This number of BCKs is referred to as the slot width. The data word depth is automatically matched to the slot width. The receive slot widths are configured using the `ASP_RX_WIDTH` (see [p. 103](#)). All transmit slot widths are uniform in size and configured using the `ASP_TX_WIDTH` (see [p. 104](#)). For more information on the slot width configurations refer to [Section 4.11.5](#).

##### 4.11.2.1 Audio Serial Port Slot Locations—I<sup>2</sup>S Mode

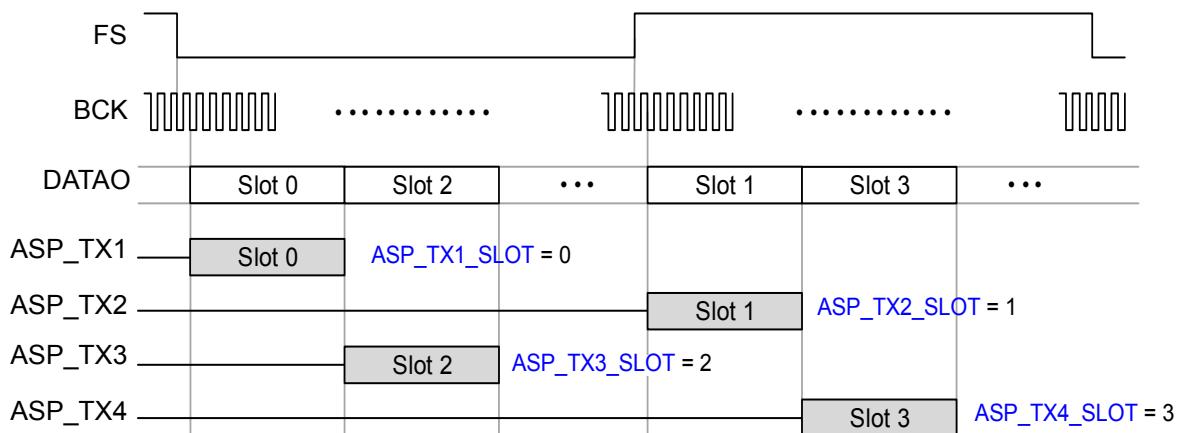
In I<sup>2</sup>S Mode, the even number slot locations reside on the left channel of the I<sup>2</sup>S sample period and the odd number slot locations reside on the right channel of the I<sup>2</sup>S sample period. The slot locations are organized from lowest to highest on each channel, starting with 0 on the I<sup>2</sup>S left data channel and 1 on the I<sup>2</sup>S right data channel.

The CS35L38A only contains one receiving data packet (AMP\_PCM\_RX). Fig. 4-25 shows an example of I<sup>2</sup>S format where the data received is on the left channel. If the CS35L38A needed to receive the data on the first location of the right channel instead of the left channel, [ASP\\_RX1\\_SLOT](#) (see p. 111) must be configured to slot location 1 instead.



**Figure 4-25. I<sup>2</sup>S Receive Slot Configuration Example**

Fig. 4-26 shows a transmitting configuration example when operating in I<sup>2</sup>S Mode. Four data channels are enabled. These are channels allocated to time slots 0 through 3 using their respective [ASP\\_TXn\\_SLOT](#) controls. Slot locations 0 and 2 are located consecutively on the left channel data, and slot locations 1 and 3 are located consecutively on the right channel data of the I<sup>2</sup>S sample period.



**Figure 4-26. I<sup>2</sup>S Transmit Slot Configuration Example**

#### 4.11.2.2 Audio Serial Port Slot Locations—TDM Modes

In the TDM Modes, the slot locations are organized from lowest to highest on each channel, starting with 0 and incrementing consecutively by one slot location until reaching the end of the sample period.

The data formatting of TDM 1 Mode and TDM 1.5 Mode is the same with the exception of the start location of the data. The start of the data frame is shifted a half of a clock cycle between the two modes. This means that slot location 0 starts one half of a BCK period later in TDM 1.5 Mode than in TDM 1 Mode. This shift translates to the start location of each consecutive slot following slot 0.

For more information on the data formatting of TDM 1 Mode and TDM 1.5 Mode refer to [Section 4.11.1.3](#). The examples [Fig. 4-27](#) and [Fig. 4-28](#) refer to TDM 1 Mode. The slot locations are shifted later by one-half clock cycle in TDM 1.5 Mode.

Fig. 4-27 provides a data receive example of TDM 1 Mode receiving the amplifier audio data (AMP\_PCM\_RX) in slot 0 along with the location register configuration.

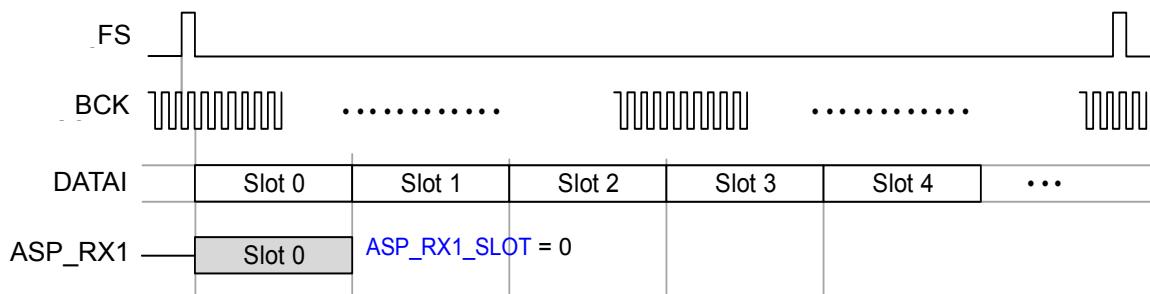


Figure 4-27. TDM 1 Mode Receive Slot Example

Fig. 4-28 provides a data transmit example of TDM 1 Mode using five data channel packets in consecutive slot locations (0–4) with the corresponding register configurations.

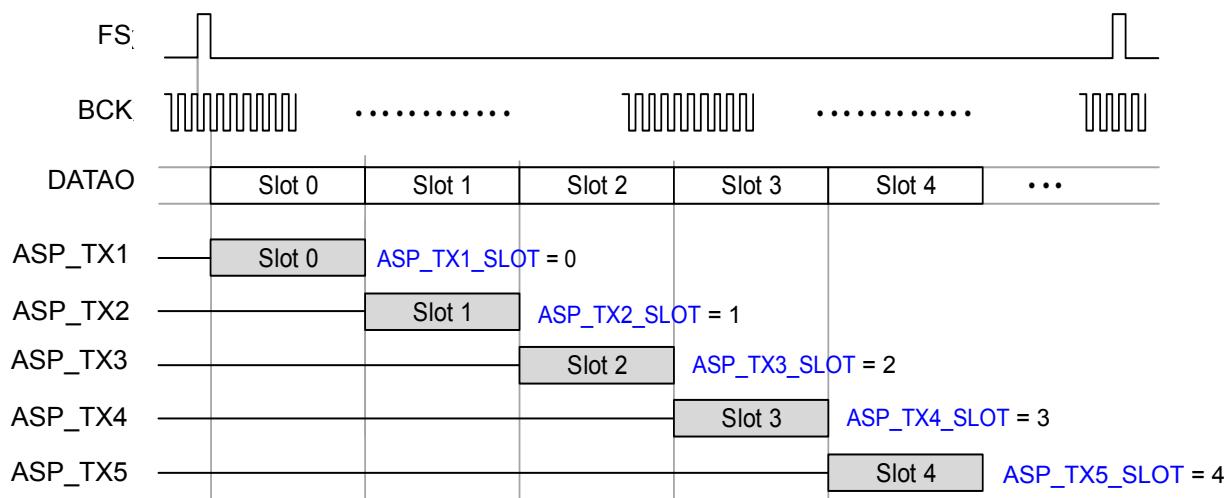


Figure 4-28. TDM 1 Mode Transmit Slot Example

#### 4.11.3 Audio Serial Port Channel Enables (ASP\_RX1\_EN and ASP\_TXn\_EN)

Each receive and transmit data channel has an enable and disable control (ASP\_RX1\_EN and ASP\_TXn\_EN). A full list of the receive and transmit data packets and their corresponding enables are available in Table 4-34. A detailed description of each of the available data packets is available in Table 4-29 and Table 4-31.

When the ASP\_RX1 input audio receive channel is disabled ( $\text{ASP\_RX1\_EN} = 0$ ), the amplifier input receives zero-fill data, regardless of what data is present on the DATAI pin.

When the transmitting channel of a given data packet is disabled, the monitoring or status data is no longer output via the DATAO pin. The state of the `ASP_TX_DAT_HIZ` determines the state of the DATAO for a disabled slot location (see Section 4.11.3.1).

To put the serial port in Low Power Mode, the serial port must be configured in Slave Mode and the `ASP_RX1_EN` and `ASP_TXn_EN` must be configured to disable all channels (see Section 4.11.3).

Table 4-34 lists the channel enable and slot controls for the audio serial port as well as the default data from the PCM data routing block (see Section 4.10).

**Table 4-34. ASP RX and TX Enable, Slot Location, and Routing Select Registers**

Data Packet Name	PCM Routing Source Select	Default Routed Data	ASP Enable Control	ASP Slot Location
ASP_RX1	AMP_PCM_RX_SEL	ASP_RX1 (to amplifier datapath)	ASP_RX1_EN	ASP_RX1_SLOT
ASP_TX1	ASP_TX1_SEL	VMON	ASP_TX1_EN	ASP_TX1_SLOT
ASP_TX2	ASP_TX2_SEL	IMON	ASP_TX2_EN	ASP_TX2_SLOT
ASP_TX3	ASP_TX3_SEL	VBATMON	ASP_TX3_EN	ASP_TX3_SLOT
ASP_TX4	ASP_TX4_SEL	VBSTMON	ASP_TX4_EN	ASP_TX4_SLOT
ASP_TX5	ASP_TX5_SEL	ERR_VOL	ASP_TX5_EN	ASP_TX5_SLOT
ASP_TX6	ASP_TX6_SEL	ZERO_FILL	ASP_TX6_EN	ASP_TX6_SLOT

#### 4.11.3.1 Audio Serial Port Transmit Hi-Z Controls (ASP\_TX\_DAT\_HIZ and ASP\_HIZ\_FRC)

While the CS35L38A is globally powered down (GLOBAL\_EN = 0), the DATAO pin drives low when [ASP\\_HIZ\\_FRC](#) = 0 and remains Hi-Z when [ASP\\_HIZ\\_FRC](#) = 1.

When the CS35L38A is enabled (GLOBAL\_EN = 1) and all transmitting slot are disabled (ASP\_TXn\_EN = 0), the DATAO pin state depends on the [ASP\\_HIZ\\_FRC](#) setting. Setting [ASP\\_HIZ\\_FRC](#) will enforce DATAO to be in a Hi-Z state. Otherwise, the DATAO pin drives low.

When the CS35L38A is enabled (GLOBAL\_EN = 1) and any transmitting slot is enabled (ASP\_TXn\_EN = 1), the DATAO pin state during unused slot locations does not depend on the [ASP\\_HIZ\\_FRC](#) setting any more, but on [ASP\\_TX\\_DAT\\_HIZ](#)'s setting. Setting [ASP\\_TX\\_DAT\\_HIZ](#) will enforce DATAO to be in a Hi-Z state during unused slot locations. Otherwise, the DATAO pin drives low during unused slot locations.

[Table 4-35](#) lists the DATAO behavior and output drive configuration of DATAO when a slot is enabled, disabled, in power-down, and in reset.

**Table 4-35. DATAO Hi-Z and Output Behavior**

RST	GLOBAL_EN	ASP_HIZ_FRC	ASP_TX_DAT_HIZ	ASP_TXn_EN	DATAO Behavior per Given Slot Location
Released	0	0	X	X	Driven Low
	0	0	X	X	
	0	1	X	X	Hi-Z
	0	1	X	X	
	1	0	X	0	Driven Low
	1	1	X	0	Hi-Z
	1	X	0	1	Data output
	1	X	1	1	
Asserted			X		Hi-Z

The Hi-Z configurations allow the serial port to be shared with other devices that are capable of configuring their DATAO pins to a Hi-Z state.

[Fig. 4-29](#) provides an example of a serial port bus being shared between two CS35L38A devices and a host processor. The DATAO output pins from each device can be connected together on a single data line, as when one device is transmitting on DATAO the other is configured to be in a Hi-Z state and vice versa. In order for the DATAO data line to be shared, the transmit slot locations must be configured so that only one of the CS35L38A slot locations are enabled at any one point in time. If no data needs to be transmitted, it is valid for both devices to be Hi-Z at the same time, regardless of if another device or external component is actively driving the bus.

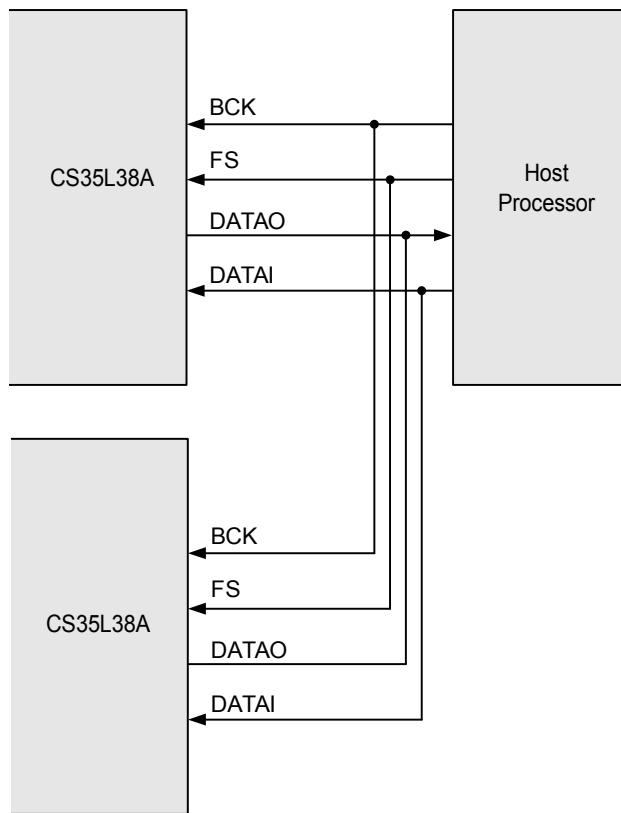


Figure 4-29. Shared Serial Port Bus Example

#### 4.11.4 Audio Serial Port BCK and FS Invert (ASP\_BCK\_INV and ASP\_FS\_INV)

The BCK signal can be inverted in Slave Mode using the [ASP\\_BCK\\_INV](#) bit (see p. 100).

The FS signal can be inverted in Slave Mode using the [ASP\\_FS\\_INV](#) bit (see p. 101).

These bits do not move the location of the DATAI/DATAO data, but simply invert the polarity of the BCK and FS respectively.

#### 4.11.5 Audio Serial Port Slot and Packet Depth (ASP\_RX\_WIDTH and ASP\_TX\_WIDTH)

The serial port packet depth configurations determines both the slot width and the packet size depth of the transmit and receiving data on the serial port. The receiving packet and slot width is configured via [ASP\\_RX\\_WIDTH](#) (see p. 103) and the transmit packet and slot width is configured via [ASP\\_TX\\_WIDTH](#) (see p. 104).

Only the single AMP\_PCM\_RX packet is received by the CS35L38A (see [Table 4-30](#)) via the serial port. Slot width will always match the native packet depth.

The CS35L38A is capable of transmitting multiple monitor and data packets (see [Table 4-31](#)) via the serial port. The serial port can transmit up to 24 bits of monitor data in a single packet.

Not all transmit packets have the same actual data depth though. For example, VMON1, VMON2 and IMON can provide up to 24 bits, but VBATMON, VBSTMON, and ERR\_VOL only contain up to 12-bits of data. If the [ASP\\_TX\\_WIDTH](#) is configured to a value less than 24 bits, the VMON1, VMON2 and IMON data transmit is reduced to the configured packet depth (as described in [Section 4.5.2](#) and [Section 4.5.3](#)).

Conversely, if the [ASP\\_TX\\_WIDTH](#) is configured to a value larger than 12-bits for a 12-bit data packet, the smaller data packets are MSB aligned with the additional LSBs being zero-filled.

#### 4.11.6 Audio Serial Port Sample Rate

The serial port sample rate (FS) is configured via the GLOBAL\_FS control (see [Section 4.9.2](#)).

#### 4.11.7 Additional ASP Data Interface Clock Calibration Steps

The following ASP data interface clock calibration steps are required based on the BCK rate setting. This should be completed after ASP setup is finished and before GLOBAL\_EN is set.

		Address	Data
1	Write:	0x00000020	0x00000055
2	Write:	0x00000020	0x000000AA
3	Write:	0x00002D10	Hex(REG_VALUE) <sup>1</sup>
4	Write:	0x00000020	0x000000CC
5	Write:	0x00000020	0x00000033

1. REG\_VALUE is determined based on [Section 4.11.7.1](#)

##### 4.11.7.1 How to Determine REG\_VALUE

REG\_VALUE is determined based on the comparison of BCK rate in megahertz (BCK\_RATE\_MHz) to the NOM\_6\_MHZ (PLL\_OUT\_FREQ\_MHz/32) rate. PLL\_OUT\_FREQ\_MHz is the PLL output frequency in megahertz.

If BCK\_RATE is greater than NOM\_6\_MHz, then REG\_VALUE = Dec(147472)

If BCK\_RATE is equal to or less than NOM\_6\_MHz, then the following equation is used to determine the value of REG\_VALUE:

$$A = \text{ceiling}(3 \times (4 \times \text{NOM\_6\_MHz} / \text{BCK\_RATE\_MHz})) + 4$$

$$B = \text{ceiling}(5 \times (4 \times \text{NOM\_6\_MHz} / \text{BCK\_RATE\_MHz})) + 4$$

$$\text{REG\_VALUE} = A + B \times 4096$$

### 4.12 Interrupt Reporting

Events and conditions throughout the CS35L38A can be communicated back to an applications processor using any of several reporting mechanisms, each of which are detailed in the following sections.

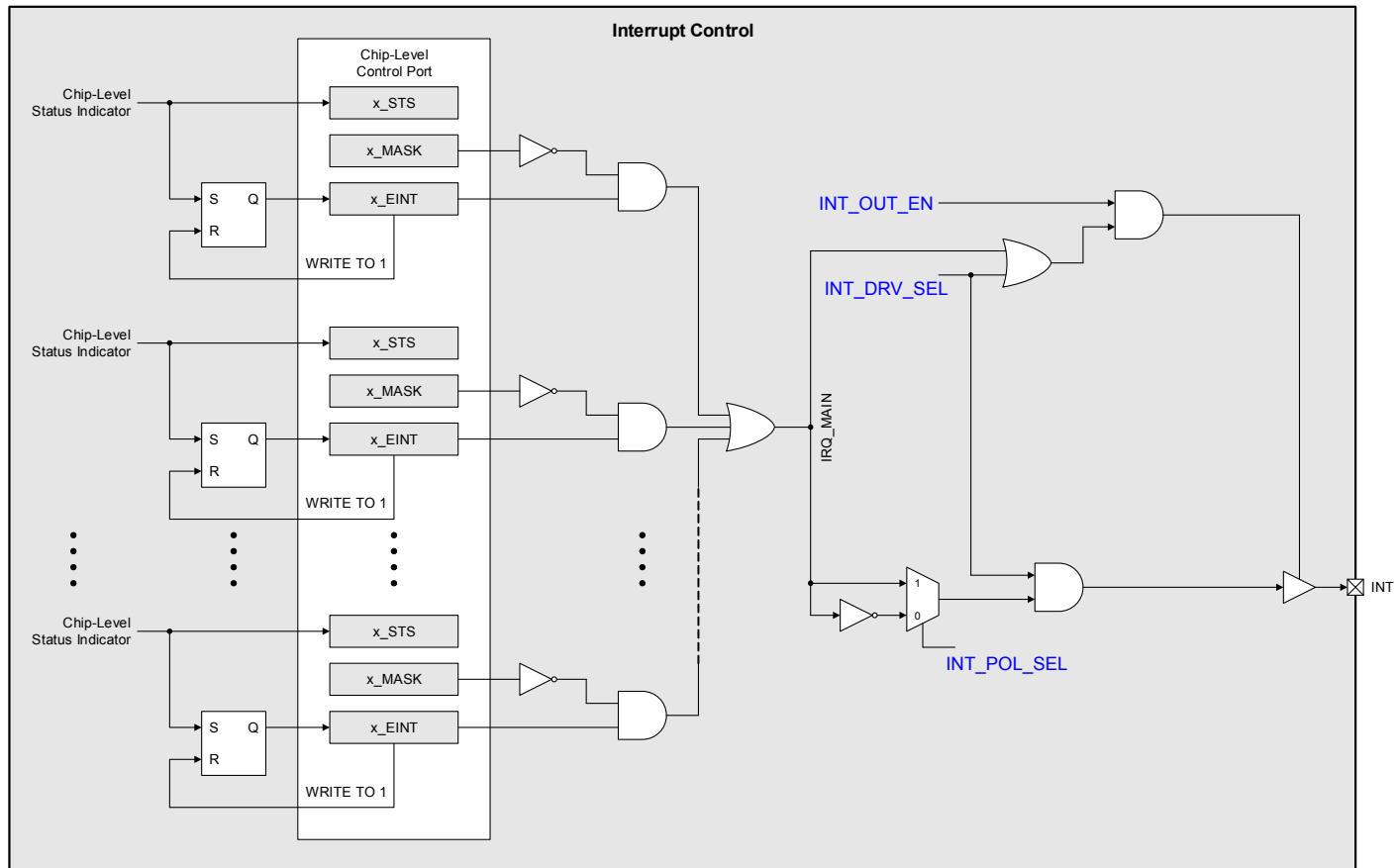
#### 4.12.1 Control-Port Fields

The CS35L38A maps various status indicators, many of which are described throughout [Section 4](#), to control-port fields that can be queried through the I<sup>2</sup>C interface. These read-only fields, appended with \_STS in their name, reflect the raw level of their source in real time.

Due to their dynamic nature, x\_STS fields may be asserted when status is present and subsequently deasserted too quickly after the status is removed. This transient behavior can sometimes happen too quickly to be read from the control port. To assuage this problem, each status indicator is accompanied by a rising-edge “sticky” field that is asserted when its corresponding raw status indicator is first asserted. Each sticky field, appended with \_EINT in its name, remains asserted until written with a one. The sticky nature of these fields allows an applications processor to identify past events or changes in state that have occurred since the last read from the control port.

#### 4.12.2 Programmable Interrupt Outputs

The CS35L38A can assert the interrupt output based on the assertion of one or more x\_EINT sticky fields according to the logic shown in Fig. 4-30.



**Figure 4-30. Interrupt Control**

All sticky fields throughout the CS35L38A are paired with a mask control that gates the associated x\_EINT field to the inputs of an OR gate, the output of which is labeled in Fig. 4-30 as IRQ\_MAIN. If an interrupt source's x\_EINT field is asserted and its associated x\_MASK control is equal to zero, IRQ\_MAIN is asserted internally. Due to the sticky nature of each x\_EINT field, IRQ\_MAIN remains asserted until all offending and unmasked x\_EINT fields have been written with a one. Interrupt sources for which their associated x\_MASK control is equal to one do not affect IRQ\_MAIN.

If the INT\_OUT\_EN control is set (see p. 92) the INT pin is mapped to IRQ\_MAIN. The Class D amplifier must operate with the audio serial port selected as its source (AMP\_PCM\_RX\_SEL = 0x08).

INT can operate as active-low/open-drain, active-low/push-pull or active-high/push-pull outputs. Table 4-36 specifies the appropriate register settings for each configuration.

**Table 4-36. INT Configuration Details**

INT_OUT_EN	INT_DRV_SEL	INT_POL_SEL	Output Selection	Driver Type	Polarity
0	x	x	None	—	—
1	0	0	INT	Open-Drain	Active-Low
1	1	0	INT	Push-Pull	Active-Low
1	1	1	INT	Push-Pull	Active-High

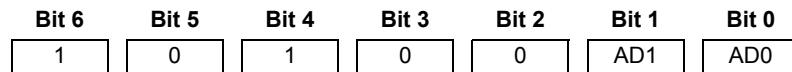
## 4.13 I<sup>2</sup>C Control Port

Control fields and status indicators are organized within the CS35L38A as an array of 32-bit registers to form the device's control port. The control port is accessible over I<sup>2</sup>C. While both interfaces may operate independently and simultaneously, it is recommended that only one interface is used in order to reduce system complexity.

The I<sup>2</sup>C interface can be operated asynchronously to the audio serial port. Furthermore, the I<sup>2</sup>C interface remains available in the absence of the device's selected reference clock, or if GLOBAL\_EN = 0.

### 4.13.1 Device Address

The seven-bit I<sup>2</sup>C slave address for the CS35L38A is defined as follows:



As described in [Section 4.1.1](#), the AD1 and AD0 fields are resolved based on the state of the ADS2 and ADS1 pins upon the deassertion of the RST input.

### 4.13.2 Protocol

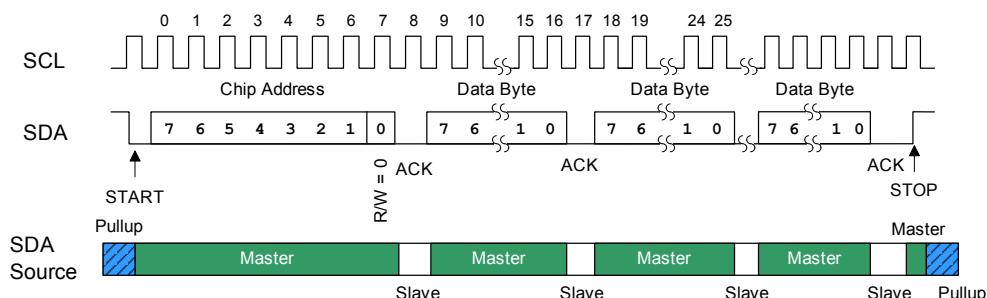
The CS35L38A operates exclusively as an I<sup>2</sup>C slave. To allow many devices to share a single two-wire control bus, every device on the bus has a unique seven-bit address, followed by an eighth bit to specify a read or write.

SCL is a clock input, while SDA is a bidirectional data pin. To allow arbitration of multiple slaves on the same interface, the CS35L38A transmits logic 1 by tri-stating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the logic 1 can be recognized by the master.

The I<sup>2</sup>C control port supports START and STOP conditions, acknowledge, and standard format. It can operate in Standard-mode (Sm) with a bit rate of up to 100 kbit/s, Fast-mode (Fm) with a bit rate of up to 400 kbit/s, and Fast-mode plus (Fm+) with a bit rate of up to 1 Mbit/s.

#### 4.13.2.1 I<sup>2</sup>C Write

In an I<sup>2</sup>C write transaction, any number of data bytes is sent to the CS35L38A. [Fig. 4-31](#) shows the format of an I<sup>2</sup>C write command.



**Figure 4-31. I<sup>2</sup>C Write Waveform**

#### 4.13.2.2 I<sup>2</sup>C Write-Then-Read (with Repeated Start Condition)

In a write-then-read operation (e.g., register read), the CS35L38A from a slave device. Fig. 4-32 shows how an I<sup>2</sup>C read is performed with repeated start condition after the write operation finishes.

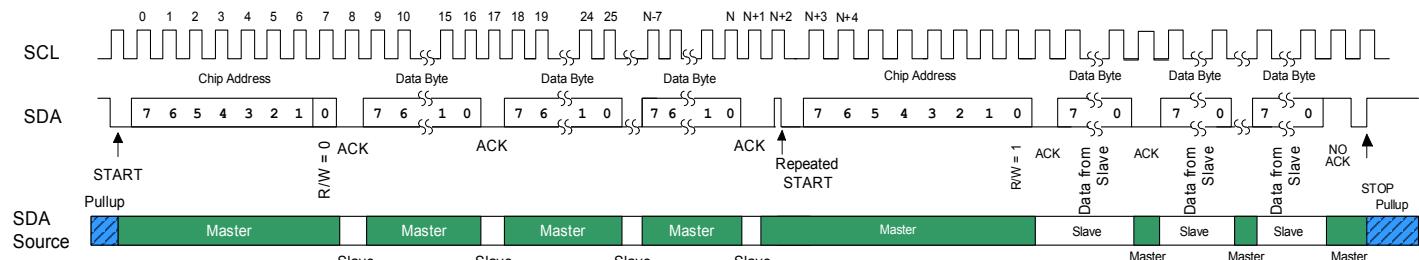


Figure 4-32. I<sup>2</sup>C Write-Then-Read Waveform (with Repeated Start Condition)

#### 4.13.2.3 Transaction Types

The standard transaction supports a 32-bit register address and 32-bit data width. The register address must be word aligned, i.e. the two LSBs must be 0, for 32-bit transactions.

The legend shown in Fig. 4-33 is used in the following transaction examples.

- [ ] Address or Data from Master to Slave
- [ ] Data from Slave to Master
- [S] Start Condition
- [R] 0 in LSB of I<sup>2</sup>C Address specifies a write
- [R] 1 in LSB of I<sup>2</sup>C Address specifies a read
- [A] ACK from Slave to Master
- [Sr] Repeated Start Condition
- [A] ACK from Master to Slave
- [A] NACK from Master to Slave
- [P] Stop Condition

Figure 4-33. Transaction Example Legend

Fig. 4-34 shows a single 32-bit register write to a specified address.

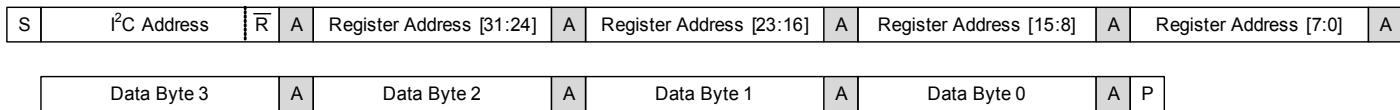
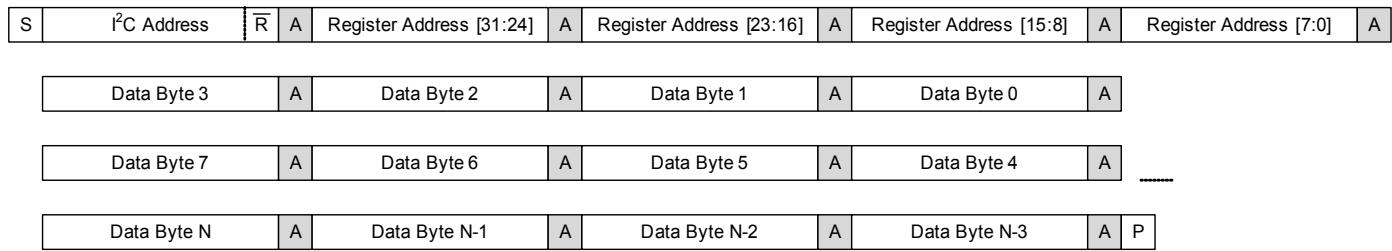


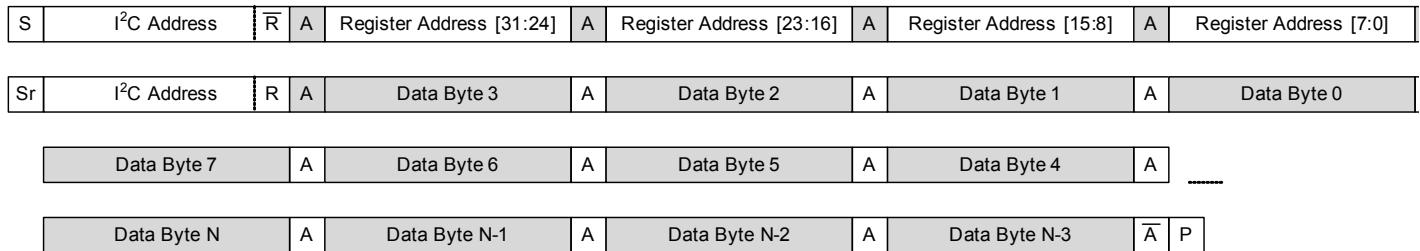
Figure 4-34. Single 32-bit Register Write Transaction

Fig. 4-35 shows multiple 32-bit register write to a specified address. Multiple 32-bit writes may be submitted sequentially without sending the register address again. Each will be submitted to the internal control bus during the ACK after every fourth data byte. If the multiple write goes past the end of the 32-bit address space, then those writes shall be discarded.



**Figure 4-35. Multiple 32-bit Register Write Transaction**

Fig. 4-36 shows multiple 32-bit register read to a specified address. Multiple 32-bit registers may be fetched sequentially without sending the register address again. After the first read, each will be prefetched from the internal control bus during the MSB of the first read being shifted onto the I<sup>2</sup>C bus. If the multiple read goes past the end of the 32-bit address space, then those reads will return all 0's data.



**Figure 4-36. Multiple 32-bit Register Read Transaction (with Repeated Start Condition)**

Note that the CS35L38A only supports auto incrementing addresses for multiple register I<sup>2</sup>C read transactions.

## 5 Applications

This section contains use-case information, configuration information, example sequencing, and typical startup times and power consumption for the various examples. Functional device information for individual blocks can be found in [Section 4](#).

### 5.1 Power-Up and Power-Down

The CS35L38A allows for a wide variety of use cases and configurations. This includes how the device can be powered up and powered down.

For powering up and powering down the CS35L38A, in general it is recommended to first pre-configure the device for the desired use case and then set or clear the GLOBAL\_EN to initiate the power up or power down as the last control register write.

The power-up and power-down examples provided are not intended to encompass all use cases, but to provide register write and order of operation examples for potential use cases when operating as a single, mono device.

#### 5.1.1 Example Power-Up Sequence—Audio Serial Port PCM Input with Monitoring

[Ex. 5-1](#) describes the procedure for starting up the CS35L38A when using the ASP's PCM input source: ASP in I<sup>2</sup>S slave mode; ASP 24 bit data width; FS = 48 kHz; BCK = 3.072 MHz used as REFCLK for PLL; ASP TX channel 1-4 enabled; ASP RX channel 1 enabled; Class H with no BST\_CTL limiting (default), Weak-FET power management enabled (default); AMP gain = 19.0 dB (default); AMP volume = 0 dB (default).

In [Ex. 5-1](#), the clock rates and audio serial port are both re-configured to a non-default mode of operation for purposes of illustration.

##### Example 5-1. Power-Up Sequence—Mono Device, PCM Input

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Turn on all supplies to the amplifier and wait for them to settle.			
2	Release reset to the CS35L38A			
3	Perform device initialization sequence detailed in <a href="#">Section 4.1.3</a>			
4	Configure the CS35L38A's clocking frequency	<a href="#">REFCLK_INPUT p. 93</a>	0x0000 0C20	
		PLL_OPEN_LOOP	1	PLL forced into open loop mode
		PLL_REFCLK_FREQ	100 001	REFCLK frequency = 3.072 MHz
		PLL_REFCLK_EN	0	REFCLK input disabled
		PLL_REFCLK_SEL	000	BCK selected as REFCLK input
5	Enable the CS35L38A's clocking reference	<a href="#">REFCLK_INPUT p. 93</a>	0x0000 0430	
		PLL_OPEN_LOOP	0	PLL not forced in open loop mode
		PLL_REFCLK_FREQ	100 001	REFCLK frequency = 3.072 MHz
		PLL_REFCLK_EN	1	REFCLK input enabled
		PLL_REFCLK_SEL	000	BCK selected as REFCLK input
6	Configure startup calibration registers	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
		0x0000 0020	0x0000 0055	
		0x0000 0020	0x0000 00AA	
		0x0000 7064	0x0929 A800	
		0x0000 7850	0x0000 2FA9	
		0x0000 7854	0x0003 F1D5	
		0x0000 7858	0x0003 F5E3	
		0x0000 785C	0x0000 1137	
		0x0000 7860	0x0001 A7A5	
		0x0000 7864	0x0002 F16A	
		0x0000 7868	0x0000 3E21	
		0x0000 7848	0x0000 0001	
		0x0000 2020	0x0000 0000	
		0x0000 0020	0x0000 00CC	
		0x0000 0020	0x0000 0033	

† Indicates bit fields for which the provided values are typical, but are not required for configuring the key functionality of the sequence. In the target application, these fields can be set as desired without affecting the configuration goal of this start-up sequence.

†† Performing optional device configurations may affect the total power-up time of the example sequence.

**Example 5-1. Power-Up Sequence—Mono Device, PCM Input (Cont.)**

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
7	Perform additional ASP data interface clock calibration steps according <a href="#">Section 4.11.7</a>			
8	Configure Performance Improvements			
		0x0000 0020	0x0000 0055	
		0x0000 0020	0x0000 00AA	
		0x0000 7418	0x9090 01C8	
		0x0000 394C	0x0287 64B7	
		0x0000 3810	0x0000 3C3C	
		0x0000 381C	0x0000 0051	
		0x0000 3854	0x0518 0240	
		0x0000 0020	0x0000 00CC	
		0x0000 0020	0x0000 0033	
9	Configure the audio serial port transmit source			
		AIFTX_INPUT_0_SOURCE p. 113	0x0000 0019	
		ASP_TX1_SEL	001 1001	ASP_TX1 = IMON
		AIFTX_INPUT_1_SOURCE p. 113	0x0000 001A	
		ASP_TX2_SEL	001 1010	ASP_TX2 = VMON2
		AIFTX_INPUT_2_SOURCE p. 113	0x0000 0018	
		ASP_TX3_SEL	001 1000	ASP_TX3 = VMON1
		AIFTX_INPUT_3_SOURCE p. 114	0x0000 0028	
		ASP_TX4_SEL	010 1000	ASP_TX4 = VBATMON
10	Configure the audio serial port format			
		ASP_FORMAT p. 102	0x0000 0002	
		ASP_FMT	010	ASP format = I <sup>2</sup> S Mode
11	Configure the audio serial port slot widths			
		ASP_FRAME_CTRL_1 p. 103	0x0018 0010	
		ASP_RX_WIDTH	0001 1000	ASP RX Slot Width = 24 bit; Data Width = 24 bit
		ASP_TX_WIDTH	0001 0000	ASP TX Slot Width = 16-bit; Data Width = 16-bit
12	Configure the audio serial port transmit slot locations			
		ASP_FRAME_CTRL_2 p. 105	0x0002 0000	
		ASP_TX2_SLOT	00 0010	ASP_TX2 (VMON1) = data slot 2
		ASP_TX1_SLOT	00 0000	ASP_TX1 (IMON) = data slot 0
13	Configure the audio serial port transmit slot locations			
		ASP_FRAME_CTRL_3 p. 107	0x0003 0001	
		ASP_TX4_SLOT	00 0011	ASP_TX4 (VBATMON) = data slot 3
		ASP_TX3_SLOT	00 0001	ASP_TX3 (VMON2) = data slot 1
14	Configure the audio serial port channel enables			
		ASP_RX_TX_ENABLES p. 112	0x0001 000F	
		ASP_RX1_EN	1	ASP_RX1 enabled
		ASP_TX6_EN	0	ASP_TX6 disabled
		ASP_TX5_EN	0	ASP_TX5 disabled
		ASP_TX4_EN	1	ASP_TX4 enabled
		ASP_TX3_EN	1	ASP_TX3 enabled
		ASP_TX2_EN	1	ASP_TX2 enabled
		ASP_TX1_EN	1	ASP_TX1 enabled
15	Configure the sub-blocks to enable upon setting GLOBAL_EN			
		BLOCK_ENABLES p. 88	0x0000 3F21	
		IMON_EN	1	IMON enabled
		VMON_EN	1	VMON enabled
		VMON_EN_SEL	1	VMON1 and VMON2 controlled with VMON_EN
		TEMPMON_EN	1	TEMPMON enabled
		VBSTMON_EN	1	VBSTMON enabled
		VBATMON_EN	1	VBATMON enabled
		BST_EN	10	Boost converter enabled
		AMP_EN	1	Amplifier enable
16	Apply clocks and muted data to the audio serial port. Audio serial port clocks and data may be applied any time after Step 2 and prior to Step 18.			
17	Optional: Configure any other functional block, power management, or error handling subsystem (i.e. VBATBR, Level-dependent Muting, Class H, etc.) prior to Step 18.			
18	Set the GLOBAL_EN to power up the CS35L38A			
		GLOBAL_ENABLES p. 88	0x0000 0001	
		GLOBAL_EN	1	Set the global enable to power up the device
19	Wait for GLOBAL_PUP_DONE_EINT in INT_EINT_4 to be set or wait approximately $t_{AMP\_PUP}$ (see <a href="#">Table 3-4</a> ) from the completion of Step 18. <sup>††</sup>			

<sup>†</sup> Indicates bit fields for which the provided values are typical, but are not required for configuring the key functionality of the sequence. In the target application, these fields can be set as desired without affecting the configuration goal of this start-up sequence.

<sup>††</sup> Performing optional device configurations may affect the total power-up time of the example sequence.

**Example 5-1. Power-Up Sequence—Mono Device, PCM Input (Cont.)**

STEP	TASK
20	Read the <a href="#">INT_EINT_1</a> , <a href="#">INT_EINT_2</a> , <a href="#">INT_EINT_3</a> , and <a href="#">INT_EINT_4</a> registers to identify any flags associated with startup and clear (if necessary).
21	Use the amplifier output and boost converter in normal operation.

† Indicates bit fields for which the provided values are typical, but are not required for configuring the key functionality of the sequence. In the target application, these fields can be set as desired without affecting the configuration goal of this start-up sequence.

†† Performing optional device configurations may affect the total power-up time of the example sequence.

### 5.1.2 Example Power-Down Sequence

[Ex. 5-2](#) describes the procedure for shutting down the CS35L38A in PCM mode after being powered up in a manner such as [Ex. 5-1](#). This procedure assumes that the audio is first muted at the source and that digital volume soft-ramping is disabled in order to produce a fast power down condition without waiting on the digital soft-ramp down to complete.

**Example 5-2. Power-Down Sequence—Mono Device**

STEP	TASK
1	Mute the audio stream from the source to prevent discontinuous audio upon shutdown. If soft-ramping is enabled, wait for the volume control to reach a muted state.
2	Clear the GLOBAL_EN to power down the CS35L38A
	REGISTER/BIT FIELDS
	<a href="#">GLOBAL_ENABLES p. 88</a>
	GLOBAL_EN
	0
	Power down the device
3	Wait for the GLOBAL_PDN_DONE_EINT in <a href="#">INT_EINT_4</a> to be set or a time period of $t_{AMP\_PDN}$ (see <a href="#">Table 3-4</a> ) from the completion of Step 2.
4	Optional: Remove the audio serial port clocks.
5	Optional: Assert RST, and/or remove VDDD to trigger the VDDD POR.
6	Optional: Remove VBAT. VDDD must not be present if VBAT is to be removed.

† Indicates bit fields for which the provided values are typical, but are not required for configuring the key functionality of the sequence. In the target application, these fields can be set as desired without affecting the configuration goal of this start-up sequence.

†† Performing optional device configurations may affect the total power-up time of the example sequence.

## 6 Register Quick Reference

**Table 6-1. Block Base Addresses**

Base Address—I <sup>2</sup> C	Block Name	Register Quick Reference	Register Description Reference
0x00 0000	Software Reset and Hardware ID (SW_RESET)	Section 6.1	Section 7.1
0x00 2000	Power, Global, and Release Control (MSM)	Section 6.2	Section 7.2
0x00 2400	Digital I/O Pad Control (PAD_INTF)	Section 6.3	Section 7.3
0x00 2C00	Device Clocking and Sample Rate Control (CCM)	Section 6.4	Section 7.4
0x00 3800	Boost Converter (BOOST)	Section 6.5	Section 7.5
0x00 4000	VMON1 and IMON Signal Monitoring (VIMON1)	Section 6.6	Section 7.6
0x00 4200	Die Temperature Monitoring (TEPPMON)	Section 6.7	Section 7.7
0x00 4800	Audio Serial Port Data Interface (DATAIF)	Section 6.8	Section 7.8
0x00 4C00	PCM Audio and Data Routing (MIXER)	Section 6.9	Section 7.9
0x00 4E00	VMON2 Signal Monitoring (VIMON2)	Section 6.10	Section 7.10
0x00 6000	Amplifier Volume Control (INTP)	Section 6.11	Section 7.11
0x00 6400	VBAT Brownout Prevention + Temp Warning (ERROR_VOLUME)	Section 6.12	Section 7.12
0x00 6800	Power Management - Class H, Weak-FET, and Level-Dependent Muting (PWRMGMT)	Section 6.13	Section 7.13
0x00 6C00	Dynamic Range Enhancement (DRE)	Section 6.14	Section 7.14
0x00 7400	Amplifier Control (DAC_MSM)	Section 6.15	Section 7.15
0xD0 0000	Interrupt Status and Mask Control (IRQ_MAIN)	Section 6.16	Section 7.16

### 6.1 Software Reset and Hardware ID (SW\_RESET)

Block Base Address—I <sup>2</sup> C		0x00 0000															
Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

+0x000	SOFTWARE_RESET p. 88	SFT_RST_DEVID1[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
+0x008	HARDWARE_REVISION p. 88	SFT_RST_DEVID1[15:0]															
		0	1	0	1	1	0	1	0	0	0	1	1	1	0	0	0
+0x014	GLOBAL_ENABLES p. 88	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### 6.2 Power, Global, and Release Control (MSM)

Block Base Address—I <sup>2</sup> C		0x00 2000															
Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

+0x014	GLOBAL_ENABLES p. 88	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x018 p. 88	BLOCK_ENABLES	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	IMON_EN	VMON_EN	VMON_EN_SEL	TEMPMO_N_EN	VBSTMO_N_EN	VBATMO_N_EN	—	BST_EN	—	—	AMP_EN	—	—	—	AMP_EN
		0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1
+0x01C p. 89	BLOCK_ENABLES2	0	0	0	0	0	0	0	WKFET_AMP_EN	—	AMP_DRE_EN	—	—	—	—	—	—
		—	BR_EN	—	—	—	—	—	—	—	CLASSH_EN	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
+0x020 p. 90	GLOBAL_OVERRIDES	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x02C p. 90	DISCH_FILT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x034 p. 91	ERROR_RELEASE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

### 6.3 Digital I/O Pad Control (PAD\_INTF)

Block Base Address—I <sup>2</sup> C	0x00 2400
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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x000 p. 92	INTERRUPT_CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

## 6.4 Device Clocking and Sample Rate Control (CCM)

Block Base Address—I <sup>2</sup> C												0x00 2C00						
-------------------------------------	--	--	--	--	--	--	--	--	--	--	--	-----------	--	--	--	--	--	--

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x004	REFCLK_INPUT <a href="#">p. 93</a>	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PLL_FORCE_EN 0	PLL_FORCE_EN 0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	—	PLL_OPEN_LOOP 0	—	PLL_REFCLK_FREQ 0	—	PLL_REFCLK_FREQ 0	—	PLL_REFCLK_EN 1	—	PLL_REFCLK_EN 0	—	PLL_REFCLK_SEL 0	—	PLL_REFCLK_SEL 0	
+0x00C	GLOBAL_SAMPLE_RATE <a href="#">p. 94</a>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x010	DATA_FS_SEL <a href="#">p. 94</a>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	SPKMON_FS_SEL 0	SPKMON_FS_SEL 0

## 6.5 Boost Converter (BOOST)

Block Base Address—I <sup>2</sup> C												0x00 3800						
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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x000	VBST_CTL_1 <a href="#">p. 94</a>	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	—	—	—	—	—	—	—	—	—	—	—	—	—	BST_CTL 0	0
+0x004	VBST_CTL_2 <a href="#">p. 95</a>	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	—	—	—	—	—	—	—	—	—	—	—	—	—	BST_CTL_LIM_EN 0	BST_CTL_SEL 0
+0x008	BST_IPK_CTL <a href="#">p. 95</a>	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	—	—	—	—	—	—	—	—	—	—	—	—	—	BST_IPK 1	0
+0x00C	SOFT_RAMP <a href="#">p. 96</a>	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	—	—	—	—	—	—	—	—	—	—	—	—	—	BST_SFT_RAMP 0	0
+0x010	BST_LOOP_COEFF <a href="#">p. 96</a>	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		BST_K2 0	0	0	1	0	0	1	0	0	0	0	0	0	0	BST_K1 0	0
+0x014	LBST_SLOPE <a href="#">p. 96</a>	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		BST_SLOPE 0	0	1	1	1	0	1	0	1	0	0	0	0	0	—	BST_LBST_VAL 0

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
+0x018 p. 97	BST_SW_FREQ	BST_DCM_FREQ_MIN										—						
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
		BST_DCM_FREQ[7:0]										—				BST_CCM_FREQ		
+0x01C p. 97	BST_DCM_CTL	—										—						
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		—										BST_DCM_EXIT_SEL	BST_DCM_ENTRY_SEL	—				BST_AUTO_DCM_EN
+0x020 p. 98	DCM_FORCE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	
		—										—						
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
+0x030 p. 98	VBST_OVP	—										—						
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		—										BST_OVP_EN	—				BST_OVP_THLD	
		0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	

## 6.6 VMON1 and IMON Signal Monitoring 1 (VIMON1)

Block Base Address—I <sup>2</sup> C	0x00 4000
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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x004 p. 99	SPKMON_FILTERS	—										—					
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—										—					
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	IMON_POL	VMON1_POL
		1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

## 6.7 Die Temperature Monitoring (TEMPMON)

Block Base Address—I <sup>2</sup> C	0x00 4200
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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
+0x020 p. 99	WARN_LIMIT_THRESHOLD	—										—						
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		—										—						TEMP_WARN_THLD
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x100	STATUS	TEMPMO N_ ENABLE D 0	TEMP_ N_ IS_VALID 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
p. 99																TEMPMO N_ERR_ STS 0	TEMPMO N_WARN_ STS 0

## 6.8 Audio Serial Port Data Interface (DATAIF)

Block Base Address—I <sup>2</sup> C	0x00 4800
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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x000	ASP_TX_PIN_CTRL	—	—	—	—	—	—	ASP_TX_HIZ_DLY	—	—	ASP_TX_DAT_HIZ	—	—	—	—	—	—
p. 100		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x004	ASP_RATE_PIN_CTRL	ASP_TX_RATE	—	—	—	—	—	—	—	—	ASP_RX_RATE	—	—	ASP_HIZ_FRC	—	—	—
p. 101		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x008	ASP_FORMAT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
p. 102		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x018	ASP_FRAME_CTRL_1	—	—	—	—	—	—	—	—	—	ASP_RX_WIDTH	—	—	—	—	—	—
p. 103		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x01C	ASP_FRAME_CTRL_2	—	—	—	—	—	—	—	—	—	ASP_TX2_SLOT	—	—	—	—	—	—
p. 105		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x020	ASP_FRAME_CTRL_3	—	—	—	—	—	—	—	—	—	ASP_TX4_SLOT	—	—	—	—	—	—
p. 107		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x024	ASP_FRAME_CTRL_4	—	—	—	—	—	—	—	—	—	ASP_TX6_SLOT	—	—	—	—	—	—
p. 109		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x02C	ASP_FRAME_CTRL_5	—	—	—	—	—	—	—	—	—	ASP_RX1_SLOT	—	—	—	—	—	—
p. 111		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x038 p. 111	ASP_TX_RX_LATENCY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
+0x03C p. 112	ASP_RX_TX_ENABLES	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		ASP_TX6_EN	ASP_TX5_EN	ASP_TX4_EN	ASP_TX3_EN	ASP_TX2_EN	ASP_TX1_EN	ASP_TX6_EN	ASP_TX5_EN	ASP_TX4_EN	ASP_TX3_EN	ASP_TX2_EN	ASP_TX1_EN	ASP_TX6_EN	ASP_TX5_EN	ASP_TX4_EN	ASP_TX3_EN

## 6.9 PCM Audio and Data Routing (MIXER)

Block Base Address—I <sup>2</sup> C	0x00 4C00
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Offset	Register	31 ... 8	7	6	5	4	3	2	1	0
+0x000 p. 112	DACPCM_INPUT_SOURCE	—	—	—	—	—	AMP_PCM_RX_SEL	—	—	—
		0x0000 00	0	0	0	0	1	0	0	0
+0x020 p. 113	AIFTX_INPUT_0_SOURCE	—	—	0	0	1	1	0	0	0
+0x024 p. 113	AIFTX_INPUT_1_SOURCE	—	—	0	0	1	1	0	0	1
+0x028 p. 113	AIFTX_INPUT_2_SOURCE	—	—	0	1	0	1	0	0	0
+0x02C p. 114	AIFTX_INPUT_3_SOURCE	—	—	0	1	0	1	0	0	1
+0x030 p. 114	AIFTX_INPUT_4_SOURCE	—	—	0	1	0	0	0	0	0
+0x034 p. 114	AIFTX_INPUT_5_SOURCE	—	—	0	0	0	0	0	0	0

## 6.10 VMON Signal Monitoring 2 (VIMON2)

Block Base Address—I <sup>2</sup> C	0x00 4E00
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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x004 p. 115	SPKMON_FILTERS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	—	—	—	—	—	—	—	—	—	—	—	—	—	VMON2_POL	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

## 6.11 Amplifier Volume Control (INTP)

Block Base Address—I <sup>2</sup> C												0x00 6000						
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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x000 <a href="#">p. 115</a>	AMP_CTRL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		AMP_ HPF_ PCM_EN	AMP_ INV_PCM	— AMP_VOL_PCM											AMP_RAMP_PCM		
		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

## 6.12 Brownout Prevention + Temp Warning (ERROR\_VOLUME)

Block Base Address—I <sup>2</sup> C										0x00 6400								
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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x004 <a href="#">p. 116</a>	BR_CONFIG	—	—	—	—	—	BR_REL_TRIG	BR_REL_AUTO	BR_MUTE_EN	BR_REL_RATE			BR_WAIT		BR_ATK_RATE		
		0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0
		BR_ATK_VOL				BR_MAX_ATT				—	BR_THLD1				0	1	0
+0x00C <a href="#">p. 117</a>	BR_STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—								BR_STATUS							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x014 <a href="#">p. 117</a>	OTW_CONFIG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—								TEMP_WARN_VOL							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
+0x050 <a href="#">p. 117</a>	VOL_STATUS_TO_DSP	—														FINAL_ERROR_VOL[8:7]	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		FINAL_ERROR_VOL[6:0]								0	0	0	0	0	0	0	0

## 6.13 Power Management - Class H, Weak-FET, and Level-dependent Muting (PWRMGMT)

Block Base Address—I <sup>2</sup> C										0x00 6800							
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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x000 <a href="#">p. 118</a>	CLASSH_CONFIG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CH_HD_RM	—
		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
		CH_REL_RATE								—	—	—	—	—	—	CH_MEM_DEPTH	—
+0x004 <a href="#">p. 118</a>	WKFET_AMP_CONFIG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—				WKFET_AMP_THLD				—				WKFET_AMP_DLY		WKFET_AMP_FRC_EN	WKFET_AMP_FRC
		0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1
+0x008 <a href="#">p. 119</a>	LDM_CONFIG	—														LDM_PCM_THLD	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—		LDM_SEL				—		LDM_DELAY		—		0	1	1	0

## 6.14 Dynamic Range Enhancement (DRE)

Block Base Address—I <sup>2</sup> C												0x00 6C00							
-------------------------------------	--	--	--	--	--	--	--	--	--	--	--	-----------	--	--	--	--	--	--	--

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x004 <a href="#">p. 120</a>	AMP_GAIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	—	—	—	AMP_GAIN_ZC	AMP_GAIN_PCM										

## 6.15 Amplifier Control (DAC\_MSM)

Block Base Address—I <sup>2</sup> C												0x00 7400							
-------------------------------------	--	--	--	--	--	--	--	--	--	--	--	-----------	--	--	--	--	--	--	--

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x090 <a href="#">p. 121</a>	DAC_DC_DET	—	—	—	—	—	—	—	—	—	—	—	—	DCIN_WD_THLD	DCIN_WD_THLD	DCIN_WD_THLD	DCIN_WD_THLD
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	—	WD_MODE	WD_MODE	DCIN_WD_DUR	DCIN_WD_EN	DCIN_WD_EN	DCIN_WD_EN	DCIN_WD_EN							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

## 6.16 Interrupt Status and Mask Control (IRQ\_MAIN)

Block Base Address—I <sup>2</sup> C												0xD0 0000							
-------------------------------------	--	--	--	--	--	--	--	--	--	--	--	-----------	--	--	--	--	--	--	--

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
+0x000 <a href="#">p. 122</a>	INT_EINT_1	—	—	—	—	TEMP_ERR_EINT	TEMP_WARN_EINT	BR_ATT_CLR_EINT	BR_EINT	—	—	—	BST_IPK_EINT	BST_SHORT_ERR_EINT	BST_DCM_UVP_ERR_EINT	BST_OVP_ERR_EINT	BST_OVP_ERR_EINT	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		BST_OVP_EINT	LDM_PCM_ON_FALL_EINT	LDM_PCM_ON_RISE_EINT	—	—	—	—	—	—	—	—	—	—	—	—	—	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
+0x004 <a href="#">p. 123</a>	INT_EINT_2	—	—	IMON_CLIP_EINT	VMON_CLIP_EINT	VBSTMOMN_CLIP_EINT	MON_CLIP_EINT	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x008 <a href="#">p. 123</a>	INT_EINT_3	—	—	AMP_SHORT_ERR_EINT	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x00C  p. 124	INT_EINT_4	—			DC_ERR_INT	VMON2_CLIP_EINT	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	PLL_UNLOCK_EINT	—	—	—	—	—	GLOBAL_PUP_DONE_EINT	GLOBAL_PDN_DONE_EINT	GLOBAL_EN_ASSERT_EINT	—	0	0	0	0	0
+0x020  p. 125	INT_STS_1	—					TEMP_ERR_STS	TEMP_WARN_STS	BR_ATT_CLR_STS	BR_STS	—	BST_IPK_STS	BST_SHORT_ERR_STS	BST_DCM_UVP_ERR_STS	BST_OVP_ERR_STS	BST_OVP_ERR_STS	BST_OVP_ERR_STS
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		BST_OVP_STS	—	LDM_PCM_STS	—	—	—	—	—	—	—	—	0	0	0	0	0
+0x024  p. 126	INT_STS_2	—						IMON_CLIP_STS	VMON_CLIP_STS	VBSTMON_CLIP_STS	MON_CLIP_STS	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
+0x028  p. 126	INT_STS_3	—						—	—	—	—	—	—	—	—	—	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	AMP_SHORT_ERR_STS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
+0x02C  p. 127	INT_STS_4	—			DC_ERR_STS	VMON2_CLIP_STS	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—	PLL_UNLOCK_STS	—	—	—	—	—	GLOBAL_PUP_DONE_STS	GLOBAL_PDN_DONE_STS	GLOBAL_EN_ASSERT_STS	—	—	—	—	—	—
+0x040  p. 128	INT_MASK_1	—					TEMP_ERR_MASK	TEMP_WARN_MASK	BR_ATT_CLR_MASK	BR_MASK	—	BST_IPK_MASK	BST_SHORT_ERR_MASK	BST_DCM_UVP_ERR_MASK	BST_OVP_ERR_MASK	BST_OVP_ERR_MASK	BST_OVP_ERR_MASK
		1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
		BST_OVP_MASK	LDM_PCM_ON_RISE_MASK	LDM_PCM_ON_RISE_MASK	—	—	—	—	—	—	—	—	—	—	—	—	—
+0x044  p. 129	INT_MASK_2	—						IMON_CLIP_MASK	VMON_CLIP_MASK	VBSTMON_CLIP_MASK	MON_CLIP_MASK	—	—	—	—	—	—
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x048 <a href="#">p. 129</a>	INT_MASK_3	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1
		—	—	AMP_SHORT_ERR_MASK	1	1	1	1	1	1	1	1	1	1	1	1	1
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
+0x04C <a href="#">p. 130</a>	INT_MASK_4	—	—	DC_ERR_MASK	VMON2_CLIP_MASK	1	1	0	0	0	1	1	1	1	1	1	1
		0	0	0	1	1	1	—	—	GLOBAL_PUP_DONE_MASK	1	1	1	1	1	1	1
		—	PLL_UNLOCK_MASK	1	1	1	1	1	1	1	1	1	1	1	1	1	1

## 7 Register Descriptions

### 7.1 Software Reset and Hardware ID (SW\_RESET)

#### 7.1.1 SOFTWARE\_RESET

**I<sup>2</sup>C Address: 0x00 0000**

RO	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SFT_RST_DEVID1																																
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0	0	1	1	1	0	0	0		

Bits	Name	Description
31:0	SFT_RST_DEVID1	Writing to this register resets all registers to their default state. Reading from this register returns the Device ID (0x0003_5A38). <b>Note:</b> Writing 0x5AXX_XXXX to this register triggers a soft reset.

#### 7.1.2 HARDWARE\_REVISION

**I<sup>2</sup>C Address: 0x00 0008**

RO	31...8	7	6	5	4	—	3	2	1	0
	—					HW_REV				
Default	0x00 0000	X	X	X	X		X	X	X	X

Bits	Name	Description
31:8	—	Reserved
7:0	HW_REV	Hardware device revision. Incremented for every new revision of the device.

### 7.2 Power, Global, and Release Control (MSM)

#### 7.2.1 GLOBAL\_ENABLES

**I<sup>2</sup>C Address: 0x00 2014**

RW	31...8	7	6	5	4	—	3	2	1	0
	—					—				GLOBAL_EN
Default	0x00 0000	0	0	0	0		0	0	0	0

Bits	Name	Description
31:1	—	Reserved
0	GLOBAL_EN	Global device enable. Enables and disables all functionality of the device. When GLOBAL_EN = 0, it is equivalent to disabling all of the sub-blocks and their associated circuitry. When GLOBAL_EN = 1, if all of the subblocks are enabled (x_EN = 1), the entire device will power up. Individual sub-blocks may be disabled using their respective enable control bits. If a functional block contains a global override (x_GLOBAL_OVR), setting the x_GLOBAL_OVR = 1 allows that block to remain enabled when GLOBAL_EN = 0. This permits various low power and fast power up modes of operation. 0 (Default) Device is disabled and put into a power down state (unless one or more x_GLOBAL_OVR is set) 1 Device is enabled

#### 7.2.2 BLOCK\_ENABLES

**I<sup>2</sup>C Address: 0x00 2018**

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	IMON_EN	VMON_EN	VMON_EN_SEL	TEMPM_ON_EN	VBSTM_ON_EN	VBATM_ON_EN	—	BST_EN	—	—	AMP_EN				
Default	0x0000	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1

Bits	Name	Description
31:14	—	Reserved
13	IMON_EN	IMON speaker current monitoring enable. Configures whether the IMON speaker current monitoring is disabled or enabled. 0 IMON monitoring disabled 1 (Default) IMON monitoring enabled
12	VMON_EN	VMON speaker voltage monitoring enable. Configures whether the VMON speaker voltage monitoring is disabled or enabled. 0 VMON monitoring disabled 1 (Default) VMON monitoring enabled

Bits	Name	Description
11	VMON_EN_SEL	VMON speaker voltage monitoring mode. Configures whether the second VMON speaker voltage monitoring is disabled or enabled when VMON_EN is toggled. 0 (Default) VMON1 only controlled by VMON_EN 1 VMON1 and VMON2 controlled by VMON_EN
10	TEMPMON_EN	TEMPMON chip temperature monitoring enable. Configures whether the TEMPMON chip temperature monitoring is enabled. Other subblocks that require the TEMPMON (e.g. boost converter) can automatically enable the TEMPMON monitoring even if TEMPMON_EN = 0. 0 (Default) TEMPMON monitoring disabled 1 TEMPMON monitoring enabled
9	VBSTMON_EN	VBSTMON supply voltage monitoring enable. Configures whether the VBSTMON supply monitoring is enabled. Other subblocks that require the VBSTMON (e.g. boost converter) can automatically enable the VBSTMON supply monitoring even when VBSTMON_EN = 0. 0 VBSTMON monitoring disabled (if no other block is requesting VBSTMON to be enabled) 1 (Default) VBSTMON monitoring enabled
8	VBATMON_EN	MON supply voltage monitoring enable. Configures whether the VBATMON supply monitoring is enabled. Other subblocks that require the MON (e.g. boost converter) can automatically enable the VBATMON supply monitoring even when VBATMON_EN = 0. 0 VBATMON monitoring disabled (if no other block requesting VBATMON to be enabled) 1 (Default) VBATMON monitoring enabled
7:6	—	Reserved
5:4	BST_EN	Digital boost converter enable/disable control. Configures the power state of the boost converter and bypass FET. When GLOBAL_EN=0 and BST_GLOBAL_OVR = 0, the boost converter's bypass FET is off. 00 Reserved 01 Boost converter disabled with bypass FET on (VBST = ) 10 (Default) Boost converter enabled 11 Reserved
3:1	—	Reserved
0	AMP_EN	Class D amplifier enable/disable control. Configures the operational power state of the Class D amplifier and most of the amplifier's audio chain (channel select, digital gain, modulator, and output stage). 0 Amplifier functionality disabled 1 (Default) Amplifier functionality enabled

### 7.2.3 BLOCK\_ENABLES2

**I<sup>2</sup>C Address: 0x00 201C**

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	WKFET_AMP_EN	—	—	—	AMP_DRE_EN	—	—	—	—
Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	—	—	VBATBR_EN	—	—	—	—	—	—	—	—	CLASSH_EN	—	—	—	—
	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Name	Description
31:25	—	Reserved
24	WKFET_AMP_EN	Amplifier weak-FET automatic tracking enable. Configures whether the weak-FET signal based tracking and automatic management for the amplifier's switching outputs is enabled or disabled. 0 Amplifier weak-FET tracking disabled 1 (Default) Amplifier weak-FET tracking enabled
23:21	—	Reserved
20	AMP_DRE_EN	Amplifier dynamic range enhancement enable. Configures whether the dynamic range enhancement is enabled and automatically managing the analog gain of the amplifier in order to reduce the noise floor of the amplifier. 0 (Default) DRE disabled 1 DRE enabled
19:13	—	Reserved
12	VBATBR_EN	brownout prevention enable. Configures whether the brownout prevention algorithm is enabled or disabled. 0 (Default) brownout prevention disabled 1 brownout prevention enabled
11:9	—	Reserved

Bits	Name	Description							
8:5	—	Reserved							
4	CLASSH_EN	Class H enable. Configures whether the Class H tracking is enabled or disabled (and the memory buffer bypassed). When the Class H is enabled, the BST_CTL_SEL must be configured to use the Class H target in order for VBST tracking to occur. 0 Class H disabled 1 (Default) Class H enabled							
3:0	—	Reserved							

#### 7.2.4 GLOBAL\_OVERRIDES

**I<sup>2</sup>C Address: 0x00 2020**

RW	31..8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	TEMPPMON_GLOBAL_OVR	FILT_GLOBAL_OVR	—	BST_GLOBAL_OVR
Default	0x00 0000	0	0	0	0	0	0	1	0

Bits	Name	Description							
31:4	—	Reserved							
3	TEMPPMON_GLOBAL_OVR	TEMPPMON global enable override. Setting TEMPPMON_GLOBAL_OVR allows the TEMPPMON to continue to function and remain in an operational state while GLOBAL_EN = 0. 0 (Default) The TEMPPMON is disabled when GLOBAL_EN = 0 1 Assumes the configuration of TEMPPMON_EN, regardless of the state of GLOBAL_EN							
2	FILT_GLOBAL_OVR	FILT global enable override. Setting FILT_GLOBAL_OVR allows the FILT capacitor to be pre-charged and remain charged while GLOBAL_EN = 0 in order to enable a faster device power up, or to allow rapidly transitioning between a power up and power down the device via the GLOBAL_EN control. 0 (Default) The FILT capacitor is not actively charged when GLOBAL_EN = 0 1 The FILT capacitor is actively charged, regardless of the state of GLOBAL_EN							
1	—	Reserved							
0	BST_GLOBAL_OVR	Boost converter global enable override. Setting BST_GLOBAL_OVR allows the boost converter's enable control (BST_EN) to operate independently from the GLOBAL_EN control. This allows the boost converter to be powered up when GLOBAL_EN = 0 and the rest of the IC is disabled. 0 (Default) The boost converter is disabled when GLOBAL_EN = 0 1 The configuration of BST_EN is applied, regardless of the state of GLOBAL_EN							

#### 7.2.5 DISCH\_FILT

**I<sup>2</sup>C Address: 0x00 202C**

RW	31..8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	DISCH_FILT
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description							
31:1	—	Reserved							
0	DISCH_FILT	Discharge FILT capacitor. Configures the state of the internal clamp on the FILT pin. 0 (Default) FILT is not clamped to GND 1 FILT is clamped to GND. Only set if GLOBAL_EN = 0 and FILT_GLOBAL_OVR = 0.							

### 7.2.6 ERROR\_RELEASE

**I<sup>2</sup>C Address: 0x00 2034**

RW	31...8	7	6	5	4	3	2	1	0
—	—	TEMP_ERR_RLS	TEMP_WARN_RLS	BST_UVP_ERR_RLS	BST_OVP_ERR_RLS	BST_SHORT_ERR_RLS	AMP_SHORT_ERR_RLS	—	—
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:7	—	Reserved
6	TEMP_ERR_RLS	<p>Overtemperature error protection release. Releases overtemperature error protection that places the device into Speaker-Safe Mode if the overtemperature error condition is no longer present. The present overtemperature error condition can be determined by reading the TEMP_ERR_EINT bit twice.</p> <p>At the end of the protection release sequence (0 -&gt; 1 -&gt; 0), if the overtemperature error condition is no longer present, then the overtemperature error-caused Speaker-Safe Mode is cleared (the device may remain in Speaker-Safe Mode if another error is present).</p> <p><b>Note:</b> For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the potential protection release sequence, then protection is not removed, the related interrupt status bit is set again and, if unmasked, a new interrupt is generated.</p> <p>0 (Default) If the overtemperature error condition is present, Speaker-Safe Mode is applied. 1 Reserved</p>
5	TEMP_WARN_RLS	<p>Overtemperature warning release. Releases overtemperature warning if the overtemperature warning condition is no longer present. The present overtemperature warning condition can be determined by reading the TEMP_WARN_EINT bit twice.</p> <p>At the end of the warning release sequence (0 -&gt; 1 -&gt; 0), if the overtemperature warning condition is no longer present, then the overtemperature warning is cleared.</p> <p><b>Note:</b> For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the potential protection release sequence, then protection is not removed, the related interrupt status bit is set again and, if unmasked, a new interrupt is generated.</p> <p>0 (Default) If the overtemperature warning condition is present, attenuation is applied. 1 Reserved</p>
4	BST_UVP_ERR_RLS	<p>Boost converter undervoltage error protection release. Releases boost converter undervoltage error protection that places the device into Speaker-Safe Mode if the boost converter undervoltage error condition is no longer present. The present boost converter undervoltage error condition can be determined by reading the BST_DCM_UVP_ERR_EINT bit twice.</p> <p>At the end of the protection release sequence (0 -&gt; 1 -&gt; 0), if the boost converter undervoltage error condition is no longer present, then the boost converter undervoltage error-caused Speaker-Safe Mode is cleared (the device may remain in Speaker-Safe Mode if another error is present).</p> <p><b>Note:</b> For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the potential protection release sequence, then protection is not removed, the related interrupt status bit is set again and, if unmasked, a new interrupt is generated.</p> <p>0 (Default) If the boost converter undervoltage error condition is present, Speaker-Safe Mode is applied. 1 Reserved</p>
3	BST_OVP_ERR_RLS	<p>Boost converter overvoltage error protection release. Releases boost converter overvoltage error protection that places the device into Speaker-Safe Mode if the boost converter overvoltage error condition is no longer present. The present boost converter overvoltage error condition can be determined by reading the BST_OVP_ERR_EINT bit twice.</p> <p>At the end of the protection release sequence (0 -&gt; 1 -&gt; 0), if the boost converter overvoltage error condition is no longer present, then the boost converter overvoltage error-caused Speaker-Safe Mode is cleared (the device may remain in Speaker-Safe Mode if another error is present).</p> <p><b>Note:</b> For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the potential protection release sequence, then protection is not removed, the related interrupt status bit is set again and, if unmasked, a new interrupt is generated.</p> <p>0 (Default) If the boost converter overvoltage error condition is present, Speaker-Safe Mode is applied. 1 Reserved</p>

Bits	Name	Description
2	BST_SHORT_ERR_RLS	<p>Boost converter inductor short error protection release. Releases boost converter inductor short error protection that places the device into Speaker-Safe Mode if the boost converter inductor short error condition is no longer present. The present boost converter inductor short error condition can be determined by reading the BST_SHORT_ERR_EINT bit twice.</p> <p>At the end of the protection release sequence (0 → 1 → 0), if the boost converter inductor short error condition is no longer present, then the boost converter inductor short error-caused Speaker-Safe Mode is cleared (the device may remain in Speaker-Safe Mode if another error is present).</p> <p><b>Note:</b> For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the potential protection release sequence, then protection is not removed, the related interrupt status bit is set again and, if unmasked, a new interrupt is generated.</p> <p>0 (Default) If the boost converter inductor short error condition is present, Speaker-Safe Mode is applied. 1 Reserved</p>
1	AMP_SHORT_ERR_RLS	<p>Amplifier short protection release. Releases amplifier short protection that places the device into Speaker-Safe Mode if the amplifier short condition is no longer present. The present amplifier short condition can be determined by reading the AMP_SHORT bit twice.</p> <p>At the end of the protection release sequence (0 → 1 → 0), if the amplifier short condition is no longer present, the amplifier short-caused Speaker-Safe Mode is cleared (the device may remain Speaker-Safe Mode if another error is present).</p> <p><b>Note:</b> For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the protection potential release sequence, protection is not removed, the related interrupt status bit is set again, and, if unmasked, a new interrupt is generated.</p> <p>0 (Default) If the amplifier short condition is present, Speaker-Safe Mode is applied. 1 Reserved</p>
0	—	Reserved

## 7.3 Digital I/O Pad Control (PAD\_INTF)

### 7.3.1 INTERRUPT\_CONTROL

**I2C Address: 0x00 2400**

RW	31..8	7	6	5	4	3	2	1	0
—	—	—	—	INT_DRV_SEL	—	—	INT_POL_SEL	—	INT_OUT_EN
Default	0x00 0000	0	0	1	1	1	0	0	0

Bits	Name	Description
31:6	—	Reserved
5	INT_DRV_SEL	<p>Selects the driver type of the selected interrupt output.</p> <p>0 Open-drain 1 (Default) Push-pull</p>
4:3	—	Reserved
2	INT_POL_SEL	<p>Selects the polarity of the selected interrupt output when in push-pull mode.</p> <p><b>Note:</b> When the selected interrupt output is in open-drain mode, INT_POL_SEL must be set to 0.</p> <p>0 (Default) Active-low 1 Active-high</p>
1	—	Reserved
0	INT_OUT_EN	<p>Enables or disables the selected interrupt output.</p> <p>0 (Default) Disabled 1 Enabled</p>

## 7.4 Device Clocking and Sample Rate Control (CCM)

### 7.4.1 REFCLK\_INPUT

**I<sup>2</sup>C Address: 0x00 2C04**

RW	31	30	29	28	27	26	25	24	—	23	22	21	20	19	18	17	16	PLL_FORCE_EN
Default	0	0	0	0	0	0	0	0	—	0	0	0	0	0	0	0	0	
RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	PLL_REFCLK_SEL	
Default	0	0	0	0	0	0	0	0	PLL_OPEN_LOOP	PLL_REFCLK_FREQ				PLL_REFCLK_EN	—	PLL_REFCLK_SEL	PLL_REFCLK_SEL	

Bits	Name	Description																	
31:17	—	Reserved																	
16	PLL_FORCE_EN	PLL force enable. Forces the PLL to remain on and selected as the clock source during operational states instead of using the internal oscillator. 0 (Default) Normal operation (PLL not forced on/selected) 1 PLL is forced as the internal clock selection source instead of the internal oscillator for low power modes.																	
15:12	—	Reserved																	
11	PLL_OPEN_LOOP	PLL open loop operation control. Configures whether the PLL is operating in an open loop or closed loop configuration. The PLL must be configured to operate open loop if the REFCLK source or frequency is being reconfigured. After the REFCLK has been reconfigured and is stable, the PLL can be set back to a closed loop configuration to resume normal operation. 0 (Default) Closed loop (PLL tracks REFCLK) 1 Open loop																	
10:5	PLL_REFCLK_FREQ	PLL input reference clock frequency. This value must match the input frequency present at the selected REFCLK source in order to properly configure the internal clocking of the device.																	
		00 0000 (Default) 32768Hz	10 0000 3000000 Hz	00 0001 8000 Hz	10 0001 3072000 Hz	00 0010 11025 Hz	10 0010 3200000 Hz	00 0011 12000 Hz	10 0011 4000000 Hz	00 0100 16000 Hz	10 0100 4096000 Hz	00 0101 22050 Hz	10 0101 4800000 Hz	00 0110 24000 Hz	10 0110 5644800 Hz	00 0111 32000 Hz	10 0111 6000000 Hz	00 1000 44100 Hz	10 1000 6144000 Hz
		00 1001 48000 Hz	10 1001 6250000 Hz	00 1010 88200 Hz	10 1010 6400000 Hz	00 1011 96000 Hz	10 1011 6500000 Hz	00 1100 128000 Hz	10 1100 6750000 Hz	00 1101 176400 Hz	10 1101 7526400 Hz	00 1110 192000 Hz	10 1110 8000000 Hz	00 1111 256000 Hz	10 1111 8192000 Hz	01 0000 352800 Hz	11 0000 9600000 Hz	01 0001 384000 Hz	11 0001 11289600 Hz
		01 0010 512000 Hz	11 0010 12000000 Hz	01 0011 705600 Hz	11 0011 12288000 Hz	01 0100 750000 Hz	11 0100 12500000 Hz	01 0101 768000 Hz	11 0101 12800000 Hz	01 0110 1000000 Hz	11 0110 13000000 Hz	01 0111 1024000 Hz	11 0111 13500000 Hz	01 1000 1200000 Hz	11 1000 19200000 Hz	01 1001 1411200 Hz	11 1001 22579200 Hz	01 1010 1500000 Hz	11 1010 24000000 Hz
		01 1011 1536000 Hz	11 1011 24576000 Hz	01 1100 2000000 Hz	11 1100 25000000 Hz	01 1101 2048000 Hz	11 1101 25600000 Hz	01 1110 2400000 Hz	11 1110 26000000 Hz	01 1111 2822400 Hz	11 1111 27000000 Hz								
4	PLL_REFCLK_EN	Input reference clock enable. Enables the selected reference input clock for purposes of power savings when the device is on a shared bus. 0 Reference clock input disabled 1 (Default) Enabled (normal mode)																	

Bits	Name	Description
3	—	Reserved
2:0	PLL_REFCLK_SEL	Device reference clock input select. Selects the reference clock the device uses to generate an internal master clock. 000 (Default) BCK input 001 FS input 010–111 Reserved

#### 7.4.2 GLOBAL\_SAMPLE\_RATE

**I<sup>2</sup>C Address: 0x00 2C0C**

RW	31...8	7	6	5	4	3	2	1	0
	—	—	—						GLOBAL_FS
Default	0x00 0000	0	0	0	0	0	0	1	1

Bits	Name	Description
31:5	—	Reserved
4:0	GLOBAL_FS	Serial port sample rate frequency. Configures the global sample rate of the serial port (I <sup>2</sup> S/TDM). 0 0000 Reserved 0 0001 12.0 kHz 0 0010 24.0 kHz 0 0011 (Default) 48.0 kHz 0 0100 96.0 kHz 0 0101 192.0 kHz 0 0110 384.0 kHz 00111–0 1000 Reserved 0 1001 11.025 kHz 0 1010 22.050 kHz 0 1011 44.100 kHz 0 1100 88.200 kHz 0 1101 176.400 kHz 01110–1 0000 Reserved 1 0001 8 kHz 1 0010 16 kHz 1 0011 32 kHz 10100–1 1111 Reserved

#### 7.4.3 DATA\_FS\_SEL

**I<sup>2</sup>C Address: 0x00 2C10**

RW	31...8	7	6	5	4	3	2	1	0
	—	—	—	—	—				SPKMON_FS_SEL
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:2	—	Reserved
1:0	SPKMON_FS_SEL	Speaker monitoring (ADC datapath) internal sample rate clock reference selection. Determines which source the ADC sample rate reference clock locks to. Allows the user to manage group delay variability relative to the selected TX port. 00 (Default) Serial Port 01 10 Off (free running) 11 Reserved

### 7.5 Boost Converter (BOOST)

#### 7.5.1 VBST\_CTL\_1

**I<sup>2</sup>C Address: 0x00 3800**

RW	31...8	7	6	5	4	3	2	1	0
	—	—	—	—	—	BST_CTL	—	—	—
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:8	—	Reserved
7:0	BST_CTL	Boost converter target control word. Configures the boost converter's output mode and voltage when BST_CTL_SEL is configured to use the control port value. When Class H is enabled and BST_CTL_LIM = 1, configures the maximum allowable VBST voltage for when the target boost voltage is controlled by either Class H or multidevice synchronization. When the BST_CTL target is less than VBAT, the boost converter remains in bypass mode (VBST = VBAT). Step size is 50 mV. 0000 0000 (Default) VBST = VBAT 0000 0001 2.55 V 0000 0010 2.60 V ... 1011 1100 11.90 V 1011 1101 11.96 V 1011 1110 12.00 V

### 7.5.2 VBST\_CTL\_2

**I<sup>2</sup>C Address: 0x00 3804**

RW	31...8	7	6	5	4	3	2	1	0
	—	—	—	—	—	BST_CTL_LIM_EN	BST_CTL_SEL		
Default	0x00 0000	0	0	0	0	0	0	0	1

Bits	Name	Description
31:3	—	Reserved
2	BST_CTL_LIM_EN	Class H boost control maximum limit. Controls whether the Class H's or multidevice SYNC's maximum generated maximum boost control voltage is limited by the BST_CTL configuration. 0 (Default) No user-configured limit 1 Maximum Class H BST_CTL generation is limited by BST_CTL configuration
1:0	BST_CTL_SEL	Boost converter control source selection. Selects the source of the BST_CTL target VBST voltage for the boost converter to generate. This allows the user to select how to manage the control of the target VBST voltage without enabling and disabling other functional blocks, potentially changing the audio path (i.e. Class H tracking). <b>Note:</b> When Class H tracking is selected as the BST_CTL target source, and the Class H is disabled (CH_TRK_EN = 0) the boost converter remains in bypass mode (VBST = ). 00 Control port BST_CTL register value                           10 Reserved 01 (Default) Class H tracking value                           11 Reserved

### 7.5.3 BST\_IPK\_CTL

**I<sup>2</sup>C Address: 0x00 3808**

RW	31...8	7	6	5	4	3	2	1	0
	—	—	—	—	—	BST_IPK			
Default	0x00 0000	0	1	0	0	1	0	1	0

Bits	Name	Description
31:7	—	Reserved
6:0	BST_IPK	Boost converter peak current limit. Configures the peak current by monitoring the current through the boost FET. If the amplifier attempts to draw enough power to where the boost FET reaches the configured IMAX(B) limit, only the set limit current is provided and, consequently, the boosted VBST voltage droops. Step size is 100 mA. 000 0000–010 1100 Reserved                                   100 1010 (Default) 4.50 A 010 1101 1.60 A   100 1011 4.60 A 010 1110 1.70 A   ... ...   101 1101 6.4 A 100 1000 4.30 A   101 1110 6.5 A 100 1001 4.40 A   101 1111–111 1111 Reserved

### 7.5.4 SOFT\_RAMP

**I<sup>2</sup>C Address: 0x00 380C**

RW	31..8	7	6	5	4		3	2	1	0
	—		—				BST_SFT_RAMP			
Default	0x00 0000	0	0	0	0		0	0	1	1

Bits	Name	Description
31:4	—	Reserved
3:0	BST_SFT_RAMP	<p>Boost converter VBST voltage soft ramp. Configures how quickly the VBST voltage is allowed to change in response to a BST_CTL or target VBST voltage configuration change. This limits the amount of inrush or backpowering current associated with charging or discharging the C<sub>BST</sub> capacitor. Absolute time is based on a f<sub>PLL_OUT</sub> = 192 MHz. Larger values produce a slower change in voltage and are intended for use cases with large C<sub>BST</sub> values.</p> <p>0000 50.0mV/us (old reference of 0.1 V in 12/MCLKINT)      0001 33.3mV/us (old reference of 0.1 V in 18/MCLKINT)      0010 25.0mV/us (old reference of 0.1 V in 24/MCLKINT)      0011 (Default) 18.8 mV/us (old reference of 0.1V in 32/MCLKINT)      0100 12.5mV/us (old reference of 0.1 V in 48/MCLKINT)      0101 9.4mV/us (old reference of 0.1 V in 64/MCLKINT)      0110 4.7mV/us (old reference of 0.1 V in 128/MCLKINT)      0111 2.3mV/us (old reference of 0.1 V in 256/MCLKINT)      1000 1.2mV/us (old reference of 0.1 V in 512/MCLKINT)      1001 585mV/ms (old reference of 0.1 V in 1024/MCLKINT)      1010 292mV/ms (old reference of 0.1 V in 2048/MCLKINT)      1011 146mV/ms old reference of (0.1 V in 4096/MCLKINT)      1100 73mV/ms (old reference of 0.1 V in 8192/MCLKINT)      1101 36mV/ms (old reference of 0.1 V in 16384/MCLKINT)      1110 18mV/ms (old reference of 0.1 V in 32768/MCLKINT)      1111 9mV/ms (old reference of 0.1 V in 65536/MCLKINT)</p>

### 7.5.5 BST\_LOOP\_COEFF

**I<sup>2</sup>C Address: 0x00 3810**

RW	31..16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—					BST_K2								BST_K1			
Default	0x0000	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0

Bits	Name	Description
31:16	—	Reserved
15:8	BST_K2	<p>Along with BST_K1, adjusts the boost converter's feedback loop to compensate for the changes produced by using a different LBST inductance or different system requirements. See the functional description for more information and recommended configurations for various use cases.</p> <p><b>Note:</b> Adjusting for a lower inductance reduces the loop bandwidth.</p>
7:0	BST_K1	<p>Along with BST_K2, adjusts the boost converter's feedback loop to compensate for the changes produced by using a different LBST inductance or different system requirements. See the functional description for more information and recommended configurations for various use cases.</p> <p><b>Note:</b> Adjusting for a lower inductance reduces the loop bandwidth.</p>

### 7.5.6 LBST\_SLOPE

**I<sup>2</sup>C Address: 0x00 3814**

RW	31..16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—					BST_SLOPE								—		BST_LBST_VAL	
Default	0x0000	0	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description				
31:16	—	Reserved				
15:8	BST_SLOPE	Allows for adjustment of the boost converter's internal ramp-gen slope to compensate for the changes produced by using a different LBST inductance. See the functional description for more information.				
7:2	—	Reserved				
1:0	BST_LBST_VAL	<p>Inductor estimation LBST reference value. Seeds the digital boost converter's inductor estimation block with the initial inductance value to reference.</p> <table style="margin-left: 20px;"> <tr> <td>00 (Default) 1.0 uH</td> <td>10 1.5 uH</td> </tr> <tr> <td>01 1.2 uH</td> <td>11 2.2 uH</td> </tr> </table>	00 (Default) 1.0 uH	10 1.5 uH	01 1.2 uH	11 2.2 uH
00 (Default) 1.0 uH	10 1.5 uH					
01 1.2 uH	11 2.2 uH					

### 7.5.7 BST\_SW\_FREQ

**I<sup>2</sup>C Address: 0x00 3818**

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	BST_DCM_FREQ_MIN					—				BST_DCM_FREQ				—				BST_CCM_FREQ									BST_CCM_FREQ						
Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:24	BST_DCM_FREQ_MIN	Boost converter's minimum DCM mode switching frequency. Configures the minimum allowable net switching frequency the boost converter can produce while operating in DCM Mode. The maximum allowable number of consecutive skipped periods is set by BST_DCM_FREQ_MIN. If the BST_DCM_FREQ_MIN = 0, then no switching period is allowed to be skipped; if BST_DCM_FREQ_MIN = 1, then 1 switching period is allowed to be skipped, etc. The minimum allowable switching period = BST_DCM_FREQ/(BST_DCM_FREQ_MIN+1) MHz.  0000 0000 DCM mode frequency skipping disabled (BST_DCM_FREQ/1) 0000 0001 (Default) BST_DCM_FREQ/2 0000 0010 BST_DCM_FREQ/3 0000 0011 BST_DCM_FREQ/4  ... 1111 1110 BST_DCM_FREQ/255 1111 1111 BST_DCM_FREQ/256
23:18	—	Reserved
17:8	BST_DCM_FREQ	Boost converter's DCM mode switching frequency. Configures the base rate net switching frequency when operating in DCM Mode. All frequencies listed with a f <sub>PLL_OUT</sub> of 192 MHz. Other f <sub>PLL_OUT</sub> frequencies scale ratiometrically. Step size: f <sub>PLL_OUT</sub> /(8*(12+n)) MHz.  0x000 2.00000 MHz 0x080 (Default) 0.17143 MHz 0x001 1.84615 MHz ... 0x002 1.71429 MHz 0x3FE 0.02321 MHz ... 0x3FF 0.02319 MHz
7:4	—	Reserved
3:0	BST_CCM_FREQ	Boost converter's CCM mode switching frequency. Controls the fundamental output switching frequency of the digital boost converter's net when operating in CCM mode. The frequency listed is based on a f <sub>PLL_OUT</sub> = 192 MHz. Other f <sub>PLL_OUT</sub> frequencies scale ratiometrically.  0000 (Default) 2.000 MHz 1000 1.200 MHz 0001 1.846 MHz 1001 1.143 MHz 0010 1.714 MHz 1010 1.091 MHz 0011 1.600 MHz 1011 1.043 MHz 0100 1.500 MHz 1100 1.000 MHz 0101 1.412 MHz 1101 0.960 MHz 0110 1.333 MHz 1110 0.923 MHz 0111 1.263 MHz 1111 0.889 MHz

### 7.5.8 BST\_DCM\_CTL

**I<sup>2</sup>C Address: 0x00 381C**

RW	31..16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—					BST_DCM_EXIT_SEL			BST_DCM_ENTRY_SEL			—				BST_DCM_EN
Default	0x0000	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description
31:8	—	Reserved
7:6	BST_DCM_EXIT_SEL	Boost converter DCM exit source selection. Selects the signal source for the automatic DCM exit to CCM Mode. 00 (Default) Reserved. 01 Level-dependent muting control triggers DCM Mode exit 10 Reserved 11 Automatic load detection disabled. User must manually force in/out of DCM Mode via BST_DCM_FRC registers.

Bits	Name	Description
5:4	BST_DCM_ENTRY_SEL	Boost converter DCM entry source selection. Selects the signal source for the automatic DCM entry from CCM Mode. 00 (Default) Reserved. 01 Level-dependent muting control triggers DCM Mode entry 10 Reserved 11 Automatic load detection disabled. User must manually force in/out DCM Mode via BST_DCM_FRC registers.
3:1	—	Reserved
0	BST_AUTO_DCM_EN	Boost converter automatic DCM Mode enable. This enables the digital boost converter to operate in a low power (DCM) mode during low loading conditions. 0 Boost converter automatic low power mode disabled 1 (Default) Boost converter automatic low power mode enabled

### 7.5.9 DCM\_FORCE

**I<sup>2</sup>C Address: 0x00 3820**

RW	31...8	7	6	5	4	—	3	2	1	0
	—					—			BST_DCM_FRC_EN	BST_DCM_FRC
Default	0x00 0000	0	0	0	0	—	0	0	0	0

Bits	Name	Description
31:2	—	Reserved
1	BST_DCM_FRC_EN	Boost converter DCM force mode control enable. Setting this field enables the DCM/CCM control functionality of BST_DCM_FRC. Do not force the boost converter in to DCM Mode when there is a load greater than 8 mA on the VBST supply. Device damage may occur. 0 (Default) BST_DCM_FRC control disabled 1 BST_DCM_FRC control enabled
0	BST_DCM_FRC	Force the boost converter to operate in DCM Mode. When enabled by BST_DCM_FRC_EN, manually puts the boost converter in either DCM Mode or CCM Mode. When BST_DCM_FRC_EN = 0, this control has no functionality. [Sequence: 0 -> 1]: Force transition to DCM Mode [Sequence: 1 -> 0]: Force transition to CCM mode 0 (Default) Remain in CCM mode when automatic control is disabled (BST_AUTO_DCM_EN = 0) 1 Remain in DCM mode if no error condition is present and automatic control disabled (BST_AUTO_DCM_EN = 0).

### 7.5.10 VBST\_OVP

**I<sup>2</sup>C Address: 0x00 3830**

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—					—			BST_OVP_EN	—				BST_OVP_THLD			
Default	0x0000	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0

Bits	Name	Description
31:9	—	Reserved
8	BST_OVP_EN	Boost converter overvoltage protection enable. Setting to 0 disabled the boost converter active protection limit (configured by BST_OVP_THLD). This has no impact on the VBST overvoltage error protection (BST_VBST_ERR). 0 Overvoltage protection disabled 1 (Default) Overvoltage protection enabled
7:6	—	Reserved
5:0	BST_OVP_THLD	Boost converter overvoltage protection limit. Threshold to actively limit any VBST voltage overshoot caused by a rapid load change. Intended to allow for the protection of external components such as C <sub>BST</sub> . Step size: 0.0625V. 00 0000 10.0000 V 00 0001 10.0625 V 00 0010 10.1250 V ... 11 1110 13.8750 V 11 1111 13.9375 V

## 7.6 VMON1 and IMON Signal Monitoring (VIMON1)

### 7.6.1 SPKMON\_FILTERS

**I<sup>2</sup>C Address: 0x00 4004**

RW	31...8	7	6	5	4	—	3	2	1	0
Default	0x00 0000	0	0	0	0	—	0	0	1	1
									IMON_POL	VMON1_POL

Bits	Name	Description
31:2	—	Reserved
1	IMON_POL	IMON output polarity control. Configures the polarity of the IMON monitor signal relative to the amplifier's output. 0 Inverted 1 (Default) Not inverted
0	VMON1_POL	VMON1 output polarity control. Configures the polarity of the VMON1 monitor signal relative to the amplifier's output. 0 Inverted 1 (Default) Not inverted

## 7.7 Die Temperature Monitoring (TEMPMON)

### 7.7.1 WARN\_LIMIT\_THRESHOLD

**I<sup>2</sup>C Address: 0x00 4220**

RW	31...8	7	6	5	4	—	3	2	1	0
Default	0x00 0000	0	0	0	0	—	0	0	1	0
									TEMP_WARN_THLD	

Bits	Name	Description
31:2	—	Reserved
1:0	TEMP_WARN_THLD	Amplifier overtemperature warning threshold. Configures the threshold at which the overtemperature warning condition occurs. When the threshold is met, the overtemperature warning attenuation is applied and the TEMP_WARN_EINT interrupt status bit is set. If TEMP_WARN_MASK = 0, INTb is asserted. 00 105 °C 01 115 °C 10 (Default) 125 °C 11 135 °C

### 7.7.2 STATUS

**I<sup>2</sup>C Address: 0x00 4300**

RO	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TEMPMON_ON_ENABLE_D	TEMP_IS_VALID								—						
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	—				TEMPMON_ON_ERR_STS	TEMPMON_ON_WARN_STS		

Bits	Name	Description
31	TEMPMON_ENABLED	TEMPMON enable status. Reports the status if the die temperature monitoring function is enabled by the user or other functionality. See functional description section for details on other functionalities that may enable TEMPMON. 0 (Default) Disabled 1 Enabled
30	TEMP_IS_VALID	TEMPMON function valid status. Reports the status if the die temperature monitoring is functioning normally. 0 (Default) Not normal 1 Normal

Bits	Name	Description
29:2	—	Reserved
1	TEMPMON_ERR_STS	Overtemperature error status. Reports the status if the die temperature has exceeded the overtemperature error threshold. 0 (Default) Overtemperature error condition inactive 1 Overtemperature error condition active
0	TEMPMON_WARN_STS	Overtemperature warning status. Reports the status if the die temperature has exceeded the overtemperature warning threshold. 0 (Default) Overtemperature warning condition inactive 1 Overtemperature warning condition active

## 7.8 Audio Serial Port Data Interface (DATAIF)

### 7.8.1 ASP\_TX\_PIN\_BCK\_CTRL

**I<sup>2</sup>C Address: 0x00 4800**

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	ASP_TX_HIZ_DLY	—	—	—	ASP_TX_DAT_HIZ	—	—	—	—	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ASP_BCK_INV	—	—	—	—	—	ASP_BCK_FREQ	—	—	—
Default	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

Bits	Name	Description
31:26	—	Reserved
25:24	ASP_TX_HIZ_DLY	Audio serial port data transmit Hi-Z delay. Refer to the electrical characteristics for timing figures. 00 (Default) No additional delay in de-asserting Hi-Z operation during unused timeslots; 11 ns 01 15 ns 10 20 ns 11 25 ns
23:22	—	Reserved
21	ASP_TX_DAT_HIZ	Audio serial port data transmit Hi-Z control. 0 (Default) is actively driven low (logic 0) during unused time slots 1 is Hi-Z during unused time slots
20:9	—	Reserved
8	ASP_BCK_INV	Audio serial port audio interface inversion control. 0 (Default) ASP not inverted 1 ASP inverted

Bits	Name	Description																																																																																																												
7:6	—	Reserved																																																																																																												
5:0	ASP_BCK_FREQ	<p>ASP frequency.</p> <table> <tbody> <tr><td>000000–00 1011</td><td>Reserved</td><td>10 0110</td><td>5,644,800</td></tr> <tr><td>00 1100</td><td>128,000</td><td>10 0111</td><td>6,000,000</td></tr> <tr><td>00 1101</td><td>176,400</td><td>10 1000</td><td>(Default) 6,144,000</td></tr> <tr><td>00 1110</td><td>192,000</td><td>10 1001</td><td>6,250,000</td></tr> <tr><td>00 1111</td><td>256,000</td><td>10 1010</td><td>6,400,000</td></tr> <tr><td>01 0000</td><td>352,800</td><td>10 1011</td><td>6,500,000</td></tr> <tr><td>01 0001</td><td>384,000</td><td>10 1100</td><td>6,750,000</td></tr> <tr><td>01 0010</td><td>512,000</td><td>10 1101</td><td>7,526,400</td></tr> <tr><td>01 0011</td><td>705,600</td><td>10 1110</td><td>8,000,000</td></tr> <tr><td>01 0100</td><td>750,000</td><td>10 1111</td><td>8,192,000</td></tr> <tr><td>01 0101</td><td>768,000</td><td>11 0000</td><td>9,600,000</td></tr> <tr><td>01 0110</td><td>1,000,000</td><td>11 0001</td><td>11,289,600</td></tr> <tr><td>01 0111</td><td>1,024,000</td><td>11 0010</td><td>12,000,000</td></tr> <tr><td>01 1000</td><td>1,200,000</td><td>11 0011</td><td>12,288,000</td></tr> <tr><td>01 1001</td><td>1,411,200</td><td>11 0100</td><td>12,500,000</td></tr> <tr><td>01 1010</td><td>1,500,000</td><td>11 0101</td><td>12,800,000</td></tr> <tr><td>01 1011</td><td>1,536,000</td><td>11 0110</td><td>13,000,000</td></tr> <tr><td>01 1100</td><td>2,000,000</td><td>11 0111</td><td>13,500,000</td></tr> <tr><td>01 1101</td><td>2,048,000</td><td>11 1000</td><td>19,200,000</td></tr> <tr><td>01 1110</td><td>2,400,000</td><td>11 1001</td><td>22,579,200</td></tr> <tr><td>01 1111</td><td>2,822,400</td><td>11 1010</td><td>24,000,000</td></tr> <tr><td>10 0000</td><td>3,000,000</td><td>11 1011</td><td>24,576,000</td></tr> <tr><td>10 0001</td><td>3,072,000</td><td>11 1100–11 1111</td><td>Reserved</td></tr> <tr><td>10 0010</td><td>3,200,000</td><td></td><td></td></tr> <tr><td>10 0011</td><td>4,000,000</td><td></td><td></td></tr> <tr><td>10 0100</td><td>4,096,000</td><td></td><td></td></tr> <tr><td>10 0101</td><td>4,800,000</td><td></td><td></td></tr> </tbody> </table>	000000–00 1011	Reserved	10 0110	5,644,800	00 1100	128,000	10 0111	6,000,000	00 1101	176,400	10 1000	(Default) 6,144,000	00 1110	192,000	10 1001	6,250,000	00 1111	256,000	10 1010	6,400,000	01 0000	352,800	10 1011	6,500,000	01 0001	384,000	10 1100	6,750,000	01 0010	512,000	10 1101	7,526,400	01 0011	705,600	10 1110	8,000,000	01 0100	750,000	10 1111	8,192,000	01 0101	768,000	11 0000	9,600,000	01 0110	1,000,000	11 0001	11,289,600	01 0111	1,024,000	11 0010	12,000,000	01 1000	1,200,000	11 0011	12,288,000	01 1001	1,411,200	11 0100	12,500,000	01 1010	1,500,000	11 0101	12,800,000	01 1011	1,536,000	11 0110	13,000,000	01 1100	2,000,000	11 0111	13,500,000	01 1101	2,048,000	11 1000	19,200,000	01 1110	2,400,000	11 1001	22,579,200	01 1111	2,822,400	11 1010	24,000,000	10 0000	3,000,000	11 1011	24,576,000	10 0001	3,072,000	11 1100–11 1111	Reserved	10 0010	3,200,000			10 0011	4,000,000			10 0100	4,096,000			10 0101	4,800,000		
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### 7.8.2 ASP\_RATE\_FS\_PIN\_CTRL

 I<sup>2</sup>C Address: 0x00 4804

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ASP_TX_RATE				—				ASP_RX_RATE				—			
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				—				—				ASP_FS_INV	—	—	
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:27	ASP_TX_RATE	Do not modify this field from the default setting when changing other fields in this register.
26:24	—	Reserved
23:19	ASP_RX_RATE	Do not modify this field from the default setting when changing other fields in this register.
18:17	—	Reserved
16	ASP_HIZ_FRC	Audio serial port Hi-Z force control. Forces the audio serial port pin(s) which are configured as outputs to go to a Hi-Z state. 0 Normal 1 (Default) ASP output pins are forced to Hi-Z
15:3	—	Reserved
2	ASP_FS_INV	Audio serial port polarity inversion control. 0 (Default) ASP not inverted 1 ASP inverted
1:0	—	Reserved

### 7.8.3 ASP\_FORMAT

**I<sup>2</sup>C Address: 0x00 4808**

RW	31..8	7	6	5	4	3	2	1	0
	—			—				ASP_FMT	
Default	0x00 0000	0	0	0	0	0	0	1	0

Bits	Name	Description
31:3	—	Reserved
2:0	ASP_FMT	<p>Audio serial port interface format. This field is locked when any serial port channels are enabled. Disable all audio serial port channels (ASP_x_EN) prior to changing the configured format.</p> <ul style="list-style-type: none"> <li>000 TDM 1 (DSP Mode A)</li> <li>001 Reserved</li> <li>010 (Default) I<sup>2</sup>S mode</li> <li>011 Reserved</li> <li>100 TDM 1.5 (TDM 1 with RX is relative to the negative edge of )</li> <li>101 –111 Reserved</li> </ul>

### 7.8.4 ASP\_FRAME\_CTRL\_1

**I<sup>2</sup>C Address: 0x00 4818**

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				ASP_RX_WIDTH								—				ASP_TX_WIDTH															
Default	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	

Bits	Name	Description																																																																																																																																																																																																																																																																								
31:24	—	Reserved																																																																																																																																																																																																																																																																								
23:16	ASP_RX_WIDTH	<p>Audio serial port RX slot width and data width. Configures the number of cycles per RX slot. Slot width is valid from 12 to 128; data width is valid from 12 to 24.</p> <table> <tr><td>0000 0000</td><td>Not supported</td><td>0100 0110</td><td>Slot width: 70, data width: 24</td></tr> <tr><td>00000001–0000 1011</td><td>Reserved</td><td>0100 0111</td><td>Slot width: 71, data width: 24</td></tr> <tr><td>0000 1100</td><td>Slot width: 12, data width: 12</td><td>0100 1000</td><td>Slot width: 72, data width: 24</td></tr> <tr><td>0000 1101</td><td>Slot width: 13, data width: 13</td><td>0100 1001</td><td>Slot width: 73, data width: 24</td></tr> <tr><td>0000 1110</td><td>Slot width: 14, data width: 14</td><td>0100 1010</td><td>Slot width: 74, data width: 24</td></tr> <tr><td>0000 1111</td><td>Slot width: 15, data width: 15</td><td>0100 1011</td><td>Slot width: 75, data width: 24</td></tr> <tr><td>0001 0000</td><td>Slot width: 16, data width: 16</td><td>0100 1100</td><td>Slot width: 76, data width: 24</td></tr> <tr><td>0001 0001</td><td>Slot width: 17, data width: 17</td><td>0100 1101</td><td>Slot width: 77, data width: 24</td></tr> <tr><td>0001 0010</td><td>Slot width: 18, data width: 18</td><td>0100 1110</td><td>Slot width: 78, data width: 24</td></tr> <tr><td>0001 0011</td><td>Slot width: 19, data width: 19</td><td>0100 1111</td><td>Slot width: 79, data width: 24</td></tr> <tr><td>0001 0100</td><td>Slot width: 20, data width: 20</td><td>0101 0000</td><td>Slot width: 80, data width: 24</td></tr> <tr><td>0001 0101</td><td>Slot width: 21, data width: 21</td><td>0101 0001</td><td>Slot width: 81, data width: 24</td></tr> <tr><td>0001 0110</td><td>Slot width: 22, data width: 22</td><td>0101 0010</td><td>Slot width: 82, data width: 24</td></tr> <tr><td>0001 0111</td><td>Slot width: 23, data width: 23</td><td>0101 0011</td><td>Slot width: 83, data width: 24</td></tr> <tr><td>0001 1000</td><td>(Default) Slot width: 24, data width: 24</td><td>0101 0100</td><td>Slot width: 84, data width: 24</td></tr> <tr><td>0001 1001</td><td>Slot width: 25, data width: 24</td><td>0101 0101</td><td>Slot width: 85, data width: 24</td></tr> <tr><td>0001 1010</td><td>Slot width: 26, data width: 24</td><td>0101 0110</td><td>Slot width: 86, data width: 24</td></tr> <tr><td>0001 1011</td><td>Slot width: 27, data width: 24</td><td>0101 0111</td><td>Slot width: 87, data width: 24</td></tr> <tr><td>0001 1100</td><td>Slot width: 28, data width: 24</td><td>0101 1000</td><td>Slot width: 88, data width: 24</td></tr> <tr><td>0001 1101</td><td>Slot width: 29, data width: 24</td><td>0101 1001</td><td>Slot width: 89, data width: 24</td></tr> <tr><td>0001 1110</td><td>Slot width: 30, data width: 24</td><td>0101 1010</td><td>Slot width: 90, data width: 24</td></tr> <tr><td>0001 1111</td><td>Slot width: 31, data width: 24</td><td>0101 1011</td><td>Slot width: 91, data width: 24</td></tr> <tr><td>0010 0000</td><td>Slot width: 32, data width: 24</td><td>0101 1100</td><td>Slot width: 92, data width: 24</td></tr> <tr><td>0010 0001</td><td>Slot width: 33, data width: 24</td><td>0101 1101</td><td>Slot width: 93, data width: 24</td></tr> <tr><td>0010 0010</td><td>Slot width: 34, data width: 24</td><td>0101 1110</td><td>Slot width: 94, data width: 24</td></tr> <tr><td>0010 0011</td><td>Slot width: 35, data width: 24</td><td>0101 1111</td><td>Slot width: 95, data width: 24</td></tr> <tr><td>0010 0100</td><td>Slot width: 36, data width: 24</td><td>0110 0000</td><td>Slot width: 96, data width: 24</td></tr> <tr><td>0010 0101</td><td>Slot width: 37, data width: 24</td><td>0110 0001</td><td>Slot width: 97, data width: 24</td></tr> <tr><td>0010 0110</td><td>Slot width: 38, data width: 24</td><td>0110 0010</td><td>Slot width: 98, data width: 24</td></tr> <tr><td>0010 0111</td><td>Slot width: 39, data width: 24</td><td>0110 0011</td><td>Slot width: 99, data width: 24</td></tr> <tr><td>0010 1000</td><td>Slot width: 40, data width: 24</td><td>0110 0100</td><td>Slot width: 100, data width: 24</td></tr> <tr><td>0010 1001</td><td>Slot width: 41, data width: 24</td><td>0110 0101</td><td>Slot width: 101, data width: 24</td></tr> <tr><td>0010 1010</td><td>Slot width: 42, data width: 24</td><td>0110 0110</td><td>Slot width: 102, data width: 24</td></tr> <tr><td>0010 1011</td><td>Slot width: 43, data width: 24</td><td>0110 0111</td><td>Slot width: 103, data width: 24</td></tr> <tr><td>0010 1100</td><td>Slot width: 44, data width: 24</td><td>0110 1000</td><td>Slot width: 104, data width: 24</td></tr> <tr><td>0010 1101</td><td>Slot width: 45, data width: 24</td><td>0110 1001</td><td>Slot width: 105, data width: 24</td></tr> <tr><td>0010 1110</td><td>Slot width: 46, data width: 24</td><td>0110 1010</td><td>Slot width: 106, data width: 24</td></tr> <tr><td>0010 1111</td><td>Slot width: 47, data width: 24</td><td>0110 1011</td><td>Slot width: 107, data width: 24</td></tr> <tr><td>0011 0000</td><td>Slot width: 48, data width: 24</td><td>0110 1100</td><td>Slot width: 108, data width: 24</td></tr> <tr><td>0011 0001</td><td>Slot width: 49, data width: 24</td><td>0110 1101</td><td>Slot width: 109, data width: 24</td></tr> <tr><td>0011 0010</td><td>Slot width: 50, data width: 24</td><td>0110 1110</td><td>Slot width: 110, data width: 24</td></tr> <tr><td>0011 0011</td><td>Slot width: 51, data width: 24</td><td>0110 1111</td><td>Slot width: 111, data width: 24</td></tr> <tr><td>0011 0100</td><td>Slot width: 52, data width: 24</td><td>0111 0000</td><td>Slot width: 112, data width: 24</td></tr> <tr><td>0011 0101</td><td>Slot width: 53, data width: 24</td><td>0111 0001</td><td>Slot width: 113, data width: 24</td></tr> <tr><td>0011 0110</td><td>Slot width: 54, data width: 24</td><td>0111 0010</td><td>Slot width: 114, data width: 24</td></tr> <tr><td>0011 0111</td><td>Slot width: 55, data width: 24</td><td>0111 0011</td><td>Slot width: 115, data width: 24</td></tr> <tr><td>0011 1000</td><td>Slot width: 56, data width: 24</td><td>0111 0100</td><td>Slot width: 116, data width: 24</td></tr> <tr><td>0011 1001</td><td>Slot width: 57, data width: 24</td><td>0111 0101</td><td>Slot width: 117, data width: 24</td></tr> <tr><td>0011 1010</td><td>Slot width: 58, data width: 24</td><td>0111 0110</td><td>Slot width: 118, data width: 24</td></tr> <tr><td>0011 1011</td><td>Slot width: 59, data width: 24</td><td>0111 0111</td><td>Slot width: 119, data width: 24</td></tr> <tr><td>0011 1100</td><td>Slot width: 60, data width: 24</td><td>0111 1000</td><td>Slot width: 120, data width: 24</td></tr> <tr><td>0011 1101</td><td>Slot width: 61, data width: 24</td><td>0111 1001</td><td>Slot width: 121, data width: 24</td></tr> <tr><td>0011 1110</td><td>Slot width: 62, data width: 24</td><td>0111 1010</td><td>Slot width: 122, data width: 24</td></tr> <tr><td>0011 1111</td><td>Slot width: 63, data width: 24</td><td>0111 1011</td><td>Slot width: 123, data width: 24</td></tr> <tr><td>0100 0000</td><td>Slot width: 64, data width: 24</td><td>0111 1100</td><td>Slot width: 124, data width: 24</td></tr> <tr><td>0100 0001</td><td>Slot width: 65, data width: 24</td><td>0111 1101</td><td>Slot width: 125, data width: 24</td></tr> <tr><td>0100 0010</td><td>Slot width: 66, data width: 24</td><td>0111 1110</td><td>Slot width: 126, data width: 24</td></tr> <tr><td>0100 0011</td><td>Slot width: 67, data width: 24</td><td>0111 1111</td><td>Slot width: 127, data width: 24</td></tr> <tr><td>0100 0100</td><td>Slot width: 68, data width: 24</td><td>1000 0000</td><td>Slot width: 128, data width: 24</td></tr> <tr><td>0100 0101</td><td>Slot width: 69, data width: 24</td><td colspan="8">10000001–1111 1111 Reserved</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr> </table>	0000 0000	Not supported	0100 0110	Slot width: 70, data width: 24	00000001–0000 1011	Reserved	0100 0111	Slot width: 71, data width: 24	0000 1100	Slot width: 12, data width: 12	0100 1000	Slot width: 72, data width: 24	0000 1101	Slot width: 13, data width: 13	0100 1001	Slot width: 73, data width: 24	0000 1110	Slot width: 14, data width: 14	0100 1010	Slot width: 74, data width: 24	0000 1111	Slot width: 15, data width: 15	0100 1011	Slot width: 75, data width: 24	0001 0000	Slot width: 16, data width: 16	0100 1100	Slot width: 76, data width: 24	0001 0001	Slot width: 17, data width: 17	0100 1101	Slot width: 77, data width: 24	0001 0010	Slot width: 18, data width: 18	0100 1110	Slot width: 78, data width: 24	0001 0011	Slot width: 19, data width: 19	0100 1111	Slot width: 79, data width: 24	0001 0100	Slot width: 20, data width: 20	0101 0000	Slot width: 80, data width: 24	0001 0101	Slot width: 21, data width: 21	0101 0001	Slot width: 81, data width: 24	0001 0110	Slot width: 22, data width: 22	0101 0010	Slot width: 82, data width: 24	0001 0111	Slot width: 23, data width: 23	0101 0011	Slot width: 83, data width: 24	0001 1000	(Default) Slot width: 24, data width: 24	0101 0100	Slot width: 84, data width: 24	0001 1001	Slot width: 25, data width: 24	0101 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97, data width: 24	0010 0110	Slot width: 38, data width: 24	0110 0010	Slot width: 98, data width: 24	0010 0111	Slot width: 39, data width: 24	0110 0011	Slot width: 99, data width: 24	0010 1000	Slot width: 40, data width: 24	0110 0100	Slot width: 100, data width: 24	0010 1001	Slot width: 41, data width: 24	0110 0101	Slot width: 101, data width: 24	0010 1010	Slot width: 42, data width: 24	0110 0110	Slot width: 102, data width: 24	0010 1011	Slot width: 43, data width: 24	0110 0111	Slot width: 103, data width: 24	0010 1100	Slot width: 44, data width: 24	0110 1000	Slot width: 104, data width: 24	0010 1101	Slot width: 45, data width: 24	0110 1001	Slot width: 105, data width: 24	0010 1110	Slot width: 46, data width: 24	0110 1010	Slot width: 106, data width: 24	0010 1111	Slot width: 47, data width: 24	0110 1011	Slot width: 107, data width: 24	0011 0000	Slot width: 48, data width: 24	0110 1100	Slot width: 108, data width: 24	0011 0001	Slot width: 49, data width: 24	0110 1101	Slot width: 109, data width: 24	0011 0010	Slot width: 50, data width: 24	0110 1110	Slot width: 110, data width: 24	0011 0011	Slot width: 51, data width: 24	0110 1111	Slot width: 111, data width: 24	0011 0100	Slot width: 52, data width: 24	0111 0000	Slot width: 112, data width: 24	0011 0101	Slot width: 53, data width: 24	0111 0001	Slot width: 113, data width: 24	0011 0110	Slot width: 54, data width: 24	0111 0010	Slot width: 114, data width: 24	0011 0111	Slot width: 55, data width: 24	0111 0011	Slot width: 115, data width: 24	0011 1000	Slot width: 56, data width: 24	0111 0100	Slot width: 116, data width: 24	0011 1001	Slot width: 57, data width: 24	0111 0101	Slot width: 117, data width: 24	0011 1010	Slot width: 58, data width: 24	0111 0110	Slot width: 118, data width: 24	0011 1011	Slot width: 59, data width: 24	0111 0111	Slot width: 119, data width: 24	0011 1100	Slot width: 60, data width: 24	0111 1000	Slot width: 120, data width: 24	0011 1101	Slot width: 61, data width: 24	0111 1001	Slot width: 121, data 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Slot width is valid from 12 to 128; data width is valid from 12 to 24.</p> <table> <tbody> <tr><td>0000 0000</td><td>Not supported</td><td>0100 0110 Slot width: 70, data width: 24</td></tr> <tr><td>00000001–0000 1011</td><td>Reserved</td><td>0100 0111 Slot width: 71, data width: 24</td></tr> <tr><td>0000 1100</td><td>Slot width: 12, data width: 12</td><td>0100 1000 Slot width: 72, data width: 24</td></tr> <tr><td>0000 1101</td><td>Slot width: 13, data width: 13</td><td>0100 1001 Slot width: 73, data width: 24</td></tr> <tr><td>0000 1110</td><td>Slot width: 14, data width: 14</td><td>0100 1010 Slot width: 74, data width: 24</td></tr> <tr><td>0000 1111</td><td>Slot width: 15, data width: 15</td><td>0100 1011 Slot width: 75, data width: 24</td></tr> <tr><td>0001 0000</td><td>Slot width: 16, data width: 16</td><td>0100 1100 Slot width: 76, data width: 24</td></tr> <tr><td>0001 0001</td><td>Slot width: 17, data width: 17</td><td>0100 1101 Slot width: 77, data width: 24</td></tr> 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0101</td><td>Slot width: 69, data width: 24</td><td>10000001–1111 1111 Reserved</td></tr> </tbody> </table>	0000 0000	Not supported	0100 0110 Slot width: 70, data width: 24	00000001–0000 1011	Reserved	0100 0111 Slot width: 71, data width: 24	0000 1100	Slot width: 12, data width: 12	0100 1000 Slot width: 72, data width: 24	0000 1101	Slot width: 13, data width: 13	0100 1001 Slot width: 73, data width: 24	0000 1110	Slot width: 14, data width: 14	0100 1010 Slot width: 74, data width: 24	0000 1111	Slot width: 15, data width: 15	0100 1011 Slot width: 75, data width: 24	0001 0000	Slot width: 16, data width: 16	0100 1100 Slot width: 76, data width: 24	0001 0001	Slot width: 17, data width: 17	0100 1101 Slot width: 77, data width: 24	0001 0010	Slot width: 18, data width: 18	0100 1110 Slot width: 78, data width: 24	0001 0011	Slot width: 19, data width: 19	0100 1111 Slot width: 79, data width: 24	0001 0100	Slot width: 20, data width: 20	0101 0000 Slot width: 80, data width: 24	0001 0101	Slot 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33, data width: 24	0101 1101 Slot width: 93, data width: 24	0010 0010	Slot width: 34, data width: 24	0101 1110 Slot width: 94, data width: 24	0010 0011	Slot width: 35, data width: 24	0101 1111 Slot width: 95, data width: 24	0010 0100	Slot width: 36, data width: 24	0110 0000 Slot width: 96, data width: 24	0010 0101	Slot width: 37, data width: 24	0110 0001 Slot width: 97, data width: 24	0010 0110	Slot width: 38, data width: 24	0110 0010 Slot width: 98, data width: 24	0010 0111	Slot width: 39, data width: 24	0110 0011 Slot width: 99, data width: 24	0010 1000	Slot width: 40, data width: 24	0110 0100 Slot width: 100, data width: 24	0010 1001	Slot width: 41, data width: 24	0110 0101 Slot width: 101, data width: 24	0010 1010	Slot width: 42, data width: 24	0110 0110 Slot width: 102, data width: 24	0010 1011	Slot width: 43, data width: 24	0110 0111 Slot width: 103, data width: 24	0010 1100	Slot width: 44, data width: 24	0110 1000 Slot width: 104, data width: 24	0010 1101	Slot width: 45, data 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### 7.8.5 ASP\_FRAME\_CTRL\_2

**I<sup>2</sup>C Address: 0x00 481C**

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
	—														ASP_TX2_SLOT	—														ASP_TX1_SLOT							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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31:22	—	Reserved																																																																																																																																	
21:16	ASP_TX2_SLOT	<p>Audio serial port TX channel 2 data packet slot location. Configures the TX location of the channel 2 data packet relative to the start of the sample frame. The ASP frame format is defined by the configuration of ASP_FMT.</p> <p>Step size: 1 slot location. Use of slot locations beyond the end of the ASP frame are not supported.</p> <table> <tr><td>00 0000</td><td>Slot 0</td><td>10 0000</td><td>Slot 32</td></tr> <tr><td>00 0001</td><td>(Default) Slot 1</td><td>10 0001</td><td>Slot 33</td></tr> <tr><td>00 0010</td><td>Slot 2</td><td>10 0010</td><td>Slot 34</td></tr> <tr><td>00 0011</td><td>Slot 3</td><td>10 0011</td><td>Slot 35</td></tr> <tr><td>00 0100</td><td>Slot 4</td><td>10 0100</td><td>Slot 36</td></tr> <tr><td>00 0101</td><td>Slot 5</td><td>10 0101</td><td>Slot 37</td></tr> <tr><td>00 0110</td><td>Slot 6</td><td>10 0110</td><td>Slot 38</td></tr> <tr><td>00 0111</td><td>Slot 7</td><td>10 0111</td><td>Slot 39</td></tr> <tr><td>00 1000</td><td>Slot 8</td><td>10 1000</td><td>Slot 40</td></tr> <tr><td>00 1001</td><td>Slot 9</td><td>10 1001</td><td>Slot 41</td></tr> <tr><td>00 1010</td><td>Slot 10</td><td>10 1010</td><td>Slot 42</td></tr> <tr><td>00 1011</td><td>Slot 11</td><td>10 1011</td><td>Slot 43</td></tr> <tr><td>00 1100</td><td>Slot 12</td><td>10 1100</td><td>Slot 44</td></tr> <tr><td>00 1101</td><td>Slot 13</td><td>10 1101</td><td>Slot 45</td></tr> <tr><td>00 1110</td><td>Slot 14</td><td>10 1110</td><td>Slot 46</td></tr> <tr><td>00 1111</td><td>Slot 15</td><td>10 1111</td><td>Slot 47</td></tr> <tr><td>01 0000</td><td>Slot 16</td><td>11 0000</td><td>Slot 48</td></tr> <tr><td>01 0001</td><td>Slot 17</td><td>11 0001</td><td>Slot 49</td></tr> <tr><td>01 0010</td><td>Slot 18</td><td>11 0010</td><td>Slot 50</td></tr> <tr><td>01 0011</td><td>Slot 19</td><td>11 0011</td><td>Slot 51</td></tr> <tr><td>01 0100</td><td>Slot 20</td><td>11 0100</td><td>Slot 52</td></tr> <tr><td>01 0101</td><td>Slot 21</td><td>11 0101</td><td>Slot 53</td></tr> <tr><td>01 0110</td><td>Slot 22</td><td>11 0110</td><td>Slot 54</td></tr> <tr><td>01 0111</td><td>Slot 23</td><td>11 0111</td><td>Slot 55</td></tr> <tr><td>01 1000</td><td>Slot 24</td><td>11 1000</td><td>Slot 56</td></tr> <tr><td>01 1001</td><td>Slot 25</td><td>11 1001</td><td>Slot 57</td></tr> <tr><td>01 1010</td><td>Slot 26</td><td>11 1010</td><td>Slot 58</td></tr> <tr><td>01 1011</td><td>Slot 27</td><td>11 1011</td><td>Slot 59</td></tr> <tr><td>01 1100</td><td>Slot 28</td><td>11 1100</td><td>Slot 60</td></tr> <tr><td>01 1101</td><td>Slot 29</td><td>11 1101</td><td>Slot 61</td></tr> <tr><td>01 1110</td><td>Slot 30</td><td>11 1110</td><td>Slot 62</td></tr> <tr><td>01 1111</td><td>Slot 31</td><td>11 1111</td><td>Slot 63</td></tr> </table>	00 0000	Slot 0	10 0000	Slot 32	00 0001	(Default) Slot 1	10 0001	Slot 33	00 0010	Slot 2	10 0010	Slot 34	00 0011	Slot 3	10 0011	Slot 35	00 0100	Slot 4	10 0100	Slot 36	00 0101	Slot 5	10 0101	Slot 37	00 0110	Slot 6	10 0110	Slot 38	00 0111	Slot 7	10 0111	Slot 39	00 1000	Slot 8	10 1000	Slot 40	00 1001	Slot 9	10 1001	Slot 41	00 1010	Slot 10	10 1010	Slot 42	00 1011	Slot 11	10 1011	Slot 43	00 1100	Slot 12	10 1100	Slot 44	00 1101	Slot 13	10 1101	Slot 45	00 1110	Slot 14	10 1110	Slot 46	00 1111	Slot 15	10 1111	Slot 47	01 0000	Slot 16	11 0000	Slot 48	01 0001	Slot 17	11 0001	Slot 49	01 0010	Slot 18	11 0010	Slot 50	01 0011	Slot 19	11 0011	Slot 51	01 0100	Slot 20	11 0100	Slot 52	01 0101	Slot 21	11 0101	Slot 53	01 0110	Slot 22	11 0110	Slot 54	01 0111	Slot 23	11 0111	Slot 55	01 1000	Slot 24	11 1000	Slot 56	01 1001	Slot 25	11 1001	Slot 57	01 1010	Slot 26	11 1010	Slot 58	01 1011	Slot 27	11 1011	Slot 59	01 1100	Slot 28	11 1100	Slot 60	01 1101	Slot 29	11 1101	Slot 61	01 1110	Slot 30	11 1110	Slot 62	01 1111	Slot 31	11 1111	Slot 63	
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5:0	ASP_TX1_SLOT	<p>Audio serial port TX channel 1 (ASP_TX1) data packet slot location. Configures the transmit location of the channel 1 data packet (ASP_TX1) relative to the start of the sample frame. The ASP frame format is defined by the configuration of ASP_FMT.</p> <p>Step size: 1 slot location. Use of slot locations beyond the end of the ASP frame are not supported.</p> <table> <tbody> <tr><td>00 0000</td><td>(Default) Slot 0</td><td>10 0000 Slot 32</td></tr> <tr><td>00 0001</td><td>Slot 1</td><td>10 0001 Slot 33</td></tr> <tr><td>00 0010</td><td>Slot 2</td><td>10 0010 Slot 34</td></tr> <tr><td>00 0011</td><td>Slot 3</td><td>10 0011 Slot 35</td></tr> <tr><td>00 0100</td><td>Slot 4</td><td>10 0100 Slot 36</td></tr> <tr><td>00 0101</td><td>Slot 5</td><td>10 0101 Slot 37</td></tr> <tr><td>00 0110</td><td>Slot 6</td><td>10 0110 Slot 38</td></tr> <tr><td>00 0111</td><td>Slot 7</td><td>10 0111 Slot 39</td></tr> <tr><td>00 1000</td><td>Slot 8</td><td>10 1000 Slot 40</td></tr> <tr><td>00 1001</td><td>Slot 9</td><td>10 1001 Slot 41</td></tr> <tr><td>00 1010</td><td>Slot 10</td><td>10 1010 Slot 42</td></tr> <tr><td>00 1011</td><td>Slot 11</td><td>10 1011 Slot 43</td></tr> <tr><td>00 1100</td><td>Slot 12</td><td>10 1100 Slot 44</td></tr> <tr><td>00 1101</td><td>Slot 13</td><td>10 1101 Slot 45</td></tr> <tr><td>00 1110</td><td>Slot 14</td><td>10 1110 Slot 46</td></tr> <tr><td>00 1111</td><td>Slot 15</td><td>10 1111 Slot 47</td></tr> <tr><td>01 0000</td><td>Slot 16</td><td>11 0000 Slot 48</td></tr> <tr><td>01 0001</td><td>Slot 17</td><td>11 0001 Slot 49</td></tr> <tr><td>01 0010</td><td>Slot 18</td><td>11 0010 Slot 50</td></tr> <tr><td>01 0011</td><td>Slot 19</td><td>11 0011 Slot 51</td></tr> <tr><td>01 0100</td><td>Slot 20</td><td>11 0100 Slot 52</td></tr> <tr><td>01 0101</td><td>Slot 21</td><td>11 0101 Slot 53</td></tr> <tr><td>01 0110</td><td>Slot 22</td><td>11 0110 Slot 54</td></tr> <tr><td>01 0111</td><td>Slot 23</td><td>11 0111 Slot 55</td></tr> <tr><td>01 1000</td><td>Slot 24</td><td>11 1000 Slot 56</td></tr> <tr><td>01 1001</td><td>Slot 25</td><td>11 1001 Slot 57</td></tr> <tr><td>01 1010</td><td>Slot 26</td><td>11 1010 Slot 58</td></tr> <tr><td>01 1011</td><td>Slot 27</td><td>11 1011 Slot 59</td></tr> <tr><td>01 1100</td><td>Slot 28</td><td>11 1100 Slot 60</td></tr> <tr><td>01 1101</td><td>Slot 29</td><td>11 1101 Slot 61</td></tr> <tr><td>01 1110</td><td>Slot 30</td><td>11 1110 Slot 62</td></tr> <tr><td>01 1111</td><td>Slot 31</td><td>11 1111 Slot 63</td></tr> </tbody> </table>	00 0000	(Default) Slot 0	10 0000 Slot 32	00 0001	Slot 1	10 0001 Slot 33	00 0010	Slot 2	10 0010 Slot 34	00 0011	Slot 3	10 0011 Slot 35	00 0100	Slot 4	10 0100 Slot 36	00 0101	Slot 5	10 0101 Slot 37	00 0110	Slot 6	10 0110 Slot 38	00 0111	Slot 7	10 0111 Slot 39	00 1000	Slot 8	10 1000 Slot 40	00 1001	Slot 9	10 1001 Slot 41	00 1010	Slot 10	10 1010 Slot 42	00 1011	Slot 11	10 1011 Slot 43	00 1100	Slot 12	10 1100 Slot 44	00 1101	Slot 13	10 1101 Slot 45	00 1110	Slot 14	10 1110 Slot 46	00 1111	Slot 15	10 1111 Slot 47	01 0000	Slot 16	11 0000 Slot 48	01 0001	Slot 17	11 0001 Slot 49	01 0010	Slot 18	11 0010 Slot 50	01 0011	Slot 19	11 0011 Slot 51	01 0100	Slot 20	11 0100 Slot 52	01 0101	Slot 21	11 0101 Slot 53	01 0110	Slot 22	11 0110 Slot 54	01 0111	Slot 23	11 0111 Slot 55	01 1000	Slot 24	11 1000 Slot 56	01 1001	Slot 25	11 1001 Slot 57	01 1010	Slot 26	11 1010 Slot 58	01 1011	Slot 27	11 1011 Slot 59	01 1100	Slot 28	11 1100 Slot 60	01 1101	Slot 29	11 1101 Slot 61	01 1110	Slot 30	11 1110 Slot 62	01 1111	Slot 31	11 1111 Slot 63
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### 7.8.6 ASP\_FRAME\_CTRL\_3

**I<sup>2</sup>C Address: 0x00 4820**

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
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21:16	ASP_TX4_SLOT	<p>Audio serial port TX channel 4 data packet slot location. Configures the TX location of the channel 4 data packet relative to the start of the sample frame. The ASP frame format is defined by the configuration of ASP_FMT.</p> <p>Step size: 1 slot location. Use of slot locations beyond the end of the ASP frame are not supported.</p> <table> <tbody> <tr><td>00 0000</td><td>Slot 0</td><td>10 0000</td><td>Slot 32</td></tr> <tr><td>00 0001</td><td>Slot 1</td><td>10 0001</td><td>Slot 33</td></tr> <tr><td>00 0010</td><td>Slot 2</td><td>10 0010</td><td>Slot 34</td></tr> <tr><td>00 0011</td><td>(Default) Slot 3</td><td>10 0011</td><td>Slot 35</td></tr> <tr><td>00 0100</td><td>Slot 4</td><td>10 0100</td><td>Slot 36</td></tr> <tr><td>00 0101</td><td>Slot 5</td><td>10 0101</td><td>Slot 37</td></tr> <tr><td>00 0110</td><td>Slot 6</td><td>10 0110</td><td>Slot 38</td></tr> <tr><td>00 0111</td><td>Slot 7</td><td>10 0111</td><td>Slot 39</td></tr> <tr><td>00 1000</td><td>Slot 8</td><td>10 1000</td><td>Slot 40</td></tr> <tr><td>00 1001</td><td>Slot 9</td><td>10 1001</td><td>Slot 41</td></tr> <tr><td>00 1010</td><td>Slot 10</td><td>10 1010</td><td>Slot 42</td></tr> <tr><td>00 1011</td><td>Slot 11</td><td>10 1011</td><td>Slot 43</td></tr> <tr><td>00 1100</td><td>Slot 12</td><td>10 1100</td><td>Slot 44</td></tr> <tr><td>00 1101</td><td>Slot 13</td><td>10 1101</td><td>Slot 45</td></tr> <tr><td>00 1110</td><td>Slot 14</td><td>10 1110</td><td>Slot 46</td></tr> <tr><td>00 1111</td><td>Slot 15</td><td>10 1111</td><td>Slot 47</td></tr> <tr><td>01 0000</td><td>Slot 16</td><td>11 0000</td><td>Slot 48</td></tr> <tr><td>01 0001</td><td>Slot 17</td><td>11 0001</td><td>Slot 49</td></tr> <tr><td>01 0010</td><td>Slot 18</td><td>11 0010</td><td>Slot 50</td></tr> <tr><td>01 0011</td><td>Slot 19</td><td>11 0011</td><td>Slot 51</td></tr> <tr><td>01 0100</td><td>Slot 20</td><td>11 0100</td><td>Slot 52</td></tr> <tr><td>01 0101</td><td>Slot 21</td><td>11 0101</td><td>Slot 53</td></tr> <tr><td>01 0110</td><td>Slot 22</td><td>11 0110</td><td>Slot 54</td></tr> <tr><td>01 0111</td><td>Slot 23</td><td>11 0111</td><td>Slot 55</td></tr> <tr><td>01 1000</td><td>Slot 24</td><td>11 1000</td><td>Slot 56</td></tr> <tr><td>01 1001</td><td>Slot 25</td><td>11 1001</td><td>Slot 57</td></tr> <tr><td>01 1010</td><td>Slot 26</td><td>11 1010</td><td>Slot 58</td></tr> <tr><td>01 1011</td><td>Slot 27</td><td>11 1011</td><td>Slot 59</td></tr> <tr><td>01 1100</td><td>Slot 28</td><td>11 1100</td><td>Slot 60</td></tr> <tr><td>01 1101</td><td>Slot 29</td><td>11 1101</td><td>Slot 61</td></tr> <tr><td>01 1110</td><td>Slot 30</td><td>11 1110</td><td>Slot 62</td></tr> <tr><td>01 1111</td><td>Slot 31</td><td>11 1111</td><td>Slot 63</td></tr> </tbody> </table>	00 0000	Slot 0	10 0000	Slot 32	00 0001	Slot 1	10 0001	Slot 33	00 0010	Slot 2	10 0010	Slot 34	00 0011	(Default) Slot 3	10 0011	Slot 35	00 0100	Slot 4	10 0100	Slot 36	00 0101	Slot 5	10 0101	Slot 37	00 0110	Slot 6	10 0110	Slot 38	00 0111	Slot 7	10 0111	Slot 39	00 1000	Slot 8	10 1000	Slot 40	00 1001	Slot 9	10 1001	Slot 41	00 1010	Slot 10	10 1010	Slot 42	00 1011	Slot 11	10 1011	Slot 43	00 1100	Slot 12	10 1100	Slot 44	00 1101	Slot 13	10 1101	Slot 45	00 1110	Slot 14	10 1110	Slot 46	00 1111	Slot 15	10 1111	Slot 47	01 0000	Slot 16	11 0000	Slot 48	01 0001	Slot 17	11 0001	Slot 49	01 0010	Slot 18	11 0010	Slot 50	01 0011	Slot 19	11 0011	Slot 51	01 0100	Slot 20	11 0100	Slot 52	01 0101	Slot 21	11 0101	Slot 53	01 0110	Slot 22	11 0110	Slot 54	01 0111	Slot 23	11 0111	Slot 55	01 1000	Slot 24	11 1000	Slot 56	01 1001	Slot 25	11 1001	Slot 57	01 1010	Slot 26	11 1010	Slot 58	01 1011	Slot 27	11 1011	Slot 59	01 1100	Slot 28	11 1100	Slot 60	01 1101	Slot 29	11 1101	Slot 61	01 1110	Slot 30	11 1110	Slot 62	01 1111	Slot 31	11 1111	Slot 63	
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5:0	ASP_TX3_SLOT	<p>Audio serial port TX channel 3 data packet slot location. Configures the TX location of the channel 3 data packet relative to the start of the sample frame. The ASP frame format is defined by the configuration of ASP_FMT. Step size: 1 slot location. Use of slot locations beyond the end of the ASP frame are not supported.</p> <table> <tbody> <tr><td>00 0000</td><td>Slot 0</td><td>10 0000</td><td>Slot 32</td></tr> <tr><td>00 0001</td><td>Slot 1</td><td>10 0001</td><td>Slot 33</td></tr> <tr><td>00 0010</td><td>(Default) Slot 2</td><td>10 0010</td><td>Slot 34</td></tr> <tr><td>00 0011</td><td>Slot 3</td><td>10 0011</td><td>Slot 35</td></tr> <tr><td>00 0100</td><td>Slot 4</td><td>10 0100</td><td>Slot 36</td></tr> <tr><td>00 0101</td><td>Slot 5</td><td>10 0101</td><td>Slot 37</td></tr> <tr><td>00 0110</td><td>Slot 6</td><td>10 0110</td><td>Slot 38</td></tr> <tr><td>00 0111</td><td>Slot 7</td><td>10 0111</td><td>Slot 39</td></tr> <tr><td>00 1000</td><td>Slot 8</td><td>10 1000</td><td>Slot 40</td></tr> <tr><td>00 1001</td><td>Slot 9</td><td>10 1001</td><td>Slot 41</td></tr> <tr><td>00 1010</td><td>Slot 10</td><td>10 1010</td><td>Slot 42</td></tr> <tr><td>00 1011</td><td>Slot 11</td><td>10 1011</td><td>Slot 43</td></tr> <tr><td>00 1100</td><td>Slot 12</td><td>10 1100</td><td>Slot 44</td></tr> <tr><td>00 1101</td><td>Slot 13</td><td>10 1101</td><td>Slot 45</td></tr> <tr><td>00 1110</td><td>Slot 14</td><td>10 1110</td><td>Slot 46</td></tr> <tr><td>00 1111</td><td>Slot 15</td><td>10 1111</td><td>Slot 47</td></tr> <tr><td>01 0000</td><td>Slot 16</td><td>11 0000</td><td>Slot 48</td></tr> <tr><td>01 0001</td><td>Slot 17</td><td>11 0001</td><td>Slot 49</td></tr> <tr><td>01 0010</td><td>Slot 18</td><td>11 0010</td><td>Slot 50</td></tr> <tr><td>01 0011</td><td>Slot 19</td><td>11 0011</td><td>Slot 51</td></tr> <tr><td>01 0100</td><td>Slot 20</td><td>11 0100</td><td>Slot 52</td></tr> <tr><td>01 0101</td><td>Slot 21</td><td>11 0101</td><td>Slot 53</td></tr> <tr><td>01 0110</td><td>Slot 22</td><td>11 0110</td><td>Slot 54</td></tr> <tr><td>01 0111</td><td>Slot 23</td><td>11 0111</td><td>Slot 55</td></tr> <tr><td>01 1000</td><td>Slot 24</td><td>11 1000</td><td>Slot 56</td></tr> <tr><td>01 1001</td><td>Slot 25</td><td>11 1001</td><td>Slot 57</td></tr> <tr><td>01 1010</td><td>Slot 26</td><td>11 1010</td><td>Slot 58</td></tr> <tr><td>01 1011</td><td>Slot 27</td><td>11 1011</td><td>Slot 59</td></tr> <tr><td>01 1100</td><td>Slot 28</td><td>11 1100</td><td>Slot 60</td></tr> <tr><td>01 1101</td><td>Slot 29</td><td>11 1101</td><td>Slot 61</td></tr> <tr><td>01 1110</td><td>Slot 30</td><td>11 1110</td><td>Slot 62</td></tr> <tr><td>01 1111</td><td>Slot 31</td><td>11 1111</td><td>Slot 63</td></tr> </tbody> </table>	00 0000	Slot 0	10 0000	Slot 32	00 0001	Slot 1	10 0001	Slot 33	00 0010	(Default) Slot 2	10 0010	Slot 34	00 0011	Slot 3	10 0011	Slot 35	00 0100	Slot 4	10 0100	Slot 36	00 0101	Slot 5	10 0101	Slot 37	00 0110	Slot 6	10 0110	Slot 38	00 0111	Slot 7	10 0111	Slot 39	00 1000	Slot 8	10 1000	Slot 40	00 1001	Slot 9	10 1001	Slot 41	00 1010	Slot 10	10 1010	Slot 42	00 1011	Slot 11	10 1011	Slot 43	00 1100	Slot 12	10 1100	Slot 44	00 1101	Slot 13	10 1101	Slot 45	00 1110	Slot 14	10 1110	Slot 46	00 1111	Slot 15	10 1111	Slot 47	01 0000	Slot 16	11 0000	Slot 48	01 0001	Slot 17	11 0001	Slot 49	01 0010	Slot 18	11 0010	Slot 50	01 0011	Slot 19	11 0011	Slot 51	01 0100	Slot 20	11 0100	Slot 52	01 0101	Slot 21	11 0101	Slot 53	01 0110	Slot 22	11 0110	Slot 54	01 0111	Slot 23	11 0111	Slot 55	01 1000	Slot 24	11 1000	Slot 56	01 1001	Slot 25	11 1001	Slot 57	01 1010	Slot 26	11 1010	Slot 58	01 1011	Slot 27	11 1011	Slot 59	01 1100	Slot 28	11 1100	Slot 60	01 1101	Slot 29	11 1101	Slot 61	01 1110	Slot 30	11 1110	Slot 62	01 1111	Slot 31	11 1111	Slot 63
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### 7.8.7 ASP\_FRAME\_CTRL\_4

**I<sup>2</sup>C Address: 0x00 4824**

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### 7.8.8 ASP\_FRAME\_CTRL\_5

**I<sup>2</sup>C Address: 0x00 482C**

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01 1001	Slot 25	11 1001	Slot 57																																																																																																																															
01 1010	Slot 26	11 1010	Slot 58																																																																																																																															
01 1011	Slot 27	11 1011	Slot 59																																																																																																																															
01 1100	Slot 28	11 1100	Slot 60																																																																																																																															
01 1101	Slot 29	11 1101	Slot 61																																																																																																																															
01 1110	Slot 30	11 1110	Slot 62																																																																																																																															
01 1111	Slot 31	11 1111	Slot 63																																																																																																																															

### 7.8.9 ASP\_TX\_RX\_LATENCY

**I<sup>2</sup>C Address: 0x00 4838**

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ASP_TX_DLY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ASP_RX_DLY	—	—	
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description								
31:18	—	Reserved								
17:16	ASP_TX_DLY	<p>Audio serial port TX delay. This is the number of samples added to the TX audio channels to achieve synchronization in the ASP FIFO.</p> <table> <tr><td>00</td><td>0 sample delay</td><td>10</td><td>2 sample delay</td></tr> <tr><td>01</td><td>(Default) 1 sample delay</td><td>11</td><td>Reserved</td></tr> </table>	00	0 sample delay	10	2 sample delay	01	(Default) 1 sample delay	11	Reserved
00	0 sample delay	10	2 sample delay							
01	(Default) 1 sample delay	11	Reserved							
15:2	—	Reserved								
1:0	ASP_RX_DLY	<p>Audio serial port RX delay. This is the number of samples added to the RX audio channels to achieve synchronization in the ASP FIFO.</p> <table> <tr><td>00</td><td>0 sample delay</td><td>10</td><td>2 sample delay</td></tr> <tr><td>01</td><td>(Default) 1 sample delay</td><td>11</td><td>Reserved</td></tr> </table>	00	0 sample delay	10	2 sample delay	01	(Default) 1 sample delay	11	Reserved
00	0 sample delay	10	2 sample delay							
01	(Default) 1 sample delay	11	Reserved							

### 7.8.10 ASP\_RX\_TX\_ENABLES

**I<sup>2</sup>C Address: 0x00 483C**

RW	31	30	29	28	27	26	25	24	—	23	22	21	20	19	18	17	16
Default	0	0	0	0	0	0	0	0	—	0	0	0	0	0	0	0	ASP_RX1_EN
RW	15	14	13	12	11	10	9	8	—	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	—	0	0	0	0	0	0	0	ASP_TX6_EN ASP_TX5_EN ASP_TX4_EN ASP_TX3_EN ASP_TX2_EN ASP_TX1_EN

Bits	Name	Description
31:17	—	Reserved
16	ASP_RX1_EN	Audio serial port audio RX channel 1 enable (ASP_RX1). 0 (Default) Disabled 1 Enabled
15:6	—	Reserved
5	ASP_TX6_EN	Audio serial port audio TX channel 6 enable (ASP_TX6). 0 (Default) Disabled 1 Enabled
4	ASP_TX5_EN	Audio serial port audio TX channel 5 enable (ASP_TX5). 0 (Default) Disabled 1 Enabled
3	ASP_TX4_EN	Audio serial port audio TX channel 4 enable (ASP_TX4). 0 (Default) Disabled 1 Enabled
2	ASP_TX3_EN	Audio serial port audio TX channel 3 enable (ASP_TX3). 0 (Default) Disabled 1 Enabled
1	ASP_TX2_EN	Audio serial port audio TX channel 2 enable (ASP_TX2). 0 (Default) Disabled 1 Enabled
0	ASP_TX1_EN	Audio serial port audio TX channel 1 enable (ASP_TX1). 0 (Default) Disabled 1 Enabled

## 7.9 PCM Audio and Data Routing (MIXER)

### 7.9.1 DACPCM\_INPUT\_SOURCE

**I<sup>2</sup>C Address: 0x00 4C00**

RW	31..8	7	6	5	4	—	AMP_PCM_RX_SEL	3	2	1	0
Default	0x00 0000	0	0	0	0	—	AMP_PCM_RX_SEL	1	0	0	0

Bits	Name	Description
31:7	—	Reserved
6:0	AMP_PCM_RX_SEL	Amplifier audio PCM RX source select. Selects the PCM audio source which is provided to the amplifier's internal audio path. 000 0000 Zero fill data (ZERO_FILL) 0000001-000 0111 Reserved 000 1000 (Default) Audio serial port RX1 channel (ASP_RX1) 0001001-111 1111 Reserved

### 7.9.2 AIIFTX\_INPUT\_0\_SOURCE

**I<sup>2</sup>C Address: 0x00 4C20**

RW	31..8	7	6	5	4	3	2	1	0					
—	—	—	—	—	—	ASP_TX1_SEL								
Default	0x00 0000	0	0	0	1	1	0	0	0					

Bits	Name	Description
31:7	—	Reserved
6:0	ASP_TX1_SEL	Audio serial port TX1 data source select. Selects the source of the PCM data provided to the Audio Serial Port interface TX1 channel (ASP_TX1). 000 0000 Zero fill data (ZERO_FILL) 0000001–000 0111 Reserved 000 1000 Audio serial port RX1 channel (ASP_RX1) 0001001–001 0111 Reserved 001 1000 (Default) VMON1 voltage data (VMON) 001 1001 IMON current data (IMON) 001 1010 VMON2 voltage data 001 1011–001 1111 Reserved 010 0000 Error volume (ERR_VOL) 010 0001–010 0111 Reserved 010 1000 VBATMON voltage data (VBATMON) 010 1001 VBSTMON voltage data (VBSTMON)

### 7.9.3 AIIFTX\_INPUT\_1\_SOURCE

**I<sup>2</sup>C Address: 0x00 4C24**

RW	31..8	7	6	5	4	3	2	1	0					
—	—	—	—	—	—	ASP_TX2_SEL								
Default	0x00 0000	0	0	0	1	1	0	0	1					

Bits	Name	Description
31:7	—	Reserved
6:0	ASP_TX2_SEL	Audio serial port TX2 data source select. Selects the source of the PCM data provided to the Audio Serial Port interface TX2 channel (ASP_TX2). 000 0000 Zero fill data (ZERO_FILL) 0000001–000 0111 Reserved 000 1000 Audio serial port RX1 channel (ASP_RX1) 0001001–001 0111 Reserved 001 1000 VMON1 voltage data (VMON) 001 1001 (Default) IMON current data (IMON) 001 1010 VMON2 voltage data 001 1011–001 1111 Reserved 010 0000 Error volume (ERR_VOL) 010 0001–010 0111 Reserved 010 1000 VBATMON voltage data (VBATMON) 010 1001 VBSTMON voltage data (VBSTMON)

### 7.9.4 AIIFTX\_INPUT\_2\_SOURCE

**I<sup>2</sup>C Address: 0x00 4C28**

RW	31..8	7	6	5	4	3	2	1	0					
—	—	—	—	—	—	ASP_TX3_SEL								
Default	0x00 0000	0	0	1	0	1	0	0	0					

Bits	Name	Description
31:7	—	Reserved
6:0	ASP_TX3_SEL	Audio serial port TX3 data source select. Selects the source of the PCM data provided to the Audio Serial Port interface TX3 channel (ASP_TX3). 000 0000 Zero fill data (ZERO_FILL) 0000001–000 0111 Reserved 000 1000 Audio serial port RX1 channel (ASP_RX1) 0001001–001 0111 Reserved 001 1000 VMON1 voltage data (VMON) 001 1001 IMON current data (IMON) 001 1010 VMON2 voltage data 001 1011–001 1111 Reserved 010 0000 Error volume (ERR_VOL) 010 0001–010 0111 Reserved 010 1000 (Default) VBATMON voltage data (VBATMON) 010 1001 VBSTMON voltage data (VBSTMON)

### 7.9.5 AIFTX\_INPUT\_3\_SOURCE

**I<sup>2</sup>C Address: 0x00 4C2C**

RW	31..8	7	6	5	4	3	2	1	0					
	—	—	—	—	—	ASP_TX4_SEL								
Default	0x00 0000	0	0	1	0	1	0	0	1					

Bits	Name	Description
31:7	—	Reserved
6:0	ASP_TX4_SEL	Audio serial port TX4 data source select. Selects the source of the PCM data provided to the Audio Serial Port interface TX4 channel (ASP_TX4). 000 0000 Zero fill data (ZERO_FILL) 0000001–000 0111 Reserved 000 1000 Audio serial port RX1 channel (ASP_RX1) 0001001–001 0111 Reserved 001 1000 VMON1 voltage data (VMON) 001 1001 IMON current data (IMON) 001 1010 VMON2 voltage data 001 1011–001 1111 Reserved 010 0000 Error volume (ERR_VOL) 010 0001–010 0111 Reserved 010 1000 VBATMON voltage data (VBATMON) 010 1001 (Default) VBSTMON voltage data (VBSTMON)

### 7.9.6 AIFTX\_INPUT\_4\_SOURCE

**I<sup>2</sup>C Address: 0x00 4C30**

RW	31..8	7	6	5	4	3	2	1	0					
	—	—	—	—	—	ASP_TX5_SEL								
Default	0x00 0000	0	0	1	0	0	0	0	0					

Bits	Name	Description
31:7	—	Reserved
6:0	ASP_TX5_SEL	Audio serial port TX5 data source select. Selects the source of the PCM data provided to the Audio Serial Port interface TX5 channel (ASP_TX5). 000 0000 Zero fill data (ZERO_FILL) 0000001–000 0111 Reserved 000 1000 Audio serial port RX1 channel (ASP_RX1) 0001001–001 0111 Reserved 001 1000 VMON1 voltage data (VMON) 001 1001 IMON current data (IMON) 001 1010 VMON2 voltage data 001 1011–001 1111 Reserved 010 0000 (Default) Error volume (ERR_VOL) 010 0001–010 0111 Reserved 010 1000 VBATMON voltage data (VBATMON) 010 1001 VBSTMON voltage data (VBSTMON)

### 7.9.7 AIFTX\_INPUT\_5\_SOURCE

**I<sup>2</sup>C Address: 0x00 4C34**

RW	31..8	7	6	5	4	3	2	1	0					
	—	—	—	—	—	ASP_TX6_SEL								
Default	0x00 0000	0	0	0	0	0	0	0	0					

Bits	Name	Description
31:7	—	Reserved
6:0	ASP_TX6_SEL	Audio serial port TX6 data source select. Selects the source of the PCM data provided to the Audio Serial Port interface TX6 channel (ASP_TX6). 000 0000 (Default) Zero fill data (ZERO_FILL) 0000001–000 0111 Reserved 000 1000 Audio serial port RX1 channel (ASP_RX1) 0001001–001 0111 Reserved 001 1000 VMON1 voltage data (VMON) 001 1001 IMON current data (IMON) 001 1010 VMON2 voltage data 001 1011–001 1111 Reserved 010 0000 Error volume (ERR_VOL) 010 0001–010 0111 Reserved 010 1000 VBATMON voltage data (VBATMON) 010 1001 VBSTMON voltage data (VBSTMON)

## 7.10 VMON2 Signal Monitoring (VIMON2)

### 7.10.1 SPKMON\_FILTERS

**I<sup>2</sup>C Address: 0x00 4E04**

RW	31...8	7	6	5	4		3	2	1	0
—	—	—	—	—	—	—	—	—	VMON2_POL	—
Default	0x00 0000	0	0	0	0	0	0	0	1	1

Bits	Name	Description
31:2	—	Reserved
0	VMON2_POL	VMON2 output polarity control. Configures the polarity of the VMON2 monitor signal relative to the amplifier's output. This control must be set to the same value as VMON1_POL when using both VMON1 and VMON2. 0 Inverted 1 (Default) Not inverted

## 7.11 Amplifier Volume Control (INTP)

### 7.11.1 AMP\_CTRL

**I<sup>2</sup>C Address: 0x00 6000**

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	AMP_HPF_PCM_EN	AMP_INV_PCM	—	—	—	—	—	—	—	—	—	—	—	AMP_VOL_PCM	—	—	AMP_RAMP_PCM
Default	0x0000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:16	—	Reserved
15	AMP_HPF_PCM_EN	Amplifier PCM audio high-pass filter enable. Enables the internal high-pass filter at the input of the PCM path. The high pass filter is applied to serial port PCM audio source. The corner frequency of the HPF is 0.94Hz. 0 Disabled. Not recommended for normal use. 1 (Default) Enabled
14	AMP_INV_PCM	Amplifier PCM audio inversion. Inverts the polarity of the audio signal output from the Class D amplifier. 0 (Default) PCM audio not inverted 1 PCM audio inverted
13:3	AMP_VOL_PCM	Amplifier PCM audio digital volume control. Sets the volume of the amplifier's digital audio path. Register configuration values beyond listed range are clamped to the corresponding min/max values. Step size: 0.125 dB. Range +12.0 dB to -102 dB. Values below -102 dB digitally mute the audio stream. 0x000 (Default) 0.0 dB 0x001 0.125 dB ... 0x05F 11.875 dB 0x060 12.0 dB 0x061-0 x3FF Reserved 0x400 Mute 0x401-0 x4CF Reserved 0x4D0 -102.0 dB 0x4D1 -101.875 dB ... 0x7FE -0.25 dB 0x7FF -0.125 dB
2:0	AMP_RAMP_PCM	Amplifier PCM audio digital soft-ramp rate. Selects the soft-ramp rate for all digital volume changes. This register must not be changed during a volume ramp. 000 (Default) No Ramp 001 0.5 ms/6 dB 010 1 ms/6 dB 011 2 ms/6 dB 100 4 ms/6 dB 101 8 ms/6 dB 110 15 ms/6 dB 111 30 ms/6 dB

## 7.12 VBAT Brownout Prevention + Temp Warning (ERROR\_VOLUME)

### 7.12.1 VBATBR\_CONFIG

**I<sup>2</sup>C Address: 0x00 6404**

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—				VBATBR_REL_TRIGGER	VBATBR_REL_AUTO	VBATBR_MUTE_EN		VBATBR_REL_RATE	VBATBR_WAIT			VBATBR_ATK_RATE			
Default	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0
RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	VBATBR_ATK_VOL				VBATBR_MAX_ATT				—	VBATBR_THLD1						
	0	0	0	1	1	0	0	1	0	0	0	0	0	1	0	1

Bits	Name	Description														
31:27	—	Reserved														
26	VBATBR_REL_TRIGGER	brownout prevention manual release trigger. When sequencing when configured in manual release mode (BR_REL_AUTO = 0), triggers the brownout prevention to enter the release state.  <b>Note:</b> BR_REL_TRIGGER has no effect if BR_REL_AUTO = 1. 0 -> 1 -> 0 sequence. At the end of the sequence, if the brownout prevention is in the manual wait state and no BR condition is present, triggers it to enter the release state. 0 (Default) Pulse low. When in a wait state with no BR, waits indefinitely for a manual trigger to occur 1 Pulse high. When in a wait state with no BR, waits indefinitely for a manual trigger to occur														
25	VBATBR_REL_AUTO	brownout prevention automatic wait and release. Configures whether the automatic BR_WAIT timer or the manual BR_REL_TRIGGER determines when the wait state is exited and the release state is entered. 0 Manual mode; requires BR_REL_TRIGGER to be sequenced to enter release 1 (Default) Automatic wait period based on BR_WAIT														
24	VBATBR_MUTE_EN	During the attack state, if the BR_MAX_ATT value is reached, the error condition still remains, and this bit is set, the audio is muted. The audio remains muted until the error condition has cleared and the brownout prevention enters a releasing state. 0 (Default) Mute disabled 1 Mute enabled														
23:21	VBATBR_REL_RATE	Attenuation release step rate (tBR_REL). Configures the delay between consecutive volume attenuation release steps (VOLREL) when a brownout condition is no longer present and the brownout is in an attenuation release state. 000 5 ms 001 10 ms 010 25 ms 011 50 ms 100 100 ms 101 (Default) 250 ms 110 500 ms 111 1000 ms														
20:19	VBATBR_WAIT	Configures the delay between a brownout condition no longer being present and the brownout prevention entering an attenuation release state. 00 10 ms 01 (Default) 100 ms 10 250 ms 11 500 ms														
18:16	VBATBR_ATK_RATE	Attenuation attack step rate (tBR_ATK). Configures the amount delay between consecutive volume attenuation steps (VOLATTK) when a brownout condition is present and the brownout condition is in an attacking state. 000 2.5 us 001 5 us 010 (Default) 10 us 011 25 us 100 50 us 101 100 us 110 250 us 111 500 us														
15:12	VBATBR_ATK_VOL	brownout prevention attack step size. Configures the brownout prevention attacking attenuation step size when operating in either digital volume or analog gain modes. Attenuation values listed are relative to triggering BR_THLD1 / BR_THLD2 / BR_THLD3 per attack time period (BR_ATK_RATE). 0000 0.0625 dB / 0.125 dB / 0.250 dB 0001 (Default) 0.125 dB / 0.250 dB / 0.500 dB 0010 0.250 dB / 0.500 dB / 1.000 dB 0011 0.500 dB / 1.000 dB / 2.000 dB 0100 0.750 dB / 1.500 dB / 3.000 dB 0101 1.000 dB / 2.000 dB / 4.000 dB 0110 1.250 dB / 2.500 dB / 5.000 dB 0111 1.500 dB / 3.000 dB / 6.000 dB 1000–1111 Reserved														
11:8	VBATBR_MAX_ATT	Maximum attenuation that the brownout prevention can apply to the audio signal. Even if an error condition remains present, the brownout prevention only attenuates the audio signal up to the limit configured by BR_MAX_ATT. Step size: 1 dB.  <b>Note:</b> BR_MAX_ATT should not be adjusted when attenuation is being applied by the brownout prevention. 0000 0 dB 0001 1 dB 0010 2 dB ... 1110 14 dB 1111 15 dB														

Bits	Name	Description
7:5	—	Reserved
4:0	VBATBR_THLD1	Initial BR_1 threshold. Configures the brownout threshold voltage. 00000–0 0001 Reserved 0 0010 2.497 V 0 0011 2.544 V 0 0100 2.592 V 0 0101 (Default) 2.639 V 0 0110 2.687 V 0 0111 2.734 V 0 1000 2.782 V 0 1001 2.83 V 0 1010 2.877 V 0 1011 2.925 V 0 1100 2.972 V 0 1101 3.02 V 0 1110 3.067 V 0 1111 3.115 V 1 0000 3.162 V

### 7.12.2 VBATBR\_STATUS

**I<sup>2</sup>C Address: 0x00 640C**

RO	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	VBATBR_MUTED	—	—	—	—	—	—	—
Default	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:9	—	Reserved
8	VBATBR_MUTED	VBAT brownout prevention mute status. If VBATBR_MUTE_EN is set and the reactive brownout has muted the audio, this bit is set, indicating that the audio has muted.
7:0	VBATBR_STATUS	Reports how much (if any) attenuation is applied to the audio signal by the brownout prevention control. This field only reports 0 dB attenuation when no audio attenuation is being applied by the brownout prevention. Step size: 0.0625 dB 0000 0000 (Default) 0.0 dB 0000 0001 0.0625 dB ... 1110 1111 14.9375 dB 1111 0000 15.0 dB 11110001–1111 1111 Reserved

### 7.12.3 OTW\_CONFIG

**I<sup>2</sup>C Address: 0x00 6414**

RW	31...8	7	6	5	4	—	3	2	1	0
	—	—	—	—	—	—	—	—	—	TEMP_WARN_VOL
Default	0x00 0000	0	0	0	0	0	0	0	0	1

Bits	Name	Description
31:3	—	Reserved
2:0	TEMP_WARN_VOL	Overtemperature warning attenuation. Configures the digital volume attenuation of the amplifier that is applied to the signal in response to an overtemperature warning condition. This attenuation is applied until RLS_TEMP_WARN is sequenced and the overtemperature warning condition is no longer present. 000 0 dB (disabled) 001 (Default) –3 dB 010 –6 dB 011 –9 dB 100 –111 Reserved

### 7.12.4 VOL\_STATUS\_TO\_DSP

**I<sup>2</sup>C Address: 0x00 6450**

RO	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:18	—	Reserved
17:9	FINAL_ERROR_VOL	Final error volume cumulative of OTW, BR, and remote attenuation effects.
8:0	—	Reserved



## 7.13 Power Management - Class H, Weak-FET, and Level-dependent Muting (PWRMGMT)

### 7.13.1 CLASSH\_CONFIG

I<sup>2</sup>C Address: 0x00 6800

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—							CH_HD_RM							CH_REL_RATE							—							CH_MEM_DEPTH			
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1		

Bits	Name	Description
31:23	—	Reserved
22:16	CH_HD_RM	Class H algorithm headroom. Controls VBST headroom in the max detection path of the Class H algorithm. Step size: 0.1 V 000 0000 0.0 V 000 0001 0.1 V 000 0010 0.2 V ... 000 1011 (Default) 1.1 V ... 011 1110 6.2 V
15:8	CH_REL_RATE	Class H release rate. Controls the amount of time required before allowing consecutive release condition VBST supply tracking updates. 00000000–0000 0011 Reserved 0000 0100 (Default) 20 µs 0000 0101 25 µs
7:3	—	Reserved
2:0	CH_MEM_DEPTH	Class H memory depth. Controls the memory depth used in the Class H algorithm for audio-data buffering and analysis. 000 20.83 µs 001 41.67 µs 010 83.33 µs

### 7.13.2 WKFET\_AMP\_CONFIG

I<sup>2</sup>C Address: 0x00 6804

RW	31..16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	WKFET_AMP_THLD				—	WKFET_AMP_DLY				WKFET_AMP_FRC_EN	WKFET_AMP_FRC	
Default	0x0000	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1

Bits	Name	Description
31:12	—	Reserved
11:8	WKFET_AMP_THLD	Weak-FET amplifier drive threshold. Configures the signal threshold at which the PWM output stage enters weak-FET operation. 0000 Reserved 0001 (Default) 0.05 V 0010 0.1 V 0011 0.15 V 0100 0.2 V 0101 0.25 V 0110 0.3 V 0111 0.35 V
7:5	—	Reserved



Bits	Name	Description
4:2	WKFET_AMP_DLY	Weak-FET entry delay. Controls the delay (in ms) before the Class H algorithm switches to the weak-FET voltage (after the audio falls and remains below the value specified in WKFET_AMP_THLD). 000 0 ms 001 5 ms 010 10 ms 011 50 ms 100 (Default) 100 ms 101 200 ms 110 500 ms 111 1000 ms
1	WKFET_AMP_FRC_EN	Weak-FET amplifier force control enable. Enables the functionality of WKFET_AMP_FRC to manually force the amplifier to be configured into Weak-FET mode. 0 (Default) WKFET_AMP_FORCE functionality disabled 1 WKFET_AMP_FORCE functionality enabled
0	WKFET_AMP_FRC	Weak-FET amplifier mode force. Manually configures the amplifier into Weak-FET or normal operation mode when WKFET_AMP_FRC_EN is set. If WKFET_AMP_FRC_EN is cleared, this register has no functionality. 0 Amplifier power FETs are not manually put into weak-FET mode 1 (Default) Amplifier power FETs are put into weak-FET mode

## 7.13.3 LDM\_CONFIG

I<sup>2</sup>C Address: 0x00 6808

RW	31..16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—				LDM_SEL				—		LDM_DELAY		—		LDM_PCM_THLD	
Default	0x0000	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1

Bits	Name	Description
31:14	—	Reserved
13:8	LDM_SEL	Amplifier level-dependent muting enable mode selection. Configures whether the amplifier level-dependent muting is enabled for the various blocks when the selected audio source has been below the AMP_LDM_THLD for a period of time configured by AMP_LDM_DELAY. 000000 - All level-dependent muting functionality disabled xxxxx1 - Amplifier level-dependent muting detection enabled (; switching) xxxx1x - Boost converter DCM detection enabled xxx1xx - VMON low power mode detection enabled xx1xxx - IMON low power mode detection enabled x1xxxx - brownout prevention detection enabled
7	—	Reserved
6:4	LDM_DELAY	Amplifier level-dependent muting entry delay. Time that the incoming audio signal must be below the LDM_x_THLD prior to entering a level-dependent muted state. 000 5 ms 001 10 ms 010 25 ms 011 (Default) 50 ms 100 100 ms 101 250 ms 110 500 ms 111 1000 ms
3	—	Reserved
2:0	LDM_PCM_THLD	Amplifier level-dependent muting threshold. Threshold of the audio signal in which the amplifier's level-dependent muting considers the input audio to be at a low enough level to be valid to enter a level-dependent muting state of operation. Levels are output-referred. 000 0.654 mVpk 001 0.328 mVpk 010 0.164 mVpk 011 (Default) 0.082 mVpk 100 0.041 mVpk 101 0.021 mVpk 110 0.010 mVpk 111 True zero data (no LSB dither)

## 7.14 Dynamic Range Enhancement (DRE)

### 7.14.1 AMP\_GAIN

**I<sup>2</sup>C Address: 0x00 6C04**

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	AMP_GAIN_ZC	—	AMP_GAIN_PCM	—	—	—	—	—	—	—	—	—
Default	0x0000	0	0	0	0	0	0	1	0	0	1	1	1	0	0	1	1

Bits	Name	Description																																												
31:11	—	Reserved																																												
10	AMP_GAIN_ZC	Amplifier gain change at zero-cross. 0 (Default) No zero cross 1 Zero cross																																												
9:5	AMP_GAIN_PCM	Amplifier analog gain in Serial Port PCM input mode. When configured to use the Serial Port PCM input, selects the effective analog gain. When DRE is disabled, this is a fixed gain. When DRE is enabled, this configuration determines the maximum allowable output signal and the gain is managed internally. Step size: 1 dB.  <table> <tbody> <tr><td>0 0000</td><td>0 dB</td><td>0 1011</td><td>11 dB</td></tr> <tr><td>0 0001</td><td>1 dB</td><td>0 1100</td><td>12 dB</td></tr> <tr><td>0 0010</td><td>2 dB</td><td>0 1101</td><td>13 dB</td></tr> <tr><td>0 0011</td><td>3 dB</td><td>0 1110</td><td>14 dB</td></tr> <tr><td>0 0100</td><td>4 dB</td><td>0 1111</td><td>15 dB</td></tr> <tr><td>0 0101</td><td>5 dB</td><td>1 0000</td><td>16 dB</td></tr> <tr><td>0 0110</td><td>6 dB</td><td>1 0001</td><td>17 dB</td></tr> <tr><td>0 0111</td><td>7 dB</td><td>1 0010</td><td>18 dB</td></tr> <tr><td>0 1000</td><td>8 dB</td><td>1 0011</td><td>(Default) 19 dB</td></tr> <tr><td>0 1001</td><td>9 dB</td><td>1 0100</td><td>20 dB</td></tr> <tr><td>0 1010</td><td>10 dB</td><td>1 0101-1 1111</td><td>Reserved</td></tr> </tbody> </table>	0 0000	0 dB	0 1011	11 dB	0 0001	1 dB	0 1100	12 dB	0 0010	2 dB	0 1101	13 dB	0 0011	3 dB	0 1110	14 dB	0 0100	4 dB	0 1111	15 dB	0 0101	5 dB	1 0000	16 dB	0 0110	6 dB	1 0001	17 dB	0 0111	7 dB	1 0010	18 dB	0 1000	8 dB	1 0011	(Default) 19 dB	0 1001	9 dB	1 0100	20 dB	0 1010	10 dB	1 0101-1 1111	Reserved
0 0000	0 dB	0 1011	11 dB																																											
0 0001	1 dB	0 1100	12 dB																																											
0 0010	2 dB	0 1101	13 dB																																											
0 0011	3 dB	0 1110	14 dB																																											
0 0100	4 dB	0 1111	15 dB																																											
0 0101	5 dB	1 0000	16 dB																																											
0 0110	6 dB	1 0001	17 dB																																											
0 0111	7 dB	1 0010	18 dB																																											
0 1000	8 dB	1 0011	(Default) 19 dB																																											
0 1001	9 dB	1 0100	20 dB																																											
0 1010	10 dB	1 0101-1 1111	Reserved																																											
4:0	—	Reserved																																												

## 7.15 Amplifier Control (DAC\_MSM)

### 7.15.1 DAC\_DC\_DET

**I<sup>2</sup>C Address: 0x00 7490**

RW	31..16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	WD_MODE	DCIN_WD_DUR	DCIN_WD_THLD	DCIN_WD_EN								
Default	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:12	—	Reserved
11:10	WD_MODE	DC input watchdog response. Configures the response of the amplifier input when an error condition has been detected. 00 (Default) Normal operation 11 Digital PCM volume mute
9:7	DCIN_WD_DUR	DC input watchdog duration time. The amount of time that the amplifier's digital input signal must exceed the DCIN_WD_THLD before triggering the watchdog. <b>Note:</b> DCIN_WD_DUR must not be changed while the DCIN watchdog is enabled and has been triggered. 000 (Default) 20 ms 001 50 ms 010 100 ms 011 200 ms 100 500 ms 101 1000 ms 110 2000 ms 111 5000 ms
6:1	DCIN_WD_THLD	DC input watchdog amplitude threshold. Configures the amplitude of the amplifier's digital input signal that must be maintained for a duration DCIN_WD_DUR, in order to trigger the watchdog, set as a percentage of digital full-scale (FS). 00 0000 (Default) 0 00 0001 2.5% FS 00 0010 5.0% FS 00 0011 7.5% FS 00 0100 10.0% FS ... 10 0100 90% FS 10 0101 92.5% FS 10 0110 95% FS 10 0111 97.5% FS 10 1000 100% FS 10 1001-11 1111 Reserved
0	DCIN_WD_EN	DC input watchdog enable. Configures whether the DC input watchdog is enabled or disabled. 0 (Default) Disabled 1 Enabled

## 7.16 Interrupt Status and Mask Control (IRQ\_MAIN)

### 7.16.1 INT\_EINT\_1

 I<sup>2</sup>C Address: 0xD0 0000

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	TEMP_ERR_EINT	TEMP_WARN_EINT	VBATBR_ATT_CLR_EINT	VBATBR_EINT	—	—	—	—	BST_IPK_EINT	BST_SHORT_ERR_EINT	BST_DCM_UVP_ERR_EINT	BST_OVP_ERR_EINT
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BST_OVP_EINT	LDM_PCM_ON_FALL_EINT	LDM_PCM_ON_RISE_EINT	—	—	—	—	—	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:27	—	Reserved
26	TEMP_ERR_EINT	Overtemperature error. Reports when the die temperature has exceeded the overtemperature error threshold and shut down operation of the device. 0 (Default) TEMP_ERR inactive 1 TEMP_ERR active
25	TEMP_WARN_EINT	Overtemperature warning flag. Reports when the die temperature has exceeded the configured temperature warning threshold. 0 (Default) TEMP_WARN inactive 1 TEMP_WARN active
24	VBATBR_ATT_CLR_EINT	brownout prevention attenuation cleared flag. Reports when any attenuation applied by the brownout prevention due to a threshold violation has cleared and been released back to 0dB. 0 (Default) VBATBR_ATT_CLR inactive 1 VBATBR_ATT_CLR active
23	VBATBR_EINT	brownout prevention threshold flag. Reports when the brownout prevention's voltage threshold has been violated and triggered a brownout response. 0 (Default) VBATBR inactive 1 VBATBR active
22:20	—	Reserved
19	BST_IPK_EINT	Boost converter peak current limit (BST_IPK) flag. Reports when the boost converter's peak current limit has triggered and limited the peak current consumption of the boost converter. 0 (Default) BST_IPK inactive 1 BST_IPK active
18	BST_SHORT_ERR_EINT	Boost converter inductor shorts error. Reports when the boost converter's LBST inductor short detection has triggered and shut down operation of the boost converter. 0 (Default) BST_SHORT_ERR inactive 1 BST_SHORT_ERR active
17	BST_DCM_UVP_ERR_EINT	Boost converter under voltage error. Reports when the boost converter's DCM mode under voltage error protection has triggered and shut down operation of the boost converter. 0 (Default) BST_DCM_UVP_ERR inactive 1 BST_DCM_UVP_ERR active
16	BST_OVP_ERR_EINT	Boost converter over voltage error. Reports when the boost converter's over voltage error protection has triggered and shut down operation of the boost converter. 0 (Default) BST_OVP_ERR inactive 1 BST_OVP_ERR active
15	BST_OVP_EINT	Boost converter over voltage protection flag. Reports when the boost converter's over voltage protection has triggered and actively reduced the VBST voltage. 0 (Default) BST_OVP inactive 1 BST_OVP active

Bits	Name	Description
14	LDM_PCM_ON_FALL_EINT	Level-dependent muting exit in PCM mode. Reports when the level-dependent muting has exited and the device has returned to normal operation. is no longer gating the blocks selected by the LDM_SEL. Valid only when using a PCM audio input source. 0 (Default) LDM_PCM_ON inactive 1 LDM_PCM_ON active
13	LDM_PCM_ON_RISE_EINT	Level-dependent muting entry in PCM mode. Reports when the level-dependent muting condition has been entered and the blocks selected by LDM_SEL are put in a low power state. Valid only when using a PCM audio input source. 0 (Default) LDM_PCM_ON inactive 1 LDM_PCM_ON active
12:0	—	Reserved

### 7.16.2 INT\_EINT\_2

I<sup>2</sup>C Address: 0xD0 0004

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	IMON_CLIP_EINT	VMON_CLIP_EINT	VBSTMON_CLIP_EINT	VBATMON_CLIP_EINT	—	—	—	—	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:25	—	Reserved
24	IMON_CLIP_EINT	IMON signal clipped status flag. Reports when the IMON data has overflowed and the signal has been clipped. 0 (Default) IMON_CLIP inactive 1 IMON_CLIP active
23	VMON_CLIP_EINT	VMON1 signal clipped status flag. Reports when the VMON1 data has overflowed and the signal has been clipped. 0 (Default) VMON_CLIP inactive 1 VMON_CLIP active
22	VBSTMON_CLIP_EINT	VBSTMON signal clipped status flag. Reports when the VBSTMON data has overflowed and the signal has been clipped. 0 (Default) VBSTMON_CLIP inactive 1 VBSTMON_CLIP active
21	VBATMON_CLIP_EINT	MON signal clipped status flag. Reports when the MON data has overflowed and the signal has been clipped. 0 (Default) MON_CLIP inactive 1 MON_CLIP active
20:0	—	Reserved

### 7.16.3 INT\_EINT\_3

I<sup>2</sup>C Address: 0xD0 0008

RW	31..16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	AMP_SHORT_ERR_EINT	—	—	—	—	—	—	—	—	—	—	—	—	—
Default	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:13	—	Reserved
12	AMP_SHORT_ERR_EINT	AMP_SHORT_ERR status flag. 0 (Default) AMP_SHORT_ERR inactive 1 AMP_SHORT_ERR active
11:0	—	Reserved

#### 7.16.4 INT\_EINT\_4

I<sup>2</sup>C Address: 0xD0 000C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				DCIN_ERR_EINT	VMON2_CLIP_EINT											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—		PLL_UNLOCK_EINT						GLOBAL_PUP_DONE_EINT	GLOBAL_PDN_DONE_EINT	GLOBAL_EN_ASSERT_EINT					
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:14	—	Reserved
28	DCIN_ERR_EINT	DC input error. Reports that the DC input watchdog has been triggered and responded (as configured). 0 (Default) DCIN_ERR inactive 1 DCIN_ERR active
27	VMON2_CLIP_EINT	VMON2 signal clipped status flag. Reports when the VMON2 data has overflowed and the signal has been clipped. 0 (Default) VMON2_CLIP inactive 1 VMON2_CLIP active
13	PLL_UNLOCK_EINT	PLL unlock flag. Reports when the PLL is neither frequency-locked nor phase-locked. 0 (Default) PLL_UNLOCK inactive 1 PLL_UNLOCK active
12:8	—	Reserved
7	GLOBAL_PUP_DONE_EINT	GLOBAL_PUP_DONE status flag. Reports when the device has powered up after setting GLOBAL_EN. This flag is set based on the sub-block enable configuration present at the time of setting GLOBAL_EN. 0 (Default) GLOBAL_PUP_DONE inactive 1 GLOBAL_PUP_DONE active
6	GLOBAL_PDN_DONE_EINT	GLOBAL_PDN_DONE status flag. Reports when the device has powered down after clearing GLOBAL_EN and is configured in a low power, standby state. 0 (Default) GLOBAL_PDN_DONE inactive 1 GLOBAL_PDN_DONE active
5	GLOBAL_EN_ASSERT_EINT	GLOBAL_EN_ASSERT status flag. Reports when the GLOBAL_EN has been asserted. 0 (Default) GLOBAL_EN_ASSERT inactive 1 GLOBAL_EN_ASSERT active
4:0	—	Reserved

**7.16.5 INT\_STS\_1**
**I<sup>2</sup>C Address: 0xD0 0020**

RO	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
				—		TEMP_ERR_STS	TEMP_WARN_STS	VBATBR_ATT_CLR_STS	VBATBR_STS		—		BST_IPK_STS	BST_SHORT_ERR_STS	BST_DCM_UVP_ERR_STS	BST_OVP_ERR_STS
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BST_OVP_STS	—	LDM_PCM_STS	—	—					—						
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:27	—	Reserved
26	TEMP_ERR_STS	TEMP_ERR raw real-time, non-sticky status flag. Indicates when the die temperature has exceeded the overtemperature error threshold and shut down operation of the device. 0 (Default) TEMP_ERR inactive 1 TEMP_ERR active
25	TEMP_WARN_STS	TEMP_WARN raw real-time, non-sticky status flag. Indicates when the die temperature has exceeded the configured temperature warning threshold. 0 (Default) TEMP_WARN inactive 1 TEMP_WARN active
24	VBATBR_ATT_CLR_STS	BR_ATT_CLR raw real-time, non-sticky status flag. Indicates when any attenuation applied by the brownout prevention due to a threshold violation has cleared and been released back to 0dB. 0 (Default) BR_ATT_CLR inactive 1 BR_ATT_CLR active
23	VBATBR_STS	BR raw real-time, non-sticky status flag. Indicates when the brownout prevention's voltage threshold has been violated and triggered a brownout response. 0 (Default) BR inactive 1 BR active
22:20	—	Reserved
19	BST_IPK_STS	BST_IPK raw real-time, non-sticky status flag. Indicates when the boost converter's peak current limit has triggered and limited the peak current consumption of the boost converter. 0 (Default) BST_IPK inactive 1 BST_IPK active
18	BST_SHORT_ERR_STS	BST_SHORT_ERR raw real-time, non-sticky status flag. Indicates when the boost converter's LBST inductor short detection has triggered and shut down operation of the boost converter. 0 (Default) BST_SHORT_ERR inactive 1 BST_SHORT_ERR active
17	BST_DCM_UVP_ERR_STS	BST_DCM_UVP_ERR raw real-time, non-sticky status flag. Indicates when the boost converter's DCM mode under voltage error protection has triggered and shut down operation of the boost converter. 0 (Default) BST_DCM_UVP_ERR inactive 1 BST_DCM_UVP_ERR active
16	BST_OVP_ERR_STS	BST_OVP_ERR raw real-time, non-sticky status flag. Indicates when the boost converter's over voltage error protection has triggered and shut down operation of the boost converter. 0 (Default) BST_OVP_ERR inactive 1 BST_OVP_ERR active
15	BST_OVP_STS	BST_OVP raw real-time, non-sticky status flag. Indicates when the boost converter's over voltage protection has triggered and actively reduced the VBST voltage. 0 (Default) BST_OVP inactive 1 BST_OVP active
14	—	Reserved
13	LDM_PCM_STS	LDM_PCM_ON raw real-time, non-sticky status flag. Indicates when the PCM audio input source level-dependent muting condition has been entered and the blocks selected by LDM_SEL are put in a low power state. 0 (Default) LDM_PCM inactive 1 LDM_PCM active
12:0	—	Reserved

**7.16.6 INT\_STS\_2**
**I<sup>2</sup>C Address: 0xD0 0024**

RO	31	30	29	28	—	27	26	25	24	IMON_CLIP_STS	VMON_CLIP_STS	VBSTMON_CLIP_STS	VBATMON_CLIP_STS	—	19	18	17	16
Default	0	0	0	0	—	0	0	0	0	0	0	0	0	0	0	0	0	0
RO	15	14	13	12	—	11	10	9	8	7	6	5	4	—	3	2	1	0
Default	0	0	0	0	—	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:25	—	Reserved
24	IMON_CLIP_STS	IMON_CLIP raw real-time, non-sticky status flag. 0 (Default) IMON_CLIP inactive 1 IMON_CLIP active
23	VMON_CLIP_STS	VMON_CLIP raw real-time, non-sticky status flag. 0 (Default) VMON_CLIP inactive 1 VMON_CLIP active
22	VBSTMON_CLIP_STS	VBSTMON_CLIP raw real-time, non-sticky status flag. 0 (Default) VBSTMON_CLIP inactive 1 VBSTMON_CLIP active
21	VBATMON_CLIP_STS	MON_CLIP raw real-time, non-sticky status flag. 0 (Default) MON_CLIP inactive 1 MON_CLIP active
20:0	—	Reserved

**7.16.7 INT\_STS\_3**
**I<sup>2</sup>C Address: 0xD0 0028**

RO	31...16	15	14	13	12	11	10	9	8	7	6	5	4	—	3	2	1	0
—	—	—	—	AMP_SHORT_ERR_STS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Default	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:13	—	Reserved
12	AMP_SHORT_ERR_STS	AMP_SHORT_ERR raw real-time, non-sticky status flag. 0 (Default) AMP_SHORT_ERR inactive 1 AMP_SHORT_ERR active
11:0	—	Reserved

**7.16.8 INT\_STS\_4**

I<sup>2</sup>C Address: 0xD0 002C

RO	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—			DCIN_ERR_STS	VMON2_CLIP_STS						—					
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—		PLL_UNLOCK_STS		—				GLOBAL_PUP_DONE_STS	GLOBAL_PDN_DONE_STS	GLOBAL_EN_ASSERT_STS		—			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:29	—	Reserved
28	DCIN_ERR_STS	DCIN_ERR raw real-time, non-sticky status flag. 0 (Default) DCIN_ERR inactive 1 DCIN_ERR active
27	VMON2_CLIP_STS	VMON2_CLIP raw real-time, non-sticky status flag. 0 (Default) VMON2_CLIP inactive 1 VMON2_CLIP active
26:14	—	Reserved
13	PLL_UNLOCK_STS	PLL_UNLOCK raw real-time, non-sticky status flag. Indicates when the PLL is not locked. 0 (Default) PLL_UNLOCK inactive 1 PLL_UNLOCK active
12:8	—	Reserved
7	GLOBAL_PUP_DONE_STS	GLOBAL_PUP_DONE raw real-time, non-sticky status flag. 0 (Default) GLOBAL_PUP_DONE inactive 1 GLOBAL_PUP_DONE active
6	GLOBAL_PDN_DONE_STS	GLOBAL_PDN_DONE raw real-time, non-sticky status flag. 0 (Default) GLOBAL_PDN_DONE inactive 1 GLOBAL_PDN_DONE active
5	GLOBAL_EN_ASSERT_STS	GLOBAL_EN_ASSERT raw real-time, non-sticky status flag. 0 (Default) GLOBAL_EN_ASSERT inactive 1 GLOBAL_EN_ASSERT active
4:0	—	Reserved

**7.16.9 INT\_MASK\_1**
**I<sup>2</sup>C Address: 0xD0 0040**

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—				TEMP_ERR_MASK	TEMP_WARN_MASK	VBATBR_ATT_CLR_MASK	VBATBR_MASK	—				BST_IPK_MASK	BST_SHORT_ERR_MASK	BST_DCM_UVP_ERR_MASK	BST_OVP_ERR_MASK
Default	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BST_OVP_MASK	LDM_PCM_ON_FALL_MASK	LDM_PCM_ON_RISE_MASK	—	—				—							
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0

Bits	Name	Description
31:27	—	Reserved
26	TEMP_ERR_MASK	TEMP_ERR interrupt pin mask. 0 TEMP_ERR unmask 1 (Default) TEMP_ERR mask
25	TEMP_WARN_MASK	TEMP_WARN interrupt pin mask. 0 TEMP_WARN unmask 1 (Default) TEMP_WARN mask
24	VBATBR_ATT_CLR_MASK	BR_ATT_CLR interrupt pin mask. 0 BR CLR unmask 1 (Default) BR CLR mask
23	VBATBR_MASK	BR interrupt pin mask. 0 BR unmask 1 (Default) BR mask
22:20	—	Reserved
19	BST_IPK_MASK	BST_IPK interrupt pin mask. 0 BST_IPK unmask 1 (Default) BST_IPK mask
18	BST_SHORT_ERR_MASK	BST_SHORT_ERR interrupt pin mask. 0 BST_SHORT_ERR unmask 1 (Default) BST_SHORT_ERR mask
17	BST_DCM_UVP_ERR_MASK	BST_DCM_UVP_ERR interrupt pin mask. 0 BST_DCM_UVP_ERR unmask 1 (Default) BST_DCM_UVP_ERR mask
16	BST_OVP_ERR_MASK	BST_OVP_ERR interrupt pin mask. 0 BST_OVP_ERR unmask 1 (Default) BST_OVP_ERR mask
15	BST_OVP_MASK	BST_OVP interrupt pin mask. 0 BST_OVP unmask 1 (Default) BST_OVP mask
14	LDM_PCM_ON_FALL_MASK	LDM_PCM_ON fall interrupt pin mask. 0 LDM_PCM_ON unmask 1 (Default) LDM_PCM_ON mask
13	LDM_PCM_ON_RISE_MASK	LDM_PCM_ON rise interrupt pin mask. 0 LDM_PCM_ON unmask 1 (Default) LDM_PCM_ON mask
12:0	—	Reserved

**7.16.10 INT\_MASK\_2**
**I<sup>2</sup>C Address: 0xD0 0044**

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	IMON_CLIP_MASK	VMON_CLIP_MASK	VBSTMON_CLIP_MASK	VBATMON_CLIP_MASK	—	—	—	—	—	—	—	—
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	1	1	1	1	1	1	1	1	—	—	—	—	1	1	1	1

Bits	Name	Description
31:25	—	Reserved
24	IMON_CLIP_MASK	IMON_CLIP interrupt pin mask. 0 IMON_CLIP unmask 1 (Default) IMON_CLIP mask
23	VMON_CLIP_MASK	VMON_CLIP interrupt pin mask. 0 VMON_CLIP unmask 1 (Default) VMON_CLIP mask
22	VBSTMON_CLIP_MASK	VBSTMON_CLIP interrupt pin mask. 0 VBSTMON_CLIP unmask 1 (Default) VBSTMON_CLIP mask
21	VBATMON_CLIP_MASK	MON_CLIP interrupt pin mask. 0 MON_CLIP unmask 1 (Default) MON_CLIP mask
20:0	—	Reserved

**7.16.11 INT\_MASK\_3**
**I<sup>2</sup>C Address: 0xD0 0048**

RW	31..16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	AMP_SHORT_ERR_MASK	—	—	—	—	—	—	—	—	—	—	—	—	—
Default	0xFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description
31:13	—	Reserved
12	AMP_SHORT_ERR_MASK	AMP_SHORT_ERR interrupt pin mask. 0 AMP_SHORT_ERR unmask 1 (Default) AMP_SHORT_ERR mask
11:0	—	Reserved

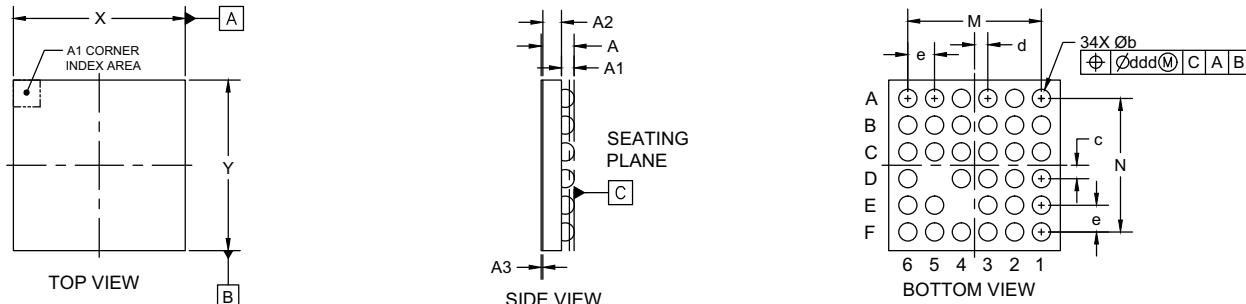
**7.16.12 INT\_MASK\_4**

I<sup>2</sup>C Address: 0xD0 004C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—			DCIN_ERR_MASK	VMON2_CLIP_MASK							—				
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	REFCLK_IN_MASK	PLL_UNLOCK_MASK		—				GLOBAL_PUP_DONE_MASK	GLOBAL_PDN_DONE_MASK	GLOBAL_EN_ASSERT_MASK		—			
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description
31:29	—	Reserved
28	DCIN_ERR_MASK	DCIN_ERR interrupt pin mask. 0 DCIN_ERR unmask 1 (Default) DCIN_ERR mask
27	VMON2_CLIP_MASK	VMON2_CLIP interrupt pin mask. 0 VMON2_CLIP unmask 1 (Default) VMON2_CLIP mask
26:14	—	Reserved
13	PLL_UNLOCK_MASK	PLL_UNLOCK interrupt pin mask. 0 PLL_UNLOCK unmask 1 (Default) PLL_UNLOCK mask
12:8	—	Reserved
7	GLOBAL_PUP_DONE_MASK	GLOBAL_PUP_DONE interrupt pin mask. 0 GLOBAL_PUP_DONE unmask 1 (Default) GLOBAL_PUP_DONE mask
6	GLOBAL_PDN_DONE_MASK	GLOBAL_PDN_DONE interrupt pin mask. 0 GLOBAL_PDN_DONE unmask 1 (Default) GLOBAL_PDN_DONE mask
5	GLOBAL_EN_ASSERT_MASK	GLOBAL_EN_ASSERT interrupt pin mask. 0 GLOBAL_EN_ASSERT unmask 1 (Default) GLOBAL_EN_ASSERT mask
4:0	—	Reserved

## 8 Package Dimensions



Dimension	Millimeters		
	Minimum	Nominal	Maximum
A	0.464	0.494	0.524
A1	0.175	0.19	0.205
A2	0.264	0.279	0.294
A3	---	0.025 REF	---
b	0.25	0.27	0.29
c	0.1925	0.2	0.2075
d	0.1925	0.2	0.2075
e	BSC	0.4	BSC
M	BSC	2	BSC
N	BSC	2	BSC
X	2.5469	2.5719	2.5969
Y	2.5289	2.5539	2.5789
ddd=0.015			

**Notes:** Controlling dimension is millimeters.

Dimensioning and tolerances per ASME Y 14.5-2009. The Ball A1 position indicator is for illustration purposes only. Dimension "b" applies to the solder sphere diameter and is measured at the maximum solder sphere diameter, parallel to primary Datum C. X/Y Tolerances can apply to an individual edge increasing or decreasing by 25um.

## 9 Thermal Characteristics

### 9.1 Typical Thermal Characteristics—JEDEC Four-layer 2s2p Board

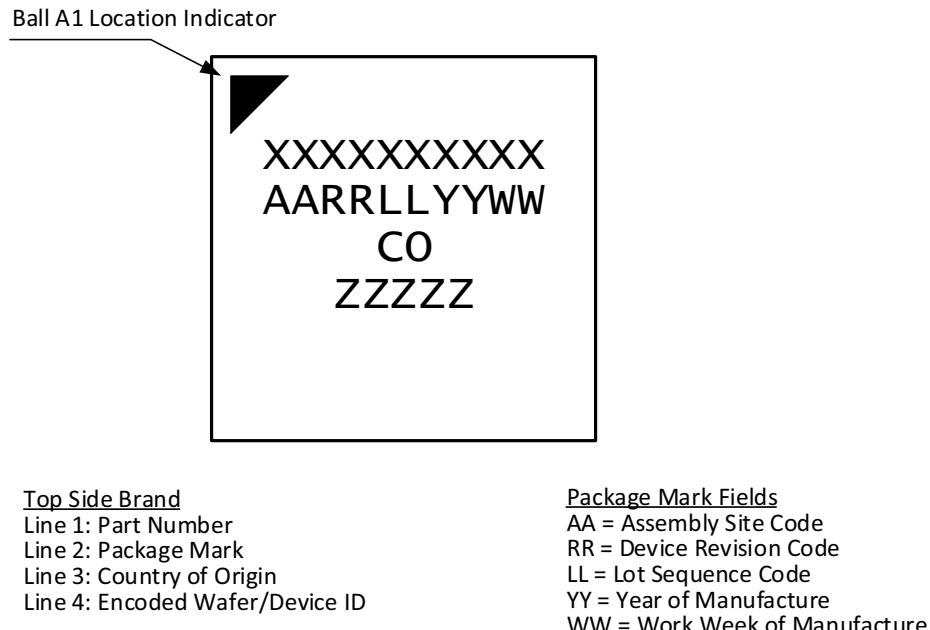
**Table 9-1. Typical JEDEC Four-layer, 2s2p Board Thermal Characteristics**

Parameter	Symbol	WLCSP	Units
Junction-to-ambient thermal resistance	$\theta_{JA}$	41.84	°C/W
Junction-to-board thermal resistance	$\theta_{JB}$	10.13	°C/W
Junction-to-case thermal resistance	$\theta_{JC}$	0.97	°C/W
Junction-to-board thermal-characterization parameter	$\Psi_{JB}$	9.94	°C/W
Junction-to-package-top thermal-characterization parameter	$\Psi_{JT}$	0.53	°C/W

**Notes:**

- Natural convection at the maximum recommended operating temperature  $T_A$  (see [Table 3-2](#))
- Four-layer, 2s2p PCB as specified by JESD51-9, and JESD51-11; dimensions: 114.5 × 101.5 × 1.6 mm
- Thermal parameters as defined by JESD51-12

## 10 Package Marking



**Figure 10-1. Package Marking**

## 11 Ordering Information

**Table 11-1. Ordering Information**

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Order Number
CS35L38A	Mono Class D Amplifier with Boost Converter and Monitoring	34-ball WLCSP	Yes	Commercial	-40°C to +85°C	Tape and reel	CS35L38A-CWZR

## 12 References

- Audio Engineering Society, AES17 Standard Measurement Methods for Digital Audio Equipment, <http://www.aes.org/>
- JEDEC Solid State Technology Association, *Test Boards for Area Array Surface Mount Package Thermal Measurements, JEDEC Standard No. JESD51-9*, July 2000, <http://www.jedec.org/>
- JEDEC Solid State Technology Association, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements, JEDEC Standard No. 51-11*, June 2001, <http://www.jedec.org/>
- JEDEC Solid State Technology Association, *Guidelines for Reporting and Using Electronic Package Thermal Information, JEDEC Standard No. JESD51-12*, May 2005, <http://www.jedec.org/>
- NXP Semiconductors, *The I2C-Bus Specification and User Manual (UM10204)*. <http://www.nxp.com/>

## 13 Revision History

**Table 13-1. Revision History**

Revision	Changes
A1 FEB 2019	Initial release
A2 APR 2019	<ul style="list-style-type: none"> <li>• Minor text corrections and cleanups in <a href="#">Section 4</a>, <a href="#">Section 7.8.1</a>, and <a href="#">Section 7.12.2</a>.</li> <li>• Updated default hardware revision to XXXX_XXXX in <a href="#">Section 6.1</a> and <a href="#">Section 7.1.2</a>.</li> <li>• Corrected RST state values in <a href="#">Table 4-8</a>.</li> <li>• Updated Power-Up sequence in <a href="#">Ex. 5-1</a>.</li> <li>• Updated BST_CTL description and value enumerations in <a href="#">Section 7.5.1</a>.</li> <li>• Corrected DAC_DC_DET register address in <a href="#">Section 7.15.1</a>.</li> </ul>

**Important:** Please check with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document.

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