CS8409

Multichannel High-Definition Audio Routing Controller

Digital Audio Serial Ports (ASPs)

- Two programmable serial ports
  - 8- to 96-kHz sample-rate support
- Time-division multiplex (TDM, up to 16 channels), I²S, and left-justified (LJ) formats
- Slave Mode support for source-synchronous inputs (SSIs)
- Eight-channel filter engine for each serial port, organized as four stereo pairs per port

High-Definition (HD) Audio Interface

- Audio function group (AFG)
  - Maps companion codec and amps to HD audio bus
  - Serial port organized as four sets of eight input and eight output widgets, one stereo pair per widget
  - Digital mic (DMIC) organized as two stereo pairs

SPI™ Master Serial Port

- Dual, independent chip-select outputs
  - Separates companion codec control from other audio devices
  - $\overline{CS2}$ and optional second master-in, slave-out (MISO) shared with general-purpose I/O (GPIO).
- Supports clock rate up to 12 MHz

Digital Microphone Interface

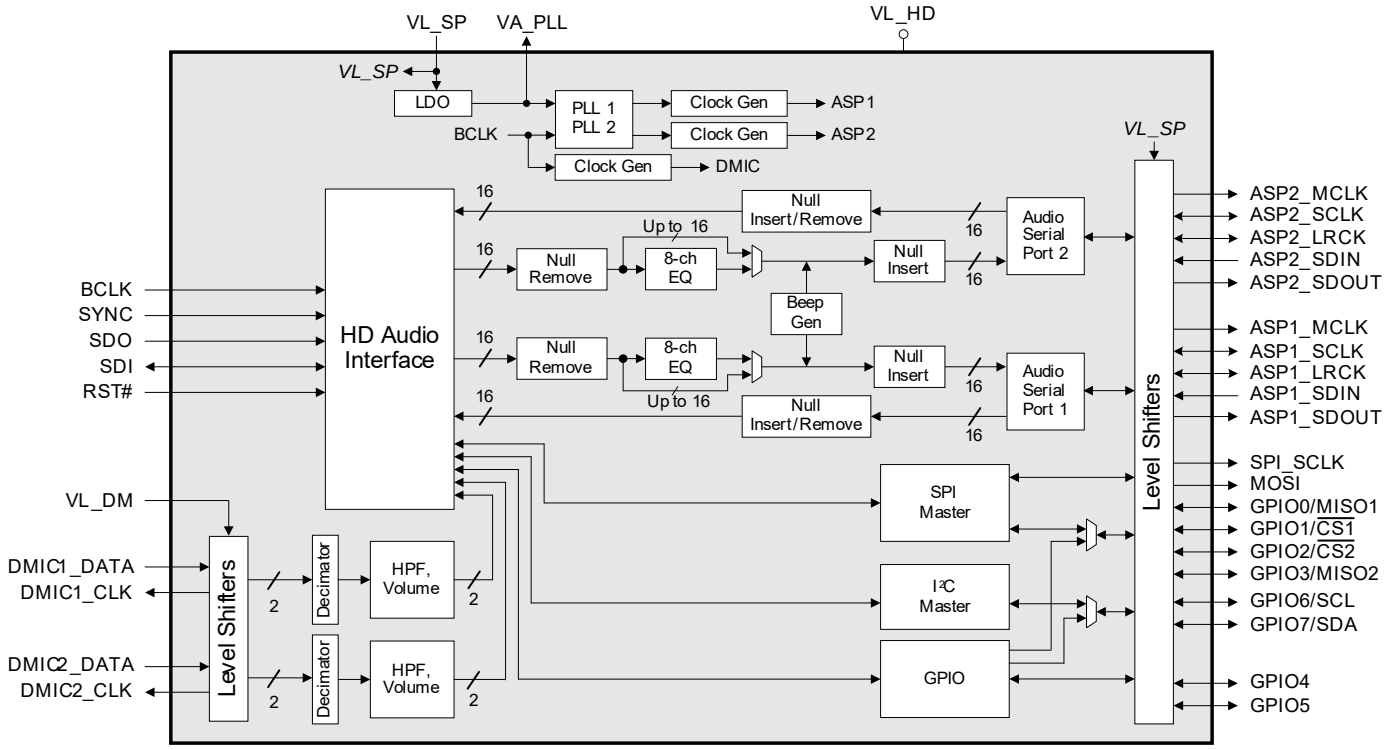
- Up to four channels of digital mic input
- Multichannel synchronization
- Digital gain control
  - Variable boost with selectable 0-, +10-, and +20-dB gain settings
  - –51.0 to +12.0 dB in 1.0-dB steps
  - Soft-ramp transition

I²C Master Serial Port

- Supports Standard Mode, Fast Mode, and Fast-Mode Plus
- Simplified HD Audio control method for subaddressed register space

System Features

- Programmable unsolicited response (UR) capability on multiple GPIOs
- Two PLLs, for independent ASP rates
- Advanced granular power controls with support for D3cold and CLKSTOP
- Detects wake event and generates power-state change request in D3hot State



General Description

The CS8409 is a multichannel HD audio routing controller. CS8409 includes support for four channels of digital microphone data and two bidirectional ASPs for up to 32 channels of TDM data or 4 channels of I²S data. The CS8409 is intended to be used with a remote companion codec that implements high performance analog functions in close physical proximity to the end-equipment audio port or speaker driver.

Each ASP supports up to 16 channels at sample rates from 8 to 96 kHz. Double Sample Mode enables 96-kHz streams to be transmitted while operating the ASP at 48-kHz frame rate (f_{LRCK} = 48 kHz). Two PLLs enable the ASPs to operate at independent base rates. The data capture edge and sync edge to valid data delay are programmable independently for each ASP. The CS8409 can generate a master clock (ASPx_MCLK) that is either a multiple of the bit clock (ASPx_SCLK) or a fixed 12 or 24 MHz for each ASP.

The CS8409 includes an I²C master serial port to configure devices attached to the ASPs. The I²C master is compatible with Standard, Fast, and Fast-Mode Plus protocols, allowing clock rates up to 1 MHz. When I²C master operation is not required, the I²C pins may be used as GPIO pins. CS8409 includes a SPI master that operates at clock rates up to 12 MHz. When enabled, the SPI master port requires a minimum of two GPIO pins for master data in (GPIO0/MISO1) and slave chip select (GPIO1/$\overline{CS1}$). An additional GPIO pin may be used as a second slave chip select (GPIO2/$\overline{CS2}$) to enable control of two independent SPI slaves on the same bus. An additional GPIO may also be used as a second master data input (GPIO3/MISO2) dedicated to the SPI slave enabled by $\overline{CS2}$. MISO2 and $\overline{CS2}$ allow the SPI port to be shared with up to two devices that do not support Hi-Z data outputs when chip select is not asserted.

CS8409 supports as many as four channels of digital microphone input. Each channel has dedicated decimation filters, digital volume control, mute, and high-pass filtering.

The CS8409 is available in a 36-pin WLCSP package and a 40-pin QFN package in Industrial Grade (–40 to +85°C) temperature range. The CDB8409 customer demonstration board is also available for device evaluation and implementation suggestions.

Table of Contents

1 Pin Descriptions

Fig. 1-1 shows the CS8409 signals, which are described in Table 1-1.

1.1 WLCSP Ballout

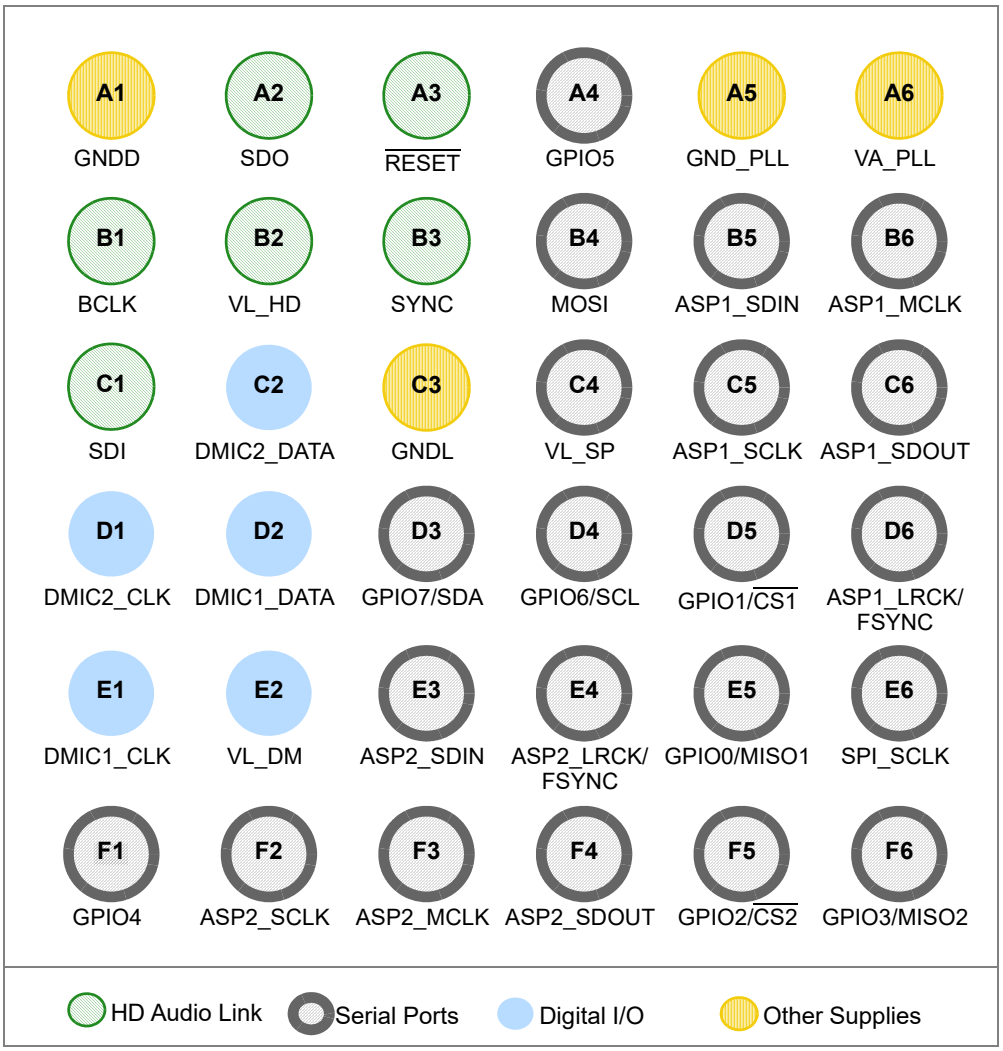


Figure 1-1. Top-Down (Through-Package) View—36-Ball WLCSP Package

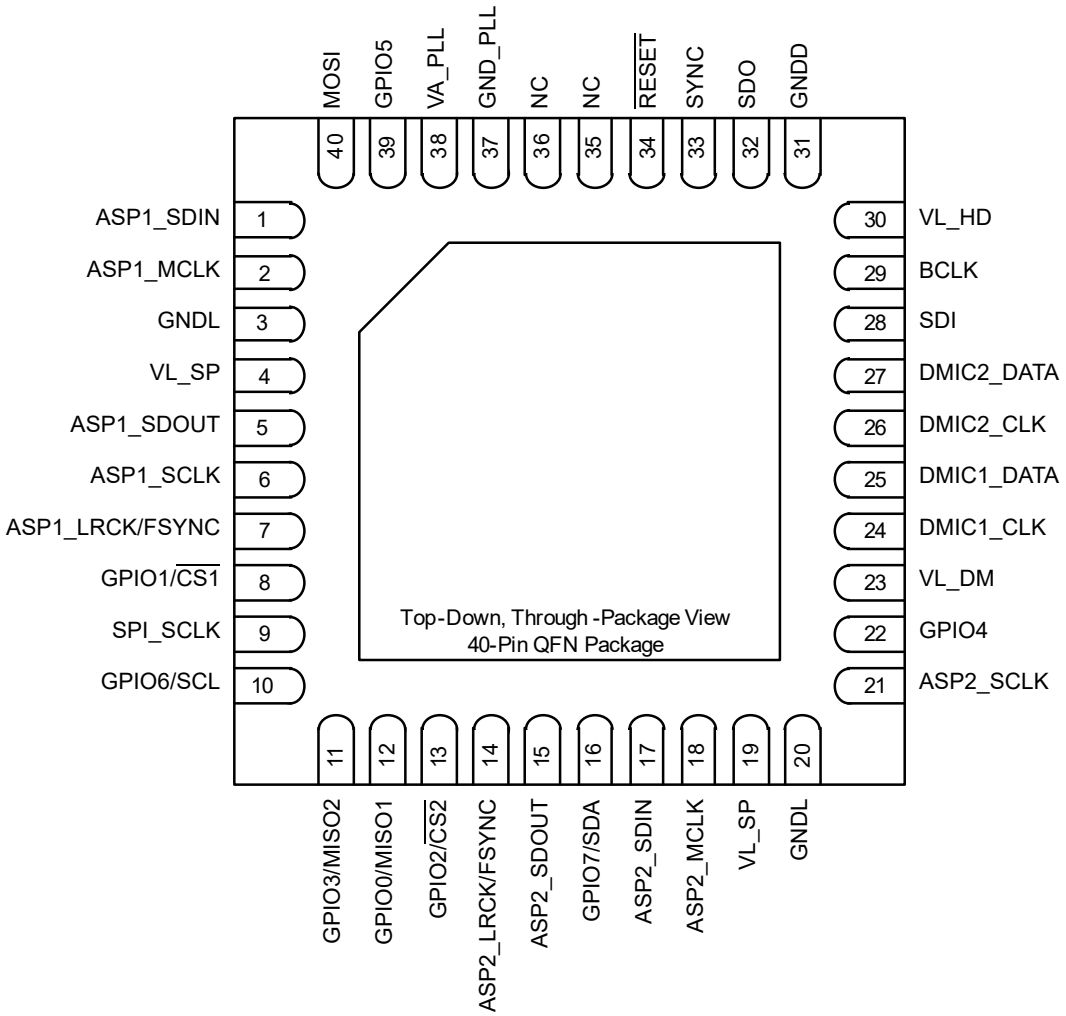


Figure 1-2. 40-Pin QFN Package

Table 1-1. Pin Descriptions

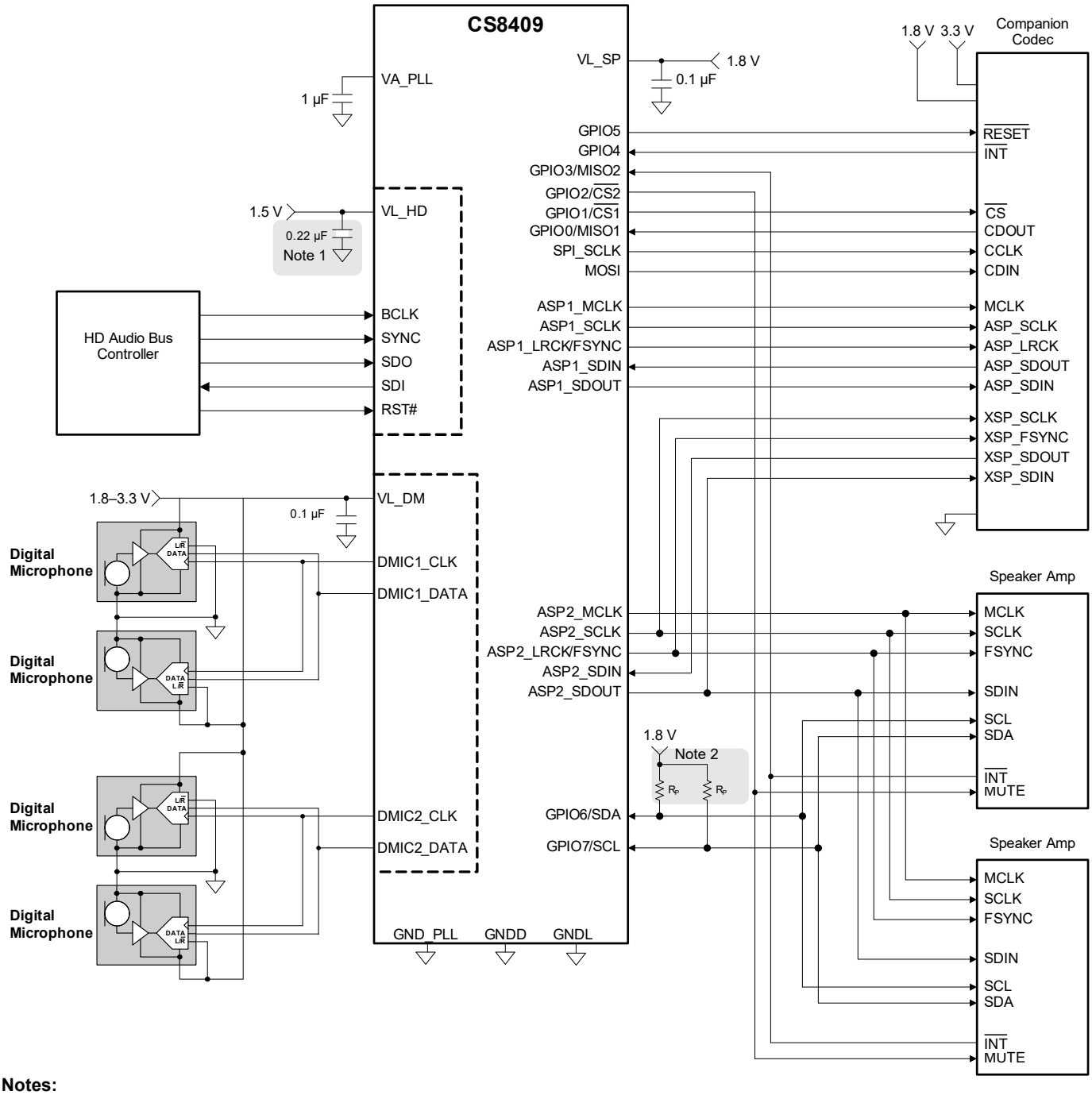
Pin Name	CSP #	QFN #	Power Supply[1]	I/O	Description	Internal Connection	Driver	Receiver	State after POR [2]
					HD Audio Link				
VL_HD	B2	30	VL_HD	I	**Digital Core Supply.** Power supply for the digital core. (1.5 or 1.8 V)	—	—	—	—
BCLK	B1	29	VL_HD	I	**Bit Clock.** 24-MHz bit clock from the HD audio bus.	—	—	CMOS input	
SYNC	B3	33	VL_HD	I	**Sync Clock.** 48-kHz frame sync signal from the HD audio bus.	—	—	CMOS input	—
SDO	A2	32	VL_HD	I	**Serial Data Input.** Serial data input stream from the HD audio bus.	—	—	CMOS input	—
SDI	C1	28	VL_HD	I/O	**Serial Data Output.** Serial data output stream to the HD audio bus.	—	Tristateable CMOS output	CMOS input	Low
RESET	A3	34	VL_HD	I	**Reset.** Reset input from the HD audio bus, negative logic.	—	—	CMOS input	—
					Serial Ports				
VL_SP	C4	4,19	VL_SP	I	**Serial Port Supply.** Power supply for the ASPs, I²C, and SPI interfaces (1.8 V).	—	—	—	—
ASP1_MCLK ASP2_MCLK	B6 F3	2 18	VL_SP	O	**Master Clock.** Master clock source for ASP interfaces.	Weak pull-down	Tristateable CMOS output	—	Hi-Z

Table 1-1. Pin Descriptions *(Cont.)*

Pin Name	CSP #	QFN #	Power Supply[1]	I/O	Description	Internal Connection	Driver	Receiver	State after POR [2]
ASP1_SCLK ASP2_SCLK	C5 F2	6 21	VL_SP	I/O	**Serial Clock.** Serial shift clock for ASP interfaces.	Weak pull-down	Tristateable CMOS output	CMOS input	Hi-Z
ASP1_LRCK/FSYNC ASP2_LRCK/FSYNC	D6 E4	7 14	VL_SP	I/O	**Left/Right Clock, Frame Sync.** Frame indicator for TDM interface and word clock for I²S or LJ interface.	Weak pull-down	Tristateable CMOS output	Hysteresis on CMOS input	Hi-Z
ASP1_SDOUT ASP2_SDOUT	C6 F4	5 15	VL_SP	O	**Serial Data Output.** Serial data output for ASP interfaces.	Weak pull-down	Tristateable CMOS output	—	Hi-Z
ASP1_SDIN ASP2_SDIN	B5 E3	1 17	VL_SP	I	**Serial Data Input.** Serial data input for ASP interfaces.	Weak pull-down	—	Hysteresis on CMOS input	Hi-Z
SPI_SCLK	E6	9	VL_SP	O	**SPI Master Clock.** Clock for the SPI interface.	Weak pull-down	CMOS output	—	Hi-Z
MOSI	B4	40	VL_SP	O	**SPI Master Data.** Output data for the SPI interface	Weak pull-down	CMOS output	—	Hi-Z
GPIO0/MISO1 GPIO1/CS1 GPIO2/CS2 GPIO3/MISO2	E5 D5 F5 F6	12 8 13 11	VL_SP	I/O	**General-Purpose I/O, SPI Master.** Mixed function: general-purpose input or output, or SPI interface	Weak pull-down	Tristateable CMOS output	Hysteresis on CMOS input	Hi-Z
GPIO6/SCL GPIO7/SDA	D4 D3	10 16	VL_SP	I/O	**General-Purpose I/O, I²C Master.** Mixed function: general-purpose input or output, or I²C interface.	Weak pull-down	Tristateable CMOS output (open-drain capable)	Hysteresis on CMOS input	Hi-Z
GPIO4 GPIO5	F1 A4	22 39	VL_SP	I/O	**General-Purpose I/O.** General-purpose input or output.	Weak pull-down	Tristateable CMOS output	Hysteresis on CMOS input	Hi-Z
Digital I/O									
VL_DM	E2	23	VL_DM	I	**Digital Mic Supply.** Power supply for the digital microphone interfaces. (1.8–3.3 V)	—	—	—	—
DMIC1_DATA DMIC2_DATA	D2 C2	25 27	VL_DM	I	**Digital Mic Data.** Data input from a pair of digital microphones.	Weak pull-down	—	Hysteresis on CMOS input	Hi-Z
DMIC1_CLK DMIC2_CLK	E1 D1	24 26	VL_DM	O	**Digital Mic Clock.** Clock output to a pair of digital microphones.	Weak pull-down	Tristateable CMOS output (open-drain capable)	—	Hi-Z
Other Supplies									
GNDL	C3	3, 20	—	I	**Digital Interface Ground.** Combined ground reference for VL_IF, and VL_SP.	—	—	—	—
GNDD	A1	31	VL_HD	I	**Digital Core Ground.** Ground reference for the digital core.	—	—	—	—
VA_PLL	A6	38	VL_SP	O	**PLL Supply.** Power supply bypass for the serial port PLL.	—	—	—	—
GND_PLL	A5	37	VA_PLL	I	**PLL Ground.** Ground reference for the serial port PLL.	—	—	—	—

1.Logic levels must not exceed the corresponding power-supply voltage. See Table 3-2.
2.Pins with weak pull-down internal connection that show Hi-Z state at reset will be weakly pulled to ground at reset.

2 Typical Connection Diagram



Notes:
1. Low ESR, X7R or better
2. Table 3-10 (Footnote 1) gives guidelines for pull-up resistor (R_P) values.

Figure 2-1. Typical Connection Diagram

3 Characteristic and Specifications

Table 3-1. Recommended Operating Conditions

Test conditions (unless specified otherwise): GNDD = GNDL = GND_PLL = 0 V; all voltages with respect to ground.

Parameters [1]			Symbol	Minimum	Maximum	Units
DC power supply	Digital microphone interface	1.8-V interface 3.3-V interface	VL_DM	1.71 3.14	1.89 3.47	V
	Digital core/HD audio bus interface	1.5-V interface 1.8-V interface	VL_HD	1.42 1.71	1.58 1.89	V
	ASP, GPIO, SPI and I²C master interfaces		VL_SP	1.71	1.89	V
Ambient temperature (industrial)			T_A	–40	+85	°C

1. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

Table 3-2. Absolute Maximum Ratings

Test conditions (unless specified otherwise): GNDD = GNDL = GND_PLL = 0 V; all voltages with respect to ground.
Warning: Operation at or beyond these limits may result in permanent damage to the device.

Parameters		Symbol	Minimum	Maximum	Units
DC power supply	Digital microphone interface	VL_DM	–0.3	4.0	V
	Digital core, HD audio bus interface	VL_HD	–0.3	2.2	V
	Serial port interfaces	VL_SP	–0.3	2.2	V
Input current [1]		I_{in}	–	±10	mA
External voltage applied to digital input [2]		V_{INDI}	–0.3	VL_xx + 0.3	V
External voltage applied to digital output		V_{INDO}	–0.3	VL_xx + 0.3	V
Ambient operating temperature (power applied)		T_A	–50	+115	°C

CAUTION: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-1, “Recommended Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins do not cause SCR latch-up.
2. Maximum over/under voltage is limited by input current.

Table 3-3. Audio Serial Port Interface Characteristics—TDM Mode

Test conditions (unless specified otherwise): GNDD = GNDL = GND_PLL = 0 V; all voltages with respect to ground; VL_HD = 1.5 V, VL_DM = VL_SP = 1.8 V; Inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL_SP; T_A = +25°C; C_{LOAD} = 60 pF; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

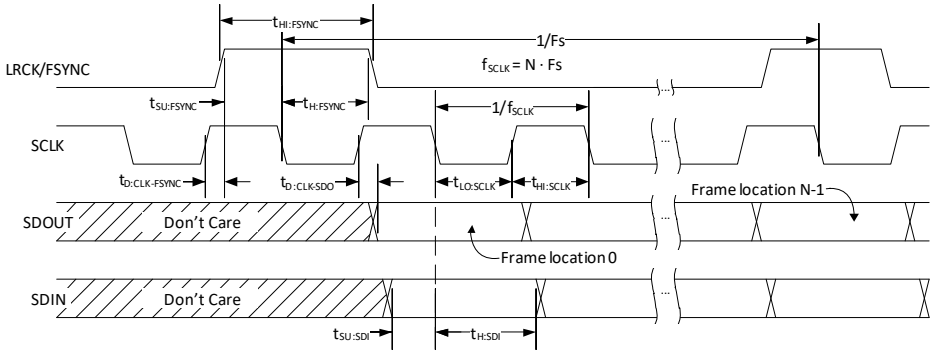
Parameters [1,2,3]			Symbol	Minimum	Typical	Maximum	Units
MCLK frequency, maximum		C_{LOAD} = 30 pF C_{LOAD} = 60 pF	f_{MCLK}	— —	24.576 12.288	25.81 —	MHz MHz
MCLK high period			—	$1/(2 \cdot f_{MCLK}) - 4.2$	—	$1/(2 \cdot f_{MCLK}) + 4.2$	ns
Master Mode	FSYNC frame rate (Section 4.2.4 gives configuration details)		Fs	(See Table 5-2)			kHz
	FSYNC high period [4]		$t_{HI:FSYNC}$	$1/f_{SCLK}$	—	$(n-1)/f_{SCLK}$	s
	FSYNC delay time after SCLK launching edge [5]		$t_{D:CLK—FSYNC}$	0	—	15	ns
	SCLK frequency		f_{SCLK}	—	—	25.81	MHz
	SCLK high period		$t_{HI:SCLK}$	$1/(2 \cdot f_{SCLK}) - 4.2$	—	$1/(2 \cdot f_{SCLK}) + 4.2$	ns
	SDIN setup time before SCLK latching edge [5]		$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [5]		$t_{H:SDI}$	5	—	—	ns
	SDOUT delay time after SCLK launching edge [5]		$t_{D:CLK—SDO}$	0	—	15	ns
	SDOUT Hi-Z delay time after SCLK latching edge [5,6]	ASPx_HIZD = 00 ASPx_HIZD = 01 ASPx_HIZD = 10 ASPx_HIZD = 11	$t_{DLY:HiZ}$	4.274 6.074 8.054 —	— — — $(0.5 \cdot f_{SCLK})^{-1}$	12 17 22 —	ns ns ns ns

Table 3-3. Audio Serial Port Interface Characteristics—TDM Mode *(Cont.)*

Test conditions (unless specified otherwise): GNDD = GNDL = GND_PLL = 0 V; all voltages with respect to ground; VL_HD = 1.5 V, VL_DM = VL_SP = 1.8 V; Inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL_SP; T_A = +25°C; C_{LOAD} = 60 pF; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameters [1,2,3]		Symbol	Minimum	Typical	Maximum	Units
Slave Mode	FSYNC frame rate (Section 4.2.4 gives configuration details)	Fs		(See Table 5-2)		kHz
	FSYNC frame rate	—	0.99	—	1.01	Fs
	FSYNC setup time before SCLK latching edge [5]	$t_{SU:FSYNC}$	10	—	—	ns
	FSYNC hold time after SCLK latching edge [5]	$t_{H:FSYNC}$	5	—	—	ns
	SCLK frequency	f_{SCLK}	—	—	25.81	MHz
	SCLK high period	$t_{HI:SCLK}$	18.5	—	—	ns
	SCLK low period	$t_{LO:SCLK}$	18.5	—	—	ns
	SCLK duty cycle	—	45	—	55	%
	SDIN setup time before SCLK latching edge [5]	$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [5]	$t_{H:SDI}$	5	—	—	ns
	SDOUT delay time after SCLK launching edge [5]	$t_{D:CLK—SDO}$	0	—	15	ns
	SDOUT Hi-Z delay time after SCLK latching edge [5,6] ASPx_HIZD = 00	$t_{DLY:HiZ}$	4.095	—	22	ns
	ASPx_HIZD = 01		6.035	—	27	ns
	ASPx_HIZD = 10		8.035	—	32	ns
	ASPx_HIZD = 11		—	$(0.5 \cdot f_{SCLK})^{-1}$	—	ns

1. Output clock frequencies follow the bit clock (BCLK) frequency proportionally. Any deviation of the bit clock source from the nominal supported rates are directly imparted to the output clock rate by the same factor (e.g., +100 ppm offset in the frequency of BCLK becomes a +100 ppm offset in MCLK, LRCK/FSYNC, and SCLK).
2. TDM interface timing (shown with TDM interface timing (shown with ASPx_FSD = 010, ASPx_LCHI = 1, ASPx_STP = 1)



3. Applies to master and slave modes, unless specified otherwise.
4. Maximum LRCK duty cycle is equal to frame length, in SCLK periods, minus 1. Maximum duty cycle occurs when LRCK_HI is set to 511 SCLK periods and LRCK period is set to 512 SCLK periods.
5. Data may be latched on either the rising or falling edge of SCLK
6. TDM interface Hi-Z timing

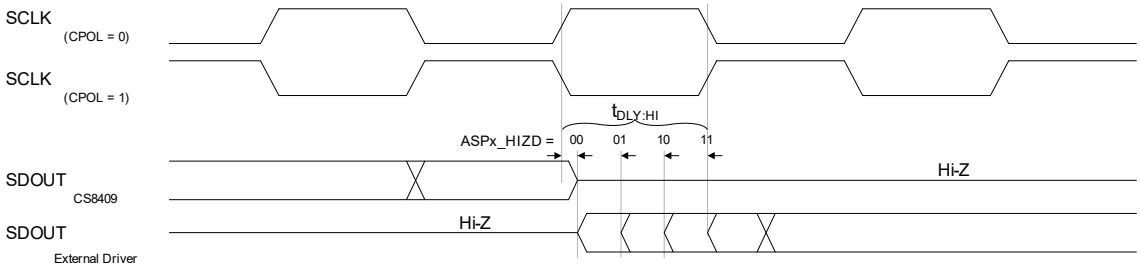
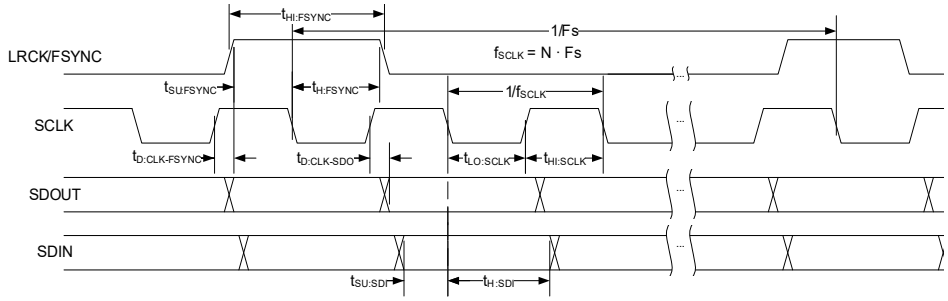


Table 3-4. Serial Port Interface Characteristics—DSP/PCM Mode

Test conditions (unless specified otherwise): GNDD = GNDL = GND_PLL = 0 V; all voltages with respect to ground; VL_HD = 1.5 V, VL_DM = VL_SP = 1.8 V; Inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL_SP; T_A = +25°C; C_{LOAD} = 60 pF; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameters [1,2,3]		Symbol	Minimum	Typical	Maximum	Units
MCLK frequency, maximum	C_{LOAD} = 30 pF C_{LOAD} = 60 pF	f_{MCLK}	— —	24.576 12.288	25.81 —	MHz MHz
MCLK high period		—	$1/(2 \cdot f_{MCLK}) - 4.2$	—	$1/(2 \cdot f_{MCLK}) + 4.2$	ns
Master Mode	FSYNC frame rate (Section 4.2.4 gives configuration details)	Fs	(See Table 5-2)			kHz
	FSYNC high period [4]	$t_{HI:FSYNC}$	$1/f_{SCLK}$	—	$(n–1)/f_{SCLK}$	s
	FSYNC delay time after SCLK launching edge [5]	$t_{D:CLK—FSYNC}$	0	—	15	ns
	SCLK frequency	f_{SCLK}	—	—	25.81	MHz
	SCLK high period	$t_{HI:SCLK}$	$1/(2 \cdot f_{SCLK}) –4.2$	—	$1/(2 \cdot f_{SCLK}) + 4.2$	ns
	SDIN setup time before SCLK latching edge [5]	$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [5]	$t_{H:SDI}$	5	—	—	ns
	SDOUT delay time after SCLK launching edge [5]	$t_{D:CLK—SDO}$	0	—	15	ns
Slave Mode	FSYNC frame rate (Section 4.2.4 gives configuration details)	Fs	(See Table 5-2)			kHz
	FSYNC frame rate	—	0.99	—	1.01	Fs
	FSYNC high period [4]	$t_{HI:FSYNC}$	$1/f_{SCLK}$	—	$(n–1)/f_{SCLK}$	s
	FSYNC setup time before SCLK latching edge [5]	$t_{SU:FSYNC}$	10	—	—	ns
	FSYNC hold time after SCLK latching edge [5]	$t_{H:FSYNC}$	5	—	—	ns
	SCLK frequency	f_{SCLK}	—	—	25.81	MHz
	SCLK high period	$t_{HI:SCLK}$	18.5	—	—	ns
	SCLK low period	$t_{LO:SCLK}$	18.5	—	—	ns
	SCLK duty cycle	—	45	—	55	%
	SDIN setup time before SCLK latching edge [5]	$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [5]	$t_{H:SDI}$	5	—	—	ns
	SDOUT delay time after SCLK launching edge [5]	$t_{D:CLK—SDO}$	0	—	15	ns

1. Output clock frequencies follow the bit clock (BCLK) frequency proportionally. Any deviation of the bit clock source from the nominal supported rates are directly imparted to the output clock rate by the same factor (e.g., +100 ppm offset in the frequency of BCLK becomes a +100 ppm offset in MCLK, LRCK/FSYNC, and SCLK).
2. DSP/PCM interface timing (shown with ASPx_FSD = 0b010, ASPx_LCHI = 1)



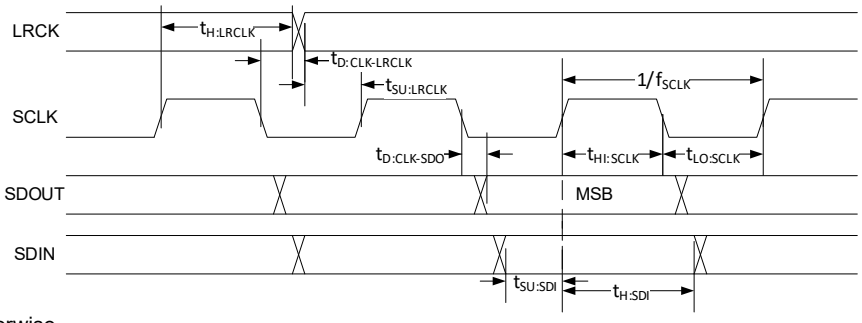
3. Applies to master and slave modes unless specified otherwise.
4. Maximum LRCK duty cycle is equal to frame length, in SCLK periods, minus 1. Maximum duty cycle occurs when LRCK_HI is set to 511 SCLK periods and LRCK period is set to 512 SCLK periods.
5. Data may be latched on either the rising or falling edge of SCLK

Table 3-5. Serial Port Interface Characteristics—I²S Mode

Test conditions (unless specified otherwise): GNDD = GNDL = GND_PLL = 0 V; all voltages with respect to ground; VL_HD = 1.5 V, VL_DM = VL_SP = 1.8 V; Inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL_SP; T_A = +25°C; C_{LOAD} = 60 pF; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameters [1,2,3]		Symbol	Minimum	Typical	Maximum	Units
MCLK frequency, maximum	C_{LOAD} = 30 pF C_{LOAD} = 60 pF	f_{MCLK}	— —	24.576 12.288	25.81 —	MHz MHz
MCLK high period		—	$1/(2 \cdot f_{MCLK}) - 4.2$	—	$1/(2 \cdot f_{MCLK}) + 4.2$	ns
Master Mode	LRCK frame rate (Section 4.2.4 gives configuration details)	Fs	(See Table 5-2)			kHz
	LRCK frame rate	—	0.99	—	1.01	Fs
	LRCK duty cycle	—	45	—	55	%
	LRCK delay time after SCLK launching edge [4]	$t_{D:CLK—LRCK}$	0	—	15	ns
	SCLK frequency	f_{SCLK}	—	—	25.81	MHz
	SCLK high period	$t_{HI:SCLK}$	$1/(2 \cdot f_{SCLK}) - 4.2$	—	$1/(2 \cdot f_{SCLK}) + 4.2$	ns
	SDIN setup time before SCLK latching edge [4]	$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [4]	$t_{H:SDI}$	5	—	—	ns
	SDOUT delay time after SCLK launching edge	$t_{D:CLK—SDO}$	0	—	15	ns
Slave Mode	LRCK frame rate (Section 4.2.4 gives configuration details)	Fs	(See Table 5-2)			kHz
	LRCK frame rate	—	0.99	—	1.01	Fs
	LRCK setup time before SCLK latching edge [4]	$t_{SU:LRCK}$	10	—	—	ns
	LRCK hold time after SCLK latching edge [4]	$t_{H:LRCK}$	5	—	—	ns
	SCLK frequency	f_{SCLK}	—	—	25.81	MHz
	SCLK high period	$t_{HI:SCLK}$	18.5	—	—	ns
	SCLK low period	$t_{LO:SCLK}$	18.5	—	—	ns
	SCLK duty cycle	—	45	—	55	%
	SDIN setup time before SCLK latching edge [4]	$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [4]	$t_{H:SDI}$	5	—	—	ns
	SDOUT delay time after SCLK launching edge	$t_{D:CLK—SDO}$	0	—	15	ns

1. Output clock frequencies follow BCLK frequency proportionally. Any deviation of the bit clock source from nominal supported rates is directly imparted to the output clock rate by the same factor (e.g., +100 ppm offset in the frequency of BCLK becomes a +100-ppm offset in MCLK, LRCK, and SCLK).
2. I²S interface timing



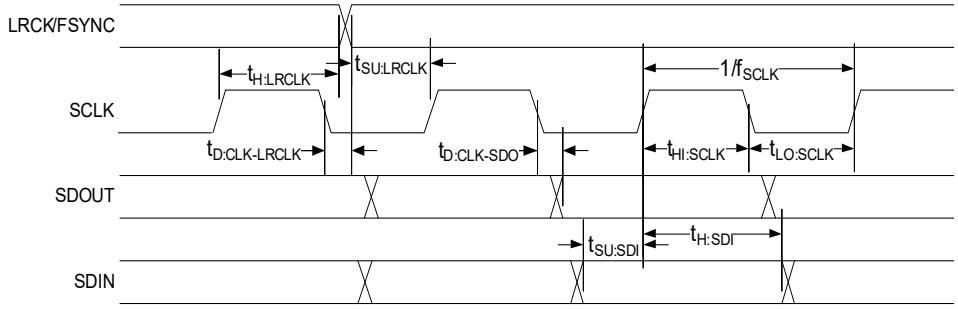
3. Applies to master and slave modes unless specified otherwise.
4. Data is latched on the rising or falling edge of SCLK as determined by ASPx_SCPOL_IN, ASPx_SCPOL_OUT, and ASPx_FSD bits (See Table 6-173).

Table 3-6. Serial Port Interface Characteristics—LJ Mode

Test conditions (unless specified otherwise): GNDD = GNDL = GND_PLL = 0 V; all voltages with respect to ground; VL_HD = 1.5 V, VL_DM = VL_SP = 1.8 V; Inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL_SP; T_A = +25°C; C_{LOAD} = 30 pF; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameters [1,2,3]		Symbol	Minimum	Typical	Maximum	Units
MCLK frequency, maximum	C_{LOAD} = 30 pF C_{LOAD} = 60 pF	f_{MCLK}	— —	24.576 12.288	25.81 —	MHz MHz
MCLK high period		—	$1/(2 \cdot f_{MCLK}) - 4.2$	—	$1/(2 \cdot f_{MCLK}) + 4.2$	ns
Master Mode	LRCK frame rate (Section 4.2.4 gives configuration details)	Fs	(See Table 5-2)			kHz
	LRCK frame rate	—	0.99	—	1.01	Fs
	LRCK duty cycle	—	45	—	55	%
	LRCK delay time after SCLK launching edge [4]	$t_{D:CLK—LRCK}$	0	—	15	ns
	SCLK frequency	f_{SCLK}	—	—	25.81	MHz
	SCLK high period	$t_{HI:SCLK}$	$1/(2 \cdot f_{SCLK}) - 4.2$	—	$1/(2 \cdot f_{SCLK}) + 4.2$	ns
	SDIN setup time before SCLK latching edge [4]	$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [4]	$t_{H:SDI}$	5	—	—	ns
	SDOUT delay time after SCLK launching edge [4]	$t_{D:CLK—SDO}$	0	—	15	ns
Slave Mode	LRCK frame rate (Section 4.2.4 gives configuration details)	Fs	(See Table 5-2)			kHz
	LRCK frame rate	—	0.99	—	1.01	Fs
	LRCK setup time before SCLK latching edge [4]	$t_{SU:LRCK}$	10	—	—	ns
	LRCK hold time after SCLK latching edge [4]	$t_{H:LRCK}$	5	—	—	ns
	SCLK frequency	f_{SCLK}	—	—	25.81	MHz
	SCLK high period	$t_{HI:SCLK}$	18.5	—	—	ns
	SCLK low period	$t_{LO:SCLK}$	18.5	—	—	ns
	SCLK duty cycle	—	45	—	55	%
	SDIN setup time before SCLK latching edge [4]	$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [4]	$t_{H:SDI}$	5	—	—	ns
	SDOUT delay time after SCLK launching edge [4]	$t_{D:CLK—SDO}$	0	—	15	ns

1. Output clock frequencies follow BCLK frequency proportionally. Any deviation of the bit clock source from nominal supported rates is directly imparted to the output clock rate by the same factor (e.g., +100 ppm offset in the frequency of BCLK becomes a +100 ppm offset in MCLK, LRCK, and SCLK).
2. LJ interface timing



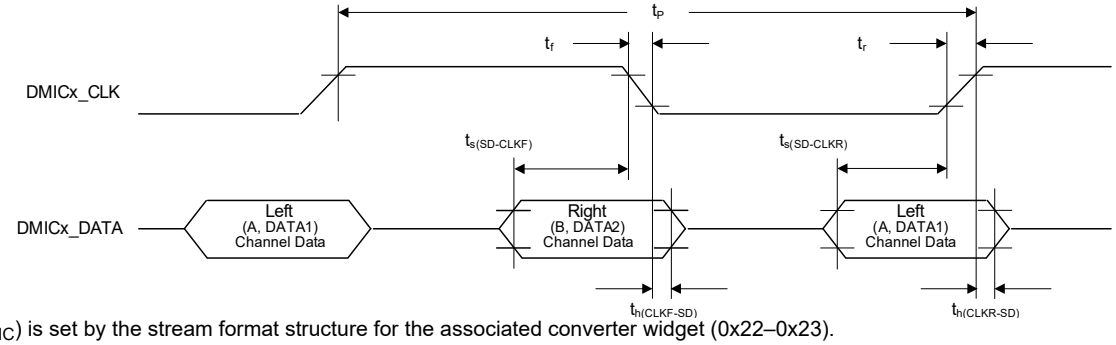
3. Applies to master and slave modes unless specified otherwise.
4. Data is latched on the rising or falling edge of SCLK as determined by ASPx_SCPOL_IN, ASPx_SCPOL_OUT, and ASPx_FSD bits (See Table 6-173).

Table 3-7. Digital Microphone Interface Characteristics

Test conditions (unless specified otherwise): GNDD = GNDL = GND_PLL = 0 V; all voltages with respect to ground; VL_HD = 1.5 V, VL_DM = VL_SP = 1.8 V; Inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL_DM; T_A = +25°C; C_{LOAD} = 30 pF; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameters [1,2]		Symbol	Minimum	Typical	Maximum	Units
Output clock (DMIC_CLK) period [3]	$Fs_{DMIC} \geq$ 44.1 kHz	t_P	—	8 • T_cyc [4]	—	s
	$Fs_{DMIC} \leq$ 32.0 kHz		—	12 • T_cyc	—	s
DMICx_CLK duty cycle		—	45	—	55	%
DMICx_CLK rise time [5]		t_r	—	—	10	ns
DMICx_CLK fall time [5]		t_f	—	—	10	ns
DMICx_DATA setup time before DMIC_CLK rising edge		$t_{s(SD-CLKR)}$	10	—	—	ns
DMICx_DATA hold time after DMIC_CLK rising edge		$t_{h(CLKR-SD)}$	0	—	—	ns
DMICx_DATA setup time before DMIC_CLK falling edge		$t_{s(SD-CLKF)}$	10	—	—	ns
DMICx_DATA hold time after DMIC_CLK falling edge		$t_{h(CLKF-SD)}$	0	—	—	ns
Full-scale 1's density		—	—	78		%

1. Output clock frequency follows the BCLK frequency proportionally. Any deviation of the bit clock source from the nominal supported rates is directly imparted to the output clock rate by the same factor (e.g., +100-ppm offset in the frequency of BCLK becomes a +100-ppm offset in DMIC_CLK).
2. Digital MIC interface timing



3. The DMIC sample rate (Fs_{DMIC}) is set by the stream format structure for the associated converter widget (0x22–0x23).
4. T_cyc is the period of the input BCLK signal.
5. Rise and fall times are measured from 0.1 • VL_DM to 0.9 • VL_DM.

Table 3-8. Digital Interface Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS8409 connections; GNDD = GNDL = GND_PLL = 0 V; voltages are with respect to ground; VL_HD = 1.5 V, VL_DM = VL_SP = 1.8 V; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameters [1]		Symbol	Minimum	Maximum	Units
Input leakage current		I_{in}	—	±10	µA
Input pin capacitance		C_{in}	—	7.5	pF
VL_HD = 1.5 V	High-level input voltage	V_{IH}	0.60 • VL_HD	—	V
	Low-level input voltage	V_{IL}	—	0.40 • VL_HD	V
	High-level output voltage (I_{OUT} = –500 µA)	V_{OH}	0.90 • VL_HD	—	V
	Low-level output voltage (I_{OUT} = 1500 µA)	V_{OL}	—	0.10 • VL_HD	V
VL_HD = 1.8 V	High-level input voltage	V_{IH}	0.65 • VL_HD	—	V
	Low-level input voltage	V_{IL}	—	0.35 • VL_HD	V
	High-level output voltage (I_{OUT} = –500 µA)	V_{OH}	0.90 • VL_HD	—	V
	Low-level output voltage (I_{OUT} = 1500 µA)	V_{OL}	—	0.10 • VL_HD	V
VL_DM = 1.8 V	High-level input voltage	V_{IH}	0.7 • VL_DM	—	V
	Low-level input voltage	V_{IL}	—	0.3 • VL_DM	V
	High-level output voltage (I_{OUT} = –100 µA)	V_{OH}	VL_DM – 0.2	—	V
	Low-level output voltage (I_{OUT} = 100 µA)	V_{OL}	—	0.2	V
VL_DM = 3.3 V	High-level input voltage	V_{IH}	0.65 • VL_DM	—	V
	Low-level input voltage	V_{IL}	—	0.35 • VL_DM	V
	High-level output voltage (I_{OUT} = –100 µA)	V_{OH}	VL_DM – 0.2	—	V
	Low-level output voltage (I_{OUT} = 100 µA)	V_{OL}	—	0.2	V
VL_SP = 1.8 V (see Table 3-10 for I^2C pin characteristics)	High-level input voltage	V_{IH}	0.7 • VL_SP	—	V
	Low-level input voltage	V_{IL}	—	0.3 • VL_SP	V
	High-level output voltage (I_{OUT} = –100 µA)	V_{OH}	0.9 • VL_SP	—	V
	Low-level output voltage (I_{OUT} = 100 µA)	V_{OL}	—	0.2	V

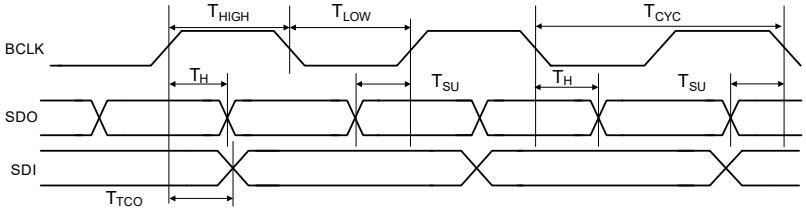
1. See Table 1-1 for HD Audio I/F and control power rails.

Table 3-9. HD Audio Interface Characteristics

Test conditions (unless specified otherwise): GNDD = GNDL = GND_PLL = 0 V; all voltages with respect to ground; VL_HD = 1.5 V, VL_DM = VL_SP = 1.8 V; Inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL_HD; T_A = +25°C; C_{LOAD} = 10 pF; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameters [1]	Symbol	Minimum	Typical	Maximum	Units
BCLK period	T_{CYC}	41.163	41.67	42.171	ns
BCLK high time	T_{HIGH}	17.50	—	24.16	ns
BCLK low time	T_{LOW}	17.50	—	24.16	ns
BCLK jitter		—	150	500	ps
SDI valid after BCLK rising edge	T_{TCO}	3	—	11	ns
SDO setup time [2]	T_{SU}	5	—	—	ns
SDO hold time	T_H	5	—	—	ns

1. HD audio interface timing.



2. SYNC and RST# have the same timing definitions as SDO, see HDA Specification Rev. 1.0a.

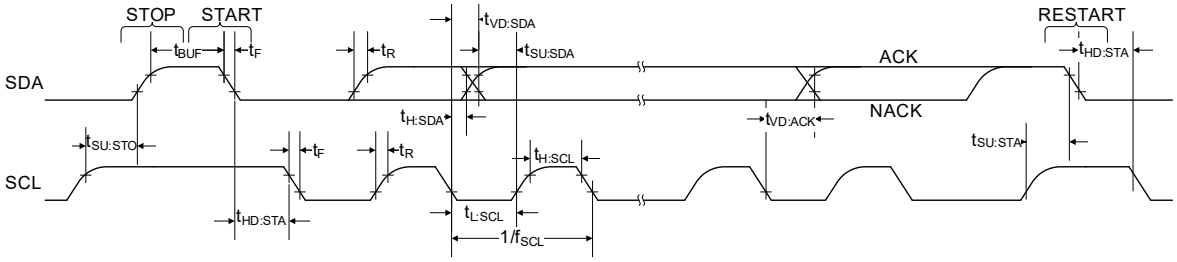
Table 3-10. I²C Master Port Characteristics

Test conditions (unless specified otherwise): GNDD = GNDL = GND_PLL = 0 V; all voltages with respect to ground; VL_HD = 1.5 V, VL_DM = VL_SP = 1.8 V; Inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL_SP; T_A = +25°C; bus capacitance equal to the maximum value of C_B specified below. [1]

Parameters[2]	Symbol	Standard Mode [3]		Fast Mode [3]		Fast Mode Plus [3]		Units
		Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
Low-level input voltage	V_{IL}	—	0.3 • VL_SP	—	0.3 • VL_SP	—	0.3 • VL_SP	V
High-level input voltage	V_{IH}	0.7 • VL_SP	—	0.7 • VL_SP	—	0.7 • VL_SP	—	V
Low-level output voltage (I_O = 3 mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V
SCL frequency	f_{SCL}	—	100	—	400	—	1000	kHz
SCL low time	$t_{L:SCL}$	4.7	—	1.3	—	0.5	—	µs
SCL high time	$t_{H:SCL}$	4	—	0.6	—	0.26	—	µs
SCL and SDA rise time	t_R	—	1000	—	300	—	120	ns
SCL and SDA fall time	t_F	—	300	—	300	—	120	ns
SCL rising to SDA falling for START condition	$t_{SU:STA}$	4.7	—	0.6	—	0.26	—	µs
SCL rising to SDA rising for STOP condition	$t_{SU:STO}$	4.0	—	0.6	—	0.26	—	µs
START condition to SCL falling	$t_{HD:STA}$	4.0	—	0.6	—	0.26	—	µs
Bus free time between STOP/START conditions [4]	t_{BUF}	20.83	—	20.83	—	20.83	—	µs
Setup time SDA input valid to SCL rising	$t_{SU:SDA}$	250	—	100	—	50	—	ns
SDA input hold time after SCL falling	$t_{HD:SDA}$	0	—	0	—	0	—	ns
SDA output valid time from SCL falling	$t_{VD:SDA}$	—	3.45	—	0.9	—	0.45	µs
Data valid acknowledge time	$t_{VD:ACK}$	—	3.45	—	0.9	—	0.45	µs
Bus capacitance	C_B	—	400	—	400	—	550	pF
I²C pull-up resistance	R_P	500	$(t_r)/(0.85 \cdot C_B)$	500	$(t_r)/(0.85 \cdot C_B)$	500	$(t_r)/(0.85 \cdot C_B)$	Ω

1. The minimum R_P value (shown in Fig. 2-1) is determined from the maximum VL_SP level, the minimum sink current strength of the output, and the maximum low-level output voltage (V_{OL}). The R_P maximum value is determined by how fast the signal must transition (e.g. the lower the R_P value, the faster the I²C bus can operate for a given bus load capacitance).

2. I²C master port timing



3. I²C speed mode determined by speed mode bit; see I2C_MODE bit in Table 6-193.

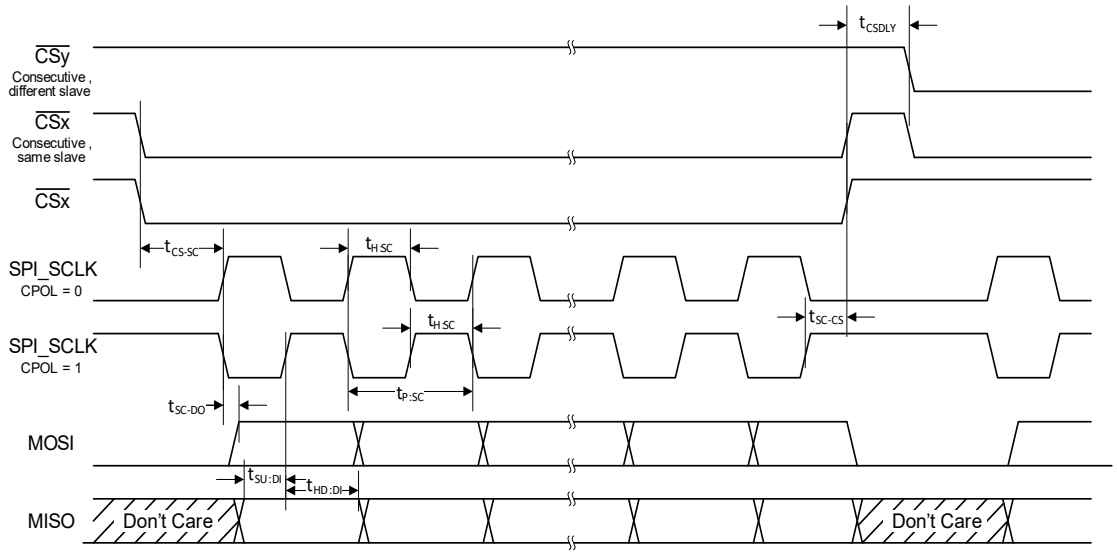
4. Minimum bus free time is limited to 1 HD Audio frame (if the STOP and START commands are sent in consecutive HDA frames).

Table 3-11. SPI Master Port Characteristics

Test conditions (unless specified otherwise): GNDD = GNDL = GND_PLL = 0 V; all voltages with respect to ground; VL_HD = 1.5 V, VL_DM = VL_SP = 1.8 V; Inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL_SP; T_A = +25°C; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameters [1]	Symbol	Minimum	Typical	Maximum	Units
SCLK frequency SPI_FRQ = 110	f_{SCLK}	—	12	—	MHz
$\overline{CS}$ falling edge to first SCLK edge	t_{CS-SC}	—	0.45 • (1/f_{SCLK})	—	ns
SCLK edge to output data valid	t_{SC-DO}	—	—	10	ns
Input data setup time	$t_{SU:DI}$	20	—	—	ns
Input data hold time	$t_{H:DI}$	5	—	—	ns
SCLK high period	$t_{H:SC}$	0.45 • (1/f_{SCLK})	—	0.55 • (1/f_{SCLK})	ns
Last SCLK edge to $\overline{CS}$ rising edge	t_{SC-CS}	0.45 • (1/f_{SCLK})	—	—	ns
$\overline{CS}$ high time between consecutive SPI transactions	t_{CSDLY}[2]	0.45 • (1/f_{SCLK})	—	—	ns

1. SPI master port timing



2. Minimum t_{CSDLY} timing is limited to three HD Audio frames: 1. Set CIR pointer; 2. write SPI count; 3. write TX data.

Table 3-12. Power Consumption

Test conditions (unless specified otherwise): All zeros input, sample rate = 48 kHz, typical load; VL_DM = 1.8 V; VL_HD = 1.5 V; VL_SP= 1.8 V. This table represents the power consumption of the device for sample use cases.

Use Case	Typical Current (mA)			Total Power of Use Case (mW)
	i_{VL_DM} VL_DM = 1.8 V	i_{VL_HD} VL_HD= 1.5 V	i_{VL_SP} VL_SP= 1.8 V	
Audio function group (AFG) in D3cold (link in reset) [1]	0.0004	0.037	0.035	0.118
AFG in D3cold (link out of reset) [2]	0.0004	0.752	0.035	1.193
AFG in D3hot (link in reset) [3]	0.0004	0.051	0.035	0.141
AFG in D3hot (link out of reset) [4]	0.001	0.875	0.035	1.378
AFG in D0 (other nodes in D3)	0.0004	3.314	0.035	5.034
Stereo DMIC [5]	0.194	4.367	0.052	6.992
Dual stereo DMIC [5]	0.377	5.183	0.069	8.578
Both ASP transmitter (MCLK from BCLK) [6]	0.001	5.146	11.178	27.841
Both ASP transmitter (MCLK from PLL) [7]	0.001	6.426	11.903	31.065
Both ASP receiver (MCLK from BCLK) [6]	0.001	6.299	10.310	28.008
Both ASP receiver (MCLK from PLL) [7]	0.001	6.996	10.885	30.088
Single ASP receiver and transmitter (MCLK from BCLK) [8]	0.001	6.061	4.550	17.283
Single ASP receiver and transmitter (MCLK from PLL) [9]	0.001	5.633	5.049	17.539
Both ASP receiver and transmitter (MCLK from BCLK) [6]	0.001	6.751	11.279	30.430
Both ASP receiver and transmitter (MCLK from PLL) [7]	0.001	7.544	11.968	32.860

1. RST# asserted, all HDA bus clocks and data lines driven low. Codec has no functionality.
2. RST# deasserted, all HDA bus clocks and data lines are running. HDA Interface running with support for detecting double function group reset only.
3. RST# asserted, all HDA bus clocks and data lines driven low. Codec is capable of jack sense, GPIO input sensing, and generating wake events.
4. RST# deasserted, all HDA bus clocks and data lines are running. HDA Interface running with support for jack sense, GPIO input sensing, and generating URs.
5. 24-bit, 48 kHz
6. ASPx_SCLK = 24 MHz (derived from BCLK), ASPx_MCLK = 12 MHz, ASPx_EN = 1, PLLx_EN = 0 (both PLL disabled), where x is 1 and 2.
7. ASPx_SCLK = 22.05 MHz (derived from PLLx), ASPx_MCLK = 12 MHz, ASPx_EN = 1, PLLx_EN = 1 (both PLL enabled), where x is 1 and 2.
8. ASPx_SCLK = 24 MHz (derived from BCLK), ASPx_MCLK = 12 MHz, ASPx_EN = 1, ASPy_EN = 0, PLLx_EN = PLLy_EN = 0 (both PLL disabled), where x is 1 or 2 and $x \neq y$.
9. ASPx_SCLK = 22.05 MHz (derived from PLLx), ASPx_MCLK = 12 MHz, ASPx_EN = 1, ASPy_EN = 0, PLLx_EN = 1, PLLy_EN = 0 (one PLL enabled), where x is 1 or 2 and $x \neq y$.

4 Functional Description

Fig. 4-1 provides a block diagram of the CS8409, showing the interconnections of the various subblocks.

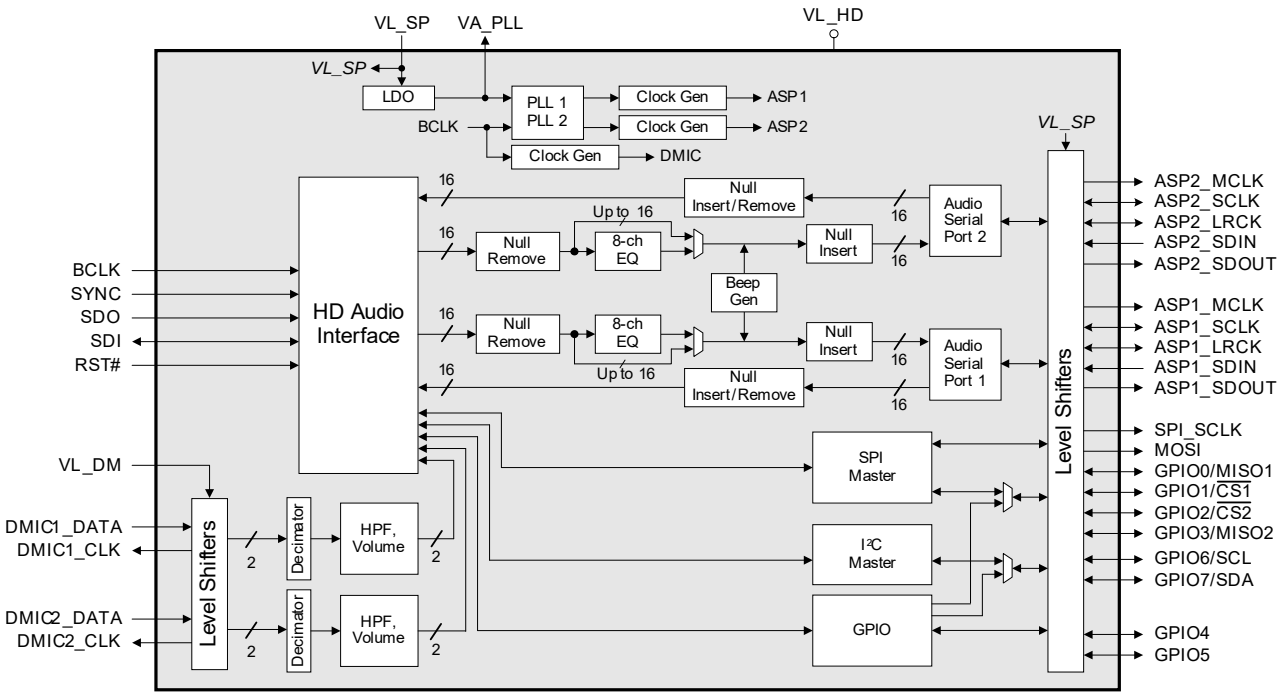


Figure 4-1. CS8409 Block Diagram

The operation of the various components is described in the following subsections:

- Section 4.1, "HD Audio"
- Section 4.2, "Audio Serial Ports (ASP1 and ASP2)"
- Section 4.3, "HD Audio Isochronous Tunneling"
- Section 4.4, "Encoded Audio Streams"
- Section 4.5, "SPI Master"
- Section 4.6, "I²C Master Port"
- Section 4.7, "Parametric Filter Engine"
- Section 4.8, "General-Purpose I/O (GPIO)"
- Section 4.9, "Internal Clock Gating"
- Section 4.10, "Register Settings across Resets"

4.1 HD Audio

4.1.1 Source Synchronous Input (SSI)

CS8409 supports HD Audio source synchronous input (SSI) for ASPs operating in Slave Mode. SSI supports only capture streams; therefore, an ASP configured to operate in Slave Mode must have streams assigned to its associated input converter widgets only. SSI support does not affect null-insert or null-remove capability of the ASP input widget data path.

4.1.2 Source Synchronous Input and Extra Data Transmission

In some cases, the CS8409 must transmit extra data on the SDI line. One such instance is when one of the ASPs is configured in Slave Mode, with SCLK and FSYNC driven slightly faster than the internal sample rate of the CS8409.

Per the *Intel HDA Specification*, when an HDA codec needs to use extra data transmission, it can do so either by inserting one or more additional complete sample blocks within the stream packet (making it larger) or by creating a second stream packet within the frame; the latter is how the CS8409 handles extra data transmission. It should be noted that the CS8409 only generates additional stream packets in accordance with the cadencing dictated by the *Intel HDA Specification*.

For the CS8409 to create a second stream packet, there must be enough bandwidth in that frame; otherwise, the CS8409 waits for the next allocated frame to create a second packet, following the cadencing pattern from the *Intel HDA Specification*. If bandwidth is insufficient in the subsequent frame, the CS8409 incurs a FIFO overflow and an error condition occurs.

4.1.3 Unsolicited Response (UR)

The HD Audio unsolicited response (UR) protocol allows a codec to send data to a controller outside of the normal command–response mechanism (the codec response to a controller command is called a solicited response, or SR). If multiple UR sources are queued in the CS8409, each UR is issued, when allowed by the HD Audio protocol, in the following order of priority (highest to lowest):

1. GPIO unique UR (see Section 4.8.1 and Section 6.3.10). Within unique URs, the lowest number GPIO has highest priority
   a) GPIO0
   b) GPIO1
   c) GPIO2
   d) GPIO3
   e) GPIO4
   f) GPIO5
   g) GPIO6
   h) GPIO7
2. Default GPIO UR (see Section 4.8.1 and Section 6.3.9)
3. I²C Master Port UR (see Section 4.6 and Section 6.11.4)
4. ASP Error UR (see Section 4.2.9 and Section 6.11.5)

4.2 Audio Serial Ports (ASP1 and ASP2)

The two audio serial ports, ASP1 and ASP2, can be configured to support several common audio interfaces—TDM, I²S, and left-justified (LJ). A reference to “ASPx” applies to ASP1 and ASP2, as appropriate.

4.2.1 HD Audio Widget–to–Serial Port Block Mapping

Each ASP supports up to 16 receive and 16 transmit channels. These are presented to the HD Audio bus as eight stereo output converter widgets (ASPx.A Out–ASPx.H Out) and eight stereo input converter widgets (ASPx.A In–ASPx.H In). A reference to “ASPx.n” applies to ASP1 or ASP2 widgets A–H, as appropriate.

Each HD ASP widget is treated as a stereo pair—the left channel of the pair is always assigned the lower ordinal hardware channel. The lowest ordinal channel pair (ASPx.A) is assigned to the lowest ordinal hardware channel. ASP channel pairs are assigned to hardware channels in ascending order. See Fig. 4-2 and Fig. 4-3.

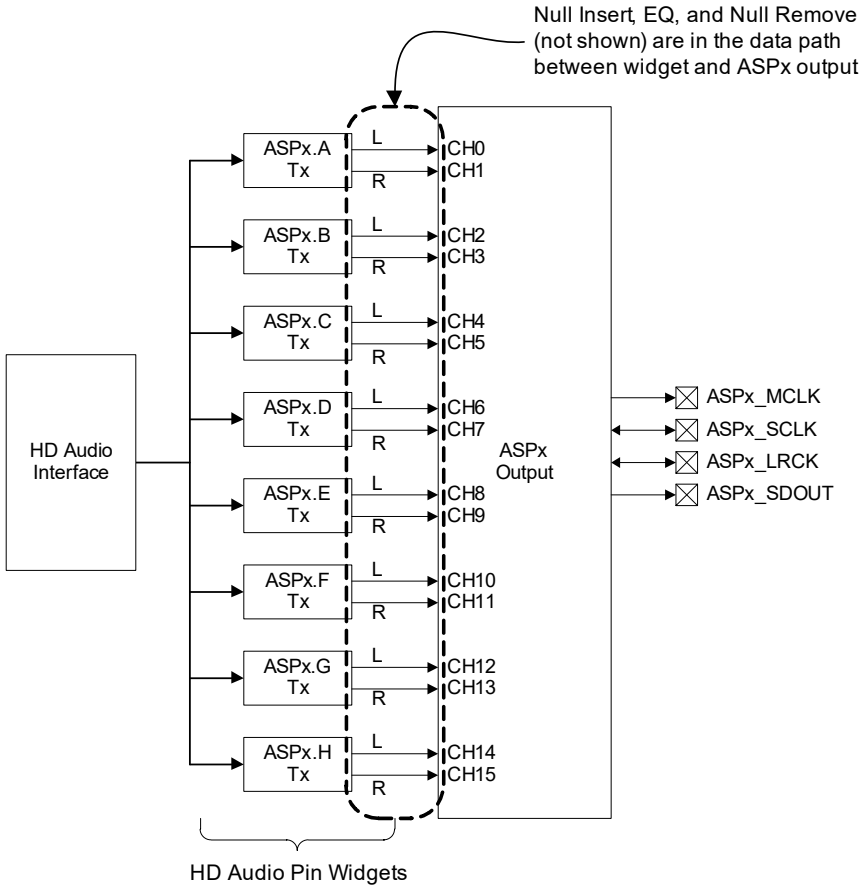


Figure 4-2. Mapping of HD Audio to ASP Transmit Channels

Because the HD Audio–to–ASP-hardware channel mapping is static, to avoid confusion, the hardware channels are referred to by their associated HD Audio widgets in the ASP configuration registers in the vendor processing widget (see Section 6.11.8.7, Section 6.11.8.8, and Section 6.11.8.9).

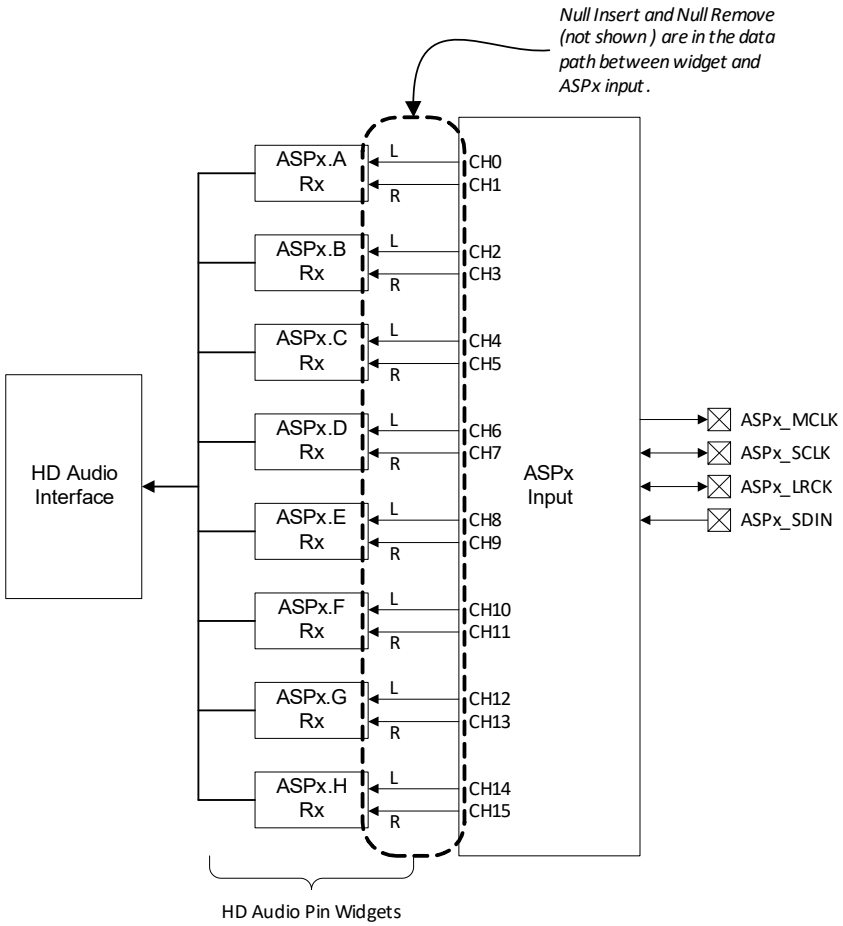


Figure 4-3. Mapping of ASP Receive Channels to HD Audio

4.2.2 Master and Slave Timing

Each ASP can operate as either the master of timing or as a slave to another device's timing, as described below:

- If ASPx_SLV (see Table 6-168) is cleared, the serial port acts as a master. In Master Mode, ASPx_SCLK and ASPx_LRCK are outputs derived from either BCLK, PLL1, or PLL2 (see Section 4.2.4).
- If ASPx_SLV is set, the serial port acts as a slave. Slave Mode operation implies that ASP widgets are operating as HD Audio SSIs (see Section 4.1.1). In Slave Mode, ASPx_SCLK and ASPx_LRCK are inputs. Although the CS8409 does not generate the interface timings in Slave Mode, the expected LRCK and SCLK format must be programmed in the same way as in Master Mode (see Section 4.2.4).

4.2.3 SDIN Timing

The ASPx_SDIN input can be latched, either based on the internally generated ASPx_SCLK signal edge or by passing the ASPx_SCLK signal through an input buffer. Passing the ASPx_SCLK signal through an input buffer retimes the clock and can improve timing robustness when the bus is heavily loaded. The input-timing source is controlled by ASPx_TIM (see Table 6-171). If ASPx_TIM = 0, ASPx_SDIN capture timing is based on the retimed ASPx_SCLK signal from the pad.

4.2.4 Clock Generation and Control

The CS8409 has a flexible serial port clock generation subsystem that allows independent clocking of the two ASPs. When operating as a master port, the ASP must provide a bit clock (ASPx_SCLK) and a left-right/frame sync signal (ASPx_LRCK/FSYNC); in addition, the ASP may provide a continuous master clock (ASPx_MCLK).

Fig. 4-4 shows the ASP SCLK and MCLK Architecture.

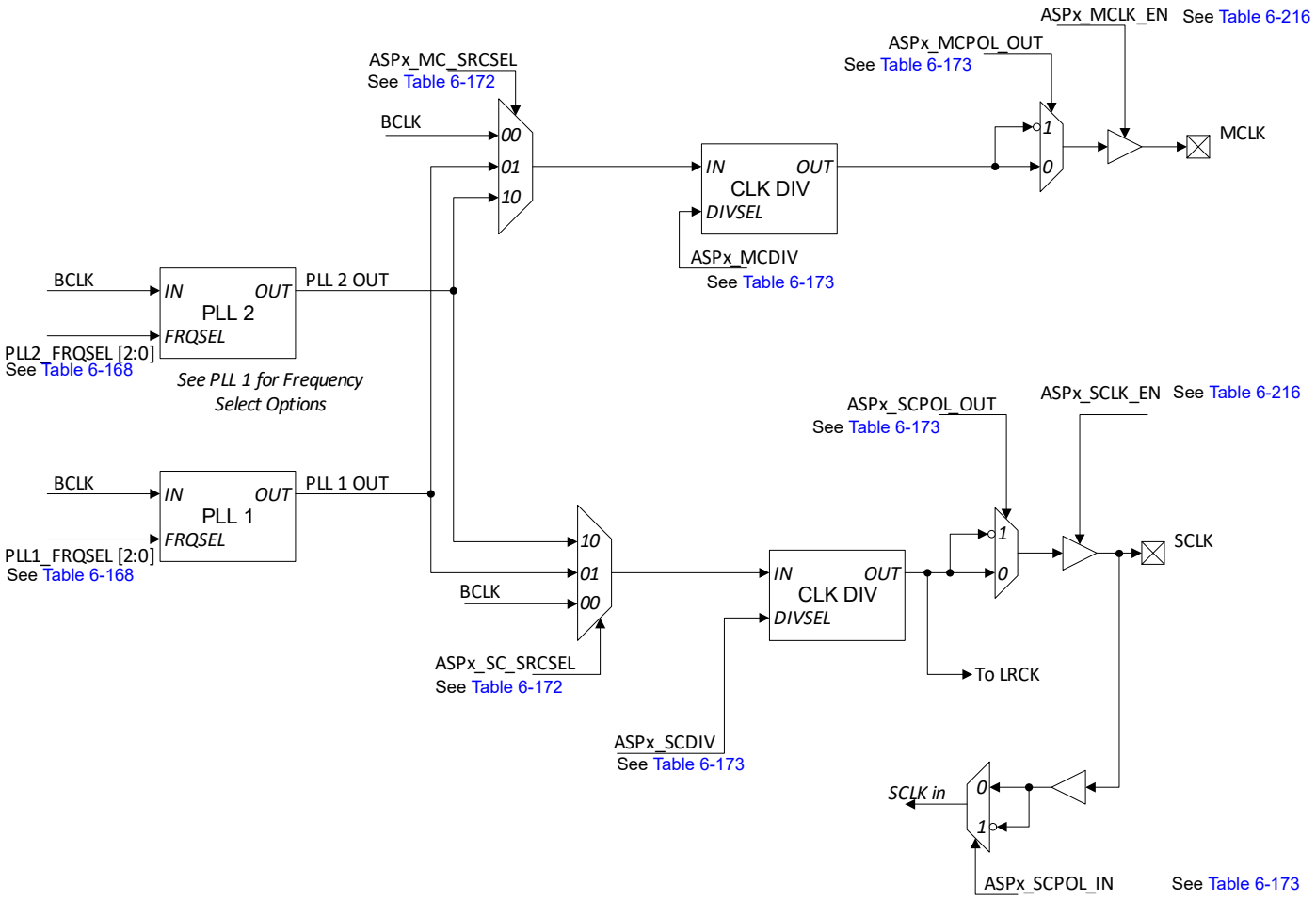


Figure 4-4. ASP SCLK and MCLK Architecture

Fig. 4-5 shows the ASP LRCK architecture.

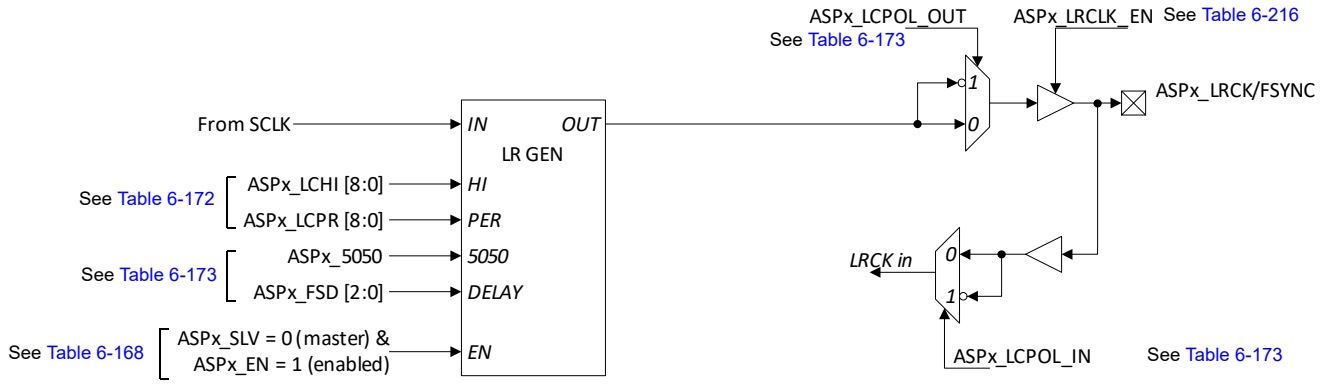


Figure 4-5. ASP LRCK Architecture

As shown in Fig. 4-6, the LRCK period (ASPx_LCPR) controls the number of SCLK periods in each frame. The LRCK period effectively sets the length of the frame and the number of SCLK periods per Fs. Frame length may be programmed in single SCLK period multiples from a minimum of 16 SCLK:Fs up to 512 SCLK:Fs.

The LRCK-high width (ASPx_LCHI) controls the number of SCLK periods for which the LRCK signal is held high during each frame. Like the LRCK period, the LRCK-high width is programmable in single SCLK periods, from a minimum of one period to a maximum of the LRCK period minus one. That is, LRCK-high width must be less than the LRCK period.

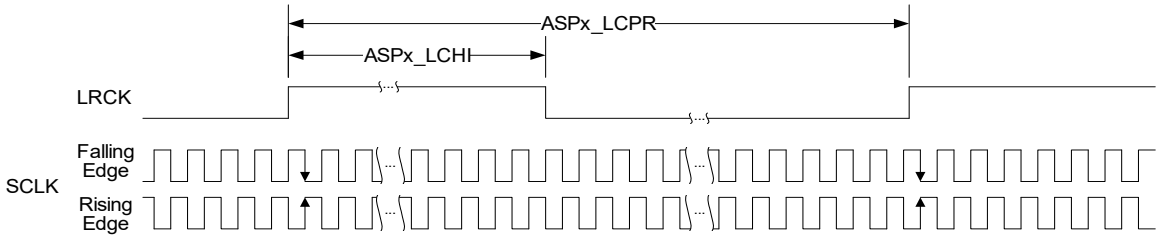


Figure 4-6. ASP LRCK Period, High Width

As shown in Fig. 4-7, if Serial Port 50/50 Mode is enabled (ASPx_5050 = 1), the LRCK high duration must be programmed to the LRCK period divided by two (rounded down to the nearest integer when the LRCK period is odd). Setting the LRCK high duration to a value other than half of the period results in erroneous operation when the serial port is in 50/50 Mode.

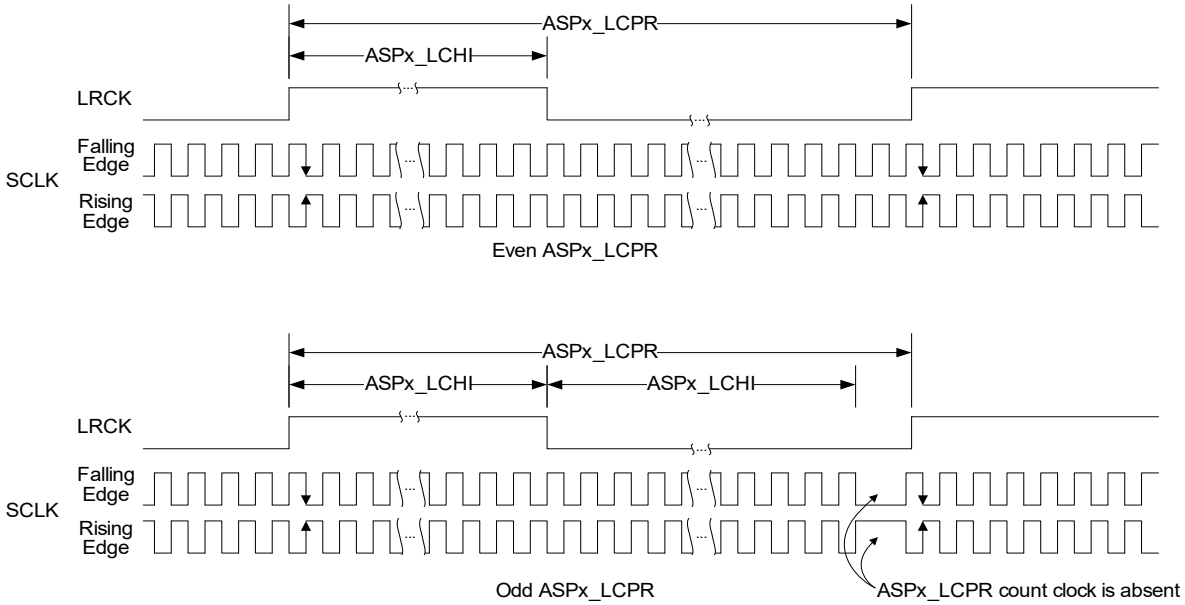


Figure 4-7. ASP LRCK Period, High Width, 50/50 Mode

Input and output SCLK polarity controls (ASPx_SCPOL_IN and ASPx_SCPOL_OUT) are also available. Fig. 4-8 shows how LRCK frame start delay (ASPx_FSD) controls the number of SCLK periods delay from the LRCK synchronization edge to the start of frame data, including the interaction of the SCLK polarity controls. As shown in Fig. 4-8, if Master Mode is used, both polarity controls affect the SCLK used by the serial port module. As an example, both polarity controls must be set (ASPx_SCPOL_IN = ASPx_SCPOL_OUT = 1) to invert the SCLK and output the data on the falling edge. In typical use cases, the value of ASPx_SCPOL_IN equals that of ASPx_SCPOL_OUT for each serial port.

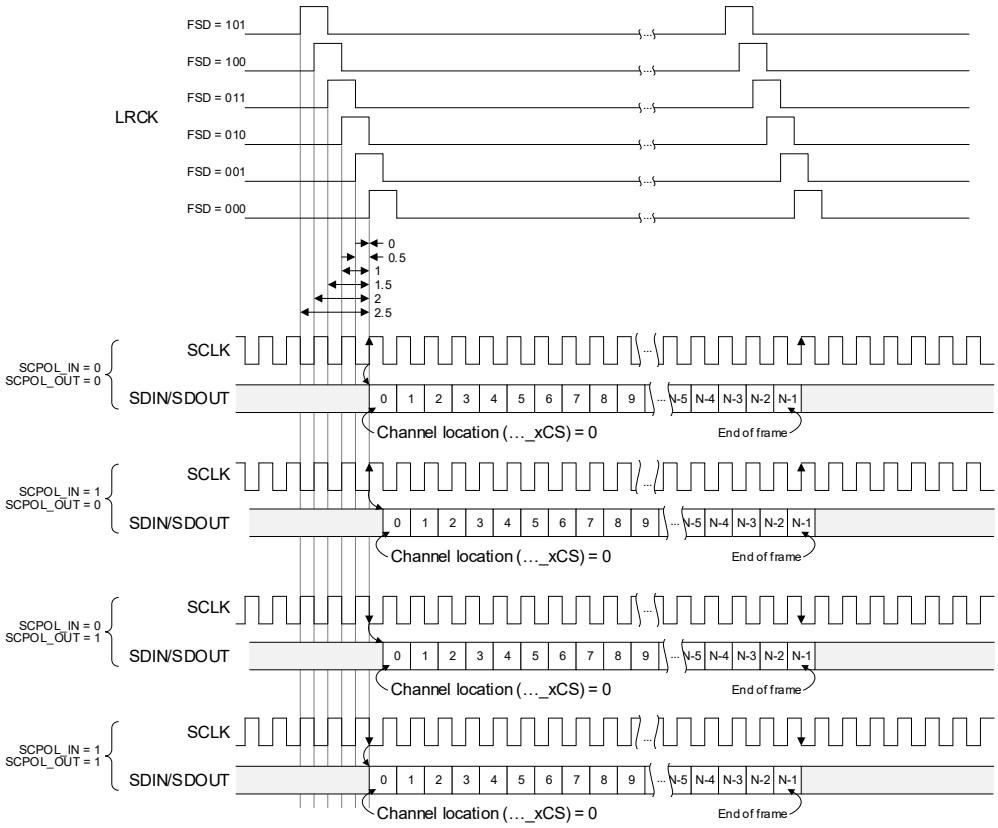


Figure 4-8. LRCK FSD Example Diagram

4.2.5 Channel Location and Size

Each serial port channel has a programmable location and offset (see the x_LCS and x_RCS bits in Section 6.11.8.9). Channel location is programmable in single SCLK period resolution. When set to the minimum location offset, the channel transmits or receives on the first SCLK period of a new frame.

Channel size is programmable in byte resolution from 8- to 32-bits. The ASP channel size is not required to match the HD Audio stream sample size; however, there are some restrictions for stream–ASP size mismatch:

- For normal streams (without HD Audio tunneling or isochronous mode), the HD Audio stream size must be at least as large as the ASP channel size.
- For isochronous render streams using the negative full-scale (NFS) encoded null samples (with or without HD Audio tunneling), the ASP channel size must equal the HD Audio stream size. See Section 4.2.6.
- For isochronous streams using null sample bit (NSB) encoded null samples without HD Audio tunneling, the ASP channel size must be equal to the HD Audio stream size plus 8 bits. See Section 4.2.6.
- For isochronous streams using NSB encoded null samples with HD Audio tunneling, the ASP channel size must be equal to the HD Audio stream size.

Channel size and location must not be programmed such that channel data extends beyond the frame boundary. Size and location must not be programmed such that data from a given SCLK period is assigned to more than one channel. The example in Fig. 4-9 shows channel location and size with ASP double rate disabled.

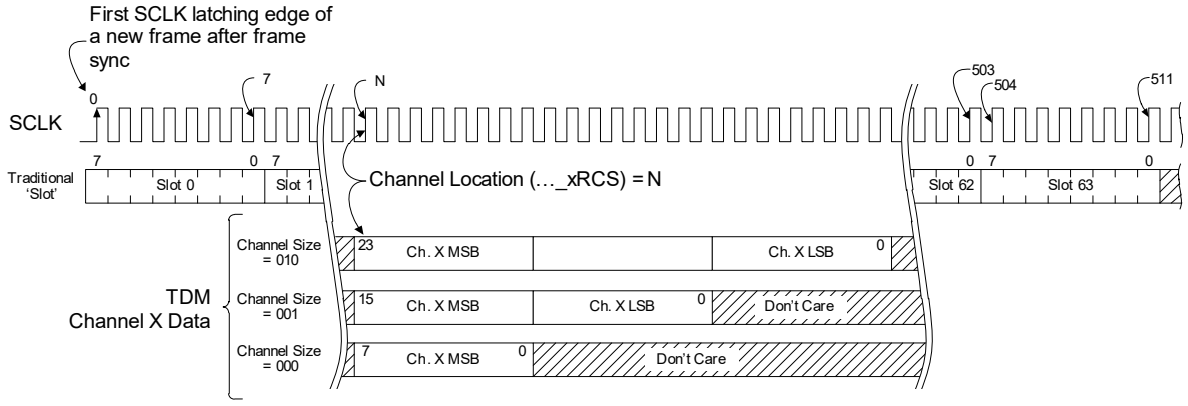


Figure 4-9. Example Channel Location and Size, ASP Double Rate Disabled

4.2.6 Isochronous Serial Port Operation

If configured for isochronous mode, audio data can be transported between the internal audio data paths and a serial port at isochronous frequencies slower than or equal to the LRCK frequency. In all cases, the sample rate/LRCK frequency ratio must be one for which there are events in time at which rising edges regularly align. The only supported LRCK rate is 48 kHz.

In isochronous mode, the stream must include nulls if its sample rate does not match the LRCK frequency. Nulls may be indicated by either the negative full-scale (NFS) code (1 followed by all 0s) or by adding nonaudio bits to the data stream. As Fig. 4-10 shows, the null sample bit (NSB) flag may be selected from any bit of the least-significant sample byte. All NSB encoded streams are assumed to contain 8 bits of nonaudio data as the LSB.

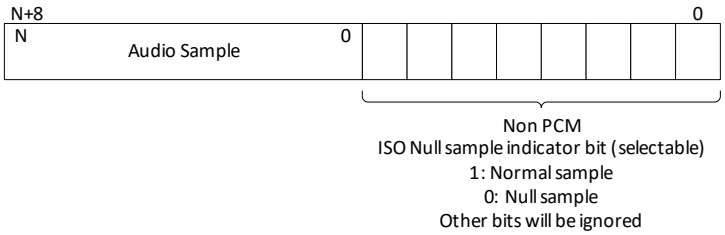


Figure 4-10. NSB Null Encoding

To send isochronous audio data to a serial port, the data pattern must be such that the LRCK/FSYNC transition preceding any given nonnull sample on the 48-kHz serial port does not deviate by more than 1 sample period from a virtual clock running at the desired sample rate. Use the following example to determine the data word as it appears on the serial port.

```
error = 0
for each LRCK
   if(error < 1/FLRCK)
     output = <<next sample>>
     error = error + (1/Fs - 1/FLRCK)
   else
     output = NULL
     error = error - 1/FLRCK
```

Table 4-1 shows null sample sequences that result from the example above for some common sample rates. Using this method ensures that the internal receive data FIFO does not underrun or overrun, which would cause loss of audio data.

Table 4-1. Isochronous Input Data Patterns

Sample Rate (kHz)	Isochronous Data Pattern for LRCK = 48 kHz
8.000	1_S5_N (repeat)
11.025	[[[1s3nx2]1s4n]x5 1s3n1s4n]x4 [[1s3nx2]1s4n]x4 1s3n1s4n [[[1s3nx2]1s4n]x5 1s3n1s4n]x3 [[1s3nx2]1s4n]x4 1s3n1s4n (repeat)
12.000	1_S3_N (repeat)
16.000	1_S2_N (repeat)
22.05	[[1s1nx6]1n [1s1nx6]1n [1s1nx5]1n]x8 [1s1nx6]1n [1s1nx5]1n (repeat)
24.000	1_S1_N (repeat)
32.000	2_S1_N (repeat)
44.100	[12s1n[11s1n]x2]x4 11s1n (repeat)
48.000	1_S (repeat)

Note: $_N$ = NULL sample, $_S$ = normal sample

Depending on the internal audio data FIFOs' startup conditions and on the serial-port clock phase relationships, isochronous data sent from a serial port may not adhere to the data patterns shown in Table 4-1. In all cases, the transmitted audio data rate matches the stream sample rate.

4.2.7 50/50 Mode

If configured for 50/50 Mode, the serial port can start a frame, regardless of whether ASPx_LRCK/FSYNC is high or low. The ASPx_STP bit controls which LRCK/FSYNC phase starts a frame in 50/50 Mode.

- If ASPx_STP = 0, the frame begins when LRCK/FSYNC transitions from high to low. See Fig. 4-11.

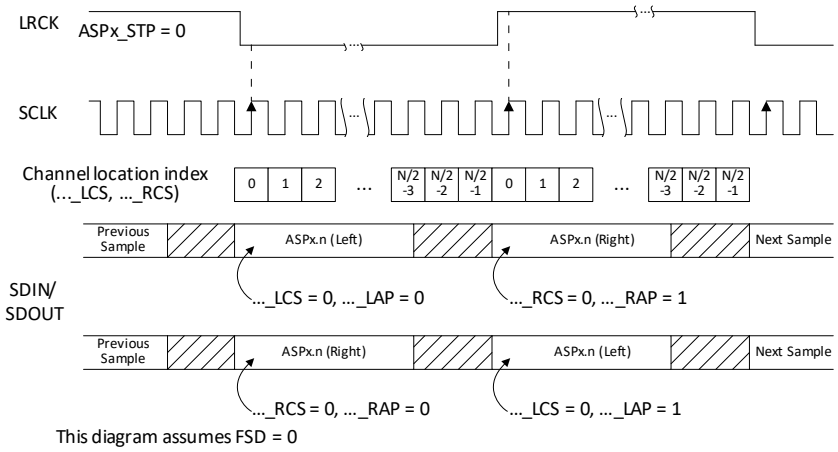


Figure 4-11. Example 50/50 Mode (ASPx_STP = 0)

- If ASPx_STP = 1, the frame begins when LRCK/FSYN transitions from low to high. See Fig. 4-12.

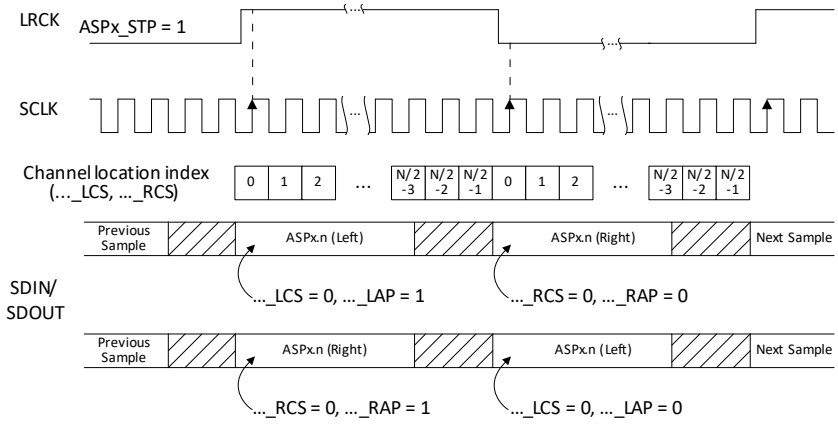


Figure 4-12. Example 50/50 Mode (ASPx_STP = 1)

Each set of ASPx.n widgets are stereo pairs. In 50/50 Mode, the left and right channel of each widget can be independently programmed to output when LRCK/FSYNC is high or low, this is called the “channel-active phase.” The ASPx.n left channel-active phase is controlled by the ASPx.n_LAP bit. The ASPx.n right channel active phase is controlled by ASPx.n_RAP. The left and right channel-active phase controls behave similarly. If the active phase control bit (ASPx.n_LAP, ASPx.n_RAP) has a value of one, the respective channel is output if LRCK/FSYNC is high. If the active phase control bit has a value of zero, the respective channel is output if LRCK/FSYNC is low.

The ASPx.n_RAP and ASPx.n_LAP bits are considered only in 50/50 Mode. Otherwise, they are “don’t cares.”

In 50/50 Mode, the channel location (see Section 4.2.5) is calculated within the channel-active phase. If there are N bits in a frame, the location of the last bit of each active phase is equal to (N/2) – 1.

4.2.8 Null-Insert and Null-Remove Blocks

The ASP data path includes both null-insert and null-remove blocks. The null operation blocks function in either NFS or NSB Mode, as defined in the ASPx_NMS bit in Section 6.11.8.1. Fig. 4-13 shows examples of null-insert block operations.

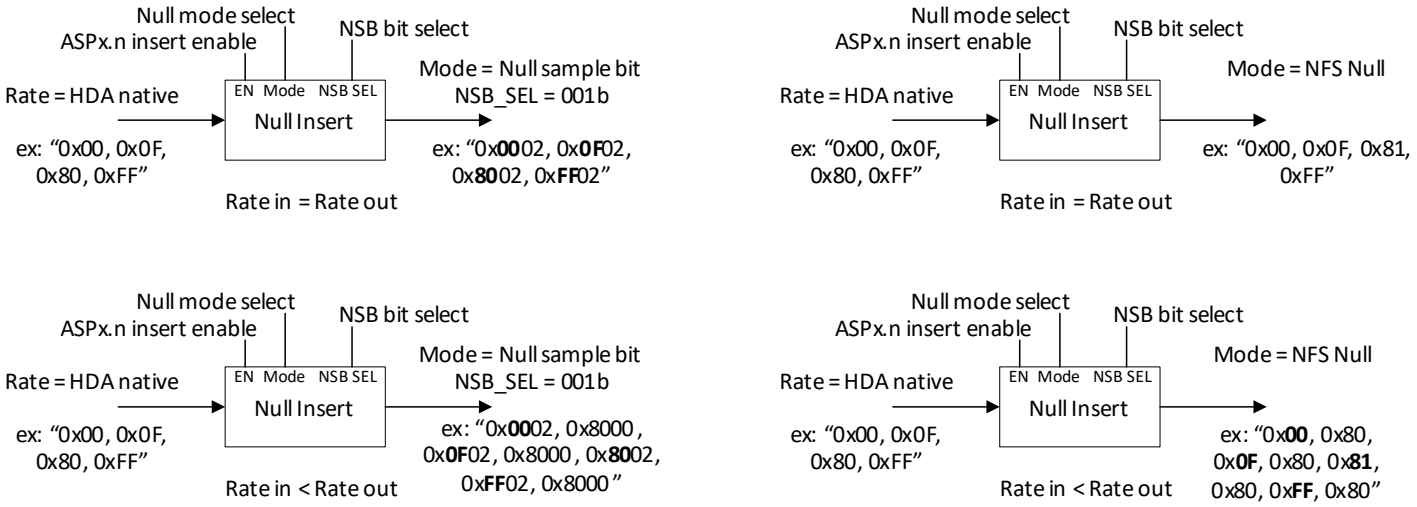


Figure 4-13. Null-Insert Block Operation

- In NFS Mode, a null-insert block adds NFS samples to the output stream in order to achieve a 48-kHz output sample rate. NFS samples that are input to the null-insert block are incremented and are passed to the output as valid, nonnull samples.
- In NSB Mode, a null-insert block adds 8 bits to the data stream and inserts null samples to achieve a 48-kHz sample rate. Inserted null samples are defined as NFS including the nonaudio bits. NFS samples that are input to the null-insert block are passed as valid, nonnull samples to the output. Valid samples are indicated by a nonzero value in the null sample indicator bit. The null sample indicator bit is globally defined by the NSB_SEL bits in Table 6-167. Total data stream sample width, including the nonaudio bits, is 32 bits. Therefore, the maximum HD audio sample width is 24 bits in NSB Mode.

In NFS Mode, a null-remove block deletes null samples, restoring the stream’s original sample rate. NFS samples that are input to the null-remove block are removed from the data stream as invalid, null samples.

In NSB Mode, a null-remove block deletes samples that have a zero null sample indicator bit, restoring the stream’s original sample rate. Furthermore, the output data has the least-significant 8 bits of nonaudio data removed. Samples with a zero null sample indicator bit are removed from the data stream as invalid, null samples. Fig. 4-14 shows examples of null-remove block operations.

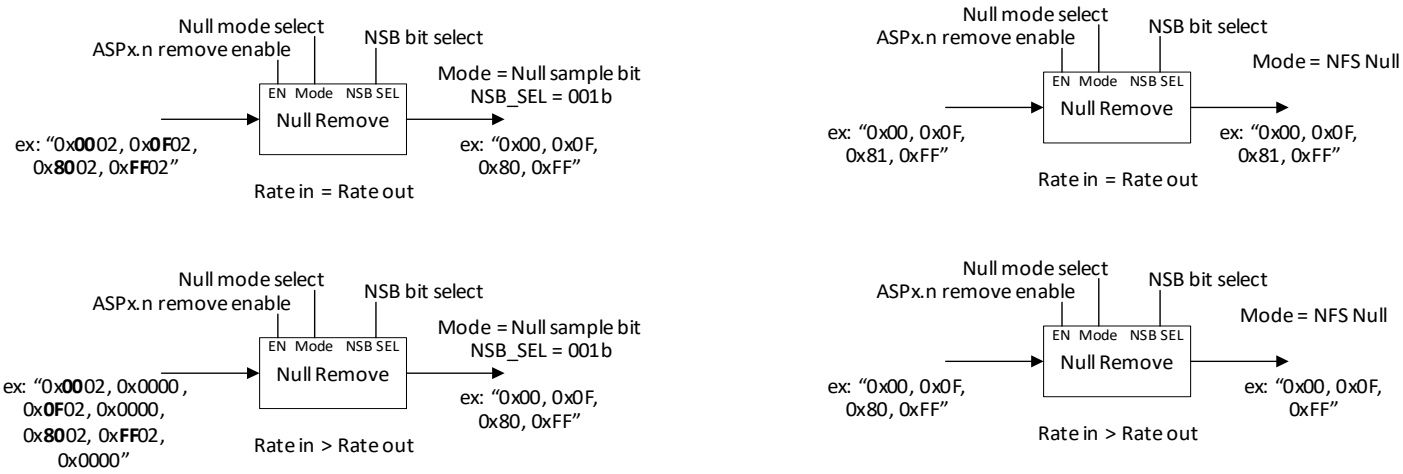


Figure 4-14. Null Remove Block Operation

In either NFS or NSB Mode, setting the Tx rate and Rx rate registers (see Section 6.11.8.7) matters only if null insertion is enabled. The ASPx Tx/Rx Rate bits are used only to help the device determine when to insert nulls.

For null-remove operations, the rates do not need to match the actual data rate. Likewise, if data is being rendered or captured at its native rate, these registers have no effect.

4.2.9 ASP Status and Associated HD Audio Unsolicited Responses (URs)

Each ASP has nine associated status report bits that are accessible in the HD Audio vendor processing widget (see Table 6-210). Five status bits are related to the capture path, and four are related to the render path. Each bit is sticky and must be written to one in order to be cleared. The ASP status bits have an associated unsolicited response (UR) in the vendor processing widget (see Section 6.11.5). If the audio serial interface unsolicited response is enabled, each status bit can be configured independently to trigger the UR using the ASP UR mask (see Table 6-214). A brief description of each status bit follows:

- ASPx Rx Request Overload is set when too many input buffers request processing at the same time. If all channel size and location registers are properly configured to nonoverlapping values, this error status should never be set.
- ASPx Rx LRCK Error is the logical OR of ASPx Rx LRCK Early and ASPx Rx LRCK Late (see below).
- ASPx Tx/Rx LRCK Early is set when the number of SCLK periods per LRCK phase (high or low) is less than the expected count as determined by ASPx_LCPR and ASPx_LCHI.
- ASPx Tx/Rx LRCK Late is set when the number of SCLK periods per LRCK phase (high or low) is greater than the expected count as determined by ASPx_LCPR and ASPx_LCHI.
- ASPx Rx No LRCK is set when the number of SCLK periods counted exceeds twice the value of LRCK period (ASPx_LCPR) without an LRCK edge.
- ASPx Tx SM Error is set when the transmit state machine cannot retrieve data from output buffers; it is analogous to ASPx Rx Request Overload. If all channel size and location registers are properly configured to nonoverlapping values, this error status should never be set.

In CIR = 0x006D/F and CIR = 0x006E/70, the RX and TX SCLK count can be read back to verify the correct number of SCLK cycles. Note, however, that this value is reported differently depending on the value of the ASPx_5050 bit, located in CIR = 0x0005/8 in the Vendor Processing Widget. If ASPx_5050 is set, SCLK is counted for only half of the LRCK period. If ASPx_5050 is cleared, SCLK is counted for the full LRCK period. Note that in I²S and Left-Justified Modes, ASPx_5050 should usually be set.

When only one data path direction (render/Tx or capture/Rx) of either ASP is used, the status bits of the unused direction may be set. Status bits of unused data path directions should have their UR mask bits cleared to prevent spurious URs. Similarly, status bits of an unused ASP should have their UR mask bits cleared to prevent spurious URs.

These error bits are not set if clocks are not present on the ASP. Likewise, clock counts are not accurate without the clocks present on the ASP.

4.2.10 Internal Loopback

Internal loopback allows an ASP to receive the data stream generated by its output. Internal loopback controls are in the vendor processing widget, see Table 6-215. Fig. 4-15 shows a functional diagram of the internal loopback path.

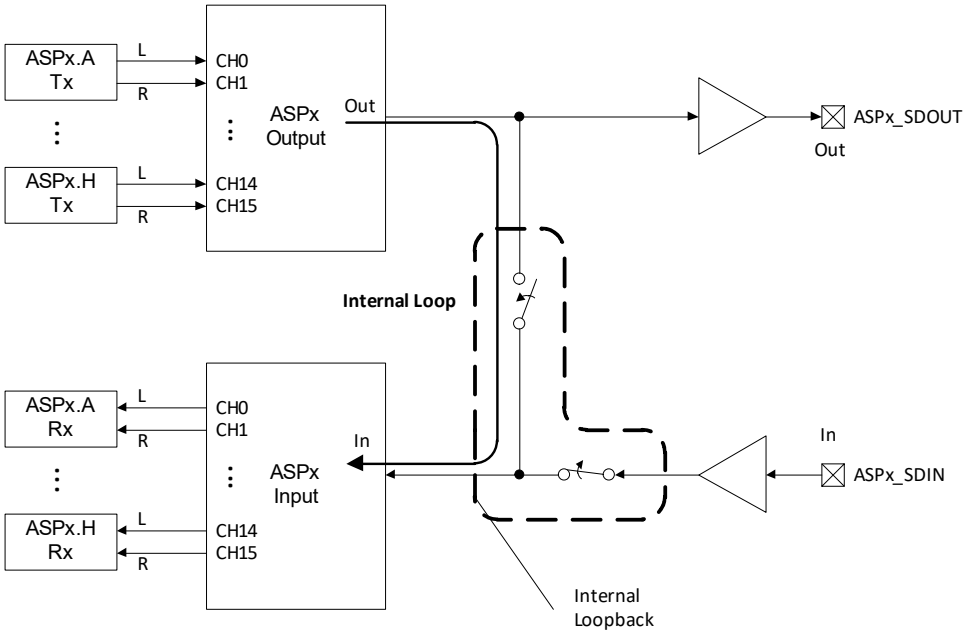


Figure 4-15. ASP Loopback Functional Diagram

4.2.11 Double Sample Mode

Double Sample Mode is used in the ASPs to allow transmission of data at twice the configured sampling rate of the ASP. To activate Double Sample Mode, the ASPx_DR bit must be set in CIR = 0x0004/7 in the Vendor Processing Widget (see Table 6-172).

In Double Sample Mode, channel slots are counted on both the rising and falling edges of LRCK, rather than just the falling edge. For example, 32 slots of data are counted in 16 LRCK periods. Double Sample Mode can be used in any data format (i.e., I²S, Left-Justified, and TDM). To use Double Sample Mode, the CS8409 must operate in 50/50 Mode, which is done by setting the ASPx_5050 bit in CIR = 0x0005/8 in the Vendor Processing Widget (see Table 6-173).

4.3 HD Audio Isochronous Tunneling

Data may be transmitted over the HD Audio bus in an isochronous manner, similar to the TDM and I²S Isochronous Mode described in Section 4.2.6. This is called “HD Audio isochronous tunneling” or “HD Audio tunneling” and may employ either NFS or NSB encoded nulls if the null method matches the ASPx_NMS bit of the rendering or capturing serial port. HD Audio tunneling is required only to support stream sample rates not natively supported by the HD Audio specification. Fig. 4-16 shows native serial-port audio tunneling operations.

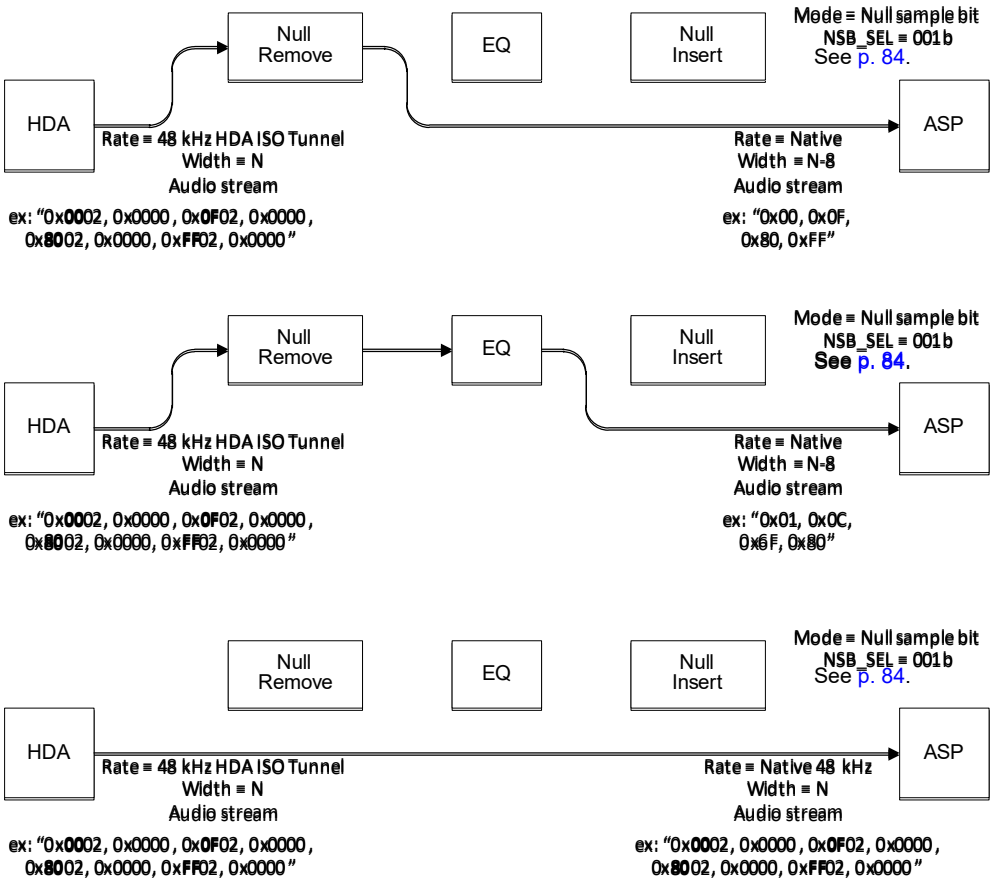


Figure 4-16. HD Audio Tunneling to Native Serial Port Operation

Fig. 4-17 shows isochronous serial-port audio tunneling operations.

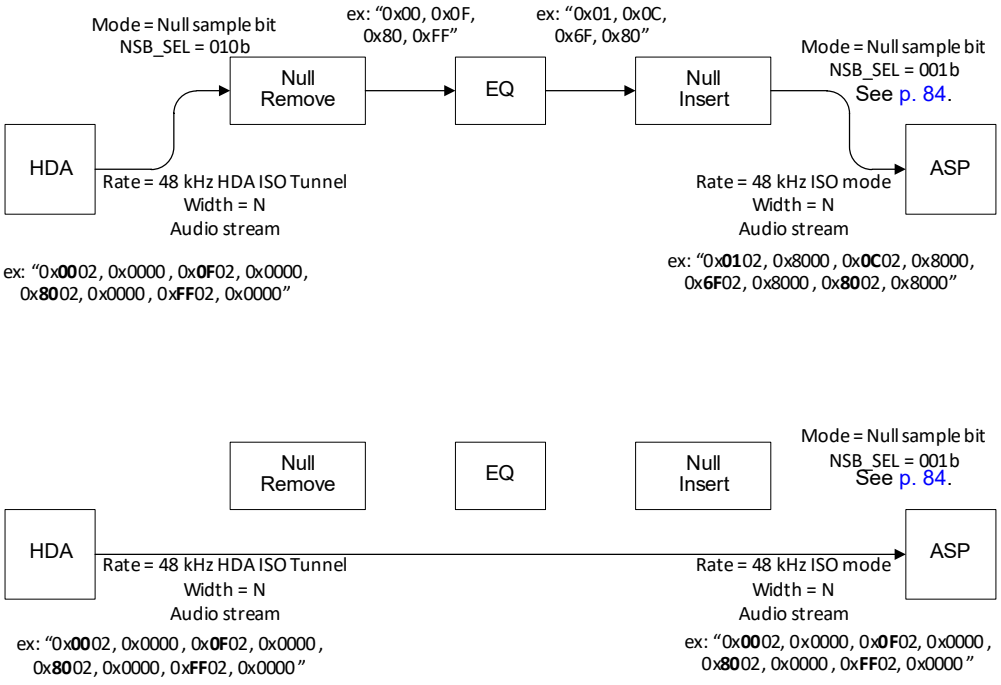


Figure 4-17. HD Audio Tunneling to Isochronous Serial Port Operation

4.4 Encoded Audio Streams

The HD Audio tunneling method described in Section 4.3 may be used to pass encoded audio streams that contain NFS data without inserting any null samples using NSB null encoding. Similarly, the audio render signal chain can be configured to automatically pad encoded data by configuring the null-insert block for NSB Mode. Fig. 4-18 shows encoded data serial-port audio tunneling.

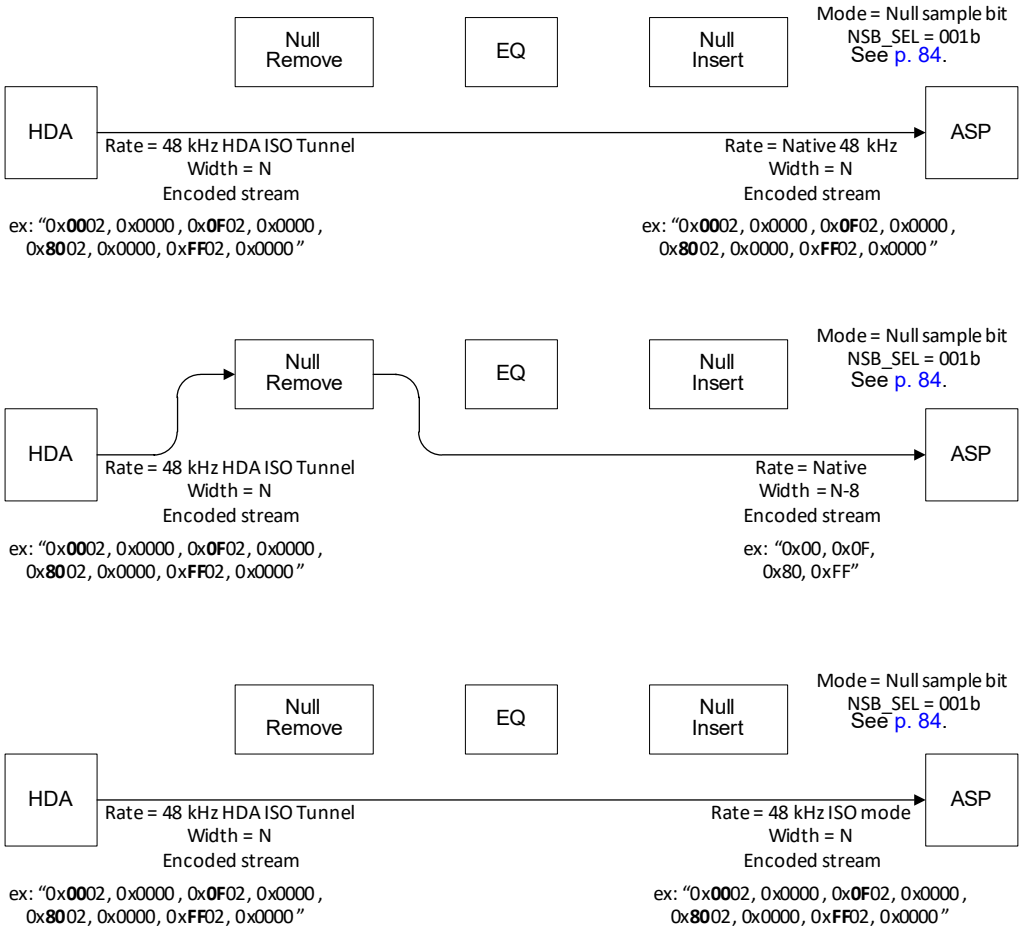


Figure 4-18. HD Audio Tunneling of Encoded Data to Serial Port Operation

Fig. 4-19 shows encoded data isochronous serial-port audio tunneling.

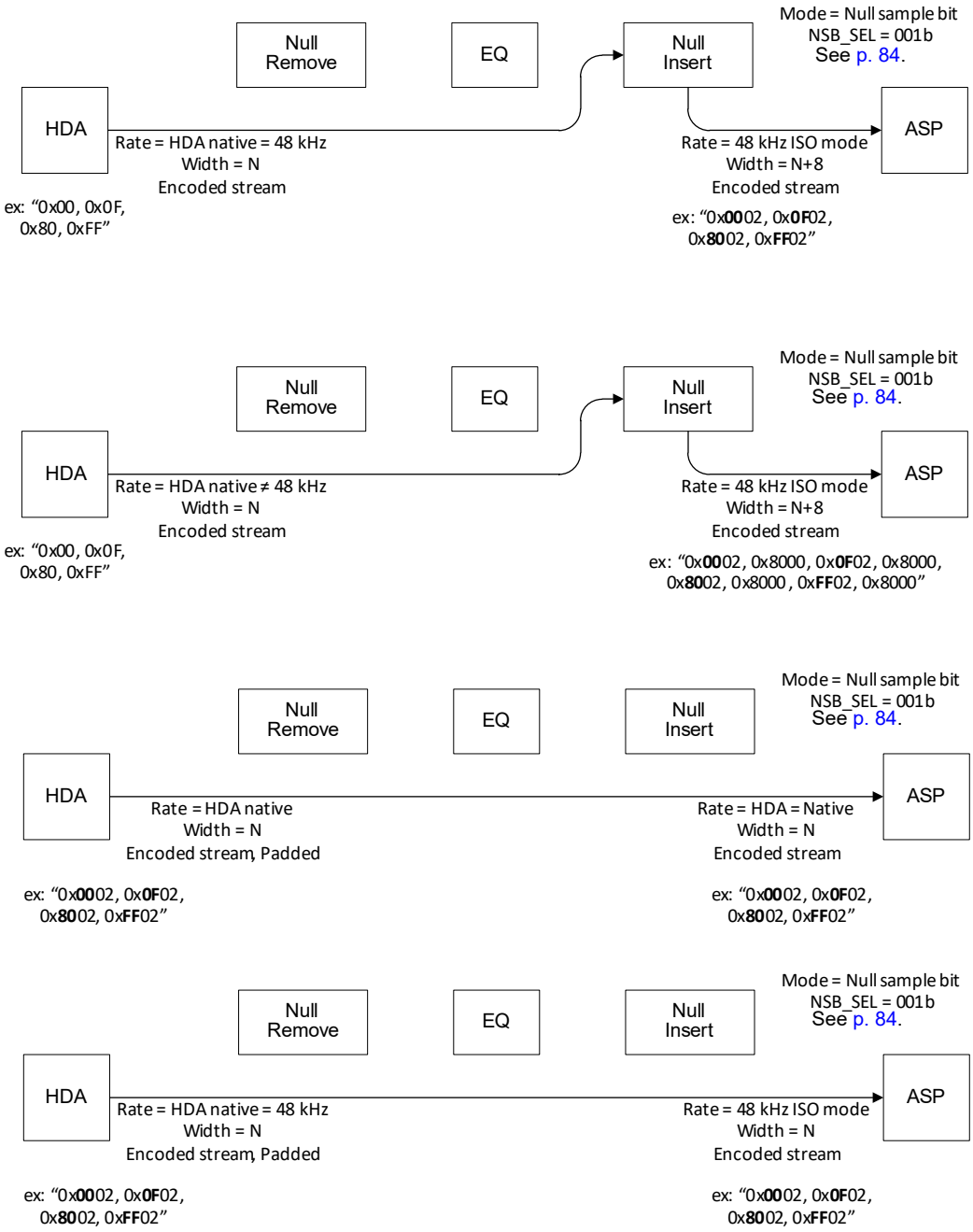


Figure 4-19. HD Audio Tunneling of Encoded Data to Isochronous Serial Port Operation

4.5 SPI Master

CS8409 includes a SPI master block to control attached peripherals. The SPI master supports programmable clock polarity. If the SPI clock polarity control bit is set, the SPI clock remains high while chip select is high (commonly referred to as CPOL = 1). If the SPI clock polarity control bit is zero, the SPI clock remains low while chip select is high (commonly referred to as CPOL = 0).

The SPI master supports fixed clock phase. The SPI interface shifts data only on clock edges. The first data bit is not driven on the falling edge of $\overline{CS}$ (commonly referred to clock phase one, CPHA = 1).

The SPI master supports programmable SPI clock rates (12, 6, 4, 3, 2, and 1.5 MHz).

Fig. 4-20 shows the SPI transaction format.

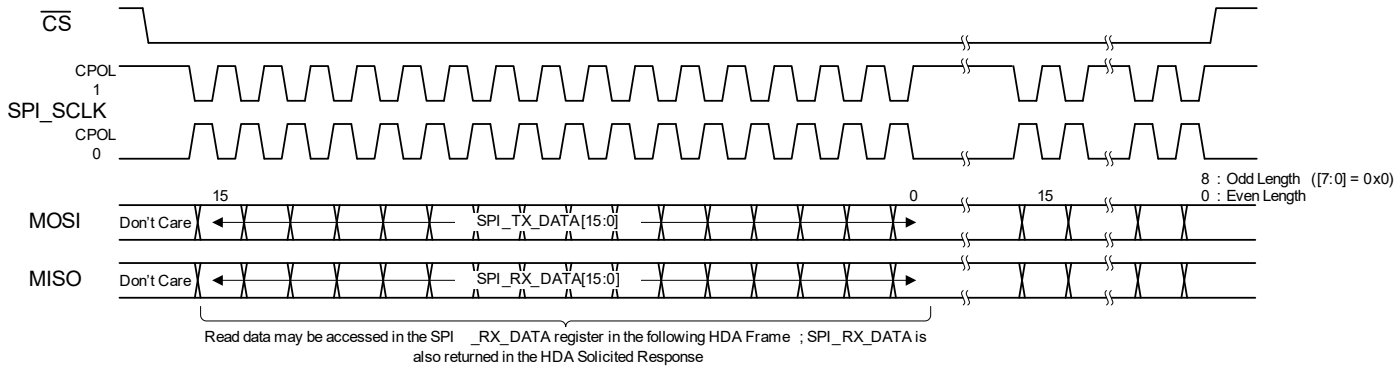


Figure 4-20. SPI Transaction Format

A SPI transaction consists of driving a slave's $\overline{CS}$ low, driving a series of clock edges while transmitting data on the output (MOSI) pin and receiving data on the input (MISO) pin. The SPI master supports transaction lengths of 8-bit multiples up to 2040 bits. Transaction length is determined by the SPI_LEN byte in Table 6-198. SPI_LEN is the total number of bytes to be shifted in a transaction. SPI_LEN should never be written during transaction except to terminate the transaction. Writing zero to the SPI_LEN followed by writing SPI Tx Data register terminates a transaction.

Writing to the SPI Tx data register (see Table 6-199) begins a SPI transaction. The selected $\overline{CSx}$ is driven low, output data is transmitted on MOSI, and input data is received on MISO. The solicited response to SPI Tx Data register writes contains the data that is read from the SPI interface.

Fig. 4-21 and Fig. 4-22 show HDA–SPI interactions for even and odd byte counts.

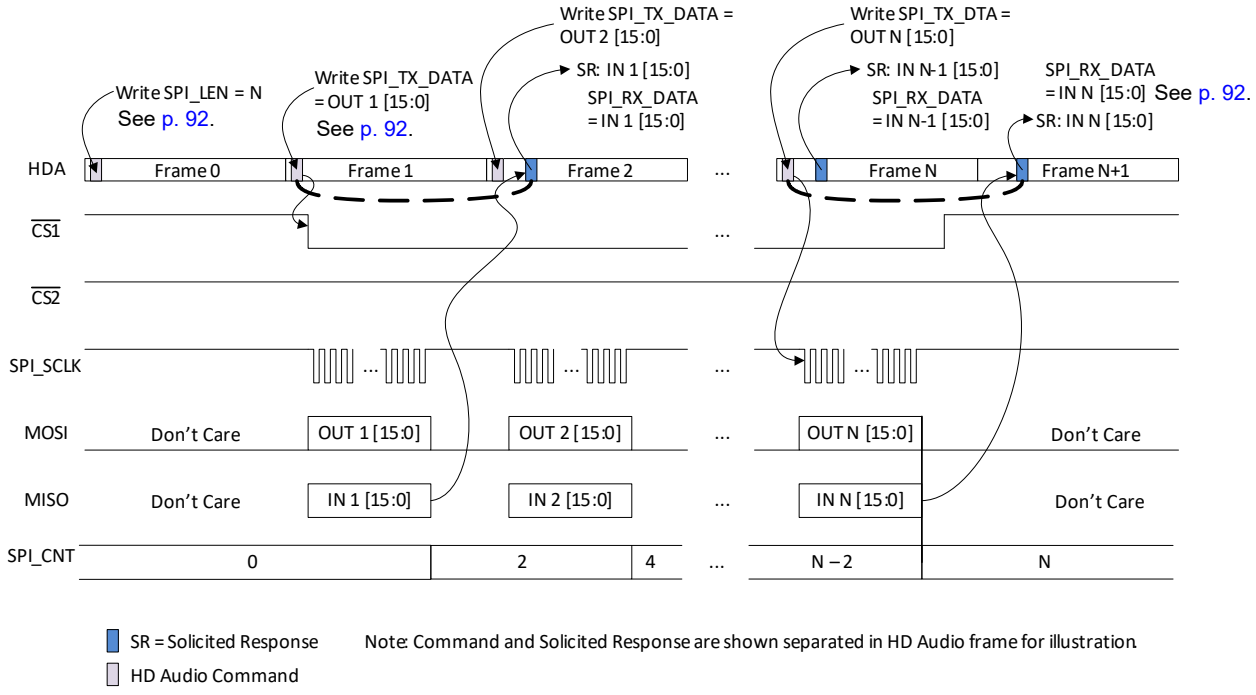


Figure 4-21. HDA–SPI Interaction, Even Byte Count

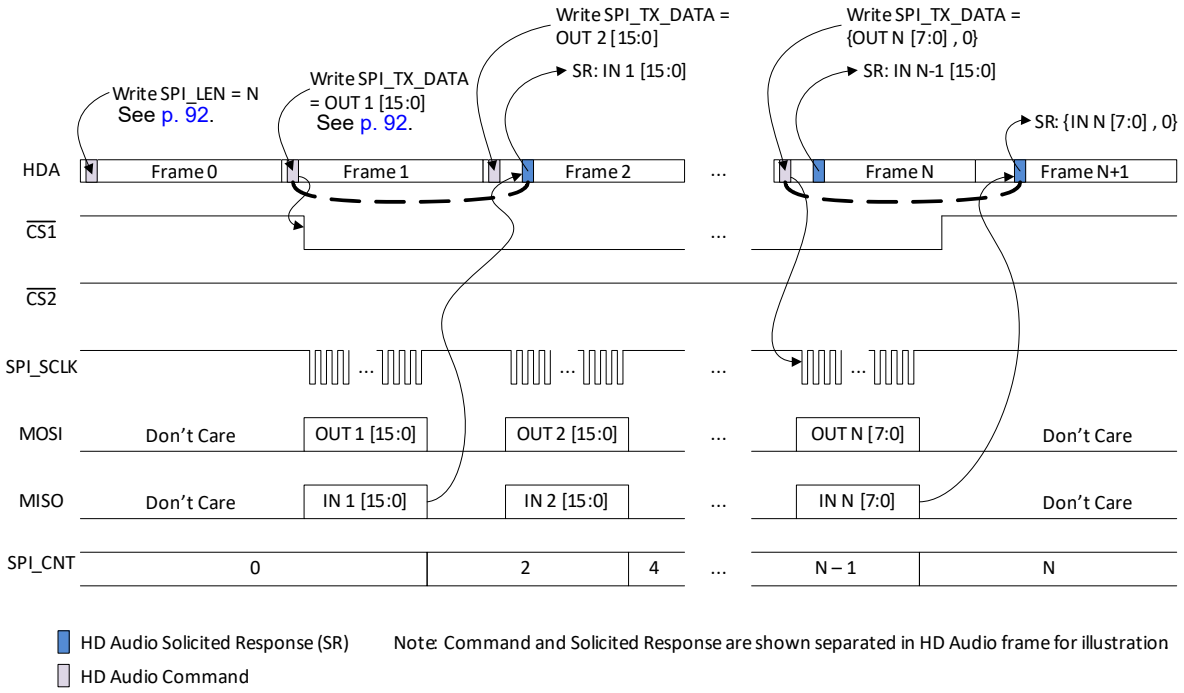


Figure 4-22. HDA–SPI Interaction, Odd Byte Count

4.5.1 MISO Timing

The MISO input is latched based on the internally generated SPI_SCLK signal edge or by passing the SPI_SCLK signal through an input buffer. Passing the SPI_SCLK signal through an input buffer retimes the clock and can improve timing robustness when the bus is heavily loaded. The input timing source is controlled by the SPI_TIM bit (see Table 6-168). If SPI_TIM = 0, MISO capture timing is based on the retimed SPI_SCLK signal from the pad.

4.6 I²C Master Port

The I²C master port operates exclusively in Master Mode and supports Start and Stop conditions, acknowledge, 7-bit slave addressing, clock stretching, standard format, and combined format. It can operate in the following modes:

- Standard Mode (SM) with a bit rate of up to 100 kbit/s
- Fast Mode (FM) with a bit rate of up to 400 kbit/s
- Fast Mode Plus (FM+), with a bit rate of up to 1 Mbit/s.

The I²C master port does not support synchronization, arbitration, or 10-bit slave addressing.

4.6.1 I²C Quick Access Modes

The I²C master includes two quick-access modes that simplify access to indexed registers on an I²C slave device. When the I²C Quick Write register is written, the hardware immediately executes a simple write transaction of 2 bytes (the subaddress and the write data) to the I²C slave device with the address specified in the I²C address register. Likewise, when the I²C quick read register is written, the hardware immediately executes a combined read transaction where 1 byte (the subaddress) is written to the I²C slave device with the address specified in the I²C address register, and subsequently 1 byte is read back from that same I²C slave device. The read/write bit in the I²C address register are disregarded when performing a quick write or quick read operation, and the hardware automatically sets the R/W bit on the I²C bus to the appropriate value for the currently executed transaction. After completing a quick read or quick write operation, an HD Audio UR is generated with the I²C status (success or fail) and read data (if appropriate) embedded in the UR payload.

Fig. 4-23 and Fig. 4-24 show HDA–I²C quick-access interactions.

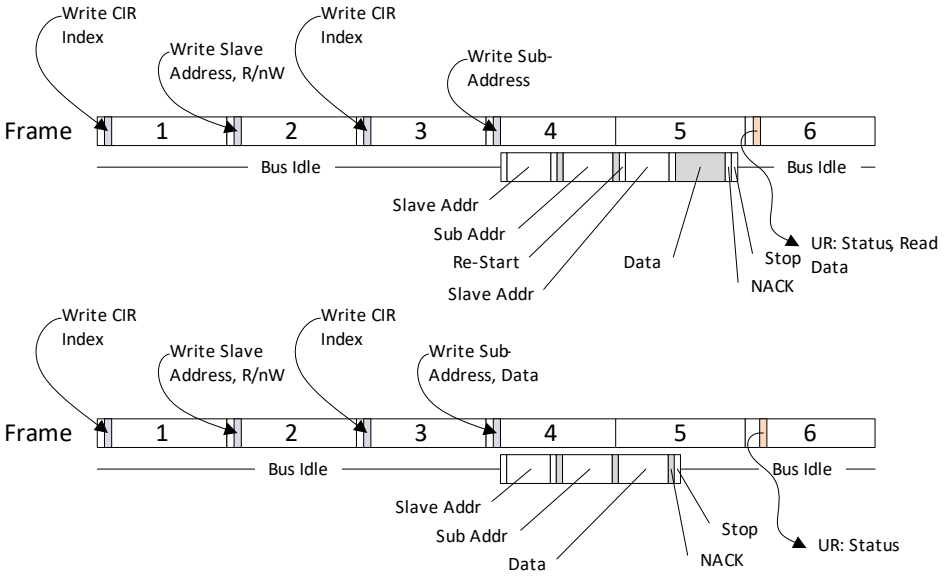


Figure 4-23. HDA–I²C Quick-Access Interaction, Fast Mode Plus (1 Mbps)

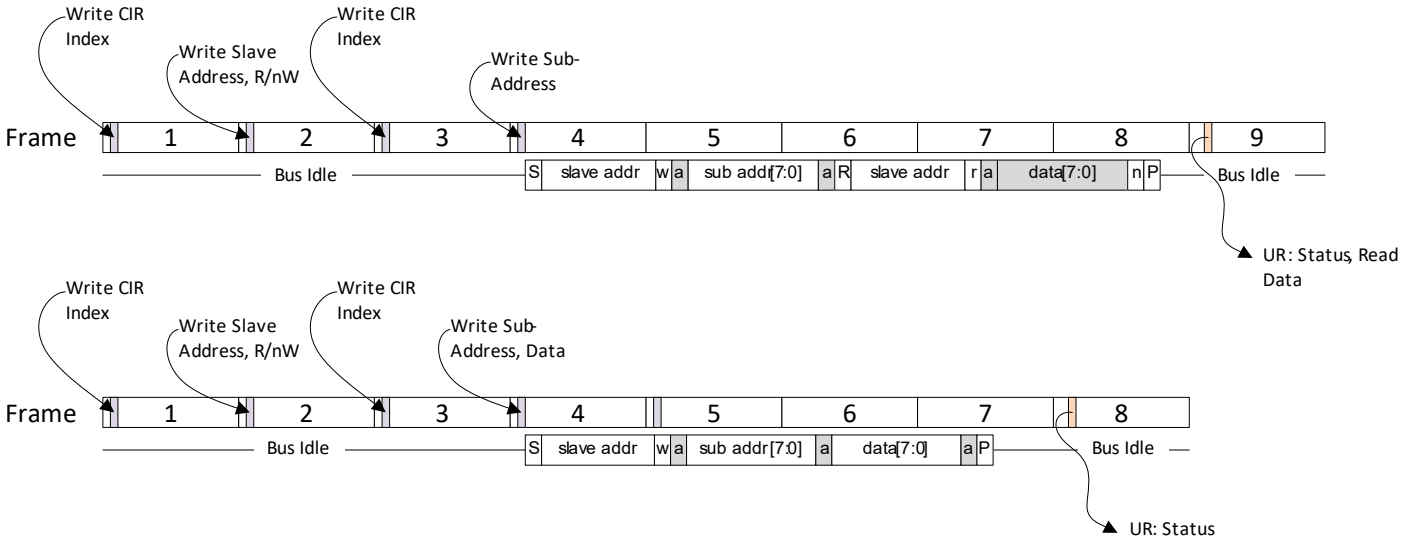


Figure 4-24. HDA–I²C Quick-Access Interaction, Fast Mode (400 kbps)

4.6.2 I²C Bus Clear

The I²C master can generate a bus-clear sequence to attempt to resolve an I²C bus contention. The bus-clear sequence is triggered by setting the bus clear bit (I2C_BC) in the I²C control register CIR = 0x005B in the Vendor Processing Widget. The I²C master does not include specific bus-fault detection and does not automatically attempt to clear the bus.

If a bus-clear sequence is triggered, the CS8409 toggles SCL nine times, followed by a STOP condition. The nine SCL cycles ensure that any slave device receives a NACK to release the I²C bus. The STOP condition ensures that all devices are in an idle state in which they listen for an I²C START condition.

Note that an I²C bus-clear sequence is triggered only when the I2C_BC bit is set from 0 to 1. To trigger a second bus-clear sequence at a later time, first the I2C_BC bit must be cleared again.

4.7 Parametric Filter Engine

The CS8409 implements two fully programmable parametric filter banks on each ASPx.A–ASPx.D render channel. For brevity, the parametric filter engine may be abbreviated “EQ”; however, each bank can be independently configured in any of the following topologies: low-pass filter (LPF), high-pass filter (HPF), all-pass filter (APF), band-pass filter (BPF), notch filter (NF), peaking EQ (PEQ), low-shelving EQ (LSEQ), or high-shelving EQ (HSEQ). Both banks are cascaded, so the Bank 1 output becomes the Bank 2 input. Therefore, the overall transfer function is the product of the two functions.

The filters are implemented in the biquad form, as shown in Fig. 4-25.

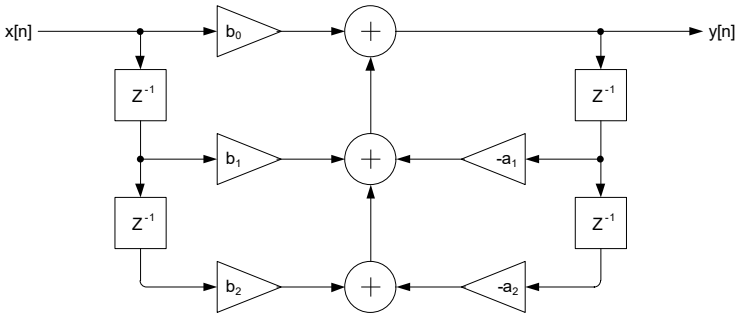


Figure 4-25. Biquad Filter Architecture

Fig. 4-25 shows the parametric filter engine topology.

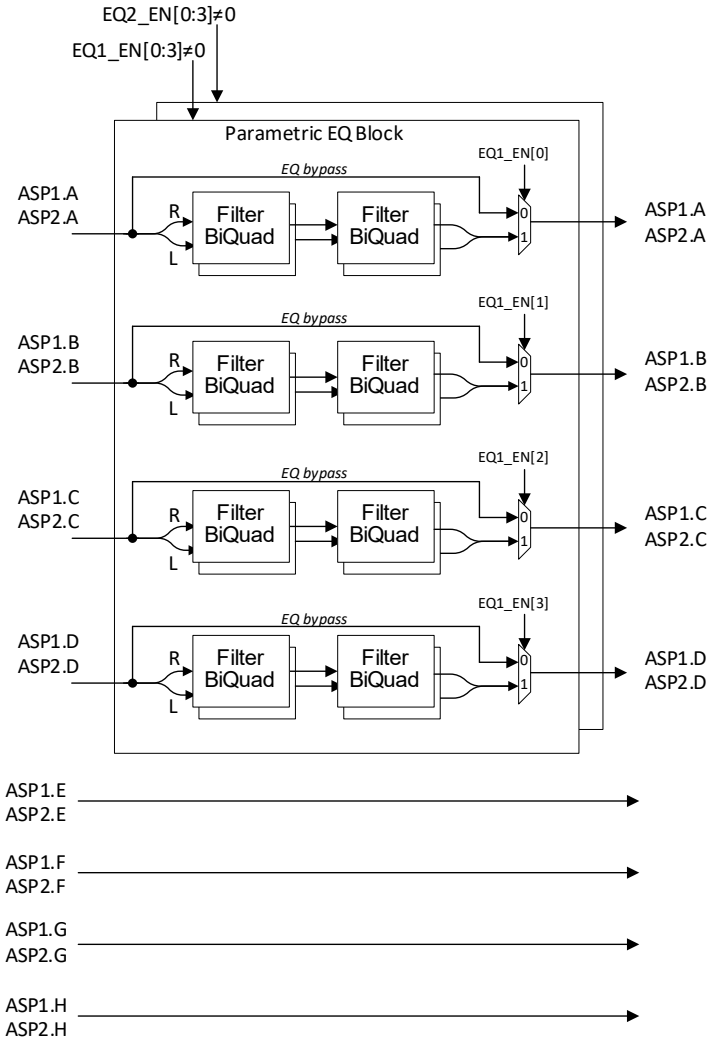


Figure 4-26. Parametric Filter Engine Topology

This architecture is represented by Eq. 4-1, where y[n] represents the output sample value and x[n] represents the input sample value.

$$y[n] = b_0x[n] + b_1x[n – 1] + b_2x[n – 2] – a_1y[n – 1] – a_2y[n – 2]$$

Equation 4-1. Biquad Filter Equation

The coefficients are represented in binary form by 24-bit signed values stored in 3.21 two's-complement format. The 3 MSBs represent the sign bit and the whole-number portion of the decimal coefficient, and the 21 LSBs represent the fractional portion of the decimal coefficient. The coefficient values must be in the range of –4.00000 decimal (0x80_0000) to 3.99996 decimal (0x7F_FFFF).

The binary coefficient values are accessed via the parametric filter engine register block, Section 6.11.8.12 of the vendor processing widget. Table 4-2 lists address values for each filter coefficient. These values are used by the EQ coefficient address bits in the parametric filter engine coefficient write 2 register, see Table 6-204.

Table 4-2. EQ Coefficient Address Values

EQ Coefficient Address	Output Channels	Filter Bank	Filter Coefficient	EQ Coefficient Address	Output Channels	Filter Bank	Filter Coefficient
0	ASP1 Tx ch 0/1 (EQ1) ASP2 Tx ch 0/1 (EQ2)	1	b_0	20	ASP1 Tx ch 4/5 (EQ1) ASP2 Tx ch 4/5 (EQ2)	1	b_0
1			b_2	21			b_2
2			b_1	22			b_1
3			a_2	23			a_2
4			a_1	24			a_1
5		2	b_0	25		2	b_0
6			b_2	26			b_2
7			b_1	27			b_1
8			a_2	28			a_2
9			a_1	29			a_1
10	ASP1 Tx ch 2/3 (EQ1) ASP2 Tx ch 2/3 (EQ2)	1	b_0	30	ASP1 Tx ch 6/7 (EQ1) ASP2 Tx ch 6/7 (EQ2)	1	b_0
11			b_2	31			b_2
12			b_1	32			b_1
13			a_2	33			a_2
14			a_1	34			a_1
15		2	b_0	35		2	b_0
16			b_2	36			b_2
17			b_1	37			b_1
18			a_2	38			a_2
19			a_1	39			a_1

The parametric EQ chain is enabled and disabled for each channel pair via the EQ enable bits (see Table 6-205). Each pair is processed independently, but always shares the same processing coefficients and are thus processed equally. The EQ select bits (see Table 6-205) specify the EQ bank addressed by the EQ coefficient address. To read from or write to coefficients, the EQ coefficient access bit (see Table 6-204) must be set. Additionally, the appropriate EQ enable bit must also be set to read or write coefficients values. When CIR 0x0064 is written to with the EQ access and write bits set, a write command is performed into the selected EQ coefficient address for the EQ bank chosen by the EQ select bits. Therefore, EQ select bits must be set correctly before writing to CIR 0x0064 with the access and write bits set.

4.8 General-Purpose I/O (GPIO)

CS8409 includes eight general-purpose input/output (GPIO) pins; several GPIO pins share an alternate function with the SPI master or I2C master port. GPIO alternate functions are enabled by control bits in Section 6.11.8.3. If configured as GPIOs, these pins are controlled through the AFG. If configured for alternate function, these pins are controlled by their respective internal logic, as shown in Fig. 4-27.

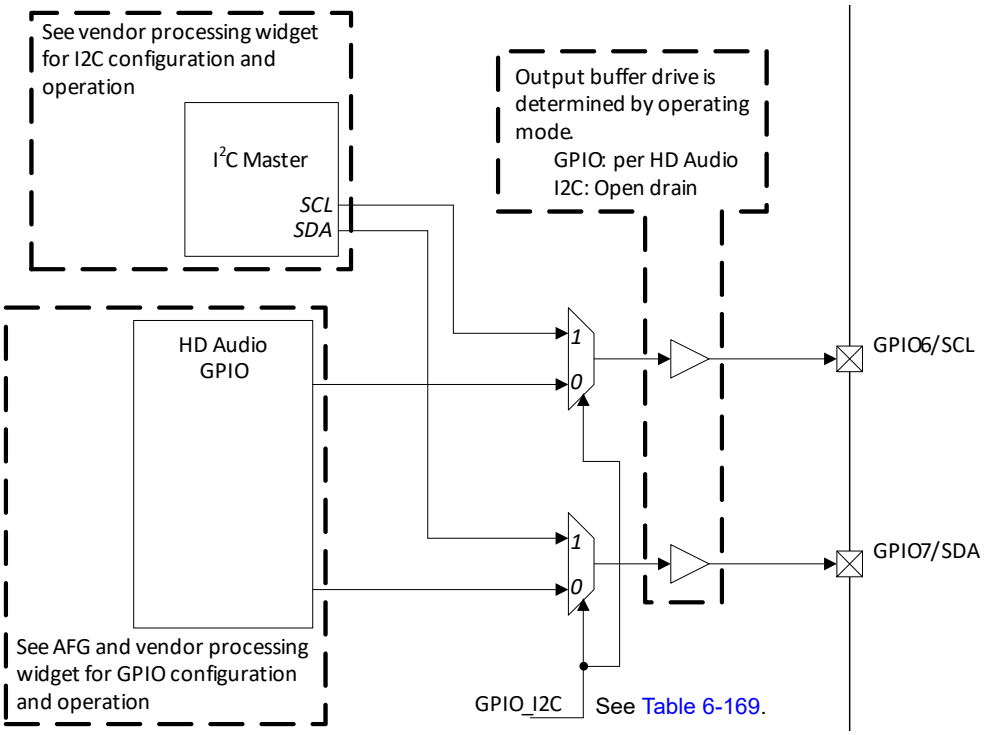


Figure 4-27. GPIO6, GPIO7 Alternate Function Select

The GPIO_I2C bit in the Section 6.11.8.3 controls GPIO6 and GPIO7 alternate function select. If GPIO_I2C is set, both pins are controlled by the I2C master logic and the output buffers function as open-drain outputs.

The GPIO_MISO1, GPIO_CS1, and GPIO_CS2 bits in the Section 6.11.8.3 control the GPIO0, GPIO1, and GPIO2 alternate function select, respectively.

- If GPIO_MISO1 is set, GPIO0 functions as the SPI port MISO input.
- If GPIO_CS1 is set, GPIO1 functions as SPI chip select for slave number one.
- If GPIO_CS2 is set, GPIO2 functions as SPI chip select for slave number two.

The GPIO_MISO2 bit in the Section 6.11.8.3 controls the second MISO input path.

- If GPIO_MISO2 is set, GPIO3 functions as a second SPI data input when the second slave device is accessed (CS2 is active).
- If GPIO_MISO2 is cleared, data from the second slave device is captured from the MISO1 input.

Table 4-3 shows SPI chip-select cases.

Table 4-3. SPI Chip-Select Cases

SPI_CSEL	GPIO_MISO1	GPIO_MISO2	Behavior
0	0	x	Output only
0	1	x	Bidirectional, input from SPI Slave 1 on GPIO0/MISO1
1	0	0	Output only
1	x	1	Bidirectional, input from SPI Slave 2 on GPIO3/MISO2
1	1	0	Bidirectional, input from SPI Slave 2 on GPIO0/MISO1

The block diagram in Fig. 4-28 shows the GPIO6, GPIO7 alternate function select logic

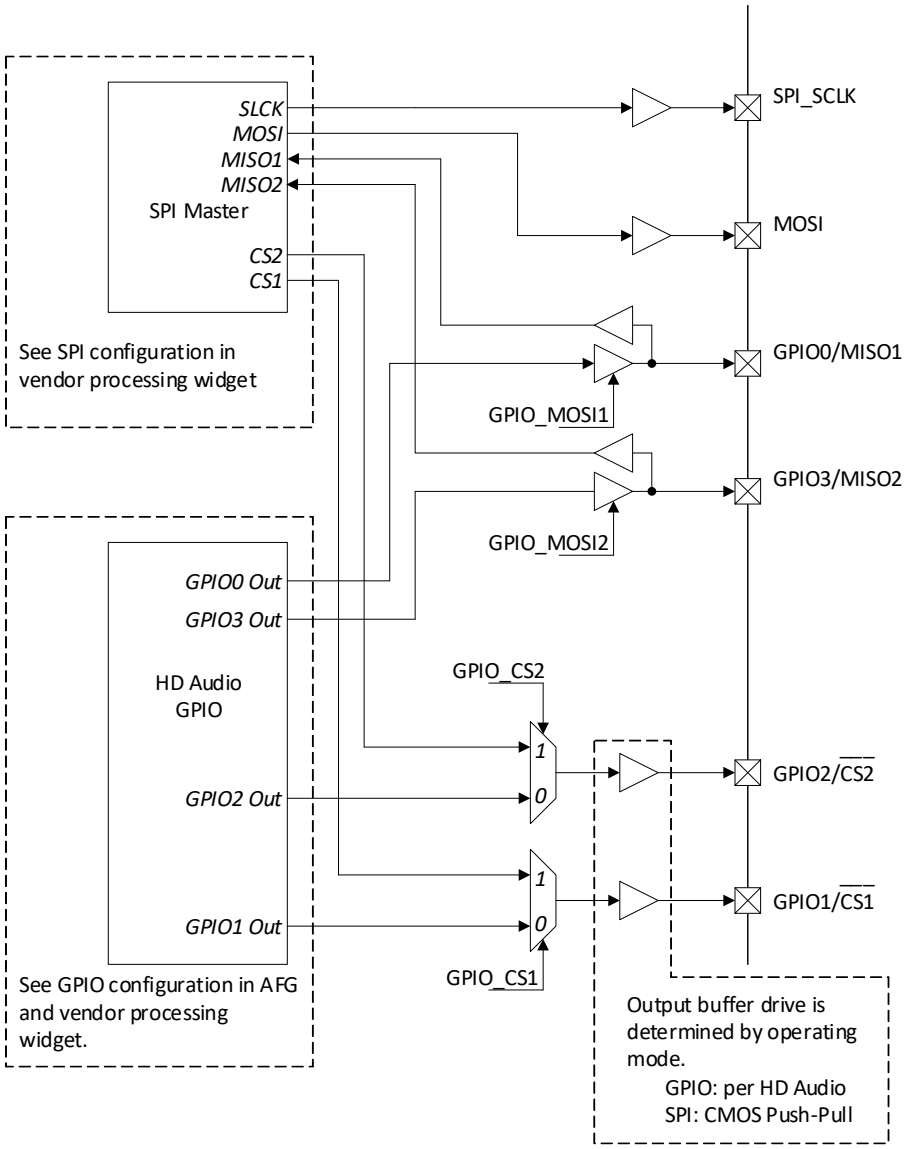


Figure 4-28. GPIO6, GPIO7 Alternate Function Select

4.8.1 GPIO Unsolicited Response Mechanism

CS8409 includes two GPIO UR mechanisms. Each GPIO may have a unique UR tag value (specified in Section 6.3.10) in addition to the default UR (specified in Section 6.3.9) specified in HD Audio. CS8409 queues an HD Audio UR when a GPIO changes state, the GPIO is configured as an input, and the GPIO has UR gating disabled. After being queued, a UR is transmitted according to HD Audio protocol, following CS8409 UR priority order. Masking or disabling a GPIO UR after a UR has been queued does not remove the UR from the queue.

If a GPIO would generate a UR and its unique UR is enabled, rather than generate a generic GPIO UR, the CS8409 generates a UR with a tag value specific to the GPIO triggering the UR. If a GPIO would generate a UR and its unique UR is disabled, the CS8409 generates a generic GPIO UR.

Having unique UR tags for individual GPIOs makes decoding GPIO-related URs easier. Unique URs prevent activity on one GPIO from masking activity on a different GPIO.

4.9 Internal Clock Gating

CS8409 includes several internal clock domains that may be gated in order to reduce current consumption. Clock gate controls are located in the Vendor Processing Widget.

- GPIO_CEN (see Table 6-167) gates the clock to GPIO logic. If GPIO_CEN = 0, the clock is gated and GPIO controls have no effect.
- I2C_EN (see Table 6-167) gates the clock to the I²C master logic. If I2C_EN = 0, the I²C master logic clock is gated and I²C controls have no effect.
- SPI_EN (see Table 6-167) gates the clock to the SPI master logic. If SPI_EN = 0, the SPI master logic clock is gated and SPI controls have no effect.
- ASP2_EN (see Table 6-168) gates the clock to the ASP2 port logic. See ASP1_EN below.
- ASP1_EN (see Table 6-168) gates the clock to the ASP1 port logic. If ASP1_EN = 0, the ASP1 port logic clock is gated and ASP1 controls have no effect. Note that, when ASP1_EN is cleared, the clock controller attempts to cleanly gate the ASP1 related clocks at a frame boundary after the ASP1 output FIFO has emptied. As a result of the clean clock gating procedure, ASP1 may continue to operate briefly after ASP1_EN is cleared.

4.10 Register Settings across Resets

The CS8409 performs a complete power-on reset (POR) initialization if the VL_HD voltage is cycled from off to on. All registers are initialized to the default state after POR. Device behavior due to other system reset conditions or power state transitions events follows the requirements in the *HDA Specification Rev. 1.0a*. Standard behavior is for register settings to persist across power state transitions, single FG resets, and link resets, and to be reset to their power-on defaults by a double FG reset. Table 4-4 lists deviations from this behavior (as mandated by the *HDA Specification Rev. 1.0a*).

Table 4-4. Register Settings across Reset Conditions

Setting	Action across D0/D3 State Transitions or Link BCLK Stopped	Action with Link Reset	Action with Double Function Group Reset	Action with Single Function Group Reset
Unique codec physical address (SDI)	Persist across Dx state transitions or BCLK stopped	Requires codec initialization sequence to acquire new unique address	Persist across double FG reset	Persist across single FG reset
Converter format. TYPE, BASE, MULT, DIV, BITS, CHAN fields (Table 6-3) (verb ID = A/2)	Persist across Dx state transitions or BCLK stopped	Persist across link reset	Reset to POR default value Ps-settings-reset set to 1	Persist across single FG reset
Amplifier gain/mute (verb ID = B/3)	Index, mute, and gain settings persist across Dx state transitions or BCLK stopped	Index, mute and gain settings persist across link reset	Reset to POR default value PS-Settings-Reset set to 1	Index, mute and gain settings persist across single FG reset
Processing coefficient (verb ID = C/4)	Persist across Dx state transitions or BCLK stopped	Persist across link Reset	Persist across double FG reset	Persist across single FG reset
Coefficient index (verb ID = D/5)	Reset to default across Dx state transitions and does not set PS-Settings-Reset to 1	Reset to default by Link reset and does not set PS-Settings-Reset to 1	Reset to POR default value PS-Settings-Reset set to 1	Reset to default by single FG reset and does not set PS-SettingsReset to 1
Processing state (verb ID = F03/703)	Persist across Dx state transitions or BCLK stopped	Persist across link reset	Persist across double FG reset	Persist across single FG reset
Power state for the function group and individual widgets (verb ID = F05/705)	Persist across BCLK stopped PS-Act and PS-Set updated to the current power state across Dx state transitions	Persist across link reset [1]	Reset to POR default value PS-Settings-Reset set to 1	Persist across single FG reset
Converter stream and channel. Stream number and lowest channel number (verb ID = F06/706)	Reset to default across Dx state transitions and does not set PS-SettingsReset to 1	Reset to default by link reset and does not set PS-Settings-Reset to 1	Reset to POR default value PS-Settings-Reset set to 1	Reset to default by single FG reset and does not set PS-SettingsReset to 1
Pin widget controls. In/out enables, Vref (verb ID = F07/707)	Persist across Dx state transitions or BCLK stopped	Persist across link reset	Reset to POR default value PS-Settings-Reset set to 1	Persist across Single FG reset
UR control. Enable and tag (verb ID = F08/708; FF0/7F0; FF1/7F1)	Persist across Dx state transitions or BCLK stopped	Persist across link reset	Reset to POR default value PS-Settings- Reset set to 1	Persist across Single FG reset

Table 4-4. Register Settings across Reset Conditions *(Cont.)*

Setting	Action across D0/D3 State Transitions or Link BCLK Stopped	Action with Link Reset	Action with Double Function Group Reset	Action with Single Function Group Reset
Beep control (verb ID = F0A/70A)	Persist across Dx state transitions or BCLK stopped	Persist across link reset	Reset to POR default value PS-Settings-Reset set to 1	Persist across single FG reset
EAPD/BTL enable. L–R Swap, EAPD and BTL (verb ID = F0C/70C)	Persist across Dx state transitions or BCLK stopped	Persist across link reset	Reset to POR default value PS-Settings-Reset set to 1	Persist across single FG reset
GPO/GPIO controls (verb ID = F14–F1A/ 714–71A)	Persist across Dx state transitions or BCLK stopped	Persist across link reset	Reset to POR default value PS-Settings-Reset set to 1	Persist across single FG reset
Pin configuration (verb ID = F1C/ 71C–71F)	Persist across Dx state transitions or BCLK stopped	Persist across link reset	Persist across double FG reset	Persist across single FG reset
Implementation ID (verb ID = F20/720–723)	Persist across Dx state transitions or BCLK stopped	Persist across link reset	Persist across double FG reset	Persist across single FG reset
Converter channel count (verb ID = F2D/72D)	Persist across Dx state transitions or BCLK stopped	Persist across link reset	Reset to POR default value PS-Settings-Reset set to 1	Persist across single FG reset

1. Exiting link reset causes function groups in D3cold to enter D3hot.

5 Applications

5.1 HD Audio

5.1.1 Audio Function Group (AFG) Power State and ASP_EN

When changing the AFG power state from D0 to D3hot, it is necessary to first disable the ASPs and implement a minimum delay of 10 LRCK cycles. If these steps are not taken, the actual power state may not reach D3hot status and the PS-Act bit in the AFG may not update. Also, the ASPs may not operate correctly upon returning to AFG D0 state.

To avoid these issues, it is necessary to first power down the ASPs by clearing the ASP1/2_EN bits, located in CIR = 0x0001 in the Vendor Processing Widget. After clearing these bits, a minimum delay of 10 LRCK cycles is necessary to allow the ASP power-down sequence to complete before the AFG power state can be changed to D3hot.

5.1.2 Read/Write Access in Different Power States

While in lower power modes, some verb commands are not available or are read only. This section summarizes the read/write access in the different power states for the CS8409.

- AFG power state = D0
  - Converter widgets with power state (e.g., DMIC 1 Node 0x22):
    - If the converter widget power state is D0, read/write access is available for every command.
    - If the converter widget power state is D3, read/write access is available for every command except for the converter stream, channel command that has read-only access.
  - Widgets without power states (e.g., ASP Transmitter 1.A Node 0x): Read/write access is available for every command.
- AFG power state = D3hot. Only commands in the AFG and the power state command in other widgets have write access. Other commands have read-only access. There is an exception to the previous rule: For the Vendor Processing Widget, there is no write access to any command and the coefficient registers do not have read access (read results in all zeros).
- AFG power state = D3cold. The only recognized command is a double function group reset.

5.1.3 UR Gating

When a driver transitions the CS8409 from normal operation to Low-Power Mode (i.e., the AFG power state goes from D0 to D3hot), to prevent interruptions during the shut-down sequence, the driver may require that the CS8409 does not generate URs during this time. To support this requirement, the UR gating bit (see Table 6-167) can be set to prevent UR generation during power-down. Non-GPIO URs triggered during the gated time period will generate a wake event after the HD Audio link is powered down, and when the link is back up the gated URs will be transmitted. GPIO URs are unique because they have a dedicated wake enable mask. A GPIO UR triggered during the gated time period will only generate a wake event if the associated GPIO wake enable mask is configured to allow wake.

Fig. 5-1 details the UR gating functionality.

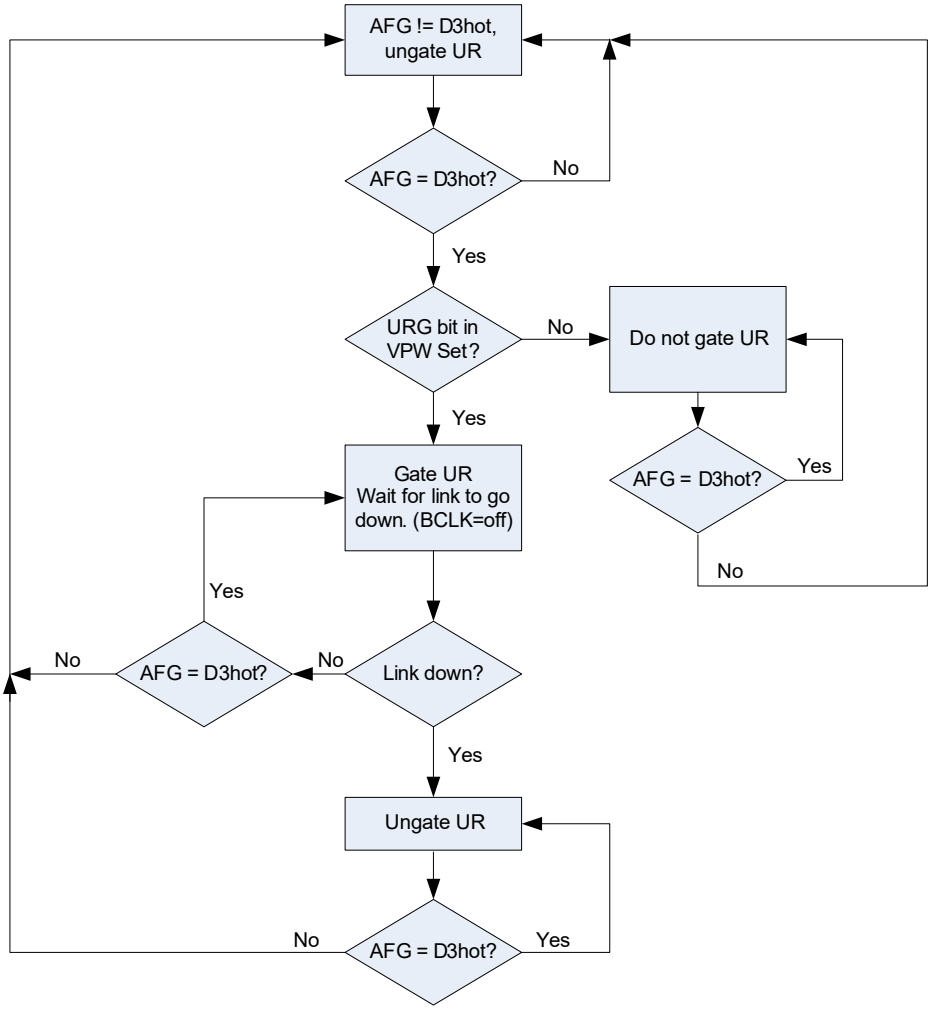


Figure 5-1. UR Gating Flowchart

5.1.4 Stream Limitations

For any shared stream, the sample rate (BASE, MULT, and DIV settings) and sample width (BITS setting) must be the same for all converter widgets in the shared stream. See Section 6.1.3 for details on these settings.

Restrictions for serial-port streaming (both input and output):

- Streams must have an even number of channels
- The LCN control value must be even or zero
- All widgets are two channel (stereo)
- When sharing a stream across serial port widgets, render widgets (see Section 6.4) may have identical LCN values.

- Each stream may be shared with up to eight widgets, some of which may have identical LCN values.
- If a stream is shared across serial-port widgets, no gaps are allowed between channels, so one port must have LCN = 0 and the others must have LCN equal to another serial port widget's LCN + 2

Fig. 5-2 shows valid and invalid configurations for stream sharing.

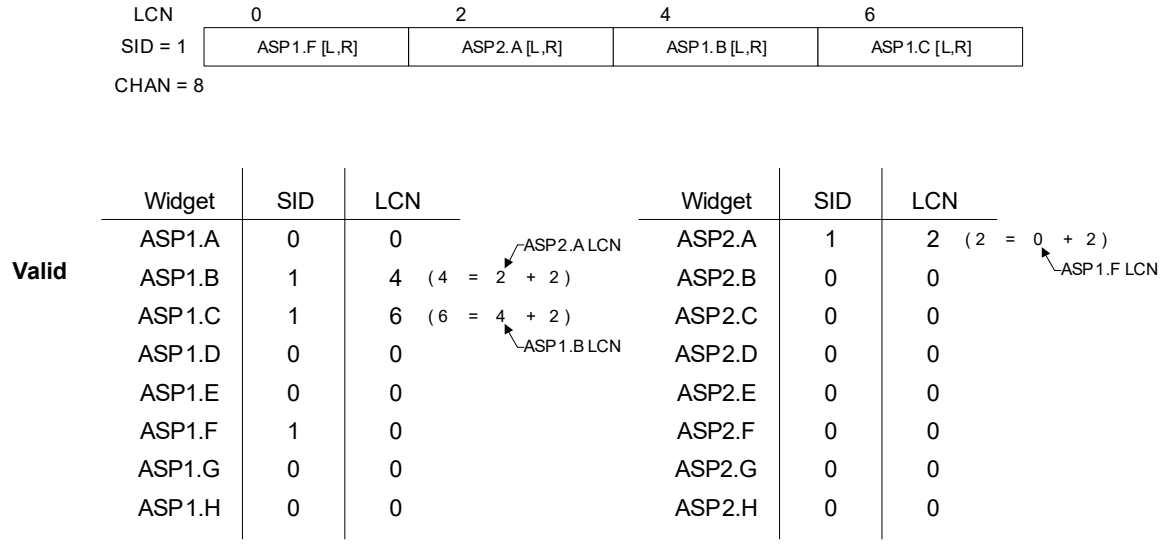
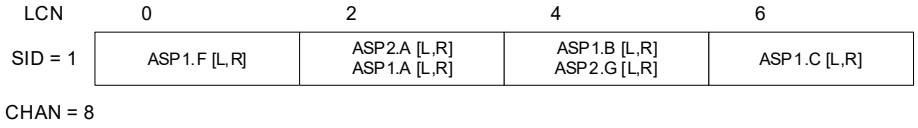


Figure 5-2. Sharing a Stream across Serial Port Widgets

Serial port widgets rendering data from HD Audio may also share the same channel data, as shown in Fig. 5-3. Widgets capturing data cannot share the same channel.



Valid

Widget	SID	LCN		Widget	SID	LCN	
ASP1.A	1	2	Channel shared with ASP2.A	ASP2.A	1	2	Channel shared with ASP1.A
ASP1.B	1	4	Channel shared with ASP2.G	ASP2.B	0	0	
ASP1.C	1	6		ASP2.C	0	0	
ASP1.D	0	0		ASP2.D	0	0	
ASP1.E	0	0		ASP2.E	0	0	
ASP1.F	1	0		ASP2.F	0	0	
ASP1.G	0	0		ASP2.G	1	4	Channel shared with ASP1.B
ASP1.H	0	0		ASP2.H	0	0	

Figure 5-3. Sharing a Channel across Serial Port Widgets

5.1.5 Synchronizing Streams and Widgets

The CS8409 supports synchronization among several converter widgets for multichannel applications. The ASP1.n and ASP2.n Rx, the ASP1.n and ASP2.n Tx, and DMIC1–DMIC2 can be synchronized by using the synchronization bit's vendor processing widget.

The following list further details the behavior of the synchronization feature.

- A single stream ID cannot be shared across multiple synchronization groups.
- Different converter widget types (DMIC, ASPx.n Rx, ASPx.n Tx) do not synchronize together. Each converter type is its own synchronization group if the sync bits for multiple converter types are set at the same time.
- If ASP_SYNC is set, widgets from ASP1.n Tx and ASP2.n Tx form a single synchronization group. Likewise, if ASP_SYNC is set, widgets from ASP1.n Rx and ASP2.n Rx form a single synchronization group.
- If ASP_SYNC is cleared, the widgets from ASP1.n Tx form one synchronization group and widgets from ASP2.n Tx form a second synchronization group. Likewise, if ASP_SYNC is cleared, the widgets from ASP1.n Rx form one synchronization group and widgets from ASP2.n Rx form a second synchronization group.
- If ASP_SYNC is set, both ASPs must be configured to source clock from the same resource (BCLK, PLL1, or PLL2)
- If ASP_SYNC is cleared, for any synchronization group, at least two synchronization bits must be set. If only one synchronization bit is set, the corresponding converter cannot stream data.
- If ASP_SYNC is set, ASP1_TXSYNC and ASP2_TXSYNC must each have at least one bit set and ASP1_RXSYNC and ASP2_RXSYNC must each have at least two bits set. If either condition is not met, the corresponding converters cannot stream data.
- If ASP_SYNC is set, the corresponding ASPx_SCLK, ASPx_LRCK/FSYNC, ASPx_SDOUT and ASPx_MCLK bits must be set at the same time to ensure synchronization between both ASPs. All of these bits reside in the same location within the Vendor Processing Widget, CIR = 0x0082. If clocks from one ASP are enabled before the other, synchronization cannot be guaranteed.
- If null removal is enabled for either ASP_RX block, the removal method must be consistent across both ASPs. If one ASP is programmed for NFS Mode and the other is programmed for NSB Mode, synchronization does no work properly across the ASPs when ASP_SYNC is set. See Section 6.11.8.7.
- The sample rate must be the same for each converter widget in a synchronization group, regardless of whether shared or individual stream IDs are used.
- HD Audio tunneling streams and 48-kHz isochronous streams cannot be synchronized with 48-kHz native streams.

- The sample width needs only to be the same for each converter widget of a shared stream in a synchronization group. The sample width for converter widgets can differ for each stream in a synchronization group.
- The stream number for all converter widgets in a synchronization group must bet set to zero while the appropriate synchronization bits are configured.
- After synchronization bits are configured, no converter begins streaming data until all of the converter widgets in the synchronization group are configured and the correct stream ID values are entered.
- After a synchronization group has started streaming, if any converter widget in the synchronization group has its power state changed to D3 or its stream ID set to zero, all converters in the synchronization group stop streaming.
- If an invalid stream ID and/or LCN (a stream not on the HDA bus or an incorrect LCN) is programmed into a converter in a synchronization group, synchronization between the converters may be lost. To resynchronize converters, clear the Stream ID for all the widgets in the synchronization group and then set them back to valid values.
- For serial-port output synchronization groups, the corresponding EQ enable bits for all members of the synchronization group must match; otherwise, the output data is not synchronized. A one-sample delay is added when the EQ block is enabled for a data path.
- Widgets in a synchronization group cannot be assigned to streams with unused channels (e.g., ASP1.A Tx cannot be synchronized if it is configured to SID = 2, LCN = 2, and no other widget is configured to SID = 2, LCN = 0).
- When capturing data in Slave Mode among multiple, synchronized widgets within one ASP, ensure that all widgets share the same Stream ID. Otherwise, synchronization cannot be guaranteed.

5.1.6 Synchronization Stream ID Constraints

When the synchronization feature is used, there are many possible combinations of synchronization groups and stream IDs. To keep the design of the CS8409 simple, some combinations are not supported. The following rules apply while the synchronization feature is used:

- For a stream ID shared between multiple converter widgets, the sync bits must be in the same state for all of the converter widgets that share the stream ID.
- For the ASPx.n TX synchronization group, some converter widgets in the group can use a shared stream ID (e.g. ASP1.A and ASP1.B) and others in the group (e.g. ASP1.C) can use another stream ID (shared or individual).

5.1.7 Starting Streams

When synchronizing multiple HDA streams from multiple widgets, care must be taken when starting a stream to maintain synchronization.

When starting a stream, stream ID (SID) and lowest channel number (LCN) of a given widget must be set before the controller places the associated stream packet on the HDA link. This ensures that the SID and LCN are not updated after the data stream starts, causing a loss of synchronization across multiple widgets.

5.2 DMICs

5.2.1 DMIC Configuration Procedure

DMIC configuration (see Table 6-174) must be done while the DMIC widgets are in the D3 state. The procedure to configure a DMIC widget is as follows:

1. Command DMIC to D3 state
2. Read DMIC PS-Act; Wait for PS-Act to return D3
3. Write DMIC configuration in Vendor Processing Widget
4. Command DMIC to D0 state
5. Assign DMIC streams

5.2.2 DMIC Clock Pin Status

The default power-on-reset configuration of the DMIC clock pins is a high-impedance output state with a weak pull down. Each DMIC clock pin (DMIC1_CLK, DMIC2_CLK) has a dedicated pad driver enable control bit (see Table 6-216). Table 5-1 shows how DMICx_CLK behaves with respect to DMICx pin widget INE and DMx_CLK_EN controls.

Table 5-1. DMIC Clock Enable

DMICx INE (See Table 6-131)	DMx_CLK_EN (See Table 6-216)	DMICx_CLK Pin
x	0	Hi-Z
0	1	Low
1	1	Clock

5.3 ASPs

5.3.1 SCLK and MCLK Source Switching

CS8409 uses two cascaded glitch-free clock select blocks to select the clock source for the SCLK and MCLK signals of each ASP. As a result, when switching an ASP clock source from BCLK to either PLL1 or PLL2, it is required to enable both PLL1 and PLL2.

When sourcing clocks from one of the PLLs, writing a value to either of the Clock Control 3 Registers requires enough time for the PLL to lock for the new value to take effect. At least 270 µs of wait time is required before ASP Clock Control 3 settings can be adjusted.

Between setting PLLx_EN = 1 and writing a value to CIR = 0x0005 or CIR = 0x0008, there must be a minimum 270-µs delay to ensure the PLL is locked.

Ex. 5-1 illustrates SCLK and MCLK source switching.

Example 5-1. SCLK and MCLK Source Switching

Step	Task	Verb	Register/Bit Fields	Payload	Description
1	Set PLL2_FRQSEL in Device Configuration 2 (CIR = 0x0001) to desired frequency for ASP1 serial data format.				
Step	Task	Verb	Register/Bit Fields	Payload	Description
1.1	Set VPW CIR to 0x0001	x4750001	Vendor processing widget coefficient index	0x0001	
1.2	Initiate VPW write to PLL2_FRQSEL bits	x474xxxx		Varied	Bits[12:10] set PLL2 frequency. To enable ASP clocks, set one or both bits [6:5].
2	Set PLL1_EN and PLL2_EN in Device Configuration 1 (CIR = 0x0000).				
Step	Task	Verb	Register/Bit Fields	Payload	Description
2.1	Set VPW CIR to 0x0000	x4750000	Vendor processing widget coefficient index	0x0000	
2.2	Initiate VPW write to enable PLLs	x474xxxx		Varied	Bits[13:12] = 1 to enable PLL2 and PLL1.
3	Set ASP1_SC_SRCSEL and ASP1_MC_SRCSEL in ASP1 Clock Control 2 (CIR = 0x00004) to 10b (PLL2 select).				
Step	Task	Verb	Register/Bit Fields	Payload	Description
3.1	Set VPW CIR to 0x0004	x4750004	Vendor processing widget coefficient index	0x0004	
3.2	Initiate VPW write to select PLL2 for MCLK, SCLK	x474xxxx		Varied	Bits[14:13] = 10 and Bits[12:11] = 10 to select PLL2 for MCLK and SCLK source.
4	Clear PLL1_EN in Device Configuration 1 (CIR = 0x0000)				
Step	Task	Verb	Register/Bit Fields	Payload	Description
4.1	Set VPW CIR to 0x0000	x4750000	Vendor processing widget coefficient index	0x0000	
4.2	Initiate VPW write to disable PLL1	x474xxxx		Varied	Bit[12] = 0 to disable PLL1.

5.3.2 Format Configuration

The ASP supports many common digital audio interface formats. Regardless of format, some common steps are required for ASP configuration.

- All widgets associated with the ASP being programmed must not be streaming.
- The ASPx_EN bit must be cleared
- The CS8409 must be programmed for either Master or Slave Mode before streaming. Switching from one to the other during streaming is not supported

After the conditions above are met, the ASP clock configuration (e.g. ASPx_LCPR, ASPx_SCDIV, etc.) may be configured.

5.3.2.1 I²S Format

Ex. 5-2 gives detailed configuration settings for accepted I²S format.

Example 5-2. I²S Configuration

Step	Task	Verb	Register/Bit Fields	Payload	Description
1	Enable TDM1 ASP transmitter pin widget	x2470740	ASP transmitter pin widget (Node ID = 0x24)	0x40	Enable TDM1.A output path
2	Enable TDM1 ASP receiver pin widget	x3470720	ASP receiver pin widget (Node ID = 0x34)	0x20	Enable TDM1.A input path
3	Enable VPW processing	x4770301	Vendor processing widget	0x01	Enable processing
4	Enable GPIO, PLL2, PLL1, I²C				
4.1	Set VPW CIR = 0x0000	x4750000	Vendor processing widget coefficient index	0x0000	PLLs, I²C, GPIO
4.2	Enable GPIO, PLLs, I²C	x474B009		0xB009	
5	Set LRCK duty cycle				
5.1	Set VPW CIR = 0x0003	x4750003	Vendor processing widget coefficient index	0x0003	LRCK high-duration = 32xFs, 50% duty cycle if SCLK =64xFs
5.2	Set LRCK high-duration to 32xFs	x474001F		0X001F	
6	Set SCLK, MCLK source select and SCLK:Fs ratio				
6.1	Set VPW CIR = 0x0004	x4750004	Vendor processing widget coefficient index	0x0004	Set SCLK = 64xFs, Select Source for SCLK, MCLK
6.2	Set MCLK source, SCLK source to PLL1, SCLK = 64xFs	x474283F		0x283F	
7	Set frame delay, SCLK/MCLK divider ratios, enable MCLK, set 50% duty cycle bit				
7.1	Set VPW CIR = 0x0005	x4750005	Vendor processing widget coefficient index	0x0005	SCLK = 3.072 MHz, MCLK enabled, frame delay = 0xSCLK. Note: For I²S Mode 50% duty cycle bit must be set.
7.2	Set SCLK divider ratio to 8:1, enable MCLK	x4748904		0x8904	
8	Set ASP1_Left transmit control for 24-bit data, I²S				
8.1	Set VPW CIR = 0x0019	x4750019	Vendor processing widget coefficient index	0x0019	Left start location = 0xSCLK, data = 24-bit, left channel active phase relative to falling LRCK edge
8.2	Clear left slot location = 0	x4740800		0x0800	
9	Set ASP1_Right transmit control for 24-bit data, I²S				
9.1	Set VPW CIR = 0x001A	x475001A	Vendor processing widget coefficient index	0x001A	Right start location = 32xSCLK, data = 24-bit, right channel active phase relative to rising LRCK edge
9.2	Set right slot location = 0	x4742800		0x2800	
10	Enable TDM pads				
10.1	Set VPW CIR = 0x0082	x4750082	Vendor processing widget coefficient index	0x0082	TDM pads enabled
10.2	TDM pad enable, normal slew rate	x474FF00		0xFF00	
11	Set PLL2, PLL1 to 49.152 MHz, enable ASP clocks, I²S Mode				
11.1	Set VPW CIR = 0x0001	x4750001	Vendor processing widget coefficient index	0x0001	PLL1, PLL2 = 49.152 MHz, ASP clocks ungated
11.2	Set PLL1, PLL2 frequency and enable clocks	x4740060		0x0060	

5.3.2.2 LJ Format

Ex. 5-3 gives detailed configuration settings for accepted LJ format.

Example 5-3. LJ Format Configuration

Step	Task	Verb	Register/Bit Fields	Payload	Description
1	Enable TDM1 ASP Transmitter Pin Widget	x2470740	ASP transmitter pin widget (Node ID = 0x24)	0x40	Enable TDM1.A input path
2	Enable TDM1 ASP Receiver Pin Widget	x3470720	ASP receiver pin widget (Node ID = 0x34)	0x20	Enable TDM1.A input path
3	Enable VPW processing	x4770301	Vendor processing widget	0x01	Enable processing
4	Enable GPIO, PLL2, PLL1, I²C				
4.1	Set VPW CIR = 0x0000	x4750000	Vendor processing widget coefficient index	0x0000	PLLs, I²C, GPIO
4.2	Enable GPIO, PLLs, I²C	x474B009		0xB009	

Example 5-3. LJ Format Configuration *(Cont.)*

Step	Task	Verb	Register/Bit Fields	Payload	Description
5	Set LRCK duty cycle				
5.1	Set VPW CIR = 0x0003	x4750003	Vendor processing widget coefficient index	0x0003	LRCK high-duration = 32xFs, 50% duty cycle if SCLK = 64xFs
5.2	Set LRCK high-duration to 32xFs	x474001F		0x001F	
6	Set SCLK, MCLK Source Select and SCLK:FS Ratio				
6.1	Set VPW CIR = 0x0004	x4750004	Vendor processing widget coefficient index	0x0004	Set SCLK = 64xFs, Select Source for SCLK, MCLK
6.2	Set MCLK source, SCLK source to PLL1, SCLK = 64xFs	x474283F		0x283F	
7	Set frame delay, SCLK/MCLK divider ratios, enable MCLK, set 50% duty cycle bit				
7.1	Set VPW CIR = 0x0005	x4750005	Vendor processing widget coefficient index	0x0005	SCLK = 3.072 MHz, MCLK enabled, frame delay = 0xSCLK. Note: For I²S Mode, 50% duty cycle bit must be set,
7.2	Set SCLK divider ratio to 8:1, enable MCLK	x4748904		0x8904	
8	Set ASP1_Left Transmit Control for 24-bit data, I²S				
8.1	Set VPW CIR = 0x0019	x4750019	Vendor processing widget coefficient index	0x0019	Left start location = 0xSCLK, data = 24 bit, left channel active phase relative to falling LRCK edge
8.2	Set Left Slot Location = 0	x4740800		0x0800	
9	Set ASP1_Right Transmit Control for 24-bit data, I2S				
9.1	Set VPW CIR = 0x001A	x475001A	Vendor processing widget coefficient index	0x001A	Right start location =32xSCLK, data = 24 bit, right channel active phase relative to rising LRCK edge
9.2	Set Right Slot Location = 0	x4742800		0x2800	
10	Enable TDM Pads				
10.1	Set VPW CIR = 0x0082	x4750082	Vendor processing widget coefficient index	0x0082	TDM pads enabled
10.2	TDM pad enable, normal slew rate	x474FF00		0xFF00	
11	Set PLL2, PLL1 to 49.152 MHz, enable ASP clocks, Left-Justified Mode				
11.1	Set VPW CIR = 0x0001	x4750001	Vendor processing widget coefficient index	0x0001	PLL1, PLL2 = 49.152 MHz, ASP clocks ungated, Left-Justified Mode
11.2	Set PLL1, PLL2 frequency and enable clocks, Left-Justified Mode	x4740062		0x0062	

5.3.2.3 TDM Format

Ex. 5-4 gives detailed configuration settings for common TDM formats, including suggested settings of ASPx_FSD that may differ among TDM interfaces.

Example 5-4. TDM Format Configuration

Step	Task	Verb	Register/Bit Fields	Payload	Description
1	Enable TDM1 ASP Transmitter Pin Widget	x2470740	ASP transmitter pin widget (Node ID = 0x24)		
2	Enable TDM1 ASP Receiver Pin Widget	x3470720	ASP receiver pin widget (Node ID = 0x34)		
3	Enable VPW processing	x4770301	Vendor processing widget		
4	Enable GPIO, PLL2, PLL1, I²C				
4.1	Set VPW CIR = 0x0000	x4750000	Vendor processing widget coefficient index	0x0000	PLLs, I²C, GPIO
4.2	Enable GPIO, PLLs, I²C	x474B009		0xB009	
5	Set LRCK duty cycle				
5.1	Set VPW CIR = 0x0003	x4750003	Vendor processing widget coefficient index	0x0003	LRCK high-duration = 1 bit pulse
5.2	Set LRCK high-duration to 128xFs	x4740000		0x0000	
6	Set SCLK, MCLK Source Select and SCLK:FS ratio				
6.1	Set VPW CIR = 0x0004	x4750004	Vendor processing widget coefficient index	0x0004	Set SCLK = 256xFs, Select Source for SCLK, MCLK
6.2	Set MCLK Source, SCLK Source to PLL1, SCLK = 256xFs	x47428FF		0x28FF	
7	Set frame delay, SCLK/MCLK divider ratios, enable MCLK				
7.1	Set VPW CIR = 0x0005	x4750005	Vendor processing widget coefficient index	0x0005	SCLK = 12.288 MHz, MCLK enabled, frame delay = 0xSCLK
7.2	Set SCLK divider ratio to 4:1, enable MCLK	x4740902		0x0902	

Example 5-4. TDM Format Configuration *(Cont.)*

Step	Task	Verb	Register/Bit Fields	Payload	Description
8	Set ASP1_Left transmit control for 24-bit data, 32-bit slots				
	Step **Task**	**Verb**	**Register/Bit Fields**	**Payload**	**Description**
	8.1 Set VPW CIR = 0x0019	x4750019	Vendor processing widget coefficient index	0x0019	Left start location = 0xSCLK, data = 24 bit
	8.2 Set left slot location = 0	x4740800		0x0800	
9	Set ASP1_Right transmit control for 24-bit data, 32-bit slots				
	Step **Task**	**Verb**	**Register/Bit Fields**	**Payload**	**Description**
	9.1 Set VPW CIR = 0x001A	x475001A	Vendor processing widget coefficient index	0x001A	Right start location = 32xSCLK, data = 24 bit
	9.2 Set right slot location = 32	x4740820		0x0820	
10	Enable TDM Pads				
	Step **Task**	**Verb**	**Register/Bit Fields**	**Payload**	**Description**
	10.1 Set VPW CIR = 0x0082	x4750082	Vendor processing widget coefficient index	0x0082	TDM pads enabled
	10.2 TDM pad enable, normal slew rate	x474FF00		0xFF00	
11	Set PLL2, PLL1 to 49.152 MHz, enable ASP clocks				
	Step **Task**	**Verb**	**Register/Bit Fields**	**Payload**	**Description**
	11.1 Set VPW CIR = 0x0001	x4750001	Vendor processing widget coefficient index	0x0001	PLL1, PLL2 = 49.152 MHz, ASP clocks ungated
	11.2 Set PLL1, PLL2 frequency; enable clocks	x4740060		0x0060	

5.3.3 Common SCLK Source and Divider Configurations

Table 5-2 gives reference values for bit fields in the vendor processing widget coefficient index registers for common ASP Fs and SCLK:FS configurations. ASPx_LCPR determines the SCLK:Fs ratio (e.g., 0x1FF selects 512 SCLK:Fs; see Table 6-172).

Note: For I²S Mode, additional CIRs must be programmed. ASPx_5050 must be set within CIR = 0x0005/8. The ASPxn_TX_RAP/LAP or ASPxn_RX_RAP/LAP bits must be opposite each other for each transmitter or receiver widget so that L/R data is clocked on each edge of LRCK.

Table 5-2. Settings for Common Configurations (SCLK in MHz)

Fs (kHz)	SCLK:Fs	fSCLK (MHz)	ASPx_SC_SRCSEL (See Table 6-172)	PLLx_FRQSEL (See Table 6-168)	ASPx_SCDIV (See Table 6-172	ASPx_LCPR (See Table 6-172)
96	512, 500, 384	Not supported				
	256	24.576	01 or 10 (PLLx)	000	001	0x0FF
	250	24.000	00 (BCLK)	—	000	0x0F9
	192	18.423	01 or 10 (PLLx)	010	001	0x0BF
	128	12.288	01 or 10 (PLLx)	000	010	0x07F
	125	12.000	00 (BCLK)	—	001	0x07C
	64	6.144	01 or 10 (PLLx)	000	011	0x03F
	48	4.608	01 or 10 (PLLx)	010	011	0x02F
	32	3.072	01 or 10 (PLLx)	000	100	0x01F
48	512	24.576	01 or 10 (PLLx)	000	001	0x1FF
	500	24.000	00 (BCLK)	—	000	0x1F3
	384	18.432	01 or 10 (PLLx)	010	001	0x17F
	256	12.288	01 or 10 (PLLx)	000	010	0x0FF
	250	12.000	00 (BCLK)	—	001	0x0F9
	192	9.216	01 or 10 (PLLx)	010	010	0x0BF
	128	6.144	01 or 10 (PLLx)	000	011	0x07F
	125	6.000	00 (BCLK)	—	010	0x07C
	64	3.072	01 or 10 (PLLx)	000	100	0x03F
	48	2.304	01 or 10 (PLLx)	010	100	0x02F
	32	1.536	01 or 10 (PLLx)	000	101	0x01F

Table 5-2. Settings for Common Configurations (SCLK in MHz) *(Cont.)*

Fs (kHz)	SCLK:Fs	fSCLK (MHz)	ASPx_SC_SRCSEL (See Table 6-172)	PLLx_FRQSEL (See Table 6-168)	ASPx_SCDIV (See Table 6-172	ASPx_LCPR (See Table 6-172)
44.1	512	22.579	01 or 10 (PLLx)	100	000	0x1FF
	500	22.050	01 or 10 (PLLx)	011	000	0x1F3
	384	16.934	01 or 10 (PLLx)	111	000	0x17F
	256	11.290	01 or 10 (PLLx)	100	001	0x0FF
	250	11.025	01 or 10 (PLLx)	011	001	0x0F9
	192	8.467	01 or 10 (PLLx)	111	001	0x0BF
	128	5.645	01 or 10 (PLLx)	100	010	0x07F
	125	5.513	01 or 10 (PLLx)	011	010	0x07C
	64	2.822	01 or 10 (PLLx)	100	011	0x03F
	48	2.117	01 or 10 (PLLx)	111	011	0x02F
	32	1.411	01 or 10 (PLLx)	100	100	0x01F
32	512	16.384	01 or 10 (PLLx)	110	000	0x1FF
	500	16.000	01 or 10 (PLLx)	101	000	0x1F3
	384	12.288	01 or 10 (PLLx)	000	010	0x17F
	256	8.192	01 or 10 (PLLx)	110	001	0x0FF
	250	8.000	01 or 10 (PLLx)	101	001	0x0F9
	192	6.144	01 or 10 (PLLx)	000	011	0x0BF
	128	4.096	01 or 10 (PLLx)	110	010	0x07F
	125	4.000	01 or 10 (PLLx)	101	010	0x07C
	64	2.048	01 or 10 (PLLx)	110	011	0x03F
	48	1.536	01 or 10 (PLLx)	000	101	0x02F
	32	1.024	01 or 10 (PLLx)	110	100	0x01F
24	512	12.288	01 or 10 (PLLx)	000	010	0x1FF
	500	12.000	00 (BCLK)	—	001	0x1F3
	384	9.216	01 or 10 (PLLx)	010	010	0x17F
	256	6.144	01 or 10 (PLLx)	000	011	0x0FF
	250	6.000	00 (BCLK)	—	010	0x0F9
	192	4.608	01 or 10 (PLLx)	010	011	0x0BF
	128	3.072	01 or 10 (PLLx)	000	100	0x07F
	125	3.000	00 (BCLK)	—	011	0x07C
	64	1.536	01 or 10 (PLLx)	000	101	0x03F
	48	1.152	01 or 10 (PLLx)	010	101	0x02F
	32	Not supported				
22.05	512	11.290	01 or 10 (PLLx)	100	001	0x1FF
	500	11.025	01 or 10 (PLLx)	011	001	0x1F3
	384	8.467	01 or 10 (PLLx)	111	001	0x17F
	256	5.645	01 or 10 (PLLx)	100	010	0x0FF
	250	5.513	01 or 10 (PLLx)	011	010	0x0F9
	192	4.234	01 or 10 (PLLx)	111	010	0x0BF
	128	2.822	01 or 10 (PLLx)	100	011	0x07F
	125	2.756	01 or 10 (PLLx)	011	011	0x07C
	64	1.411	01 or 10 (PLLx)	100	100	0x03F
	48	1.058	01 or 10 (PLLx)	111	100	0x02F
	32	Not supported				
16	512	8.192	01 or 10 (PLLx)	110	001	0x1FF
	500	8.000	01 or 10 (PLLx)	101	001	0x1F3
	384	6.144	01 or 10 (PLLx)	000	011	0x17F
	256	4.096	01 or 10 (PLLx)	110	010	0x0FF
	250	4.000	01 or 10 (PLLx)	101	010	0x0F9
	192	3.072	01 or 10 (PLLx)	000	100	0x0BF
	128	2.048	01 or 10 (PLLx)	110	011	0x07F
	125	2.000	01 or 10 (PLLx)	101	011	0x07C
	64	1.024	01 or 10 (PLLx)	110	100	0x03F
	48, 32	Not supported				

Table 5-2. Settings for Common Configurations (SCLK in MHz) *(Cont.)*

Fs (kHz)	SCLK:Fs	fSCLK (MHz)	ASPx_SC_SRCSEL (See Table 6-172)	PLLx_FRQSEL (See Table 6-168)	ASPx_SCDIV (See Table 6-172	ASPx_LCPR (See Table 6-172)
12	512	6.144	01 or 10 (PLLx)	000	011	0x1FF
	500	6.000	00 (BCLK)	—	010	0x1F3
	384	4.608	01 or 10 (PLLx)	010	011	0x17F
	256	3.072	01 or 10 (PLLx)	000	100	0x0FF
	250	3.000	00 (BCLK)	—	011	0x0F9
	192	2.304	01 or 10 (PLLx)	010	100	0x0BF
	128	1.536	01 or 10 (PLLx)	000	101	0x07F
	125	1.500	00 (BCLK)	—	100	0x07C
	64, 48, 32	Not supported				
11.025	512	5.645	01 or 10 (PLLx)	100	010	0x1FF
	500	5.513	01 or 10 (PLLx)	011	010	0x1F3
	384	4.234	01 or 10 (PLLx)	111	010	0x17F
	256	2.822	01 or 10 (PLLx)	100	011	0x0FF
	250	2.756	01 or 10 (PLLx)	011	011	0x0F9
	192	2.117	01 or 10 (PLLx)	111	011	0x0BF
	128	1.411	01 or 10 (PLLx)	100	100	0x07F
	125	1.378	01 or 10 (PLLx)	011	100	0x07C
	64, 48, 32	Not supported				
8	512	4.096	01 or 10 (PLLx)	110	010	0x1FF
	500	4.000	01 or 10 (PLLx)	101	010	0x1F3
	384	3.072	01 or 10 (PLLx)	000	100	0x17F
	256	2.048	01 or 10 (PLLx)	110	011	0x0FF
	250	2.000	01 or 10 (PLLx)	101	011	0x0F9
	192	1.536	01 or 10 (PLLx)	000	101	0x0BF
	128	1.024	01 or 10 (PLLx)	110	100	0x07F
	125	1.000	01 or 10 (PLLx)	101	100	0x07C
	64, 48, 32	Not supported				

5.3.4 Behavior When OUTE = 0 or INE = 0

If ASPx.n TX pin widget OUTE = 0 (see Table 6-109), the HD Audio interface passes all-zero data to the ASPx logic. If ASPx.n TX is enabled in the ASPx configuration and ASPx.n TX OUTE = 0, ASPx drives strong zero during the ASPx.n channel slots. The zero data passed when OUTE = 0 is not affected by null insert or remove configuration.

If ASPx.n RX pin widget INE = 0 (see Table 6-119), the HD Audio interface receives all-zero data from the ASPx logic. If ASPx.n input converter widget is streaming and ASPx.n RX INE = 0, the stream channels associated with ASPx.n are zero. The zero data passed when INE = 0 is not affected by null insert or remove configuration.

Note: Because the zero data created when either OUTE = 0 or INE = 0 is unaffected by null insert or remove configuration, care must be taken that attached devices (i.e., attached ASP slave or HD audio controller) do not overflow sample FIFOs, assuming that all-zero samples are valid isochronous data. All-zero samples appear as a valid samples in NFS Isochronous Mode.

5.3.5 Enable to Streaming Delay

The ASP requires up to six LRCK periods after it is enabled (ASPx_EN = 1 after ASPx_EN = 0) before it can read stream data from the HD Audio output widgets. If a valid stream and channel is assigned to an ASPx widget before the port is ready to stream data, the widget output FIFO may overflow. Therefore it is recommended to wait greater than six LRCK periods between enabling the port and assigning an input or output stream to an ASP widget.

The formula below gives the recommended minimum delay, in HD Audio frames, as a function of the ASP sample rate, Fs.

$$\text{Delay in HD Audio Frames} = 6\ (48\ \text{kHz})/F_S(\text{ASP})$$

5.3.6 Clock and Data Pin Status

The ASP port may operate as either a slave or master; furthermore, the ASP may be connected to a digital audio bus as a slave where all bus traffic flows between other devices (e.g., an external master and different slave device). The default power-on-reset configuration of the ASP port pins is a high-impedance output state with a weak pull down. The weak pull down holds the input path in a known state and prevents excess leakage through the input path. The weak pull down also ensures a stable bus condition even if no data streams are active.

Each output-capable ASP pin (ASPx_MCLK, ASPx_SCLK, ASPx_LRCK/FSYNC, and ASPx_SDOUT) has a dedicated pad driver enable control bit (see Table 6-173). Table 5-3 through Table 5-6 show how ASPx_MCLK, ASPx_SCLK, ASPx_LRCK/FSYNC, and ASPx_SDOUT behave with respect to their various controls.

Table 5-3. ASP MCLK Enable

ASPx_MCLK_EN (Table 6-216)	ASPx_SLV (Table 6-168)	ASPx_MCEN (Table 6-173)	ASPx.n TX OUTE [1] (Table 6-109)	ASPx.n RX INE[2] (Table 6-119)	ASPx_MCLK (Table 1-1)
0	x	x	x	x	Hi-Z [3]
1	x	0	x	x	Drive low
1	x	1	x	x	Active

1. Logical OR of all ASPx TX OUTE bits
2. Logical OR of all ASPx RX INE bits
3. The pad has a weak pull down

Table 5-4. ASP SCLK Enable

ASPx_SCLK_EN (Table 6-216)	ASPx_SLV (Table 6-168)	ASPx_EN (Table 6-168)	ASPx.n TX OUTE [1] (Table 6-109)	ASPx.n RX INE[2] (Table 6-119)	ASPx_SCLK (Table 1-1)
0	x	x	x	x	Hi-Z [3]
1	1	x	x	x	Hi-Z [3]
1	0	0	x	x	Drive low
1	0	1	x	x	Active

1. Logical OR of all ASPx TX OUTE bits
2. Logical OR of all ASPx RX INE bits
3. The pad has a weak pull down

Table 5-5. ASP LRCK/FSYNC Enable

ASPx_LRCK_EN (Table 6-216)	ASPx_SLV (Table 6-168)	ASPx_EN (Table 6-168)	ASPx.n TX OUTE [1] (Table 6-109)	ASPx.n RX INE[2] (Table 6-119)	ASPx_LRCK/FSYNC (Table 1-1)
0	x	x	x	x	Hi-Z [3]
1	1	x	x	x	Hi-Z [3]
1	0	0	x	x	Drive low
1	0	1	x	x	Active

1. Logical OR of all ASPx TX OUTE bits
2. Logical OR of all ASPx RX INE bits
3. The pad has a weak pull down

Table 5-6. ASP SDOUT Enable

ASPx_SDOUT_EN (Table 6-216)	ASPx_SLV (Table 6-168)	ASPx_EN (Table 6-168)	ASPx.n TX OUTE [1] (Table 6-109)	ASPx.n RX INE[2] (Table 6-119)	ASPx_SDOUT (Table 1-1)
0	x	x	x	x	Hi-Z [3]
1	x	0	x	x	Hi-Z [3,4]
1	x	1	0	x	Drive low [5]
1	x	1	1	x	Active

1. Logical OR of all ASPx TX OUTE bits
2. Logical OR of all ASPx RX INE bits
3. The pad has a weak pull down
4. When ASPx_EN is cleared, the port finishes transmitting any data currently in its output FIFO, after which the pad transitions to Hi-Z
5. Section 5.3.4 describes ASP behavior while OUTE = 0.

5.4 I²C Master Port

The I²C port is controlled through the following registers:

- The I²C address register (see Table 6-191) contains the 7-bit address of the slave device along with the read/write bit that determines the direction of data flow for the next transaction—except Quick Access Mode transactions. This register must be populated first, before initiating the transaction.
- The I²C data register (see Table 6-192) contains the 8-bit data value to be sent to the slave device for the next write transaction or the 8-bit data value received from the slave device from the last read. During an active I²C transaction, writing to this register immediately sends the 8-bit data packet to the slave device. This register is also embedded in the payload of any UR originating from the I²C block, eliminating the need for the host to manually read the data register. In a combined read or write transaction, the subaddress is written to the data register.
- The I²C control register (see Table 6-193) allows the host to set the speed mode for the next transaction, initiate START and STOP conditions, and specify the ACK or NACK bit to be sent to the slave transmitter. Writing to this register immediately generates a START or STOP condition or sends the ACK/NACK bit to the slave device. Only one of the 3 LSBs (start, stop, ACK/NACK) must be set when this register is written, otherwise unpredictable or undesirable behavior may result. The speed mode bit must be toggled only when a START condition is generated. All other writes to the I²C control register must maintain the previous state of the speed mode bit.
- The I²C status register (see Table 6-194) conveys the status of the I²C state machine to the host. Most importantly, it indicates when a pending transaction has been completed and the I²C engine needs attention or is can receive new commands. If either ACK ready, write ready, or read ready transition from 0 to 1, a UR with the current status and read data embedded in its payload is generated (if so configured). This eliminates a need for the host to poll the status register. Any write to the I²C control or I²C data register clears ACK ready, write ready, and read ready. If ACK status is received as 0 (NACK), the host generates a STOP condition and terminates the transaction.
- The I²C quick write register (see Table 6-195) contains the I²C register subaddress (I2C_QWSA) and data byte (I2C_QWD) to be written in an I²C quick write transaction.
- The I²C quick read register (see Table 6-196) contains the I²C register subaddress (I2C_QRSA) to be read in the next I²C quick read transaction, as well as the data byte (I2C_QRD) read in the last I²C quick read transaction.

5.5 SPI Master Port

The SPI port is controlled through the following registers:

- The SPI control register (CIR 0x005F in the Vendor Processing Widget, see Section 6.11.8.11) allows the host to set the polarity, clock frequency, and byte count of the SPI transaction. It also selects the slave device to activate during the transaction. Note that the byte count should be adjusted depending on the SPI slave device.
- The SPI data Tx/Rx registers (CIR 0x0060 and 0x0061 in the Vendor Processing Widget, see Table 6-199 and Table 6-200) contain the 16-bit value to be sent to the slave device for the next write transaction or the 16-bit data value received from the slave device from the last read. Writing to the transmit data register immediately sends the 16-bit data packet to the slave device.
- The SPI status register (CIR 0x0062 in the Vendor Processing Widget, see Table 6-201) contains information that conveys the status of the SPI state machine to the host. It relays the current state of the transaction, as well as how many bytes have been transferred in the current transaction.

Notes: CIR 0x0000 and 0x0002 must also be set to enable SPI Master clock and to configure the GPIOs so they are used for SPI functionality, respectively.

In a system that uses multiple SPI slave devices, any GPIOx/$\overline{\text{CSx}}$ pins must be used only as the SPI chip selects and not for GPIO functionality. GPIO/SPI pins are weakly pulled down when configured as GPIO pins and are not being driven. So, in a system with two SPI slave devices, this can create an error condition. If any GPIOx/$\overline{\text{CSx}}$ pin is set to GPIO Mode, the respective pin goes low. This can be mistaken by the SPI1/SPI2 slave device as an active low, in which case it may drive data during a transaction intended for the other SPI device, because they share the same MOSI and CLK.

5.6 Power Supply Sequencing

No specific power sequence is required to prevent an excess supply leakage scenario or to guarantee power-on reset operation. If possible, it is recommended to meet the following sequence guidelines for lowest supply leakage:

- VL_SP (1.8 V) turned on before VL_HD.
- VL_DM (1.8 V or 3.3 V) turned on before VL_HD.
- VL_HD (1.5 V) turned off before VL_SP and VL_DM.

Fig. 5-4 illustrates this sequence.

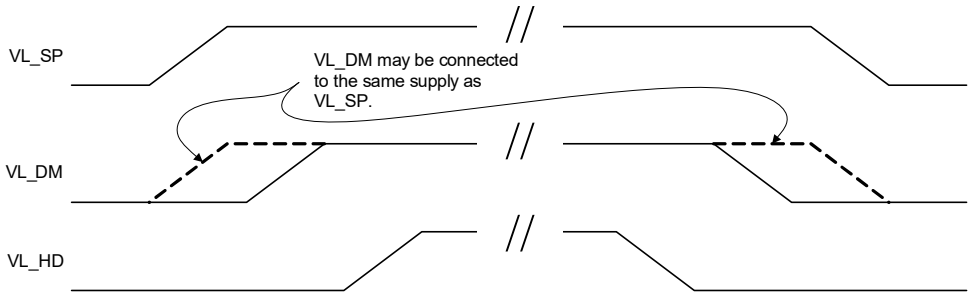


Figure 5-4. Power Supply Sequencing

All supplies are always required for normal operation.

5.7 Digital Sound Processing

Signal processing can be applied to the ASP render paths by using the parametric filter engine register block in of the vendor processing widget described in Section 6.11.8.12. The digital sound-processing block combines a prescaler and two-band parametric filter engine into a single processing chain that can be inserted into the render signal path between the HD Audio block and the two ASP outputs. The processing blocks are split into two eight-channel EQs. EQ1 is used by ASP1, EQ2 is used by ASP2. Processing is applied to channel pairs: channels 0/1, 2⁄3, 4/5, and 6/7 for each ASP output. Note that the DSP is not applied to ASP channels that use a loopback path (non-HDA bus) as a data source selected from the internal loopback control registers, described in Section 6.11.8.13.

5.7.1 Prescaler

Applying any gain to a full-scale signal in the digital domain causes the signal to clip. To prevent this, a prescaler block is included prior to the internal digital signal processing blocks. This allows the input signal to be attenuated before processing to ensure that any signal boosting, such as gain in a shelving filter, does not cause a channel to clip.

The prescaler block allows up to –15.0 dB of attenuation in 1.0-dB increments and is controlled with the prescale attenuation bits in the EQx prescale attenuation registers of the vendor processing widget, described in Section 6.11. The prescaler values apply to channel pairs—channels 0/1, 2/3, 4/5, and 6/7 for each ASP output.

5.7.2 EQ Bypass

When EQ coefficients are accessed, the EQ block should be bypassed in the data path so no noises are audible if coefficients are updated. Also, after the CS8409 is powered up, the coefficient values are random (the coefficient RAM is not cleared after power up) so the EQ should be bypassed until after the coefficient values are written. Several bits determine whether the EQ is placed in the data path or is bypassed. Bypass behavior does not rely on the state of the EQ write coefficient bit (Table 6-204), since it applies while reading or writing coefficients. Fig. 5-5 and Table 5-7 show the EQ data path bypass logic. The bypass decision is made independently for each channel pair in each bank.

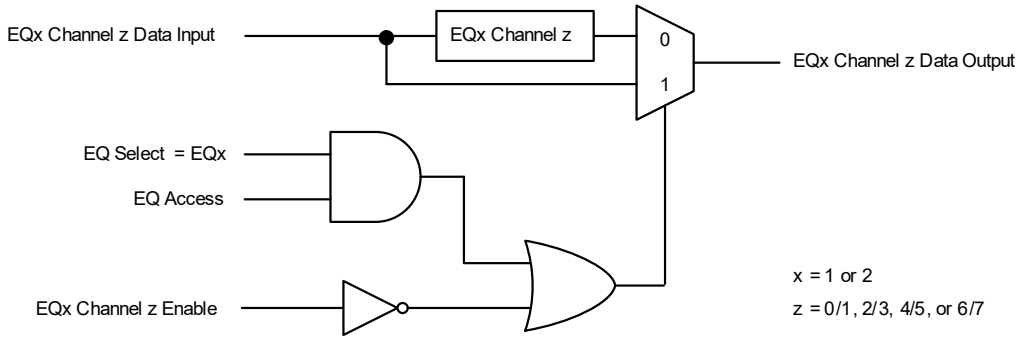


Figure 5-5. EQ Bypass Logic

Table 5-7. EQ Bypass Truth Table

EQ Select = EQx (Table 6-205)	EQ Access (Table 6-204)	EQx Channel z Enable (Table 6-205)	EQ Bypassed?	State
x	0	0	Yes	1. Normal operation, EQ off
x	1	0	Yes	2. Intermediate state
1	1	1	Yes	3. Read/Write coefficients
0	1	1	No	4. Read/Write to other EQ bank
x	0	1	No	5. Normal operation, EQ on

Note the following:

- For the initial coefficient write, the state sequence should be: 1, 2, 3, 4 (optional), then 5.
- For subsequent read/writes, the state sequence should be from 5 to 3, 4 (optional), then 5.
- To disable the EQ block, change from State 5 to 1 (clear the EQ enable bit).
- For a case where one EQ bank needs to be written to or read from while another EQ bank is streaming audio data, make sure to change the EQ select bits to the nonstreaming EQ bank before setting the EQ access bit to prevent the streaming EQ bank from entering a bypassed state.

6 HD Audio Codec Supported Verbs and Responses

6.1 Codec Node Topology

Fig. 6-1 shows the codec node topology.

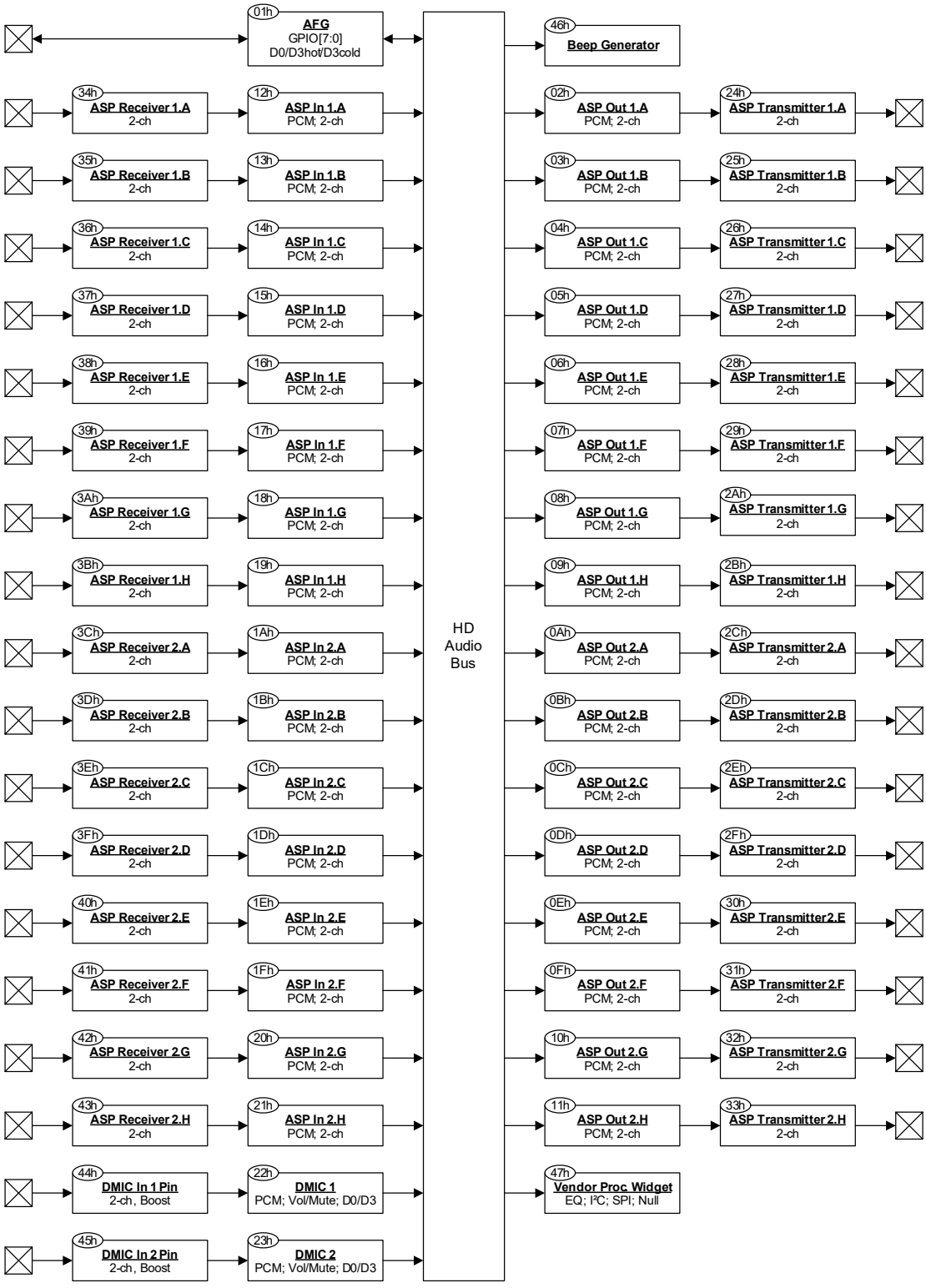


Figure 6-1. Codec Node Topology Diagram

6.1.1 Node ID Summary

Table 6-1. Device Node ID Summary

Node ID	Description	Reference Section
0x00	Root node	Section 6.2
0x01	Audio function group (AFG)	Section 6.3
0x02–0x11	ASP 1–2 output converter widgets	Section 6.4
0x12–0x21	ASP 1–2 input converter widgets	Section 6.5
0x22–0x23	DMIC 1–2 input converter widgets	Section 6.6
0x24–0x33	ASP transmitter 1–2 pin widgets	Section 6.7
0x34–0x43	ASP receiver 1–2 pin widgets	Section 6.8
0x44–0x45	DMIC 1–2 pin widgets	Section 6.9
0x46	Beep generator widget	Section 6.10
0x47	Processing widget	Section 6.11

6.1.2 Pin Configuration Register Defaults

The configuration default register**,** required for each pin widget, is used by software as an aid in determining the configuration of jacks and devices attached to the codec. When the codec is powered on, this register is internally loaded with default values, see Table 6-2, indicating the typical system use of this particular pin/jack. After this initial loading, the state, including any software writes into the register, are preserved across reset events. Its state need not be preserved across power-level changes.

Table 6-2. Pin Configuration Register Defaults

Node	Port	Location	Device	Type	Color	Miscellaneous	Association	Sequence
ASP 1.A–1.H Tx Node ID = 0x24–0x2B (see p 74)	n/c	External N/A	HP Out	Combo jack	Gray	No PDC override	F	0
ASP 2.A–2.H Tx Node ID = 0x2C–0x33 (see p 74)	n/c	Internal N/A	Speaker	Unknown	Unknown	No PDC override	F	0
ASP 1.A–1.H Rx Node ID = 0x34–0x3B (see p 76)	n/c	External N/A	Mic In	Combo Jack	Gray	No PDC override	F	0
ASP 2.A–2.H Rx Node ID = 0x3C–0x43 (see p 76)	n/c	Internal N/A	Aux In	Unknown	Unknown	No PDC override	F	0
DMIC 1–2 Node ID = 0x44–0x45 (see p 78)	n/c	Internal N/A	Mic In	Unknown	Unknown	No PDC override	F	0

6.1.3 Stream Format Structure

The stream format structure is a common construct used with the converter format control, which is mandatory for each input and output converter widget. The converter format control determines the format the converter uses. This must match the format programmed into the stream descriptor on the controller so that the data format sent on the link matches what is expected by the consumer of the data. This control must be changed only while the stream is inactive (stream number is zero) for the corresponding converter widget. Stream format includes all HD Audio–defined controls, the presence of a capability in the stream format structure does not imply capability beyond the those described by the Supported PCM Size and Rates verb (e.g., CS8409 converter widgets do not support 8-bit samples or a 192-kHz sample rate).

Table 6-3. Stream Format Structure

Bits	Type	Default	Description
31:16	Read only	0x0000	Reserved
15	Read/write	0	Stream type (TYPE). If TYPE is nonzero, the other bits in the format structure have other meanings. 0 PCM 1 Non-PCM
14	Read/write	0	Sample base rate (BASE) 0 48 kHz 1 44.1 kHz

Table 6-3. Stream Format Structure *(Cont.)*

Bits	Type	Default	Description
13:11	Read/write	000	Sample base rate multiple (MULT) 000 48 kHz/44.1 kHz or less 001 x2 (96 kHz, 88.2 kHz, 32 kHz) 010 x3 (144 kHz) 011 x4 (192 kHz, 176.4 kHz) 100–111 Reserved
10:8	Read/write	000	Sample base rate divisor (DIV) 000 Divide by 1 (48 kHz, 44.1 kHz) 001 Divide by 2 (24 kHz, 22.05 kHz) 010 Divide by 3 (16 kHz, 32 kHz) 011 Divide by 4 (11.025 kHz) 100 Divide by 5 (9.6 kHz) 101 Divide by 6 (8 kHz) 110 Divide by 7 111 Divide by 8 (6 kHz)
7	Read only	0	Reserved
6:4	Read/write	000	Bits per sample (BITS). Number of bits in each sample: 000 8 bits 001 16 bits 010 20 bits 011 24 bits 100 32 bits 101–111Reserved
3:0	Read/write	0000	Number of channels (CHAN). Number of channels in each frame of the stream: 0000 1 0001 2 … 1111 16

6.2 Root Node (Node ID = 0x00)

6.2.1 Vendor and Device ID

Table 6-1. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x00	Verb ID = 0xF00	Parameter ID = 0x00

Table 6-2. Response Format

Bits	Type	Default	Description
31:16	Read only	0x1013	Vendor ID (VID). Cirrus Logic PCI vendor ID
15:0	Read only	0x8409	Device ID (DID). CS8409 device ID

6.2.2 Revision ID

Table 6-3. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x00	Verb ID = 0xF00	Parameter ID = 0x02

Table 6-4. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Reserved
23:20	Read only	0x1	Major revision (MAJREV) of the HDA Spec
19:16	Read only	0x0	Minor revision (MINREV) of the HDA Spec
15:8	Read only	x	Revision ID (REVID). Indicates the letter rev used for all-layer changes. REVID and SID form the complete device revision ID (e.g., A0, B2). 0x01 Rev. A 0x02 Rev. B … 0x06 Rev. F
7:0	Read only	x	Stepping ID (SID). Indicates the number rev used for metal-layer changes. REVID and SID form the complete device revision ID (e.g., A0, B2). 0x00 Stepping Rev. 0 0x01 Stepping Rev. 1 … 0x0F Stepping Rev. 15

6.2.3 Subordinate Node Count

Table 6-5. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x00	Verb ID = 0xF00	Parameter ID = 0x04

Table 6-6. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Reserved
23:16	Read only	0x01	Starting node number (SNN). 1

Table 6-6. Response Format *(Cont.)*

Bits	Type	Default	Description
15:8	Read only	0x00	Reserved
7:0	Read only	0x01	Total number of nodes (TNN). 1

6.3 Audio Function Group (Node ID = 0x01)

6.3.1 Subordinate Node Count

Table 6-7. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF00	Parameter ID = 0x04

Table 6-8. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Reserved
23:16	Read only	0x02	Starting node number (SNN). 2
15:8	Read only	0x00	Reserved
7:0	Read only	0x46	Total number of nodes (TNN). 70

6.3.2 Function Group Type

Table 6-9. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF00	Parameter ID = 0x05

Table 6-10. Response Format

Bits	Type	Default	Description
31:9	Read only	0	Reserved
8	Read only	1	Unsolicited capable (UC). UR is supported on this node
7:0	Read only	0x01	Node type (NT). Audio function group

6.3.3 Audio Function Group Capabilities

Table 6-11. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF00	Parameter ID = 0x08

Table 6-12. Response Format

Bits	Type	Default	Description
31:17	Read only	0	Reserved
16	Read only	1	Beep gen. Beep generator is present
15:12	Read only	0x0	Reserved
11:8	Read only	0x0	Input delay. Reported as 0, since each widget should be queried for the actual value
7:4	Read only	0x0	Reserved
3:0	Read only	0x0	Output delay. Reported as 0, since each widget should be queried for the actual value

6.3.4 Supported PCM Size, Rates

Table 6-13. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF00	Parameter ID = 0x0A

Table 6-14. Response Format

Bits	Type	Default	Description
31:21	Read only	0x00	Reserved

Table 6-14. Response Format *(Cont.)*

Bits	Type	Default	Description
20	Read only	1	32-bit (32B). 32-bit audio format is supported.
19	Read only	1	24-Bit (24B). 24-bit audio format is supported.
18	Read only	0	20-Bit (20B). 20-bit audio format is not supported.
17	Read only	1	16-Bit (16B). 16-bit audio format is supported.
16	Read only	0	8-Bit (8B). 8-bit audio format is not supported.
15:12	Read only	0x0	Reserved
11	Read only	0	Rate-12 (R12). 384-kHz rate is not supported.
10	Read only	0	Rate-11 (R11). 192.0-kHz rate is not supported.
9	Read only	0	Rate-10 (R10). 176.4-kHz rate is not supported.
8	Read only	1	Rate-9 (R9). 96.0-kHz rate is supported.
7	Read only	0	Rate-8 (R8). 88.2-kHz rate is not supported.
6	Read only	1	Rate-7 (R7). 48.0-kHz rate is supported.
5	Read only	1	Rate-6 (R6). 44.1-kHz rate is supported.
4	Read only	1	Rate-5 (R5). 32.0-kHz rate is supported.
3	Read only	1	Rate-4 (R4). 22.05-kHz rate is supported.
2	Read only	1	Rate-3 (R3). 16.0-kHz rate is supported
1	Read only	1	Rate-2 (R2). 11.025-kHz rate is supported.
0	Read only	1	Rate-1 (R1). 8.0-kHz rate is supported.

6.3.5 Supported Stream Formats

Table 6-15. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF00	Parameter ID = 0x0B

Table 6-16. Response Format

Bits	Type	Default	Description
31:3	Read only	0	Reserved
2	Read only	0	AC-3 (AC3). AC-3 data is not supported.
1	Read only	0	Float32 (FLT32). Float32 formatted data is not supported.
0	Read only	1	Pulse code modulation (PCM). PCM formatted data is supported.

6.3.6 Supported Power States

Table 6-17. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF00	Parameter ID = 0x0F

Table 6-18. Response Format

Bits	Type	Default	Description
31	Read only	1	EPSS. Extended power states are supported
30	Read only	1	CLKSTOP. Function group supports D3 operation even if no BCLK is present on the link. See description below.
29	Read only	1	S3D3coldSup. Software should place the codec in D3cold state when the platform is entering S3 state
28:5	Read only	0	Reserved
4	Read only	1	D3coldSup. D3cold operation is supported
3	Read only	1	D3Sup. D3hot operation is supported
2	Read only	0	D2Sup. D2 operation is not supported
1	Read only	0	D1Sup. D1 operation is not supported
0	Read only	1	D0Sup. D0 operation is supported

CLKSTOP is defined only at the function group level (not at the widget level) and indicates that the function group and all widgets under it support D3 operation, even if no BCLK present is on the link. The maximum exit time back to fully functional is 10 ms from the time the clock begins operation and a codec address cycle completes. The CLKSTOP capability extends the required functionality for D3 support while the link is operational to include the following:

- Reporting of presence detect state changes, if enabled and supported by the pin widget, even if the Link Clock is not running (controller low-power state) or is currently in a link reset condition.
- Presence state changes occurring during link reset are deferred until after the reset sequence completes. Presence state change URs, if enabled, are not lost because the link clock stops or if link resets are generated before the UR for the state change has been returned to the host.
- Reporting of ClkStopOk when stopping of the clock would be permitted. The CLKSTOP is a static capability with ClkStopOk a dynamic reporting. Setting the capability CLKSTOP to 1 and not allowing the clock to stop by not reporting ClkStopOk is not permissible. Unless there is a condition or dependency that the host software cannot be made aware of that would prohibit stopping the clock, the ClkStopOk is reported as set. Host software is expected to poll the ClkStopOk before stopping the clock if the CLKSTOP is reported as being set.

6.3.7 GPIO Capabilities

Table 6-19. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF00	Parameter ID = 0x11

Table 6-20. Response Format

Bits	Type	Default	Description
31	Read only	1	GPIOWake. Wake functionality is supported.
30	Read only	1	GPIOUnsol. UR functionality is supported.
29:24	Read only	0	Reserved
23:16	Read only	0x00	NumGPIs. No dedicated GPI pins.
15:8	Read only	0x00	NumGPOs. AFG supports no GPO pins.
7:0	Read only	0x08	NumGPIOs. AFG supports 8 GPIO pins.

6.3.8 Power States

Table 6-21. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF05	Payload = 0x00

Table 6-22. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0x705	Payload = 0xXX

Table 6-23. Response Format

Bits	Type	Default	Description
31:11	Read only	0	Reserved
10	Read only	1	Power state settings reset (PS-SettingsReset). Set when, during any type of reset or low-power state transition, the settings that were changed from the defaults, either by software or hardware, have been reset to their default state. When these settings have not been reset, this is reported as 0. This bit is always set after a POR condition. See Section 4.10. This bit is cleared when read by a Get Parameter command.
9	Read only	1	Power state clock stop OK (PS-ClkStopOK). Set when the codec can continue proper operation, even if the HD audio bus BCLK has stopped. This bit is reported only at the AFG level and is reserved at the widget level. After accepting a low-power state transition request (D3 state) to the AFG node, the codec begins ramping down all the audio converters. During this time, PS-ClkStopOK is cleared, to indicate that the bus BCLK cannot be stopped. After all converters have ramped down, the codec updates PS-Act to reflect the actual transition to the D3 state. It then sets PS-ClkStopOk, to report the ability of the codec to operate correctly while in the low-power state with BCLK stopped. While in the low-power D3 state, and with the bus BCLK stopped, the pin widgets of the codec that were enabled to support URs continue to operate.
8	Read only	0	Power state error (PS-Error). Not supported and always returns 0 when read. The power state requested by software is always possible after a reasonable time required to execute the power state transition. There are no dependencies unknown to software between nodes that would inhibit transitioning to the requested power state.
7:4	Read only	0x3	Power state actual (PS-Act). Indicates the node's actual power state. Within the AFG node, this field is always equal to the PS-Set field (modulo the time required to execute a power state transition). The default state is D3hot.

Table 6-23. Response Format *(Cont.)*

Bits	Type	Default	Description
3:0	Read/write	0x3	Power state set (PS-Set). Defines the referenced node's current power setting. Since this node is an AFG node, the actual power state is this setting. Setting this field to the D3 state for the AFG node forces all other nodes with power state control to the D3 state. If the power state field for this node is set to D0, the individual power state for each converter is uniquely controlled via the corresponding node power state field. Writes to these bits set the AFG to the power state: PSS = 0000; D0—Fully on PSS = 0010; D2—Not supported PSS = 0100; D3cold—Supported PSS = 0001; D1—Not supported PSS = 0011; D3hot—Supported [1]

1. If the AFG is in this power state, only commands in the AFG and the power state command in other nodes have write access.

6.3.9 Unsolicited Response Control

Note: This control refers to the generic GPIO Unsolicited Response as defined in the HD Audio specification. See Section 6.3.10 for unique GPIO UR controls.

Table 6-24. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF08	Payload = 0x00

Table 6-25. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0x708	Payload = 0xXX

Table 6-26. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7	Read/write	0	Enable. Controls the actual generation of URs 0 Disable 1 Enable
6	Read only	0	Reserved
5:0	Read/write	0	Tag. Value assigned and used by software to determine what codec node generated the UR. The value programmed into the tag field is returned in the top 6 bits (31:26) of every UR generated by this node.

Note: Bits [31:0] are sticky and are not reset by a link reset or a function group reset.

Table 6-27. Unsolicited Response Format

Bits [31:26]	Bits [25:21]	Bits [20:8]	Bits [7:0]
Tag	Sub Tag (0_0000)	Reserved	GPIO[7:0] Data

6.3.10 GPIO[7:0] Unsolicited Response Control

Note: This is control refers to the unique GPIO Unsolicited Response that may take priority over the generic GPIO UR defined in the HD Audio specification. See Section 6.3.9 for HD Audio–defined GPIO UR controls.

Table 6-28. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xFF0 Verb ID = 0xFF1 Verb ID = 0xFF2 Verb ID = 0xFF3 Verb ID = 0xFF4 Verb ID = 0xFF5 Verb ID = 0xFF6 Verb ID = 0xFF7	GPIO0: Payload = 0x00 GPIO1: Payload = 0x00 GPIO2: Payload = 0x00 GPIO3: Payload = 0x00 GPIO4: Payload = 0x00 GPIO5: Payload = 0x00 GPIO6: Payload = 0x00 GPIO7: Payload = 0x00

Table 6-29. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0x7F0 Verb ID = 0x7F1 Verb ID = 0x7F2 Verb ID = 0x7F3 Verb ID = 0x7F4 Verb ID = 0x7F5 Verb ID = 0x7F6 Verb ID = 0x7F7	GPIO0: Payload = 0xxx GPIO1: Payload = 0xxx GPIO2: Payload = 0xxx GPIO3: Payload = 0xxx GPIO4: Payload = 0xxx GPIO5: Payload = 0xxx GPIO6: Payload = 0xxx GPIO7: Payload = 0xxx

Table 6-30. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7	Read/write	0	Enable. Controls the actual generation of URs 0 Disable 1 Enable
6	Read only	0	Reserved
5:0	Read/write	0	Tag. Value assigned and used by software to determine what codec node generated the UR. The value programmed into the tag field is returned in the top 6 bits (31:26) of every UR generated by this node.

Note: Bits [31:0] are sticky and are not reset by a link reset or a function group reset.

Table 6-31. Unsolicited Response Format

Bits [31:26]	Bits [25:21]	Bits [20:8]	Bits [7:0]
Tag	Sub Tag (0_0000)	Reserved	GPIO[7:0] Data

6.3.11 GPIO Data

Table 6-32. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF15	Payload = 0x00

Table 6-33. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0x715	Payload = 0xXX

Table 6-34. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7:0	Read/write	0x00	GPIO[7:0] data. For GPIO pins programmed as inputs, this value is read only and is the sensed value on the corresponding pin. For GPIO programmed as outputs, the value written is driven onto the corresponding pin. **Note:** If the corresponding GPIO enable mask control bit (Table 6-37) is not set, pins configured as outputs do not drive the associated bit value (because the pin must be in a Hi-Z state), but the value returned on a read still reflects the value that would be driven if the pin were to be enabled in the GPIO enable mask control.

6.3.12 GPIO Enable Mask

Table 6-35. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF16	Payload = 0x00

Table 6-36. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0x716	Payload = 0xXX

Table 6-37. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7:0	Read/write	0x00	GPIO[7:0] enable mask. If the bit associated with a pin is 0, the pin is disabled and in a Hi-Z state. If the bit is set, the GPIO pin is enabled and the pin's behavior is determined by the GPIO direction control.

6.3.13 GPIO Direction

Table 6-38. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF17	Payload = 0x00

Table 6-39. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0x717	Payload = 0xXX

Table 6-40. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7:0	Read/write	0x00	GPIO[7:0] direction. If a bit is a 0, the associated GPIO signal is configured as an input. If a bit is a 1, the associated GPIO signal is configured as an output.

6.3.14 GPIO Wake Enable Mask

Table 6-41. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF18	Payload = 0x00

Table 6-42. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0x718	Payload = 0xXX

Table 6-43. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7:0	Read/write	0x00	GPIO[7:0] wake enable mask. Controls whether a change on an input pin generates a wake event when the link is powered down. If the bit associated with an input pin is 0, no wake event is generated. If the bit is a 1, a wake event is generated.

6.3.15 GPIO Unsolicited Enable Mask

Table 6-44. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF19	Payload = 0x00

Table 6-45. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0x719	Payload = 0xXX

Table 6-46. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7:0	Read/write	0x00	GPIO[7:0] unsolicited enable mask. Controls whether a change on an input pin generates a UR when the link is powered up. If the bit associated with an input pin is 0, no UR is generated. If the bit is a 1, a UR is generated.

6.3.16 GPIO Sticky Mask

Table 6-47. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF1A	Payload = 0x00

Table 6-48. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0x71A	Payload = 0xXX

Table 6-49. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7:0	Read/write	0x00	GPIO[7:0] sticky mask. Defines GPIO input type (0 = not sticky, 1 = sticky) when a GPIO pin is configured as an input. GPIO inputs configured as sticky are cleared by writing a 0 to the corresponding bits of the GPIO data control (see Table 6-34) and by reset. The default, 00_0000, is all pins not sticky. Unimplemented GPIO pins always return zeros. Sticky is defined as edge sensitive; not sticky is defined as level sensitive.

6.3.17 Implementation Identification

This field provides the board implementation and assembly IDs of the functional group to software. It is a read/write-once register; BIOS writes to this field to configure the board implementation and assembly IDs during the boot process.

Table 6-50. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0xF20	Payload = 0x00

Table 6-51. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0x720 Verb ID = 0x721 Verb ID = 0x722 Verb ID = 0x723	Payload = 0xXX (IID bits [7:0]) Payload = 0xXX (IID bits [15:8]) Payload = 0xXX (IID bits [23:16]) Payload = 0xXX (IID bits [31:24])

Table 6-52. Response Format

Bits	Type	Default	Description
31:16	Read/write once	0x1013	Board manufacturer identification (BMID). Contains the PCI Vendor ID of the board manufacturer. Preset to Cirrus Logic's PCI Vendor ID.
15:8	Read/write once	0x84	Board SKU (BSKU). Assigned by the board manufacturer to identify the specific board design. Preset to 0x84 for Cirrus Logic digital interface devices.
7:0	Read/write once	0x09	Assembly ID (AssyID). Uniquely identifies the specific board assembly. Preset to 0x09 for the CS8409 AFG.

6.3.18 Function Reset

Function reset is an execute verb. No physical register is associated with the function reset. See the *High Definition Audio Specification*, listed in Section 10.

Table 6-53. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x01	Verb ID = 0x7FF	Payload = 0x00

6.4 ASP Output Converter Widgets (Node ID = 0x02–0x11)

6.4.1 Audio Widget Capabilities

Table 6-54. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Output Node ID = 0x02–0x09 ASP2 Output Node ID = 0x0A–0x11	Verb ID = 0xF00	Parameter ID = 0x09

Table 6-55. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Reserved
23:20	Read only	0x0	Type (TYP). Audio output converter widget
19:16	Read only	0x6	Delay (DLY). Indicates the number of sample delays through the widget.
15:13	Read only	000	Channel count extension (CCE). With CCL, indicates that this widget supports two channels.
12	Read only	0	CP caps (CPC). Widget does not support content protection.
11	Read only	0	L–R swap (LRS). This widget cannot swap the left and right channels.
10	Read only	0	Power control (PC). This widget supports power state control.
9	Read only	0	Digital (DIG). This widget is not a digital widget.
8	Read only	0	Connection list (CL). A connection list is not present on this widget.
7	Read only	0	Unsolicited capable (UC). UR is not supported on this widget.
6	Read only	0	Processing widget (PW). This widget does not support the processing capabilities parameter.
5	Read only	0	Stripe (STRP). Striping is not supported.
4	Read only	0	Format override (FO). This widget contains its own format parameters.
3	Read only	0	Amplifier parameter override (APO). This widget does not contain amplifier parameters.
2	Read only	0	Output amplifier present (OAP). Output amplifier is not present for this widget.
1	Read only	0	Input amplifier present (IAP). Input amplifier is not present for this widget.
0	Read only	1	Channel count LSB (CCL). With CCE, indicates that this widget supports two channels.

6.4.2 Converter Stream, Channel

Table 6-56. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Output Node ID = 0x02–0x09 ASP2 Output Node ID = 0x0A–0x11	Verb ID = 0xF06	Payload = 0x00

Table 6-57. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Output Node ID = 0x02–0x09 ASP2 Output Node ID = 0x0A–0x11	Verb ID = 0x706	Payload = 0xXX

Table 6-58. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7:4	Read/write	0x0	Stream number (SN). Written by software to indicate the stream number used by the output converter. 0x0 is Stream 0, 0x1 is Stream 1, etc. By convention, Stream 0 is reserved and unused, so the converter whose stream number has been cleared does not unintentionally decode data not intended for it.
3:0	Read/write	0x0	Lowest channel number (LCN). Written by software to indicate the lowest channel used by the output converter.

While the converter node is in the D3 power state, this parameter is read only (set parameter commands are ignored). As shown in Table 4-4, the parameter values are reset to default (SN = 0, LCN = 0) at power state transitions, thus the parameter can be configured only while the converter node power state is D0.

6.4.3 Converter Format

Table 6-59. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	ASP1 Output Node ID = 0x02–0x09 ASP2 Output Node ID = 0x0A–0x11	Verb ID = 0xA	Payload = 0x0000

Table 6-60. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	ASP1 Output Node ID = 0x02–0x09 ASP2 Output Node ID = 0x0A–0x11	Verb ID = 0x2	Payload = 0xXXXX

See Section 6.1.3 for the definition of the stream format structure.

6.5 ASP Input Converter Widgets (Node ID = 0x12–0x21)

6.5.1 Audio Widget Capabilities

Table 6-61. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Input Node ID = 0x12–0x19 ASP2 Input Node ID = 0x1A–0x21	Verb ID = 0xF00	Parameter ID = 0x09

Table 6-62. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Reserved
23:20	Read only	0x1	Type (TYP). Audio input converter widget
19:16	Read only	0x6	Delay (DLY). Indicates the number of sample delays through the widget.
15:13	Read only	000	Channel count extension (CCE). With CCL, indicates that this widget supports two channels.
12	Read only	0	CP caps (CPC). Widget does not support content protection.
11	Read only	0	L–R swap (LRS). This widget cannot swap the left and right channels.
10	Read only	0	Power control (PC). This widget supports power state control.
9	Read only	0	Digital (DIG). This widget is not a digital widget.
8	Read only	1	Connection list (CL). A connection list is present on this widget.
7	Read only	0	Unsolicited capable (UC). UR is not supported on this widget.
6	Read only	0	Processing widget (PW). This widget does not support the processing capabilities parameter.
5	Read only	0	Stripe (STRP). Striping is not supported.
4	Read only	0	Format override (FO). This widget contains its own format parameters.
3	Read only	0	Amplifier parameter override (APO). This widget does not contain amplifier parameters.
2	Read only	0	Output amplifier present (OAP). Output amplifier is not present for this widget.
1	Read only	0	Input amplifier present (IAP). Input amplifier is not present for this widget.
0	Read only	1	Channel count LSB (CCL). With CCE, indicates that this widget supports two channels.

6.5.2 Connection List Length

Table 6-63. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Input Node ID = 0x12–0x19 ASP2 Input Node ID = 0x1A–0x21	Verb ID = 0xF00	Parameter ID = 0x0E

Table 6-64. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved

Table 6-64. Response Format *(Cont.)*

Bits	Type	Default	Description
7	Read only	0	Long form (LF). Connection list is short form.
6:0	Read only	000_0001	Connection list length (CLL). A single hard-wired input is available for this widget.

6.5.3 Connection List Entry

Table 6-65. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Input Node ID = 0x12–0x19 ASP2 Input Node ID = 0x1A–0x21	Verb ID = 0xF02	Payload = N = 0xXX

Table 6-66. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Connection list entry (N+3). Returns 0x00 for N = 0x00–0x03 or N > 0x03.
23:16	Read only	0x00	Connection list entry (N+2). Returns 0x00 for N = 0x00–0x03 or N > 0x03.
15:8	Read only	0x00	Connection list entry (N+1). Returns 0x00 for N = 0x00–0x03 or N > 0x03.
7:0	Read only	NID = 0x12: 0x34 NID = 0x13: 0x35 NID = 0x14: 0x36 NID = 0x15: 0x37 NID = 0x16: 0x38 NID = 0x17: 0x39 NID = 0x18: 0x3A NID = 0x19: 0x3B NID = 0x1A: 0x3C NID = 0x1B: 0x3D NID = 0x1C: 0x3E NID = 0x1D: 0x3F NID = 0x1E: 0x40 NID = 0x1F: 0x41 NID = 0x20: 0x42 NID = 0x21: 0x43	Connection List Entry (N). ASP 1.A. Returns 0x34 (ASP In 1.A) for N = 0x00–0x03. ASP 1.B. Returns 0x35 (ASP In 1.B) for N = 0x00–0x03. ASP 1.C. Returns 0x36 (ASP In 1.C) for N = 0x00–0x03. ASP 1.D. Returns 0x37 (ASP In 1.D) for N = 0x00–0x03. ASP 1.E. Returns 0x38 (ASP In 1.E) for N = 0x00–0x03. ASP 1.F. Returns 0x39 (ASP In 1.F) for N = 0x00–0x03. ASP 1.G. Returns 0x3A (ASP In 1.G) for N = 0x00–0x03. ASP 1.H. Returns 0x3B (ASP In 1.H) for N = 0x00–0x03. ASP 2.A. Returns 0x3C (ASP In 2.A) for N = 0x00–0x03. ASP 2.B. Returns 0x3D (ASP In 2.B) for N = 0x00–0x03. ASP 2.C. Returns 0x3E (ASP In 2.C) for N = 0x00–0x03. ASP 2.D. Returns 0x3F (ASP In 2.D) for N = 0x00–0x03. ASP 2.E. Returns 0x40 (ASP In 2.E) for N = 0x00–0x03. ASP 2.F. Returns 0x41 (ASP In 2.F) for N = 0x00–0x03. ASP 2.G. Returns 0x42 (ASP In 2.G) for N = 0x00–0x03. ASP 2.H. Returns 0x43 (ASP In 2.H) for N = 0x00–0x03. Returns 0x00 for N > 0x03.

6.5.4 Converter Stream, Channel

Table 6-67. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Input Node ID = 0x12–0x19 ASP2 Input Node ID = 0x1A–0x21	Verb ID = 0xF06	Payload = 0x00

Table 6-68. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Input Node ID = 0x12–0x19 ASP2 Input Node ID = 0x1A–0x21	Verb ID = 0x706	Payload = 0xXX

Table 6-69. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7:4	Read/write	0x0	Stream number (SN). Written by software to indicate the stream number used by the input converter. 0x0 is Stream 0, 0x1 is Stream 1, etc. By convention, Stream 0 is reserved and unused so the converter whose stream number has been cleared does not unintentionally decode data not intended for them.
3:0	Read/write	0x0	Lowest channel number (LCN). Written by software to indicate the lowest channel used by the Input Converter.

If the converter node is in the D3 power state, this parameter is read only (set parameter commands are ignored). As shown in Table 4-4, parameter values are reset to default (SN = 0, LCN = 0) at power-state transitions, thus the parameter can be configured only while the converter node power state is D0.

6.5.5 Converter Format

Table 6-70. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	ASP1 Input Node ID = 0x12–0x19 ASP2 Input Node ID = 0x1A–0x21	Verb ID = 0xA	Payload = 0x0000

Table 6-71. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	ASP1 Input Node ID = 0x12–0x19 ASP2 Input Node ID = 0x1A–0x21	Verb ID = 0x2	Payload = 0xXXXX

Response Format: See Section 6.1.3 for the definition of the stream format structure.

6.6 DMIC Input Converter Widgets (Node ID = 0x22, 0x23)

6.6.1 Audio Widget Capabilities

Table 6-72. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0xF00	Parameter ID = 0x09

Table 6-73. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Reserved
23:20	Read only	0x1	Type (TYP). Audio input converter widget.
19:16	Read only	0x8	Delay (DLY). Indicates the number of sample delays through the widget.
15:13	Read only	000	Channel count extension (CCE). With CCL, indicates that this widget supports two channels.
12	Read only	0	CP caps (CPC). Widget does not support content protection.
11	Read only	0	L–R swap (LRS). This widget cannot swap the left and right channels.
10	Read only	1	Power control (PC). This widget supports power state control.
9	Read only	0	Digital (DIG). This widget is not a digital widget.
8	Read only	1	Connection list (CL). A connection list is present on this widget.
7	Read only	0	Unsolicited capable (UC). UR is not supported on this widget.
6	Read only	0	Processing widget (PW). This widget does not support the processing capabilities parameter.
5	Read only	0	Stripe (STRP). Striping is not supported.
4	Read only	1	Format override (FO). This widget does not contain its own format parameters.
3	Read only	1	Amplifier parameter override (APO). This widget does not contain amplifier parameters.
2	Read only	0	Output amplifier present (OAP). Output amplifier is not present for this widget.
1	Read only	1	Input amplifier present (IAP). Input amplifier is not present for this widget.
0	Read only	1	Channel count LSB (CCL). With CCE, indicates that this widget supports two channels.

6.6.2 Supported PCM Size, Rates

Table 6-74. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0xF00	Parameter ID = 0x0A

Table 6-75. Response Format

Bits	Type	Default	Description
31:21	Read only	0x000	Reserved

Table 6-75. Response Format *(Cont.)*

Bits	Type	Default	Description
20	Read only	1	32-bit (32B). 32-bit audio format is supported.
19	Read only	1	24-bit (24B). 24-bit audio format is supported.
18	Read only	1	20-bit (20B). 20-bit audio format is supported.
17	Read only	1	16-bit (16B). 16-bit audio format is supported.
16	Read only	0	8-bit (8B). 8-bit audio format is not supported.
15:12	Read only	0x0	Reserved
11	Read only	0	Rate-12 (R12). 384-kHz rate is not supported.
10	Read only	0	Rate-11 (R11). 192.0-kHz rate is not supported.
9	Read only	0	Rate-10 (R10). 176.4-kHz rate is not supported.
8	Read only	1	Rate-9 (R9). 96.0-kHz rate is supported.
7	Read only	1	Rate-8 (R8). 88.2-kHz rate is supported.
6	Read only	1	Rate-7 (R7). 48.0-kHz rate is supported.
5	Read only	1	Rate-6 (R6). 44.1-kHz rate is supported.
4	Read only	1	Rate-5 (R5). 32.0-kHz rate is supported.
3	Read only	0	Rate-4 (R4). 22.05-kHz rate is not supported.
2	Read only	1	Rate-3 (R3). 16.0-kHz rate is supported
1	Read only	0	Rate-2 (R2). 11.025-kHz rate is not supported.
0	Read only	1	Rate-1 (R1). 8.0-kHz rate is supported.

6.6.3 Supported Stream Formats

Table 6-76. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0xF00	Parameter ID = 0x0B

Table 6-77. Response Format

Bits	Type	Default	Description
31:3	Read only	0	Reserved
2	Read only	0	AC-3 (AC3). AC-3 data is not supported.
1	Read only	0	Float32 (FLT32). Float32 formatted data is not supported.
0	Read only	1	Pulse code modulation (PCM). PCM formatted data is supported.

6.6.4 Input Amplifier Capabilities

Table 6-78. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0xF00	Parameter ID = 0x0D

Table 6-79. Response Format

Bits	Type	Default	Description
31	Read only	1	Mute capable (MC). This widget supports mute.
30:23	Read only	0	Reserved
22:16	Read only	000_0011	Step size (SS). Indicates that the size of each amplifier's step gain is 1.0 dB.
15	Read only	0	Reserved
14:8	Read only	011_1111	Number of steps (NOS). There are 64 gain steps; Gain range is from +12 to –51 dB in 1.0-dB steps.
7	Read only	0	Reserved
6:0	Read only	011_0011	Offset (OFST). Indicates that programming 011_0011 into the amplifier gain control results in a 0-dB gain.

6.6.5 Connection List Length

Table 6-80. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0xF00	Parameter ID = 0x0E

Table 6-81. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7	Read only	0	Long form (LF). Connection list is short form.
6:0	Read only	000_0001	Connection list length (CLL).A single hard-wired input is available for this widget.

6.6.6 Supported Power States

Table 6-82. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0xF00	Parameter ID = 0x0F

Table 6-83. Response Format

Bits	Type	Default	Description
31	Read only	1	EPSS. Extended power states are supported.
30:4	Read only	0	Reserved
3	Read only	1	D3coldSup. D3cold operation is supported
2	Read only	0	D3Sup. D3hot operation is supported
1	Read only	0	D2Sup. D2 operation is not supported
0	Read only	1	D1Sup. D1 operation is not supported

6.6.7 Connection List Entry

Table 6-84. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0xF02	Payload = N = 0xXX

Table 6-85. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Connection list entry N+3. Returns 0x00 for N = 0x00–0x03 or N > 0x03
23:16	Read only	0x00	Connection list entry for N+2. Returns 0x00 for N = 0x00–0x03 or N > 0x03
15:8	Read only	0x00	Connection list entry for N+1. Returns 0x00 for N = 0x00–0x03 or N > 0x03
7:0	Read only	NID = 0x22: 0x44 NID = 0x23: 0x45	Connection list entry for N. DMIC1: Returns 0x44 (DMIC1) for N = 0x00–0x03. DMIC2: Returns 0x45 (DMIC2) for N = 0x00–0x03. Returns 0x00 for N > 0x03

6.6.8 Power States

Table 6-86. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0xF05	Payload = 0x00

Table 6-87. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0x705	Payload = 0xXX

Table 6-88. Response Format

Bits	Type	Default	Description
31:11	Read only	0	Reserved
10	Read only	1	Power state settings reset (PS-SettingsReset). Set when, during any type of reset or low-power state transition, settings within this widget that were changed from the defaults, either by software or hardware, have been reset to their default states. When these settings have not been reset, this is reported as 0. This bit is always set after a POR condition. Reading this bit using Get Parameter command clears this bit.
9	Read only	0	Reserved
8	Read only	0	Power-state error (PS-Error). This bit is not supported and always returns 0 when read.
7:4	Read only	0x3	Power state actual (PS-Act). Indicates the node's actual power state. Within the AFG node, this field is always equal to the PS-Set field (modulo the time required to execute a power state transition). Within this type of node, this field is the lower power consuming state of either the PS-Set field of the currently referenced node or the PS-Set field of the AFG node under which the currently referenced node was enumerated (is controlled). Default is D3.
3:0	Read/ write	0x3	Power state set (PS-Set). Defines the referenced node's current power setting. Since this node is of type other than an AFG node, the actual power state is a function of both this setting and the PowerState setting of the AFG node under which this node was enumerated (is controlled). Writes to the following bits set the node to the power state: PSS = 0000; D0—Fully on PSS = 0010; D2—Not supported PSS = 0001; D1—Not supported PSS = 0011; D3—Supported

6.6.9 Converter Stream, Channel

Table 6-89. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0xF06	Payload = 0x00

Table 6-90. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0x706	Payload = 0xXX

Table 6-91. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7:4	Read/write	0x0	Stream number (SN). Written by software to indicate the stream number used by the input converter. 0x0 is Stream 0, 0x1 is Stream 1, etc. By convention, Stream 0 is reserved and unused so that converter whose stream number has been cleared does not unintentionally decode data not intended for them.
3:0	Read/write	0x0	Lowest channel number (LCN). Written by software to indicate the lowest channel used by the Input Converter. The stereo converter uses this value plus 1 for its left and right channel.

While the converter node is in the D3 power state, this parameter is read only (set parameter commands are ignored). As shown in Table 4-4, the parameter values are reset to default (SN = 0, LCN = 0) at power state transitions; therefore, the parameter can be configured only while the converter node power state is D0.

6.6.10 Converter Format

Table 6-92. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0xA	Payload = 0x0000

Table 6-93. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0x2	Payload = 0xXXXX

Response Format: See Section 6.1.3 for the definition of the stream format structure.

6.6.11 Amplifier Gain/Mute

Table 6-94. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0xB	Payload = 0xXXXX (see Table 6-95)

Table 6-95. Payload Bits [15:0]

Bits [15:0]	Value	Description
15	0	Get output/input (GOI). Controls whether the request is for the input amplifier or the output amplifier. 0 The input amplifier is being requested. 1 The output amplifier is being requested.
14	0	Reserved
13	x	Get left/right (GLR). Controls whether the request is for the left- or right-channel amplifier. 0 The right channel amplifier is being requested. 1 The left channel amplifier is being requested.
12:4	0x000	Reserved
3:0	0x0	Index (IDX). Specifies the input index of the amplifier setting to return if the widget has multiple input amplifiers. IDX has no meaning and is ignored since the widget does not have multiple input amplifiers. It should always be 0s.

Table 6-96. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7	Read only	1	Amplifier mute (AM). Returns the requested amplifier's mute setting. The default, 1, indicates the amplifier is in the mute condition. If the amplifier does not exist, 0 is returned.
6:0	Read only	011_0011	Amplifier gain (AG). Returns the gain setting for the amplifier requested. If the amplifier requested does not exist, all 0 is returned. Default equals 0 dB.

Table 6-97. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DMIC1 Node ID = 0x22 DMIC2 Node ID = 0x23	Verb ID = 0x3	Payload = 0xXXXX (see Table 6-98)

Table 6-98. Payload Bits [15:0]

Bits	Type	Default	Description
15	Write only	0	Set output amplifier (SOA). Bit is always 0, since an output amplifier is not present.
14	Write only	x	Set input amplifier (SIA). Determines whether the value programmed refers to the input amplifier. Must be set for the value to be accepted.
13	Write only	x	Set left amplifier (SLA). Selects the left channel (Channel 0). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
12	Write only	x	Set right amplifier (SRA). Selects the right channel (Channel 1). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
11:8	Write only	0x0	Index (IDX). Used when programming the input amplifiers on selector and sum widgets. This field is ignored.
7	Write only	x	Mute (MUTE). If 1, mute is active. If 0, mute is inactive.
6:0	Write only	xx	Gain (GAIN). Specifies the amplifier gain

6.7 ASP Transmitter Pin Widgets (Node ID = 0x24–0x33)

6.7.1 Audio Widget Capabilities

Table 6-99. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Tx Node ID = 0x24–0x2B ASP2 Tx Node ID = 0x2C–0x33	Verb ID = 0xF00	Parameter ID = 0x09

Table 6-100. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Reserved
23:20	Read only	0x4	Type (TYP). Pin complex widget
19:16	Read only	0x0	Delay (DLY). Indicates the number of sample delays through the widget.
15:13	Read only	000	Channel count extension (CCE). With CCL, indicates that this widget supports two channels.
12	Read only	0	CP caps (CPC). Widget does not support content protection.
11	Read only	0	L–R swap (LRS). This widget cannot swap the left and right channels.
10	Read only	0	Power control (PC). This widget does not support power state control.
9	Read only	0	Digital (DIG). This widget is not a digital widget.
8	Read only	1	Connection list (CL). A connection list is present on this widget.
7	Read only	0	Unsolicited capable (UC). UR is not supported on this widget.
6	Read only	0	Processing widget (PW). This widget does not support the processing capabilities parameter.
5	Read only	0	Stripe (STRP). Striping is not supported.
4	Read only	0	Format override (FO). This widget does not contain its own format parameters.
3	Read only	0	Amplifier parameter override (APO). This widget does not contain amplifier parameters.
2	Read only	0	Output amplifier present (OAP). Output amplifier is not present for this widget.
1	Read only	0	Input amplifier present (IAP). Input amplifier is not present for this widget.
0	Read only	1	Channel count LSB (CCL). With CCE, indicates that this widget supports two channels.

6.7.2 Pin Capabilities

Table 6-101. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Tx Node ID = 0x24–0x2B ASP2 Tx Node ID = 0x2C–0x33	Verb ID = 0xF00	Parameter ID = 0x0C

Table 6-102. Response Format

Bits	Type	Default	Description
31:28	Read only	0x0	Reserved
27	Read only	0	High bit rate (HBR). Widget does not support high bit rate.
26:25	Read only	00	Reserved
24	Read only	0	Display port (DP). Widget does not support display port.
23:17	Read only	0	Reserved
16	Read only	0	EAPD capable (EAPDC). Widget does not control an EAPD pin.
15:8	Read only	0x00	VREF control (VREFC). Widget does not support VREF generation.
7	Read only	0	HDMI capable (HDMIC). Widget does not support HDMI.
6	Read only	0	Balanced I/O pins (BIOP). Widget does not have balanced I/O pins.
5	Read only	0	Input capable (INC). Widget is not input capable.
4	Read only	1	Output capable (OUTC). Widget is output capable.
3	Read only	0	Headphone drive capable (HDC). Widget cannot drive headphones directly.
2	Read only	0	Presence detect capable (PDC). Widget cannot perform presence detection.
1	Read only	0	Trigger required (TR). Trigger is not required for an impedance measurement.
0	Read only	0	Impedance sense capable (ISC). Widget does not support impedance sense.

6.7.3 Connection List Length

Table 6-103. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Tx Node ID = 0x24–0x2B ASP2 Tx Node ID = 0x2C–0x33	Verb ID = 0xF00	Parameter ID = 0x0E

Table 6-104. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00 0000	Reserved
7	Read only	0	Long form (LF). Connection list is short form.
6:0	Read only	000_0001	Connection list length (CLL). A single hard-wired input is available for this widget.

6.7.4 Connection List Entry

Table 6-105. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Tx Node ID = 0x24–0x2B ASP2 Tx Node ID = 0x2C–0x33	Verb ID = 0xF02	Payload = N = 0xXX

Table 6-106. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Connection list entry for N+3. Returns 0x00 for N = 0x00–0x03 or N > 0x03.
23:16	Read only	0x00	Connection list entry for N+2. Returns 0x00 for N = 0x00–0x03 or N > 0x03.
15:8	Read only	0x00	Connection list entry for N+1. Returns 0x00 for N = 0x00–0x03 or N > 0x03.
7:0	Read only	NID = 0x24: 0x02 NID = 0x25: 0x03 NID = 0x26: 0x04 NID = 0x27: 0x05 NID = 0x28: 0x06 NID = 0x29: 0x07 NID = 0x2A: 0x08 NID = 0x2B: 0x09 NID = 0x2C: 0x0A NID = 0x2D: 0x0B NID = 0x2E: 0x0C NID = 0x2F: 0x0D NID = 0x30: 0x0E NID = 0x31: 0x0F NID = 0x32: 0x10 NID = 0x33: 0x11	Connection list entry for N. ASP Out 1.A. Returns 0x02 (ASP 1.A) for N = 0x00–0x03. ASP Out 1.B. Returns 0x03 (ASP 1.B) for N = 0x00–0x03. ASP Out 1.C. Returns 0x04 (ASP 1.C) for N = 0x00–0x03. ASP Out 1.D. Returns 0x05 (ASP 1.D) for N = 0x00–0x03. ASP Out 1.E. Returns 0x06 (ASP 1.E) for N = 0x00–0x03. ASP Out 1.F. Returns 0x07 (ASP 1.F) for N = 0x00–0x03. ASP Out 1.G. Returns 0x08 (ASP 1.G) for N = 0x00–0x03. ASP Out 1.H. Returns 0x09 (ASP 1.H) for N = 0x00–0x03. ASP Out 2.A. Returns 0x0A (ASP 2.A) for N = 0x00–0x03. ASP Out 2.B. Returns 0x0B (ASP 2.B) for N = 0x00–0x03. ASP Out 2.C. Returns 0x0C (ASP 2.C) for N = 0x00–0x03. ASP Out 2.D. Returns 0x0D (ASP 2.D) for N = 0x00–0x03. ASP Out 2.E. Returns 0x0E (ASP 2.E) for N = 0x00–0x03. ASP Out 2.F. Returns 0x0F (ASP 2.F) for N = 0x00–0x03. ASP Out 2.G. Returns 0x10 (ASP 2.G) for N = 0x00–0x03. ASP Out 2.H. Returns 0x11 (ASP 2.H) for N = 0x00–0x03. Returns 0x00 for N > 0x03.

6.7.5 Pin Widget Control

Table 6-107. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Tx Node ID = 0x24–0x2B ASP2 Tx Node ID = 0x2C–0x33	Verb ID = 0xF07	Payload = 0x00

Table 6-108. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Tx Node ID = 0x24–0x2B ASP2 Tx Node ID = 0x2C–0x33	Verb ID = 0x707	Payload = 0xXX

Table 6-109. Response Format

Bits	Type	Default	Description
31:8	Read only	0	Reserved
7	Read only	0	H-Phone enable (HPE). Not supported.
6	Read/write	0	Output enable (OUTE) 0 The output path of the pin widget is shut off (muted). 1 Enables the output path of the pin widget.
5	Read only	0	Input enable (INE). Not supported.
4:3	Read only	00	Reserved
2:0	Read only	000	VREF enable (VREFE). Not supported

6.7.6 Configuration Default

Software uses the configuration default register as an aid in determining the configuration of jacks and devices attached to the codec. When the codec is powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state (including any software writes into the register) must be preserved across reset events, such as link or codec reset (the function reset verb). Its state need not be preserved across power-level changes.

Table 6-110. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Tx Node ID = 0x24–0x2B ASP2 Tx Node ID = 0x2C–0x33	Verb ID = 0xF1C	Payload = 0x00

Table 6-111. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Tx Node ID = 0x24–0x2B ASP2 Tx Node ID = 0x2C–0x33	Verb ID = 0x71C Verb ID = 0x71D Verb ID = 0x71E Verb ID = 0x71F	Payload = 0xXX (Config bits [7:0]) Payload = 0xXX (Config bits [15:8]) Payload = 0xXX (Config bits [23:16]) Payload = 0xXX (Config bits [31:24])

Table 6-112. Response Format

Bits	Type	Default	Description
31:30	Read/write	01	Port connectivity (PCON). All ASP pin widgets default to no physical connection.
29:24	Read/write	ASP1: 0x00 ASP2: 0x10	Location (LOC). Indicates the physical location of the jack or device to which the pin complex is connected. For ASP1.A–H defaults to External | N/A. For ASP2.A–H defaults to Internal | N/A.
23:20	Read/write	ASP1: 0x2 ASP2: 0x1	Default device (DD). Indicates the intended use of the jack or device. For ASP1.A–H defaults to HP Out. For ASP2.A–H defaults to Speaker.
19:16	Read/write	ASP1: 0xB ASP2: 0x0	Connection type (CTYP). Indicates the type of physical connection. For ASP1.A–H defaults to combo jack. For ASP2.A–H defaults to unknown.
15:12	Read/write	ASP1: 0x2 ASP2: 0x0	Color (COL). Indicates the color of the physical jack. For ASP1.A–H defaults to gray. For ASP2.A–H defaults to unknown.
11:8	Read/write	0x0	Miscellaneous (MISC). No PDC override.
7:4	Read/write	0xF	Default association (DA). This field is used by software to group pin complexes into functional blocks. Set in accordance with *Microsoft Pin Configuration Guidelines for HD Audio Devices*.
3:0	Read/write	0x0	Sequence (SEQ). This field indicates the order of the jacks in the association group. Set in accordance with *Microsoft Pin Configuration Guidelines for HD Audio Devices*.

Note: Bits [31:0] are sticky and are not reset by a link reset or a codec reset.

6.8 ASP Receiver Pin Widgets (Node ID = 0x34–0x43)

6.8.1 Audio Widget Capabilities

Table 6-113. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Rx Node ID = 0x34–0x3B ASP2 Rx Node ID = 0x3C–0x43	Verb ID = 0xF00	Parameter ID = 0x09

Table 6-114. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Reserved
23:20	Read only	0x4	Type (TYP). Pin complex widget.
19:16	Read only	0x0	Delay (DLY). Indicates the number of sample delays through the widget.
15:13	Read only	000	Channel count extension (CCE). With CCL, indicates that this widget supports two channels.
12	Read only	0	CP caps (CPC). Widget does not support content protection.
11	Read only	0	L–R swap (LRS). This widget cannot swap the left and right channels.

Table 6-114. Response Format *(Cont.)*

Bits	Type	Default	Description
10	Read only	0	Power control (PC). This widget does not support power state control.
9	Read only	0	Digital (DIG). This widget is not a digital widget.
8	Read only	0	Connection list (CL). A connection list is not present on this widget.
7	Read only	0	Unsolicited capable (UC). UR is not supported on this widget.
6	Read only	0	Processing widget (PW). This widget does not support the processing capabilities parameter.
5	Read only	0	Stripe (STRP). Striping is not supported.
4	Read only	0	Format override (FO). This widget does not contain format information.
3	Read only	0	Amplifier parameter override (APO). This widget does not contain amplifier parameters.
2	Read only	0	Output amplifier present (OAP). Output amplifier is not present for this widget.
1	Read only	0	Input amplifier present (IAP). Input amplifier is not present for this widget.
0	Read only	1	Channel count LSB (CCL). With CCE, indicates that this widget supports two channels.

6.8.2 Pin Capabilities

Table 6-115. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Rx Node ID = 0x34–0x3B ASP2 Rx Node ID = 0x3C–0x43	Verb ID = 0xF00	Parameter ID = 0x0C

Table 6-116. Response Format

Bits	Type	Default	Description
31:28	Read only	0x0	Reserved
27	Read only	0	High bit rate (HBR). Widget does not support high bit rate.
26:25	Read only	00	Reserved
24	Read only	0	Display port (DP). Widget does not support display port.
23:17	Read only	0	Reserved
16	Read only	0	EAPD capable (EAPDC). Widget does not control an EAPD pin.
15:8	Read only	0x00	VREF control (VREFC). Widget does not support VREF generation.
7	Read only	0	HDMI capable (HDMIC). Widget does not support HDMI.
6	Read only	0	Balanced I/O pins (BIOP). Widget does not have balanced I/O pins.
5	Read only	1	Input capable (INC). Widget is not input capable.
4	Read only	0	Output capable (OUTC). Widget is output capable.
3	Read only	0	Headphone drive capable (HDC). Widget cannot drive headphones directly.
2	Read only	0	Presence detect capable (PDC). Widget cannot perform presence detection.
1	Read only	0	Trigger required (TR). Trigger is not required for an impedance measurement.
0	Read only	0	Impedance sense capable (ISC). Widget does not support impedance sense.

6.8.3 Pin Widget Control

Table 6-117. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Rx Node ID = 0x34–0x3B ASP2 Rx Node ID = 0x3C–0x43	Verb ID = 0xF07	Payload = 0x00

Table 6-118. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Rx Node ID = 0x34–0x3B ASP2 Rx Node ID = 0x3C–0x43	Verb ID = 0x707	Payload = 0xXX

Table 6-119. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7	Read only	0	H-Phone enable (HPE). Not supported
6	Read only	0	Output enable (OUTE). Not supported

Table 6-119. Response Format *(Cont.)*

Bits	Type	Default	Description
5	Read/write	0	Input enable (INE) 0 Shuts off (mutes) input path of the pin widget 1 Enables the input path of the pin widget
4:3	Read only	00	Reserved
2:0	Read only	000	VREF enable (VREFE). Not supported

6.8.4 Configuration Default

Software uses the configuration default register as an aid in determining the configuration of jacks and devices attached to the codec. When the codec is powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as link or codec reset (the function reset verb). Its state need not be preserved across power-level changes.

Table 6-120. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Rx Node ID = 0x34–0x3B ASP2 Rx Node ID = 0x3C–0x43	Verb ID = 0xF1C	Payload = 0x00

Table 6-121. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ASP1 Rx Node ID = 0x34–0x3B ASP2 Rx Node ID = 0x3C–0x43	Verb ID = 0x71C Verb ID = 0x71D Verb ID = 0x71E Verb ID = 0x71F	Payload = 0xXX (Config bits [7:0]) Payload = 0xXX (Config bits [15:8]) Payload = 0xXX (Config bits [23:16]) Payload = 0xXX (Config bits [31:24])

Table 6-122. Response Format

Bits	Type	Default	Description
31:30	Read/write	01	Port connectivity (PCON). All ASP pin widgets default to no physical connection
29:24	Read/write	ASP1: 0x00 ASP2: 0x10	Location (LOC). Indicates the physical location of the jack or device to which the pin complex is connected. For ASP1.A–ASP1.H defaults to External | N/A. For ASP2.A–ASP2.H defaults to Internal | N/A.
23:20	Read/write	ASP1: 0xA ASP2: 0x9	Default device (DD). Indicates the intended use of the jack or device. For ASP1.A–ASP1.H defaults to Mic In. For ASP2.A–ASP2.H defaults to Aux In.
19:16	Read/write	ASP1: 0xB ASP2: 0x0	Connection type (CTYP). Indicates the type of physical connection. For ASP1.A–ASP1.H defaults to combo jack. For ASP2.A–ASP2.H defaults to unknown.
15:12	Read/write	ASP1: 0x2 ASP2: 0x0	Color (COL). Indicates the color of the physical jack. For ASP1.A–ASP1.H defaults to gray. For ASP2.A–ASP2.H defaults to unknown.
11:8	Read/write	0x0	Miscellaneous (MISC). No PDC override.
7:4	Read/write	0xF	Default association (DA). Used by software to group pin complexes into functional blocks. Set in accordance with *Microsoft Pin Configuration Guidelines for HD Audio Devices*.
3:0	Read/write	0x0	Sequence (SEQ). Indicates the order of the jacks in the association group. Set in accordance with *Microsoft Pin Configuration Guidelines for HD Audio Devices*.

Note: Bits [31:0] are sticky and are not reset by a link reset or a codec reset.

6.9 DMIC Pin Widgets (Node ID = 0x44, 0x45)

6.9.1 Audio Widget Capabilities

Table 6-123. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Pin Node ID = 0x44 DMIC2 Pin Node ID = 0x45	Verb ID = 0xF00	Parameter ID = 0x09

Table 6-124. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Reserved
23:20	Read only	0x4	Type (TYP). Pin complex widget
19:16	Read only	0x0	Delay (DLY). Indicates the number of sample delays through the widget.
15:13	Read only	000	Channel count extension (CCE). With CCL, indicates that this widget supports two channels.
12	Read only	0	CP caps (CPC). Widget does not support content protection.
11	Read only	0	L–R swap (LRS). This widget cannot swap the left and right channels.
10	Read only	0	Power control (PC). This widget does not support power-state control.
9	Read only	0	Digital (DIG). This widget is not a digital widget.
8	Read only	0	Connection list (CL). A connection list is not present on this widget.
7	Read only	0	Unsolicited capable (UC). UR is not supported on this widget.
6	Read only	0	Processing widget (PW). This widget does not support the processing capabilities parameter.
5	Read only	0	Stripe (STRP). Striping is not supported.
4	Read only	0	Format override (FO). This widget does not contain format information.
3	Read only	1	Amplifier parameter override (APO). This widget contains its own amplifier parameters.
2	Read only	0	Output amplifier present (OAP). Output amplifier is not present for this widget.
1	Read only	1	Input amplifier present (IAP). Input amplifier is present for this widget.
0	Read only	1	Channel count LSB (CCL). With CCE, indicates that this widget supports two channels.

6.9.2 Pin Capabilities

Table 6-125. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Pin Node ID = 0x44 DMIC2 Pin Node ID = 0x45	Verb ID = 0xF00	Parameter ID = 0x0C

Table 6-126. Response Format

Bits	Type	Default	Description
31:28	Read only	0x0	Reserved
27	Read only	0	High bit rate (HBR). Widget does not support high bit rate.
26:25	Read only	00	Reserved
24	Read only	0	Display port (DP). Widget does not support display port.
23:17	Read only	0	Reserved
16	Read only	0	EAPD capable (EAPDC). Widget does not control an EAPD pin.
15:8	Read only	0x00	VREF control (VREFC). Widget does not support VREF generation.
7	Read only	0	HDMI capable (HDMIC). Widget does not support HDMI.
6	Read only	0	Balanced I/O pins (BIOP). Widget does not have balanced I/O pins.
5	Read only	1	Input capable (INC). Widget is input capable.
4	Read only	0	Output capable (OUTC). Widget is not output capable.
3	Read only	0	Headphone drive capable (HDC). Widget cannot drive headphones directly.
2	Read only	0	Presence detect capable (PDC). Widget cannot perform presence detection.
1	Read only	0	Trigger required (TR). Trigger is not required for an impedance measurement.
0	Read only	0	Impedance sense capable (ISC). Widget does not support impedance sense.

6.9.3 Input Amplifier Capabilities

Table 6-127. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Pin Node ID = 0x44 DMIC2 Pin Node ID = 0x45	Verb ID = 0xF00	Parameter ID = 0x0D

Table 6-128. Response Format

Bits	Type	Default	Description
31	Read only	0	Mute capable (MC). Does not support mute.
30:23	Read only	0	Reserved
22:16	Read only	010_0111	Step size (SS). Indicates that the size of each amplifier's step gain is 10 dB.

Table 6-128. Response Format *(Cont.)*

Bits	Type	Default	Description
15	Read only	0	Reserved
14:8	Read only	0x02	Number of steps (NOS). There are three gain steps: 0 dB, +10 dB, and +20 dB.
7	Read only	0	Reserved
6:0	Read only	0x00	Offset (OFST). Indicates that programming 000_0000 into the amplifier gain control results in a 0-dB gain.

6.9.4 Pin Widget Control

Table 6-129. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Pin Node ID = 0x44 DMIC2 Pin Node ID = 0x45	Verb ID = 0xF07	Payload = 0x00

Table 6-130. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Pin Node ID = 0x44 DMIC2 Pin Node ID = 0x45	Verb ID = 0x707	Payload = 0xXX

Table 6-131. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7	Read only	0	H-Phone enable (HPE). Not supported
6	Read only	0	Output enable (OUTE). Not supported
5	Read/write	0	Input enable (INE) 0 Shuts off (mutes) input path of the pin widget 1 Enables the input path of the pin widget
4:3	Read only	00	Reserved
2:0	Read only	000	VREF enable (VREFE). Not supported

6.9.5 Configuration Default

Software uses the configuration default register as an aid in determining the configuration of jacks and devices attached to the codec. When the codec is powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as link reset or codec reset (the function reset verb). Its state need not be preserved across power-level changes.

Table 6-132. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Pin Node ID = 0x44 DMIC2 Pin Node ID = 0x45	Verb ID = 0xF1C	Payload = 0x00

Table 6-133. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DMIC1 Pin Node ID = 0x44 DMIC2 Pin Node ID = 0x45	Verb ID = 0x71C Verb ID = 0x71D Verb ID = 0x71E Verb ID = 0x71F	Payload = 0xXX (Config bits [7:0]) Payload = 0xXX (Config bits [15:8]) Payload = 0xXX (Config bits [23:16]) Payload = 0xXX (Config bits [31:24])

Table 6-134. Response Format

Bits	Type	Default	Description
31:30	Read/write	01	Port connectivity (PCON). All DMIC pin widgets default to no physical connection.
29:24	Read/write	0x10	Location (LOC). Indicates the physical location of the jack or device to which the pin complex is connected. Defaults to Internal | N/A.
23:20	Read/write	0xA	Default device (DD). Indicates the intended use of the connection is for mic in.
19:16	Read/write	0x0	Connection type (CTYP). Indicates the type of physical connection. Defaults to unknown.
15:12	Read/write	0x0	Color (COL). The color for an internal connection is unknown.

Table 6-134. Response Format *(Cont.)*

Bits	Type	Default	Description
11:8	Read/write	0x0	Miscellaneous (MISC). No PDC override.
7:4	Read/write	0xF	Default association (DA). Used by software to group pin complexes into functional blocks. Set in accordance with *Microsoft Pin Configuration Guidelines for HD Audio Devices*.
3:0	Read/write	0x0	Sequence (SEQ). Indicates the order of the jacks in the association group. Set in accordance with *Microsoft Pin Configuration Guidelines for HD Audio Devices*.

Note: Bits [31:0] are sticky and are not reset by a link reset or a codec reset.

6.9.6 Amplifier Gain/Mute

Table 6-135. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DMIC1 Pin Node ID = 0x44 DMIC2 Pin Node ID = 0x45	Verb ID = 0xB	Payload = 0xXXXX (see Table 6-136)

Table 6-136. Payload Bits [15:0]

Bits [15:0]	Value	Description
15	0	Get output/input (GOI). Controls whether the request is for the input amplifier or the output amplifier. 0 The input amplifier is being requested. 1 The output amplifier is being requested.
14	0	Reserved
13	x	Get left/right (GLR). Controls whether the request is for the left- or right-channel amplifier. 0 The right channel amplifier is being requested. 1 The left channel amplifier is being requested.
12:4	0x000	Reserved
3:0	0x0	Index (IDX). Specifies the input index of the amplifier setting to return if the widget has multiple input amplifiers. This field has no meaning and ignored since the widget does not have multiple input amplifiers. It should be always 0s.

Table 6-137. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7	Read only	0	Amplifier mute (AM). Mute is not supported by this widget.
6:0	Read only	0x00	Amplifier gain (AG). Returns the gain setting for the amplifier requested. If the amplifier requested does not exist, all 0 is returned. Default equals 0 dB.

Table 6-138. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DMIC1 Pin Node ID = 0x44 DMIC2 Pin Node ID = 0x45	Verb ID = 0x3	Payload = 0xXXXX (see Table 6-139)

Table 6-139. Payload Bits [15:0]

Bits	Type	Default	Description
15	Write only	0	Set output amplifier (SOA). Determines whether the value programmed refers to the output amplifier. This bit should always be 0, since an output amplifier is not present.
14	Write only	x	Set input amplifier (SIA). Determines whether the value programmed refers to the input amplifier. Set to 1 for the value to be accepted.
13	Write only	x	Set left amplifier (SLA). Selects the left channel (Channel 0). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
12	Write only	x	Set right amplifier (SRA). Selects the right channel (Channel 1). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
11:8	Write only	0x0	Index (IDX). Used when programming the input amplifiers on selector and sum widgets. This field is ignored.
7	Write only	0	Mute (MUTE). When 0, the mute is inactive. This field is ignored.
6:0	Write only	xx	Gain (GAIN). Specifies the amplifier gain xxx xx00 0 dB xxx xx01 +10 dB xxx xx10 +20 dB xxx xx11 Reserved, do not use Bits(6:2) are not used and are ignored.

6.10 Beep Generator Widget (Node ID = 0x46)

6.10.1 Audio Widget Capabilities

Table 6-140. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x46	Verb ID = 0xF00	Parameter ID = 0x09

Table 6-141. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Reserved
23:20	Read only	0x7	Type (TYP). Beep generator widget
19:16	Read only	0x0	Delay (DLY). Indicates the number of sample delays through the widget.
15:13	Read only	000	Channel count extension (CCE). With CCL, indicates that this widget supports one channel.
12	Read only	0	CP caps (CPC). Widget does not support content protection.
11	Read only	0	L–R swap (LRS). This widget cannot swap the left and right channels.
10	Read only	0	Power control (PC). This widget does not support power-state control.
9	Read only	1	Digital (DIG). This widget is a digital widget.
8	Read only	0	Connection list (CL). A connection list is not present on this widget.
7	Read only	0	Unsolicited capable (UC). UR is not supported on this widget.
6	Read only	0	Processing widget (PW). This widget does not support the processing capabilities parameter.
5	Read only	0	Stripe (STRP). Striping is not supported.
4	Read only	0	Format override (FO). This widget does not contain format information.
3	Read only	0	Amplifier parameter override (APO). This widget does not contain amplifier parameters.
2	Read only	0	Output amplifier present (OAP). Output amplifier is not present for this widget.
1	Read only	0	Input amplifier present (IAP). Input amplifier is not present for this widget.
0	Read only	0	Channel count LSB (CCL). With CCE, indicates that this widget supports one channel.

6.10.2 Beep Generation Control

Table 6-142. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x46	Verb ID = 0xF0A	Payload = 0x00

Table 6-143. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x46	Verb ID = 0x70A	Payload = 0xXX

Table 6-144. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7:0	Read/write	0x00	Divider. If zero, beep generation is turned off. If nonzero, the beep frequency equals 12 kHz divided by this value (e.g., if Divider = 0x0C, the beep frequency is 1 kHz).

6.11 Vendor Processing Widget (Node ID = 0x47)

6.11.1 Audio Widget Capabilities

Table 6-145. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x47	Verb ID = 0xF00	Parameter ID = 0x09

Table 6-146. Response Format

Bits	Type	Default	Description
31:24	Read only	0x00	Reserved
23:20	Read only	0xF	Type (TYP). Vendor-defined widget

Table 6-146. Response Format *(Cont.)*

Bits	Type	Default	Description
19:16	Read only	0x0	Delay (DLY). Indicates the number of sample delays through the widget.
15:13	Read only	000	Channel count extension (CCE). With CCL, indicates that this widget supports two channels.
12	Read only	0	CP caps (CPC). Widget does not support content protection.
11	Read only	0	L–R swap (LRS). This widget cannot swap the left and right channels.
10	Read only	0	Power control (PC). This widget does not support power-state control.
9	Read only	1	Digital (DIG). This widget is a digital widget.
8	Read only	0	Connection list (CL). Connection list is not present.
7	Read only	1	Unsolicited capable (UC). UR is supported on this widget.
6	Read only	1	Processing widget (PW). This widget supports the processing capabilities parameter.
5	Read only	0	Stripe (STRP). Striping is not supported.
4	Read only	0	Format override (FO). Clear to indicate that the widget does not contain format information.
3	Read only	0	Amplifier parameter override (APO). This widget does not contain amplifier parameters.
2	Read only	0	Output amplifier present (OAP). Output amplifier is not present for this widget.
1	Read only	0	Input amplifier present (IAP). Input amplifier is not present for this widget.
0	Read only	1	Channel count LSB (CCL). With CCE, indicates that this widget supports two channels.

6.11.2 Processing Capabilities

Table 6-147. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x47	Verb ID = 0xF00	Parameter ID = 0x10

Table 6-148. Response Format

Bits	Type	Default	Description
31:16	Read only	0x0000	Reserved
15:8	Read only	0xFF	NumCoeff. Number of coefficients. There are 255 coefficient registers.
7:1	Read only	0	Reserved
0	Read only	0	Benign. This processing widget is not linear and time invariant.

6.11.3 Processing State

Table 6-149. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x47	Verb ID = 0xF03	Payload = 0x00

Table 6-150. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x47	Verb ID = 0x703	Payload = 0xXX

Table 6-151. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7:0	Read/write	0x00	HDA-defined processing state. Writes to these bits set the widget to the processing state. 0x00 Processing off 0x02 Processing benign. Benign state is not supported, treated as “processing off.” 0x01 Processing on 0x03–0x7F Reserved

6.11.4 I²C Master Port Unsolicited Response Control

Table 6-152. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x47	Verb ID = 0xF08	Payload = 0x00

Table 6-153. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x47	Verb ID = 0x708	Payload = 0xXX

Table 6-154. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7	Read/write	0	Enable. Controls the actual generation of URs. 0 Disable 1 Enable
6	Read only	0	Reserved
5:0	Read/write	00_0000	Tag. Value assigned and used by software to determine what codec node generated the UR. The value programmed into the tag field is returned in the top 6 bits (31:26) of every UR generated by this node.

Note: Bits [31:0] are sticky and are not reset by a link reset or a function group reset.

Table 6-155. Unsolicited Response Format

Bits [31:26]	Bits [25:21]	Bits [20:16]	Bits [15:8]	Bits [7:0]
Tag	Sub Tag (0_0000)	Reserved	I2C Status[7:0]	I2C Data[7:0]

See Table 6-194 for UR trigger and reset conditions.

6.11.5 ASP Unsolicited Response Control

Table 6-156. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x47	Verb ID = 0xFF0	Payload = 0x00

Table 6-157. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0x47	Verb ID = 0x7F0	Payload = 0xXX

Table 6-158. Response Format

Bits	Type	Default	Description
31:8	Read only	0x00_0000	Reserved
7	Read/write	0	Enable. Controls the actual generation of URs 0 Disable 1 Enable
6	Read only	0	Reserved
5:0	Read/write	00_0000	Tag. Value assigned and used by software to determine what codec node generated the UR. The value programmed into the tag field is returned in the top 6 bits (31:26) of every UR generated by this node.

Note: Bits [31:0] are sticky and are not reset by a link reset or a function group reset.

Table 6-159. Unsolicited Response Format

Bits [31:26]	Bits [25:21]	Bits [20:0]
Tag	Sub Tag (0_0000)	Serial Interface Status [20:0] Bit20: Reserved Bit19: ASP2 Rx Request Overload Bit18: ASP2 Rx LRCK Error Bit17: ASP2 Rx LRCK Late Bit16: ASP2 Rx LRCK Early Bit15: ASP2 Rx No LRCK Bit14: Reserved Bit13: ASP2 Tx SM Error Bit12: ASP2 Tx LRCK Late Bit11: ASP2 Tx LRCK Early Bit10: ASP2 Tx No LRCK Bit9: ASP1 Rx Request Overload Bit8: ASP1 Rx LRCK Error Bit7: ASP1 Rx LRCK Late Bit6: ASP1 Rx LRCK Early Bit5: ASP1 Rx No LRCK Bit4: Reserved Bit3: ASP1 Tx SM Error Bit2: ASP1 Tx LRCK Late Bit1: ASP1 Tx LRCK Early Bit0: ASP1 Tx No LRCK

6.11.6 Coefficient Index

The coefficient index is a zero-based index into the processing coefficient list, which is either read or written using the processing coefficient control. When the coefficient has been read or written to, the coefficient index automatically increments by one so that the next set processing coefficient verb loads the coefficient into the next slot. The autoincrement feature can be disabled by setting the disable coefficient index autoincrement bit (DAI) in Table 6-167. The autoincrement feature wraps around at a coefficient index value of 0x82; that is, an index of 0x82 is autoincremented to an index of 0x00. If the coefficient index is set to exceed the number of slots in the processing coefficient list, unpredictable behavior occurs if an attempt is made to get or set the processing coefficient.

Table 6-160. Get Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Node ID = 0x47	Verb ID = 0xD	Payload = 0x0000

Table 6-161. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Node ID = 0x47	Verb ID = 0x5	Payload = 0xXXXX

Table 6-162. Response Format

Bits	Type	Default	Description
31:16	Read only	0x0000	Reserved
15:0	Read/write	0x0000	Index n. Coefficient index value.

6.11.7 Processing Coefficient

The processing coefficient loads the value *n* into the widget's coefficient array at the index determined by the coefficient index control. When the coefficient has been read or written to, the coefficient index automatically increments so that the next set processing coefficient verb loads the coefficient into the next slot.

Table 6-163. Get Parameter Command Format [1]

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Node ID = 0x47	Verb ID = 0xC	Payload = 0x0000

1. Data from the processing coefficients can only be read while the AFG power state is D0.

Table 6-164. Set Parameter Command Format

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Node ID = 0x47	Verb ID = 0x4	Payload = 0xXXXX

Table 6-165. Response Format

Bits	Type	Default	Description
31:16	Read only	0x0000	Reserved
15:0	Read/write	0x0000	Value n. The value n of the 16-bit coefficient to set.

6.11.8 Coefficient Registers

The processing coefficient loads the 16-bit value *n* into the widget's coefficient array at the index determined by the coefficient index control. When the coefficient has been loaded, the coefficient index automatically increments so that the next set processing coefficient verb loads the coefficient into the next slot.

Table 6-166. Coefficient Index Register Summary

Coefficient Index Register (CIR)	Description
0x0000–0x0002	Device configuration 1–3 (see p. 84)
0x0003–0x0008	ASP clock configuration (see p. 85)
0x0009	DMIC configuration (see p. 87)
0x000A	Beep configuration (see p. 87)

Table 6-166. Coefficient Index Register Summary *(Cont.)*

Coefficient Index Register (CIR)	Description
0x000B–0x0016	ASP null-insert/-remove control (see p. 87)
0x0017–0x0018	ASP sync control (see p. 88)
0x0019–0x0058	ASP configuration (see p. 89)
0x0059–0x005E	I²C control/status (see p. 91)
0x005F–0x0062	SPI control (see p. 92)
0x0063–0x006A	Parametric filter engine (see p. 93)
0x006B–0x0071	ASP internal status report (see p. 94)
0x0080	Loopback control (see p. 95)
0x0082	Pad configuration and slew rate control (see p. 95)

6.11.8.1 Device Configuration 1

Table 6-167. Device Configuration 1 (CIR = 0x0000)

Bits	Type	Default	Description
15	Read/write	1	GPIO logic clock enable (GPIO_CEN) 0 Disabled (the clock to GPIO logic is gated) 1 Enabled
14	Read/write	0	RC oscillator force enable (RCO_EN). 0 RCO enabled in AFG D0 and D3hot power states, otherwise disabled. 1 RCO always enabled.
13	Read/write	0	PLL2 enable (PLL2_EN). See PLL1 enable below.
12	Read/write	0	PLL1 oscillator enable (PLL1_EN). 0 Disabled 1 Enabled
11:10	Reserved	00	Reserved
9	Read/write	0	ASP2 null mode select (ASP2_NMS). See ASP1 null mode select below.
8	Read/write	0	ASP1 null mode select (ASP1_NMS). Null sample mode select. 0 NFS encoding 1 NSB encoding
7	Read/write	0	ASP2 slave clocks from APS1 (ASP2_SLV_CLKS). Selects the LRCK and SCLK source for ASP2. 0 Independent 1 ASP2 uses ASP1 LRCK and SCLK
6:4	Read/write	000	NSB select (NSB_SEL). Null sample bit select, determines the bit used to encode null samples in NSB Mode. 000 Bit 0 … 110 Bit 6 001 Bit 1 … 111 Bit 7
3	Read/write	0	I²C master internal clock enable (I2C_EN). Controls clock gating for I²C master block. 0 I²C port clock gated 1 I²C port clock enabled
2	Read/write	0	SPI master clock enable (SPI_EN). Controls clock gating for SPI master block. 0 SPI port clock gated 1 SPI port clock enabled
1	Read/write	0	UR gating (URG). Allows URs to be gated after entering D3hot before CLKSTOP. After clocking is stopped, queued URs are propagated as power state change requests. 0 Normal propagation of URs 1 URs are gated if AFG is in D3
0	Read/write	0	Disable coefficient index autoincrement (DAI). Specifies whether the coefficient index value automatically increments after a read or write operation. 0 Autoincrement on 1 Autoincrement off

6.11.8.2 Device Configuration 2

Table 6-168. Device Configuration 2 (CIR = 0x0001)

Bits	Type	Default	Description
15	Read/write	1	SPI internal timing source select. (SPI_TIM) Selects where the SPI logic sources the data capture/launch edge. 0 From IO pad (retimed SPI_SCLK) 1 Before output buffer
13:14	Read only	00	Reserved
12:10	Read/write	000	PLL2 frequency select (PLL2_FRQSEL). See below.

Table 6-168. Device Configuration 2 (CIR = 0x0001) *(Cont.)*

Bits	Type	Default	Description
9:7	Read/write	000	PLL1 frequency select (PLL1_FRQSEL). Selects the PLL1 output frequency. 000 49.152 MHz 001 48 MHz 010 36.864 MHz 011 22.05 MHz 100 22.5792 MHz 101 16 MHz 110 16.384 MHz 111 16.9344 MHz
6	Read/write	0	ASP2 internal clock enable (ASP2_EN). See ASP1 internal clock enable below
5	Read/write	0	ASP1 internal clock enable (ASP1_EN). 0 ASP1 logic clock gated. 1 ASP1 logic clock enabled.
4	Read/write	0	ASP2 slave (ASP2_SLV). See ASP1 slave below
3	Read/write	0	ASP1 slave (ASP1_SLV). Determines the master/slave mode of the ASP1 transmitter and receiver. Both blocks always operate in the same mode. 0 Master Mode 1 Slave Mode
2	Read/write	0	ASP2 LRCK start phase (ASP2_STP). See ASP1 LRCK Start Phase below.
1	Read/write	0	ASP1 LRCK start phase (ASP1_STP). Determines which LRCK state (high or low) begins a frame 0 Frame starts at LRCK/FSYNC falling edge (I^2S type) 1 Frame starts at LRCK/FSYNC rising edge (left-justified, TDM type)
0	Read/write	0	ASP1/2 sync together (ASP_SYNC). Determines whether the ASP1.n RX and ASP2.n RX widgets capture a single synchronized stream and whether the ASP1.n TX and ASP2.n TX widgets render a single synchronized stream. 0 ASP1 and ASP2 synchronize separately (form two synchronization groups) 1 ASP1 and ASP2 synchronize as one group.

6.11.8.3 Device Configuration 3

Table 6-169. Device Configuration 3 (CIR = 0x0002)

Bits	Type	Default	Description
15:14	Read/write	00	ASP2 Hi-Z delay (ASP2_HIZD). See ASP1 Hi-Z delay below.
13:12	Read/write	00	ASP1 Hi-Z delay (ASP1_HIZD). Controls the delay from last nonidle clock edge and the idle Hi-Z, if enabled. 00 12-ns delay 01 17-ns delay 10 22-ns delay 11 Hi-Z delay to next SCLK edge
11:10	Read/write	00	ASP2 bus idle behavior (ASP2_BUS_IDLE). See ASP1 bus idle below.
9:8	Read/write	00	ASP1 bus idle behavior (ASP1_BUS_IDLE). Controls the serial port output state when idle. 00 Hi-Z 01 Hi-Z 10 Pull down 11 Pull up
7	Read/write	0	GPIO/I^2C alternate function select (GPIO_I2C). 0 GPIO function 1 I^2C function (SCL, SDA)
6	Read/write	0	SPI output enable (SPI_OE). Controls the SPI_SCLK and MOSI output drive enable. 0 Disabled (Hi-Z) 1 Output enabled
5:4	Read only	00	Reserved
3	Read/write	0	GPIO-MISO2 alternate function select (GPIO_MISO2). 0 GPIO 1 SPI function (MISO2)
2	Read/write	0	GPIO-CS2 alternate function select (GPIO_CS2). See GPIO-CS1 alternate function select below.
1	Read/write	0	GPIO-CS1 alternate function select (GPIO_CS1). 0 GPIO 1 SPI function, chip select (CS1)
0	Read/write	0	GPIO-MISO1 alternate function select (GPIO_MISO1). 0 GPIO 1 SPI function (MISO1)

6.11.8.4 ASP Clock Configuration

Table 6-170. Serial Port Clock Generation Register Overview

Coefficient Index Register (CIR)	Description
0x0003	ASP1 Clock Control 1
0x0004	ASP1 Clock Control 2
0x0005	ASP1 Clock Control 3
0x0006	ASP2 Clock Control 1

Table 6-170. Serial Port Clock Generation Register Overview *(Cont.)*

Coefficient Index Register (CIR)	Description
0x0007	ASP2 Clock Control 2
0x0008	ASP2 Clock Control 3

Table 6-171. ASPx Clock Control 1 (CIR = 0x0003, 0x0006)

Bits	Type	Default	Description
15	Read/write	1	ASPx internal timing source select (ASP1_TIM, ASP2_TIM). Selects where the serial port logic sources the data capture/launch edge. 0 From I/O pad (retimed from ASPx_SCLK) 1 Before output buffer
14:9	Read only	0	Reserved
8:0	Read/write	0	ASPx LRCK high duration (ASP1_LCHI, ASP2_LCHI) 0x000 1 SCLK:FS 0x001 2 SCLK:FS 0x1FF 512 SCLK:FS

Table 6-172. ASPx Clock Control 2 (CIR = 0x0004, 0x0007)

Bits	Type	Default	Description
15	Read/write	0	ASPx Double Sample Mode enable (ASP1_DR, ASP2_DR). 0 Normal 1 Channel slots recount from rising and falling edges (double rate)
14:13	Read/write	00	ASPx MCLK source select (ASP1_MC_SRCSEL, ASP2_MC_SRCSEL). See ASPx SCLK source select below.
12:11	Read/write	00	ASPx SCLK source select (ASP1_SC_SRCSEL, ASP2_SC_SRCSEL)[1]. 00 BCLK 10 PLL2 01 PLL1 11 Reserved
10:9	Read only	00	Reserved
8:0	Read/write	1_1111_0011	ASPx LRCK period, SCLK periods per Fs (ASP1_LCPR, ASP2_LCPR) 0x000 1 SCLK:FS 0x001 2 SCLK:FS 0x1FF 512 SCLK:FS

1.PLL1 and PLL2 must be enabled before changing the SRCSEL1 bits to change the PLL selection MUX.

Table 6-173. ASPx Clock Control 3 (CIR = 0x0005, 0x0008)

Bits	Type	Default	Description
15	Read/write	0	ASPx LRCK fixed 50/50 duty (ASP1_5050, ASP2_5050). 0 Programmable duty cycle See ASP clock control 1 (Table 6-171) 1 50% duty cycle. If ASPx_5050 = 1, the corresponding ASPx_LCHI must be programmed to half the ASPx_LCPR (see Table 6-171)
14	Read/write	0	ASPx LRCK output drive polarity (ASP1_LCPOL_OUT, ASP2_LCPOL_OUT). 0 Normal 1 Output polarity inverted
13	Read/write	0	ASPx LRCK input polarity, pad to logic (ASP1_LCPOL_IN, ASP2_LCPOL_IN). 0 Normal 1 Input polarity inverted
12	Read/write	0	ASPx MCLK output drive polarity (ASP1_MCPOL_OUT, ASP2_MCPOL_OUT). 0 Normal 1 Output polarity inverted
11	Read/write	0	ASPx MCLK generation enable (ASP1_MCEN, ASP2_MCEN) 1 MCLK generation enabled 0 MCLK disabled, MCLK is drive low if ASPx_MCLK_EN = 1.
10:8	Read/write	000	ASPx MCLK divider select (ASP1_MCDIV, ASP2_MCDIV) 000 Divided by 1 001 Divided by 2 … NNN Divided by 2^N… 110 Divided by 64 111 Divided by 128
7:5	Read/write	000	ASPx frame start delay (ASP1_FSD, ASP2_FSD) 000 0 delay 010 1 delay 100 2 delay 11x Reserved 001 0.5 delay 011 1.5 delay 101 2.5 delay
4	Read/write	0	ASPx SCLK output drive polarity (ASP1_SCPOL_OUT, ASP2_SCPOL_OUT) 0 Normal 1 Output polarity inverted
3	Read/write	0	ASPx SCLK input polarity, pad to logic (ASP1_SCPOL_IN, ASP2_SCPOL_IN) 0 Normal 1 Input polarity inverted
2:0	Read/write	000	ASPx SCLK divider select (ASP1_SCDIV, ASP2_SCDIV) 000 Divided by 1 001 Divided by 2 … NNN Divided by 2^N… 110 Divided by 64 111 Divided by 128

6.11.8.5 DMIC Configuration

Table 6-174. DMIC Configuration (CIR = 0x0009)

Bits	Type	Default	Description
15	Read/write	0	DMIC VL select (DMIC_VL_SEL). Selects DMIC interface supply voltage. 0 1.8 V 1 3.3 V
14:13	Read only	000	Reserved
12:9	Read only	0000	Reserved
8	Read/write	0	DMIC sync (DMIC_SYNC). Specifies that DMIC1/2 are grouped in order to capture a single synchronized stream.
7:6	Read/write	00	DMIC2 Channel Mode[1:0] (DMIC2_MO). See below.
5:4	Read/write	00	DMIC1 Channel Mode[1:0] (DMIC1_MO). Controls the channel mapping from the ADC output to the HDA bus. 00 DMIC left channel maps to HDA left channel. DMIC right channel maps HDA right channel (normal mode). 01 DMIC left channel maps to both HDA left and right channels. DMIC right channel is discarded (mono mode). 10 DMIC right channel maps to both HDA left and right channels. DMIC left channel is discarded (alternate mono mode). 11 DMIC left channel maps to HDA right channel and DMIC right channel maps to HDA left channel (i.e., Channel Swap Mode).
3:2	Read only	00	Reserved
1	Read/write	1	DMIC2 SR Mode (DMIC2_SR). See DMIC1 SR Mode below.
0	Read/write	1	DMIC1 SR Mode (DMIC1_SR). Specifies how volume and mute changes are implemented for ADC gain control. 0 Immediate change. When this is selected, all level changes take effect immediately in one step. 1 Digital soft ramp. Allows level changes, both muting and gain/attenuation, to be implemented by incrementally ramping at a rate of 1/8 dB per audio sample period, using the digital volume control. To ramp from mute to unity gain (0 dB) requires a total of 775/Fs (~16 ms @ Fs = 48 kHz).

6.11.8.6 Beep Configuration

Table 6-175. Beep Configuration (CIR = 0x000A)

Bits	Type	Default	Description
15:8	Read/write	0x00	ASP2.n Tx beep enable (ASP2_BEEP[15:8])[1]. [15]:ASP2.H, [8]:ASP2.A. See ASP1 Tx beep enable below.
7:0	Read/write	0x00	ASP1.n Tx beep enable (ASP1_BEEP[7:0])[1]. [7]:ASP1.H, [0]:ASP1.A 0 Disable 1 Enable

1.If ASPx_BEEP is set, the corresponding ASPx.n Tx widget does not output stream data; instead, the widget outputs the beep data stream.

6.11.8.7 ASP Null Insert/Remove Control

Table 6-176. ASP Null Insert/Remove Control Register Overview

Coefficient Index Register (CIR)	Description
0x000B	ASP1 Rx Null Insert/Remove
0x000C	ASP1 Rx Rate 1
0x000D	ASP1 Rx Rate 2
0x000E	ASP1 Tx Null Insert/Remove
0x000F	ASP1 Tx Rate 1
0x0010	ASP1 Tx Rate 2
0x0011	ASP2 Rx Null Insert/Remove
0x0012	ASP2 Rx Rate 1
0x0013	ASP2 Rx Rate 2
0x0014	ASP2 Tx Null Insert/Remove
0x0015	ASP2 Tx Rate 1
0x0016	ASP2 Tx Rate 2

Table 6-177. ASPx Rx Null Insert/Remove Control (CIR = 0x000B, 0x0011)

Bits	Type	Default	Description
15:8	Read/write	0x00	ASPx.n Rx insert null (ASP1_RXINS, ASP2_RXINS). [15]:ASPx.H, [8]:ASPx.A 0 Disable 1 Enable
7:0	Read/write	0x00	ASPx.n Rx remove null (ASP1_RXREM, ASP2_RXREM). [7]:ASPx.H, [0]:ASPx.A 0 Disable 1 Enable

Table 6-178. ASPx Rx Rate 1 (CIR = 0x000C, 0x0012)

Bits	Type	Default	Description
15:12	Read/write	0xC	ASPx.A Rx rate (ASP1A_RR, ASP2A_RR). See below.
11:8	Read/write	0xC	ASPx.B Rx rate. See below (ASP1B_RR, ASP2B_RR).
7:4	Read/write	0xC	ASPx.C Rx rate. See below (ASP1C_RR, ASP2C_RR).
3:0	Read/write	0xC	ASPx.D Rx rate (ASP1D_RR, ASP2D_RR). 0000 Reserved 0011 Reserved 0110 22.05 kHz 1001 32 kHz 1100 48 kHz 0001 8 kHz 0100 12 kHz 0111 Reserved 1010 44.1 kHz OtherReserved 0010 11.025 kHz 0101 16 kHz 1000 24 kHz 1011 Reserved

Table 6-179. ASPx Rx Rate 2 (CIR = 0x000D, 0x0013)

Bits	Type	Default	Description
15:12	Read/write	0xC	ASPx.E Rx rate (ASP1E_RR, ASP2E_RR). See below.
11:8	Read/write	0xC	ASPx.F Rx rate (ASP1F_RR, ASP2F_RR). See below.
7:4	Read/write	0xC	ASPx.G Rx rate (ASP1G_RR, ASP2G_RR). See below.
3:0	Read/write	0xC	ASPx.H Rx rate (ASP1H_RR, ASP2H_RR). 0000 Reserved 0011 Reserved 0110 22.05 kHz 1001 32 kHz 1100 48 kHz 0001 8 kHz 0100 12 kHz 0111 Reserved 1010 44.1 kHz OtherReserved 0010 11.025 kHz 0101 16 kHz 1000 24 kHz 1011 Reserved

Table 6-180. ASPx Tx Null Insert/Remove Control (CIR = 0x000E, 0x0014)

Bits	Type	Default	Description
15:8	Read/write	0x00	ASPx.n Tx insert null (ASP1_TXINS, ASP2_TXINS). [15]:ASPx.H, [8]:ASPx.A 0 Disable 1 Enable
7:0	Read/write	0x00	ASPx.n Tx remove null (ASP1_TXREM, ASP2_TXREM). [7]:ASPx.H, [0]:ASPx.A 0 Disable 1 Enable

Table 6-181. ASPx Tx Rate 1 (CIR = 0x000F, 0x0015)

Bits	Type	Default	Description
15:12	Read/write	0xC	ASPx.A Tx Rate (ASP1A_TR, ASP2A_TR). See below.
11:8	Read/write	0xC	ASPx.B Tx Rate (ASP1B_TR, ASP2B_TR). See below.
7:4	Read/write	0xC	ASPx.C Tx Rate (ASP1C_TR, ASP2C_TR). See below.
3:0	Read/write	0xC	ASPx.D Tx Rate (ASP1D_TR, ASP2D_TR) 0000 Reserved 0011 Reserved 0110 22.05 kHz 1001 32 kHz 1100 48 kHz 0001 8 kHz 0100 12 kHz 0111 Reserved 1010 44.1 kHz Other Reserved 0010 11.025 kHz 0101 16 kHz 1000 24 kHz 1011 Reserved

Table 6-182. ASPx Tx Rate 2 (CIR = 0x0010, 0x0016)

Bits	Type	Default	Description
15:12	Read/write	0xC	ASPx.E Tx Rate (ASP1E_TR, ASP2E_TR). See below.
11:8	Read/write	0xC	ASPx.F Tx Rate (ASP1F_TR, ASP2F_TR). See below.
7:4	Read/write	0xC	ASPx.G Tx Rate (ASP1G_TR, ASP2G_TR). See below.
3:0	Read/write	0xC	ASPx.H Tx Rate (ASP1H_TR, ASP2H_TR). 0000 Reserved 0011 Reserved 0110 22.05 kHz 1001 32 kHz 1100 48 kHz 0001 8 kHz 0100 12 kHz 0111 Reserved 1010 44.1 kHz Other Reserved 0010 11.025 kHz 0101 16 kHz 1000 24 kHz 1011 Reserved

6.11.8.8 ASP Sync Control

Table 6-183. ASPx Sync Control Register Overview

Coefficient Index Register (CIR)	Description
0x0017	ASP1 sync control
0x0018	ASP2 sync control

Table 6-184. ASPx Sync Control (CIR = 0x0017, 0x0018)

Bits	Type	Default	Description
15:8	Read/write	0x00	ASPx.n Rx Sync (ASP1_RXSYNC, ASP2_RXSYNC). [15]:ASPx.H, [8]:ASPx.A 0 ASPx.n Rx is not synchronized 1 ASPx.n Rx is synchronized with other widgets
7:0	Read/write	0x00	ASPx.n Tx Sync (ASP1_TXSYNC, ASP2_TXSYNC). [7]:ASPx.H, [0]:ASPx.A 0 ASPx.n Tx is not synchronized 1 ASPx.n Tx is synchronized with other widgets

6.11.8.9 ASP Configuration

Table 6-185. ASP Configuration Register Overview

Coefficient Index Register (CIR)	Description
0x0019	ASP1.A transmit control 1
0x001A	ASP1.A transmit control 2
...	...
0x0027	ASP1.H transmit control 1
0x0028	ASP1.H transmit control 2
0x0029	ASP2.A transmit control 1
0x002A	ASP2.A transmit control 2
...	...
0x0037	ASP2.H transmit control 1
0x0038	ASP2.H transmit control 2
0x0039	ASP1.A receive control 1
0x003A	ASP1.A receive control 2
...	...
0x0047	ASP1.H receive control 1
0x0048	ASP1.H receive control 2
0x0049	ASP2.A receive control 1
0x004A	ASP2.A receive control 2
...	...
0x0057	ASP2.H receive control 1
0x0058	ASP2.H receive control 2

Table 6-186. ASPx.n Transmit Control 1 (CIR = 0x0019, 0x001B, 0x001D, 0x001F, 0x0021, 0x0023, 0x0025, 0x0027, 0x0029, 0x002B, 0x002D, 0x002F, 0x0031, 0x0033, 0x0035, 0x0037)

Bits	Type	Default	Description
15	Read/write	0	ASPx.n Tx left channel mute (ASPxn_TX_LMUTE, e.g., ASP1A_TX_LMUTE). Indicates channel muting. 0 The channel is unmuted. 1 The channel is muted
14	Read only	0	Reserved
13	Read/write	0	ASPx.n Tx left channel active phase (ASPxn_TX_LAP, e.g., ASP1A_TX_LAP). **Note:** This bit is considered only in 50/50 Mode. Otherwise, it is a “don’t care.” 0 Channel location relative to falling LRCK edge 1 Channel location relative to rising LRCK edge
12:10	Read/write	001	ASPx.n Tx left channel size (ASPxn_TX_LSZ, e.g., ASP1A_TX_LSZ). Indicates the size (depth) of each sample. 000 Reserved 010 24 bits 100–101 Reserved 111 Reserved 001 16 bits 011 32 bits 110 Data not available (channel disabled)
9	Read only	0	Reserved
8:0	Read/write	0	ASPx.n Tx left channel location (ASPxn_TX_LCS, e.g., ASP1A_TX_LCS). Selects the start location (lowest slot) for left channel samples in the transmitted ASP data stream. 0x000 Start on 0 SCLK … 0x001 Start on 1 SCLK 0x1F7 Start on 503 SCLK

Table 6-187. ASPx.n Transmit Control 2 (CIR = 0x001A, 0x001C, 0x001E, 0x0020, 0x0022, 0x0024, 0x0026, 0x0028, 0x002A, 0x002C, 0x002E, 0x0030, 0x0032, 0x0034, 0x0036, 0x0038)

Bits	Type	Default	Description
15	Read/write	0	ASPx.n Tx right channel mute (ASPxn_TX_RMUTE, e.g., ASP1A_TX_RMUTE). Determines whether the channel is muted. 0 The channel is unmuted. 1 The channel is muted
14	Read only	0	Reserved
13	Read/write	0	ASPx.n Tx right channel active phase (ASPxn_TX_RAP, e.g., ASP1A_TX_RAP). **Note:** This bit is considered only in 50/50 Mode. Otherwise, it is a “don’t care.” 0 Channel location relative to falling LRCK edge 1 Channel location relative to rising LRCK edge
12:10	Read/write	001	ASPx.n Tx right channel size (ASPxn_TX_RSZ, e.g., ASP1A_TX_RSZ). Indicates the size (depth) of each sample 000 Reserved 010 24 bits 100–101 Reserved 111 Reserved 001 16 bits 011 32 bits 110 Data not available (channel disabled)
9	Read only	0	Reserved
8:0	Read/write	0	ASPx.n Tx right channel location (ASPxn_TX_RCS, e.g., ASP1A_TX_RCS). Selects the start location (lowest slot) for right channel samples in the transmitted ASP data stream. 0x000 Start on 0 SCLK … 0x001 Start on 1 SCLK 0x1F7 Start on 503 SCLK

Table 6-188. ASPx.n Receive Control 1 (CIR = 0x0039, 0x003B, 0x003D, 0x003F, 0x0041, 0x0043, 0x0045, 0x0047, 0x0049, 0x004B, 0x004D, 0x004F, 0x0051, 0x0053, 0x0055, 0x0057)

Bits	Type	Default	Description
15	Read/write	0	ASPx.n Rx left channel mute (ASPxn_RX_LMUTE, e.g., ASP1A_RX_LMUTE). Determines whether the channel is muted. 0 The channel is unmuted. 1 The channel is muted
14	Read only	0	Reserved
13	Read/write	0	ASPx.n Rx left channel active phase (ASPxn_RX_LAP, e.g., ASP1A_RX_LAP). **Note:** This bit is considered only in 50/50 Mode. Otherwise, it is a “don’t care.” 0 Channel location relative to falling LRCK edge 1 Channel location relative to rising LRCK edge
12:10	Read/write	001	ASPx.n Rx left channel size (ASPxn_RX_LSZ, e.g., ASP1A_RX_LSZ). Indicates the size (depth) of each sample 000 Reserved 010 24 bits 100–101 Reserved 111 Reserved 001 16 bits 011 32 bits 110 Data not available (channel disabled)
9	Read only	0	Reserved
8:0	Read/write	0	ASPx.n Rx left channel location (ASPxn_RX_LCS, e.g., ASP1A_RX_LCS). Selects the start location (lowest slot) for left channel samples in the received ASP data stream. 0x000 Start on 0 SCLK … 0x001 Start on 1 SCLK 0x1F7 Start on 503 SCLK

Table 6-189. ASPx.n Receive Control 2 (CIR = 0x003A, 0x003C, 0x003E, 0x0040, 0x0042, 0x0044, 0x0046, 0x0048, 0x004A, 0x004C, 0x004E, 0x0050, 0x0052, 0x0054, 0x0056, 0x0058)

Bits	Type	Default	Description
15	Read/write	0	ASPx.n Rx right channel mute (ASPxn_RX_RMUTE, e.g., ASP1A_RX_RMUTE). Determines whether the channel is muted. 0 The channel is unmuted. 1 The channel is muted
14	Read only	0	Reserved
13	Read/write	0	ASPx.n Rx right channel active phase (ASPxn_RX_RAP, e.g., ASP1A_RX_RAP). **Note:** This bit is considered only in 50/50 Mode. Otherwise, it is a “don’t care.” 0 Channel location relative to falling LRCK edge 1 Channel location relative to rising LRCK edge
12:10	Read/write	001	ASPx.n Rx right channel size (ASPxn_RX_RSZ, e.g., ASP1A_RX_RSZ). Indicates the size (depth) of each sample 000 Reserved 010 24 bits 100–101 Reserved 111 Reserved 001 16 bits 011 32 bits 110 Data not available (channel disabled)
9	Read only	0	Reserved
8:0	Read/write	0	ASPx.n Tx right channel location (ASPxn_RX_RCS, e.g., ASP1A_RX_RCS). Selects the start location (lowest slot) for right channel samples in the received ASP data stream. 0x000 Start on 0 SCLK … 0x001 Start on 1 SCLK 0x1F7 Start on 503 SCLK

6.11.8.10 I²C Control/Status

Table 6-190. I²C Control/Status Register Overview

Coefficient Index Register (CIR)	Description
0x0059	I²C address
0x005A	I²C data
0x005B	I²C control
0x005C	I²C status
0x005D	I²C quick write
0x005E	I²C quick read

Table 6-191. I²C Address (CIR = 0x0059)

Bits	Type	Default	Description
15:8	Read only	0x00	Reserved
7:1	Read/write	0	Address (I2C_ADR). Specifies the slave device address.
0	Read/write	0	Read/write (I2C_RNW). Sets the read/write bit. 0 Write transaction 1 Read transaction

Table 6-192. I²C Data (CIR = 0x005A)

Bits	Type	Default	Description
15:8	Read only	0x00	Reserved
7:0	Read/write	0x00	Data (I2C_DAT). Specifies the I²C write data for a write transaction and contains I²C read data after a successful read.

Table 6-193. I²C Control (CIR = 0x005B)

Bits	Type	Default	Description
15:12	Read only	0x0	Reserved
11:8	Read/write	0x0	Stretch timeout (I2C_STO). Specifies how long the quick read/write state machine waits for the slave device to stretch the SCL clock before giving up. 0x0 Clock stretching disabled. 0x1 Slave may stretch the clock up to 1 SCL period ($1/f_{SCL}$) … 0xF Slave may stretch the clock up to 15 SCL periods ($15/f_{SCL}$).
7:6	Read only	0	Reserved
5:4	Read/write	00	Speed mode (I2C_MODE). Specifies the speed mode for the next transaction. 00 Standard Mode (f_{SCL} = 100 kHz). 01 Fast Mode (f_{SCL} = 400 kHz). 10 Fast Mode Plus (f_{SCL} = 1 MHz). 11 Reserved
3	Read/write	0	Bus clear (I2C_BC). Initiates a bus clear procedure (send 9 clock pulses) if a slave is holding SDA low.
2	Read/write	0	Start (I2C_START). Generates a START condition.
1	Read/write	0	Stop (I2C_STOP). Generates a STOP condition.
0	Read/write	0	ACK/NACK (I2C_ACK). Sends an ACK (1) or NACK (0) to the slave transmitter.

Table 6-194. I²C Status (CIR = 0x005C)

Bits	Type	Default	Description
15:6	Read only	0	Reserved
5	Read only	0	Idle status (I2C_IDL). Indicates that the I²C bus is idle (SCL sampled high).
4	Read only	0	ACK status (I2C_ACKS). Indicates ACK (1) or NACK (0) from the receiver after the last transaction.
3	Read only [1]	0	I²C quick access complete (I2C_QC). Indicates the status of the quick access state machine. 0 In progress 1 Complete
2	Read only [1]	0	ACK ready (I2C_ARDY). Indicates that the acknowledge bit (ACK or NACK) has been received from the slave device (contained in the ACK status bit).
1	Read only [1]	0	Read ready (I2C_RRDY). Indicates data byte ready when performing a read transaction.
0	Read only [1]	0	Write ready (I2C_WRDY). Indicates data byte empty when performing a write transaction.

1. These bits are sticky and trigger a UR when transitioning from 0 to 1, but not when transitioning from 1 to 0. Any write to the I²C control, I²C quick write, I²C quick read, or I²C data register resets the sticky bits to 0. A successfully sent UR or reading this register does not reset the sticky bits.

If multiple UR triggers for this node occur at the same time due to status bit state changes, only a single UR may be generated with all of the status bits correctly updated. See Section 6.11.4 for UR control and format.

Table 6-195. I²C Quick Write (CIR = 0x005D)

Bits	Type	Default	Description
15:8	Read/write	0x00	Subaddress (I2C_QWSA). Specifies the subaddress of the register to be written on the slave device.
7:0	Read/write	0x00	Write data (I2C_QWD). Specifies the data byte to be written to the given subaddress on the slave device.

Table 6-196. I²C Quick Read (CIR = 0x005E)

Bits	Type	Default	Description
15:8	Read/write	0x00	Subaddress (I2C_QRSA). Specifies the subaddress of the register to be read from the slave device.
7:0	Read only	0x00	Read data (I2C_QRD). Specifies the data byte that was read from the given subaddress on the slave device.

See Section 4.6.1 for a functional description of I²C quick-access protocol.

6.11.8.11 SPI Control

Table 6-197. SPI Control/Status Register Overview

Coefficient Index Register (CIR)	Description
0x005F	SPI Control
0x0060	SPI Tx Data
0x0061	SPI Rx Data
0x0062	SPI Status

Table 6-198. SPI Control (CIR = 0x005F)

Bits	Type	Default	Description
15:13	Read only	000	Reserved
12	Read/write	1	SPI clock polarity (SPI_CPOL). Specifies the state of the SPI clock when $\overline{CS}$ is deasserted. 0 SPI clock remains low when $\overline{CS}$ is deasserted 1 SPI clock remains high when $\overline{CS}$ is deasserted
11	Read/write	0	SPI CS select (SPI_CSEL). Select the slave to activate during SPI transactions. 0 Slave one (CS1) selected 1 Slave two (CS2) selected
10:8	Read/write	110	SPI clock frequency select (SPI_FRQ). Selects the SCLK frequency 000 Reserved 010 2 MHz 100 4 MHz 110 12 MHz 001 1.5 MHz 011 3 MHz 101 6 MHz 111 Reserved
7:0	Read/write	0x00	Byte count (SPI_LEN). Specifies how many bytes are transferred in the next SPI transaction.

Table 6-199. SPI Tx Data (CIR = 0x0060)

Bits	Type	Default	Description
15:8	Read/write	0x00	Tx data byte 1 (SPI_TX_DATA[15:8]). Writing this field specifies the first of two data bytes to be shifted out on MOSI.
7:0	Read/write	0x00	Tx data byte 2 (SPI_TX_DATA[7:0]). Writing this field specifies the last of two data bytes to be shifted out on MOSI.

Table 6-200. SPI Rx Data (CIR = 0x0061)

Bits	Type	Default	Description
15:8	Read only	0x00	Rx data byte 1 (SPI_RX_DATA[15:8]). Contains the first of two data bytes that were shifted in on MISO.
7:0	Read only	0x00	Rx data byte 2 (SPI_RX_DATA[7:0]). Contains the last of two data bytes that were shifted in on MISO.

Table 6-201. SPI Status (CIR = 0x0062)

Bits	Type	Default	Description
15:8	Read only	0x00	Reserved
7:0	Read only	0x00	Current byte count (SPI_CNT). Specifies how many bytes have been transferred in the current SPI transaction.

An initial write to the SPI Tx Data register drives $\overline{CS}$ low and shifts out the first 16 bits contained in the SPI Tx data register. Subsequent writes to the SPI Tx data register continue to shift out 16 bits at a time until the number of bytes specified in byte count is reached. After the last byte is transferred, $\overline{CS}$ is driven high and the SPI transaction concludes. If an odd number of bytes is to be transferred, the last transfer shifts out only 8 bits from the SPI data register, and Data Byte 2 is ignored. As bits are shifted out from the SPI data register on MOSI, the bits shifted in by the master on MISO are stored in the SPI data register for the host to read if desired.

6.11.8.12 Parametric Filter Engine

Table 6-202. Parametric Filter Engine Register Overview

Coefficient Index Register (CIR)	Description
0x0063	Parametric filter engine coefficient write 1
0x0064	Parametric filter engine coefficient write 2
0x0065	Parametric filter engine control 1
0x0066	Parametric filter engine control 2
0x0067–0x0068	Prescale attenuation 1, 2
0x0069	Parametric filter engine coefficient monitor 1
0x006A	Parametric filter engine coefficient monitor 2

Table 6-203. Parametric Filter Engine Coefficient Write 1 (CIR = 0x0063)

Bits	Type	Default	Description
15:0	Read/write	0x0000	EQ coefficient data[23:8] (EQ_DATA_HI). Specifies the 16 MSBs of the selected processing coefficient.

Table 6-204. Parametric Filter Engine Coefficient Write 2 (CIR = 0x0064)

Bits	Type	Default	Description
15	Read/write	0	EQ write coefficient (EQ_WRT). Set when writing a coefficient value, clear when reading a coefficient value.
14	Read/write	0	EQ coefficient access (EQ_ACC). Set when reading or writing coefficients, clear for normal operation. **Note:** If this bit is set, the corresponding EQ block (as per EQ select) is bypassed.
13:8	Read/write	0x00	EQ coefficient address (EQ_ADR). Specifies the coefficient address (0 to 39).
7:0	Read/write	0x00	EQ coefficient data[7:0] (EQ_DATA_LO). Specifies the 8 LSBs of the selected processing coefficient.

Table 6-205. Parametric Filter Engine Control 1 (CIR = 0x0065)

Bits	Type	Default	Description
15	Read only	0	Reserved
14	Read/write	0	EQ select (EQ_SEL). Selects which set of coefficients is being addressed for read or write access. 0 EQ1 coefficients (ASP1) 1 EQ2 coefficients.(ASP2)
13:8	Read only	0	Reserved
7:4	Read/write	0x0	EQ2 enable (EQ2_EN). Enables the parametric EQ for ASP2. See below
3:0	Read/write	0x0	EQ1 enable (EQ1_EN). Enables the parametric EQ for ASP1.A–ASP1.D. [0]: ASP1.A, [3]: ASP1.D 0 Disabled 1 Enabled

Table 6-206. Parametric Filter Engine Control 2 (CIR = 0x0066)

Bits	Type	Default	Description
15:0	Read/write	0x0	Reserved

Table 6-207. EQ1/2 Prescale Attenuation (CIR = 0x0067, 0x0068)

Bits	Type	Default	Description
15:12	Read/write	0x0	Channel 6/7 or ASPx.D prescale attenuation (EQ1_ATEN3, EQ2_ATEN3). See bits 3:0.
11:8	Read/write	0x0	Channel 4/5 or ASPx.C prescale attenuation (EQ1_ATEN2, EQ2_ATEN2). See bits 3:0.
7:4	Read/write	0x0	Channel 2/3 or ASPx.B prescale attenuation (EQ1_ATEN1, EQ2_ATEN1). See bits 3:0.
3:0	Read/write	0x0	Channel 0/1 or ASPx.A prescale attenuation (EQ1_ATEN0, EQ2_ATEN0). Sets prescale attenuation for both channels from 0 to –15 dB in 1-dB steps. 0000 0 dB 0010 –2 dB 1111 –15 dB 0001 –1 dB …

Table 6-208. Parametric Filter Engine Coefficient Monitor 1 (CIR = 0x0069)

Bits	Type	Default	Description
15:0	Read only	0x0000	EQ coefficient monitor[23:8] (EQ_MON_HI). Indicates the 16 MSBs of the selected processing coefficient.

Table 6-209. Parametric Filter Engine Coefficient Monitor 2 (CIR = 0x006A)

Bits	Type	Default	Description
15:8	Read only	0x00	Reserved
7:0	Read only	0x00	EQ coefficient monitor[7:0] (EQ_MON_LO). Indicates the 8 LSBs of the selected processing coefficient.

6.11.8.13 ASP Internal Status Report

Table 6-210. ASP Internal Status Report Register Overview

Coefficient Index Register (CIR)	Description
0x006B–0x006C	ASP1–ASP2 Internal Status
0x006D	ASP1 RX SCLK count
0x006E	ASP1 TX SCLK count
0x006F	ASP2 RX SCLK count
0x0070	ASP2 TX SCLK count
0x0071	ASP UR mask

Table 6-211. ASPx Internal Status (CIR = 0x006B, 0x006C)

Bits	Type	Default	Description
15:13	Read only	000	Reserved
12:8	Read only	0	ASPx RX internal status (ASP1_RX_STAT, ASP2_RX_STAT).[1] [4]: Request overload [2]: LRCK late error [0]: No LRCK [3]: LRCK error [1]: LRCK early error
7	Read only	0	ASPx isochronous rate–filter engine rate mismatch (ASP1_ISO_EQ_ERR, ASP2_ISO_EQ_ERR) [1] **Note:** ASPx_ISO_ERR cannot generate a UR; it is decoded based on ASPx.n TX Rate and EQ enables. 0 No error 1 Isochronous channel frequency does not match filter engine frequency
6:4	Read only	000	Reserved
3:0	Read only	0x0	ASPx TX internal status (ASP1_TX_STAT, ASP2_TX_STAT).[1] [3]: SM error [1]: LRCK early error [2]: LRCK late error [0]: No LRCK

1.Status bits may be cleared by writing a value of one. Reading or writing zero does not clear these bits.

Table 6-212. ASPx RX SCLK Count (CIR = 0x006D, 0x006F)

Bits	Type	Default	Description
15:11	Read only	0	Reserved
10:0	Read only	0	ASPx RX SCLK count (ASP1_RX_SC_COUNT, ASP2_RX_SC_COUNT). Reports the number of SCLKs in the last TDM frame. **Note:** The number of SCLKs reported depends on ASPx_5050 value in CIR = 0x0005/8. See Section 4.2.9.

Table 6-213. ASPx TX SCLK Count (CIR = 0x006E, 0x0070)

Bits	Type	Default	Description
15:11	Read only	0	Reserved
10:0	Read only	0	ASPx TX SCLK count (ASP1_TX_SC_COUNT, ASP2_TX_SC_COUNT). Reports the number of SCLKs in the last TDM frame. **Note:** The number of SCLKs reported depends on the value of the ASPx_5050 bit in CIR = 0x0005/8. See Section 4.2.9.

Table 6-214. ASP UR Mask (CIR = 0x0071)

Bits	Type	Default	Description
15	Read/write	0	ASP2 global UR mask (ASP2_GURM). See ASP1 global UR mask below.
14	Read/write	0	ASP1 global UR mask (ASP1_GURM). Controls the masking of URs from all serial port sources. 0 Masked–ASP1 ASP does not generate URs 1 Unmasked–ASP1 ASP status bits generate URs
13	Read only	0	Reserved
12:8	Read/write	0_0000	ASP RX status UR gate (ASP_RX_URG). When zero, the associated status does not generate a UR. When one, the associated status generates a UR. [4]: Request overload UR [2]: LRCK late error UR [0]: No LRCK UR [3]: LRCK error UR [1]: LRCK early error UR
7:4	Read only	0x0	Reserved
3:0	Read/write	0x0	ASP TX status UR gate (ASP_TX_URG). When zero, the associated status does not generate a UR. When one, the associated status generates a UR. [3]: SM error UR [1]: LRCK early error UR [2]: LRCK late error UR [0]: No LRCK UR

6.11.8.14 Loopback Control

Table 6-215. Loopback Control (CIR = 0x0080)

Bits	Type	Default	Description
15:4	Read only	0x000	Reserved
3	Read/write	0	ASP2 internal loopback enable. (ASP2_INT_LB) See ASP1 internal loopback below.
2	Read only	0	Reserved
1	Read/write	0	ASP1 internal loopback enable. (ASP1_INT_LB) 0 Disabled 1 Enabled
0	Read only	0	Reserved

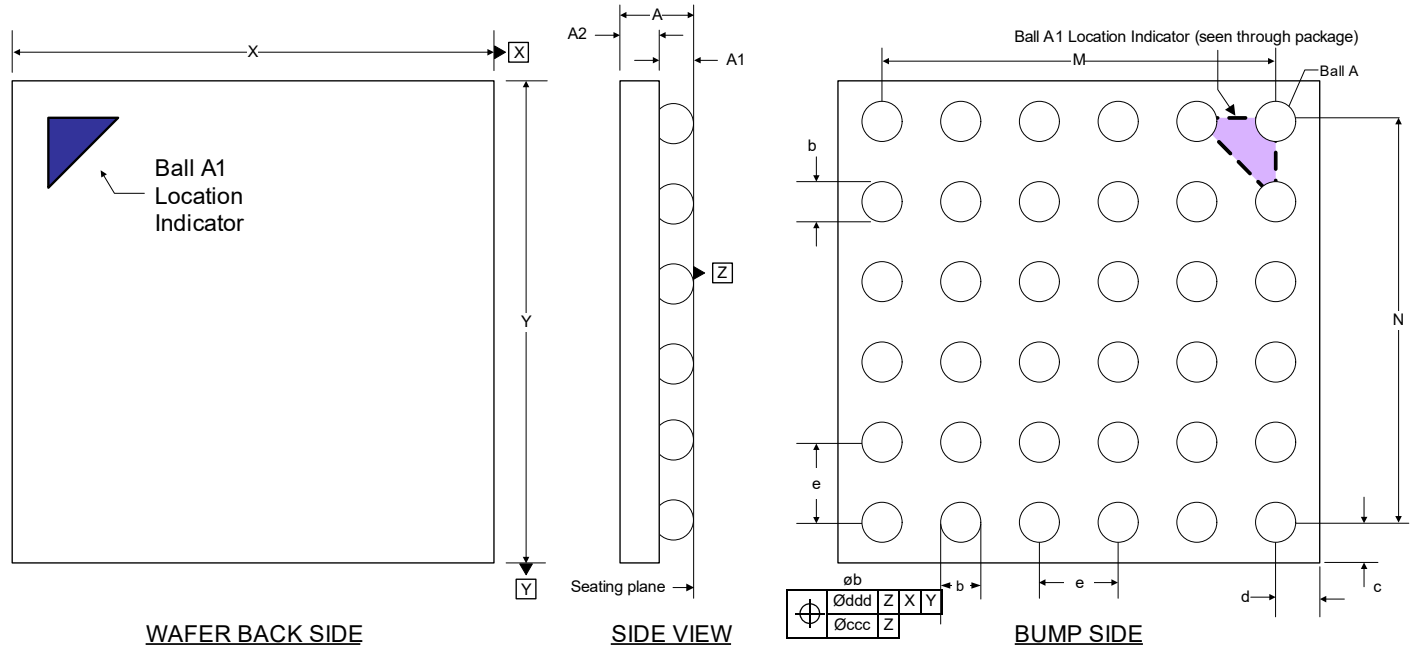
6.11.8.15 Pad Config and Slew Rate Control (CIR = 0x0082)

Table 6-216. Pad Config and Slew Rate Control (CIR = 0x0082)

Bits	Type	Default	Description
15	Read/write	0	ASP2 SDOUT enable. (ASP2_SDOUT_EN) See ASP1 SDOUT enable below.
14	Read/write	0	ASP1 SDOUT enable. (ASP1_SDOUT_EN) 0 Hi-Z, weak pull down 1 Enabled
13	Read/write	0	ASP2 SCLK enable. (ASP2_SCLK_EN) See ASP1 SCLK enabled below.
12	Read/write	0	ASP1 SCLK enable. (ASP1_SCLK_EN) 0 Hi-Z, weak pull down 1 Enabled
11	Read/write	0	ASP2 LRCK/FSYNC enable. (ASP2_LRCK_EN) See ASP1 LRCK/FSYNC enable below.
10	Read/write	0	ASP1 LRCK/FSYNC enable. (ASP1_LRCK_EN) 0 Hi-Z, weak pull down 1 Enabled
9	Read/write	0	ASP2 MCLK enable. (ASP2_MCLK_EN) See ASP1 MCLK enable below.
8	Read/write	0	ASP1 MCLK enable. (ASP1_MCLK_EN) 0 Hi-Z, weak pull down 1 Enabled
7	Read/write	0	I2C slew rate control (I2C_SLEW). Sets the slew rate for GPIO6/SCL and GPIO7/SDA. 0 Fast 1 Slow
6	Read/write	0	ASP2 slew rate control (ASP2_SLEW). See SP1 slew rate control below.
5	Read/write	0	ASP1 slew rate control (ASP1_SLEW). Sets the slew rate for ASP1_MCLK, ASP1_SCLK, ASP1_LRCK/FSYNC, ASP1_SDOUT. 0 Fast (to drive multiple CMOS loads) 1 Slow (to drive standard CMOS load)
4	Read/write	0	GPIO slew rate control (GPIO_SLEW). Sets the slew rate for GPIO2/$\overline{CS2}$, GPIO3/MISO2, GPIO4, and GPIO5. 0 Fast (to drive multiple CMOS loads) 1 Slow (to drive standard CMOS load)
3	Read/write	0	DMICx_CLK slew rate control (DMIC_SLEW). Sets the slew rate for DMIC1_CLK and DMIC2_CLK. 0 Fast 1 Slow
2	Read/write	0	SPI slew rate control (SPI_SLEW). Sets the slew rate for SPI_SCLK, MOSI, GPIO0/MISO1, and GPIO1/$\overline{CS1}$. 0 Fast (to drive multiple CMOS loads) 1 Slow (to drive standard CMOS load)
1	Read/write	0	DMIC2 CLK enable (DM2_CLK_EN) 0 Hi-Z, weak pull down 1 Enable output
0	Read/write	0	DMIC1 CLK enable (DM1_CLK_EN) 0 Hi-Z, weak pull down 1 Enable output

7 Package Dimensions

7.1 WLCSP Package Dimensions



Notes:
- Dimensioning and tolerances per ASME Y 14.5M–1994.
- The Ball A1 position indicator is for illustration purposes only and may not be to scale.
- Dimension “b” applies to the solder sphere diameter and is measured at the midpoint between the package body and the seating plane Datum Z.

Figure 7-1. 36-Ball WLCSP Package Drawing

Table 7-1. 36-Ball WLCSP Package Dimensions

Dim	Millimeters		
	Min	Nom	Max
A	0.450	0.490	0.530
A1	0.175	0.190	0.205
A2	0.275	0.300	0.325
M	BSC	2.000	BSC
N	BSC	2.000	BSC
b	0.240	0.270	0.300
c	REF	0.3525	REF
d	REF	0.3525	REF
e	BSC	0.400	BSC
X	2.680	2.705	2.730
Y	2.680	2.705	2.730
ccc = 0.05 ddd = 0.10			

7.2 QFN Package Dimensions

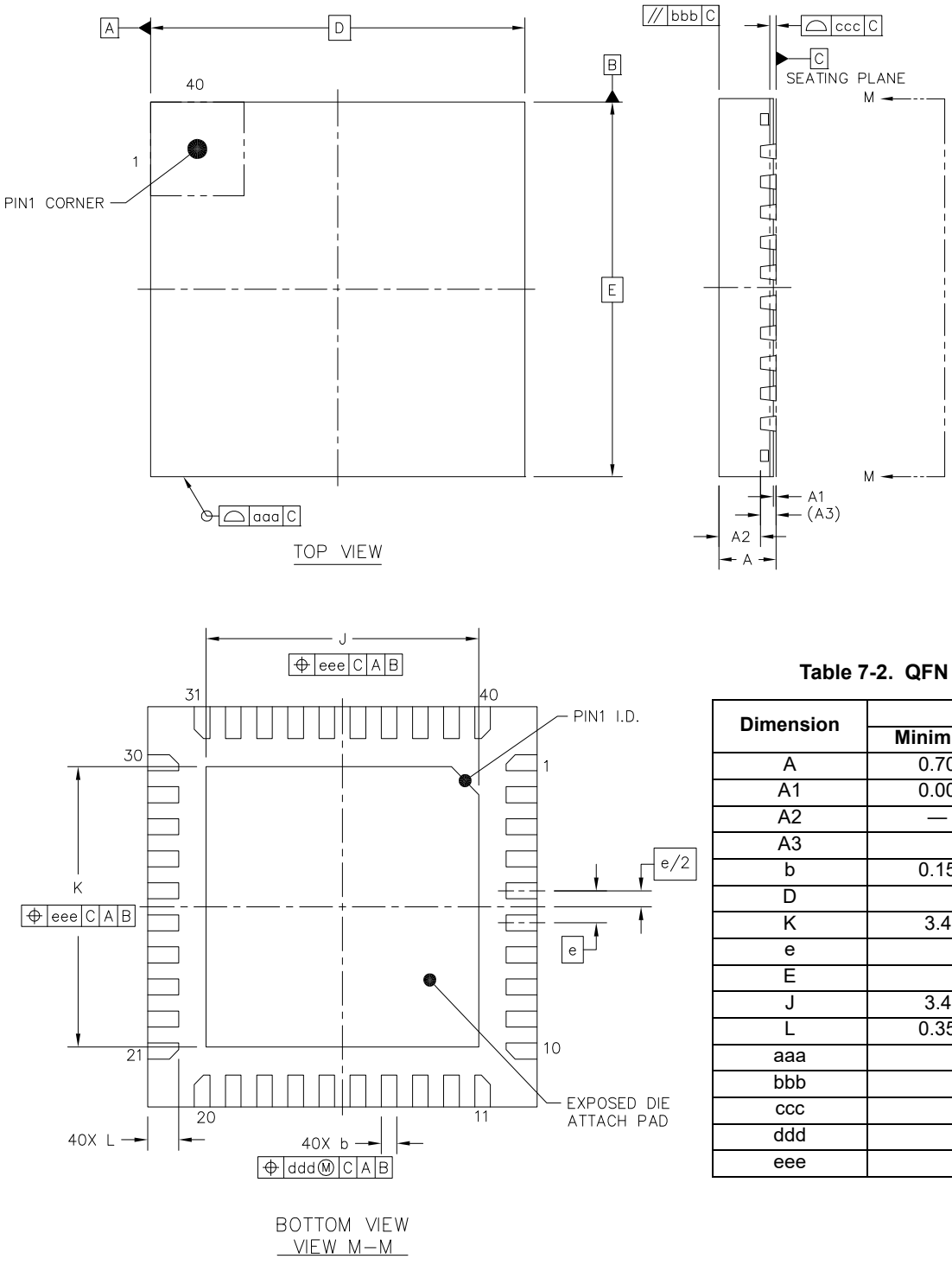
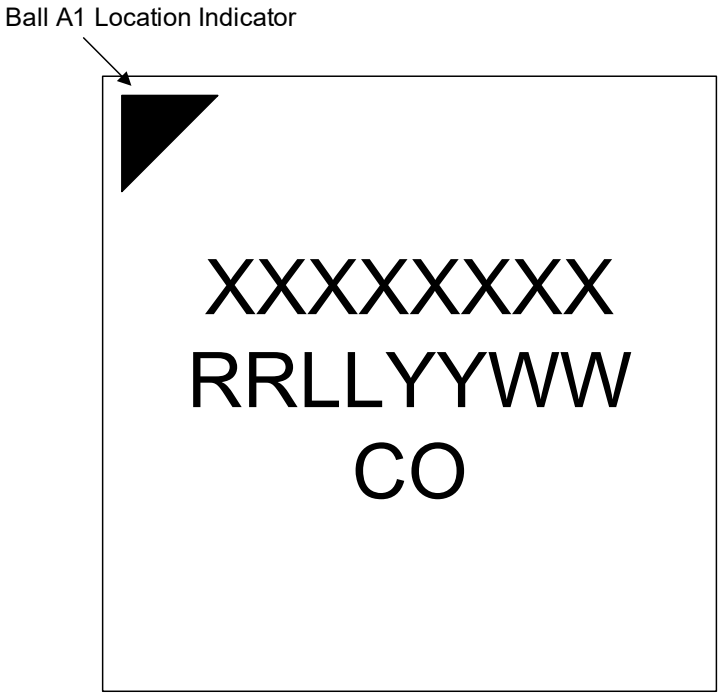


Table 7-2. QFN Package Dimensions

Dimension	mm		
	Minimum	Nominal	Maximum
A	0.70	0.75	0.80
A1	0.00	0.035	0.05
A2	—	0.55	—
A3		0.203 REF	
b	0.15	0.20	0.25
D		5.00 BSC	
K	3.4	3.5	3.6
e		0.40 BSC	
E		5.00 BSC	
J	3.4	3.5	3.6
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

Figure 7-2. QFN Package Dimensions

8 Package Marking



Top Side Brand
Line 1: Part Number
Line 2: Package Mark
Line 3: Country of Origin

Package Mark Fields
RR = Die Rev Code
LL = Lot Sequence Code
YY = Year of Manufacture
WW = Work Week of Manufacture

Figure 8-1. Package Marking

9 Thermal Characteristics

Table 9-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter [1]	Symbol	QFN	WLCSP		Units
			No Underfill	Underfill	
Junction-to-ambient thermal resistance	θ_{JA}	33.3	44.4	44.2	°C/W
Junction-to-board thermal resistance	θ_{JB}	9.3	17.4	17.2	°C/W
Junction-to-case thermal resistance	θ_{JC}	1.03	0.19	0.19	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	9.3	17.3	17.1	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	0.25	0.08	0.08	°C/W

1. Thermal setup:
   Still air @ 85°C
   JEDEC 2S2P printed wiring board
   Size: 114.5 x 101.5 x 1.6 mm
   PCB mounted to six polycarbonate anchor points at 70°C
   PCB dimensions: 25 x 50 x 0.69 mm

10 References

1. Intel Corporation, *High-Definition Audio Specification, Revision 1.0a,* June 17, 2010.
   http://www.intel.com/content/www/us/en/standards/high-definition-audio-specification.html
2. Microsoft, *Universal Audio Architecture Hardware Design Guidelines,* June 12, 2006
   http://download.microsoft.com/download/9/c/5/9c5b2167-8017-4bae-9fde-d599bac8184a/UAA_Guidelines.doc
3. Microsoft, *Pin Configuration Guidelines for High-Definition Audio Devices, Version 1.1,* March 8, 2006
   http://download.microsoft.com/download/9/c/5/9c5b2167-801797-4bae-9fde-d599bac8184a/PinConfig.doc

11 Ordering Information

Table 11-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Order Number
CS8409	Multichannel High-Definition Audio Routing Controller	36-pin WLCSP	Yes	Industrial	–40 to +85°C	Tape and reel	CS8409-CWZR
		40-pin QFN	Yes	Industrial	–40 to +85°C	Tape and reel Rail	CS8409-CNZR CS8409-CNZ

12 Revision History

Table 12-1. Revision History

Revision	Changes
F1 MAY 2018	• Initial release
F2 APR 2019	• Updated Fig. 4-8, clarifying effects of ASPx_SCPOL_IN and ASPx_SCPOL_OUT configuration.
F3 SEP 2020	• Updated to remove Confidential marking

Important:

Please check with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.