CS40L25 Layout Guidelines

INTRODUCTION

This document describes the layout Guidelines for the CS40L25 boosted haptics driver with integrated DSP.

GENERAL BOARD CONSIDERATIONS

1. Avoid routing digital signals between power planes on an adjacent layer.
2. Avoid routing analogue and digital signals next to each other

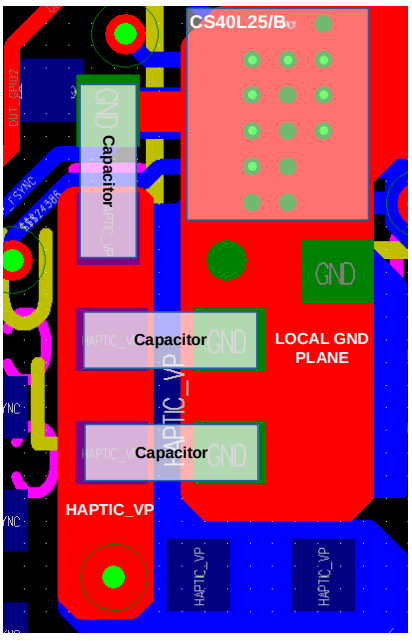
CS40L25 LAYOUT GUIDELINES

VP supply

- Place decoupling capacitors close to the device**.**
- Use power plane for HAPTIC_VP delivery to VP pin.
  - The power plane should be rated for **BST_IPK + 1A**.
  - The power plane should have a low DC resistance. Recommended DC resistance is 1% of Min load. (0.04 Ohms for 4-ohm load)
- A local ground plane should be used for the VBST and VP de-coupling. The local ground plane should be connected to the common ground plane using multiple Vias.

	Min	Typ	Max	Units
VP supply Trace DC Resistance		< 0.04		**Ω**

VP Decoupling Capacitors – Bottom Layer

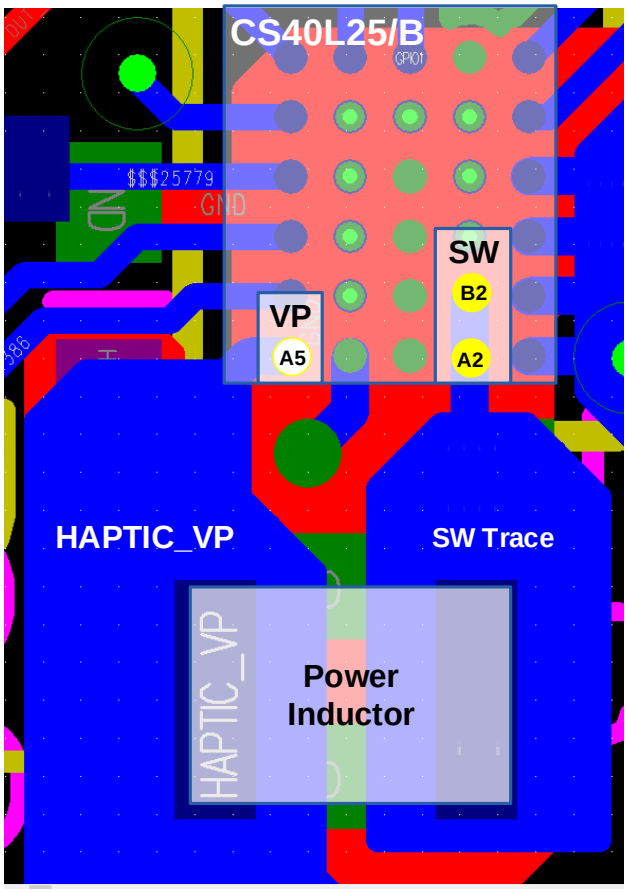


SW supply

- Place inductor close to the device.
- Use power plane for HAPTIC_VP delivery to inductor.
  - The power plane should be rated for **BST_IPK + 1A**.
  - The power plane should have a low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.04 Ohms for 4-ohm load)
- Use multiple Vias to connect HAPTIC_VP plane to the inductor.
- Use wide traces to connect inductor to SW pins.
  - The traces should be rated for **BST_IPK + 1A**.
  - The power plane should have a low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.04 Ohms for 4-ohm load)
- The trace from the inductor to the SW pins should be as short as possible.
- Place 10µF decoupling capacitor as close as possible to the inductor**.**

	Min	Typ	Max	Units
Inductor Supply Trace DC Resistance		< 0.04		**Ω**
SW Supply Trace DC Resistance		< 0.04		**Ω**

Inductor Layout – Top Layer

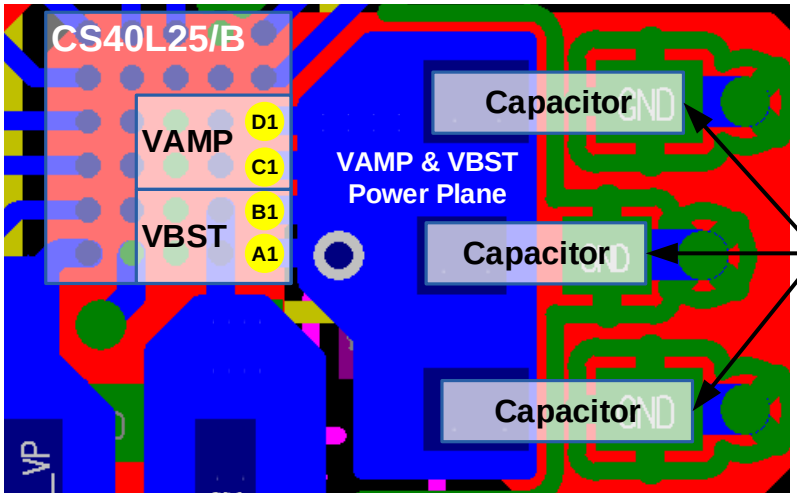


VBST & VAMP routing

- The 0.1µF capacitor should be the closest capacitor to the VBST pins.
- Connect VBST and VAMP together at the pins on the top layer, without connect through VIAs.
  - The traces should be rated for **BST_IPK + 1A**.
  - The power plane should have low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.04 Ohms for 4-ohm load)
- Place VBST capacitors close to the VBST pins.
- A local ground plane should be used for the VBST and VP de-coupling. The local ground plane should be connected to the common ground plane using multiple Vias.

	Min	Typ	Max	Units
VBST & VAMP supply Trace DC Resistance		< 0.04		**Ω**

VBST & VAMP Layout – Top Layer

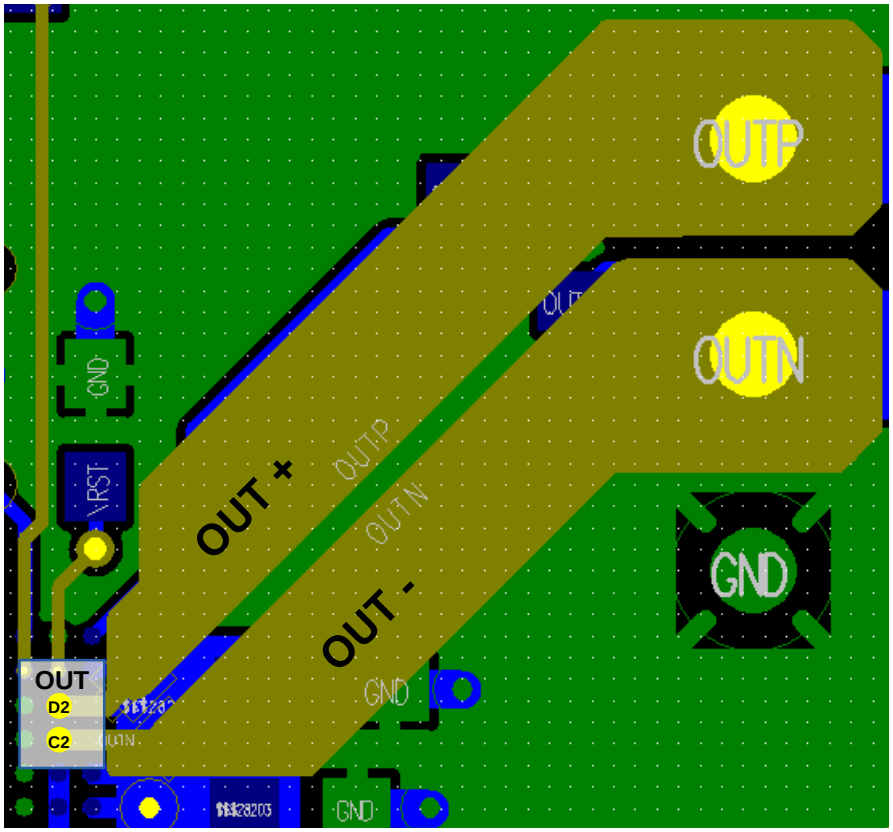


OUT±

- Route OUTP & OUTN as a pair.
- OUTP & OUTN must be routed out on a layer separated from the power supply circuits by a ground plane.
- The OUT± signal tracks should have low DC resistance tracks. Recommended DC resistance is 1% of Min load. (0.04 Ohms for 4-ohm load)

	Min	Typ	Max	Units
OUT± Trace DC Resistance		< 0.04		**Ω**

OUTP & OUTN Layout –Layer 3



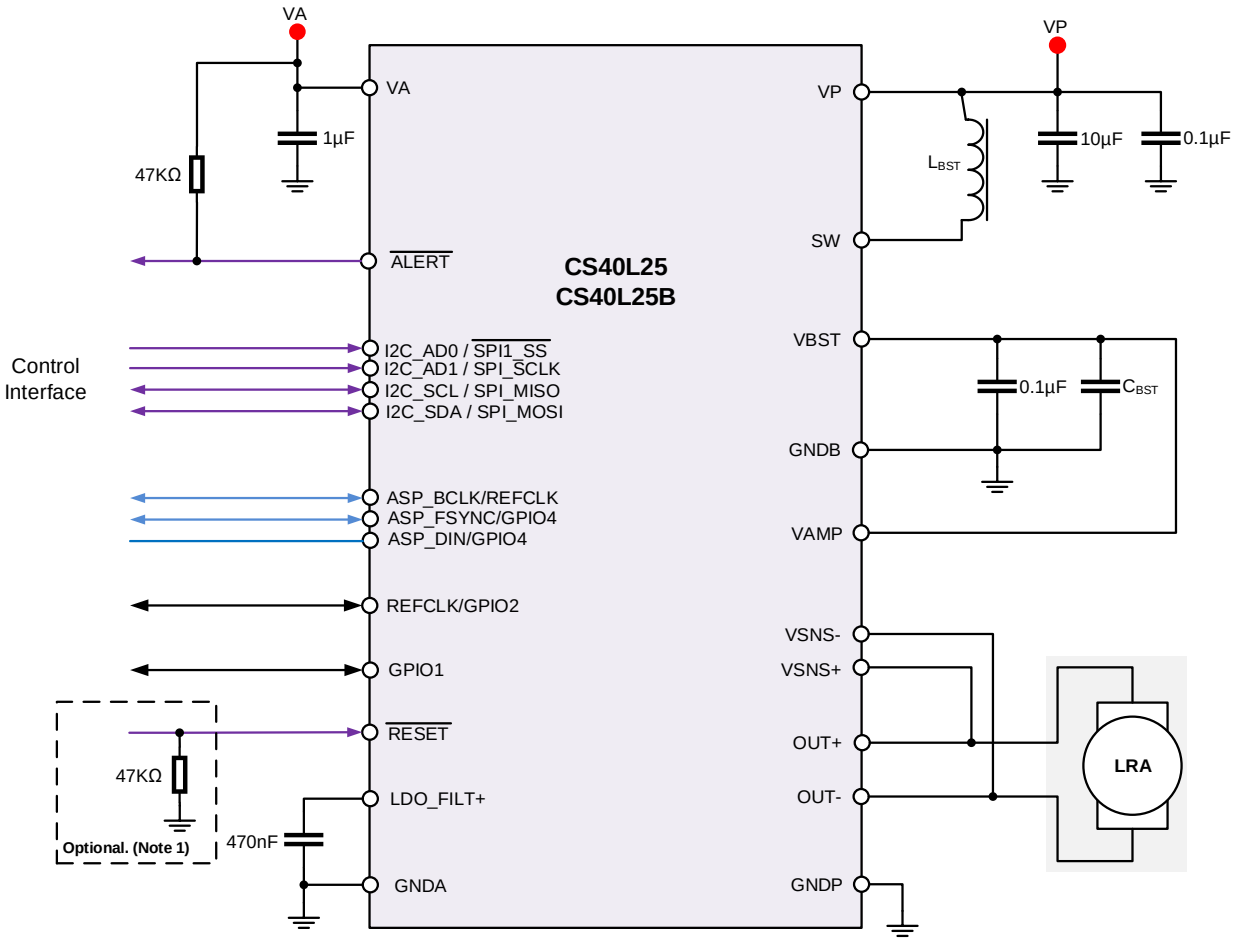
VSENSE

- Route VSNS+ & VSNS- as a pair.
- Provide GND shielding around VSNS±
- VSNS+ & VSNS- should be connected to OUT+ & OUT- traces as close as possible to the load (J1).

Device Decoupling

- Place de-coupling capacitors close to device.

RECOMMENDED EXTERNAL COMPONENTS



Note 1: A pull-down resistor is only required on the RESET pin for systems where the RESET pin is not driven continuously from power-on.

ALERT PIN PULL-UP RESISTOR

The recommended value of ALERT pin pull-up resistor to VA is 47kΩ.

	Minimum	Typical	Maximum	Units
ALERT pull-up resistance		47		kΩ

RESET PIN PULL-DOWN RESISTOR

The recommended value of RESET pin pull-down resistor is 47kΩ. The pull-down resistor is only required for systems where the RESET pin is not driven continuously from power-on

	Minimum	Typical	Maximum	Units
RESET pull-down resistance		47		kΩ

I2C PULL-UP RESISTOR

The I2C interface requires pull-up resistor to the VA supply. The pull-up resistor valve is determined by the following factors.

- Bus capacitance
- Minimum I2C drive strength of ICs on the I2C bus

Cirrus recommends the I2C pull-up resistors should be between 2.2KΩ and 10kΩ

	Min	Typ	Max	Units
I2C pull-up Resistor		2.2k to 10k		**Ω**

C_{BST} CAPACITANCE

The combined C_{BST} capacitance should not de-rate to less than 3.6 µF at 11V.

	Min	Typ	Max	Units
C_{BST} capacitance at 11V	3.6			**µF**

L_{BST} INDUCTANCE

L_{BST} inductor values of 1.0 to 2.2 µH are supported. The L_{BST} inductor must not de-rate to less 0.7 µH during device operation to maintain proper loop stability.

The inductor load rating should not be less than boost convertor current limit, set by **BST_IPK**.

REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
20/07/2018	1.0	Original document created		Craig McAdam

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.