TN0703 CS40L25 Example Power Up Timing

Introduction

The CS40L25 and CS40L25B require two power supplies at different voltage levels and an external reference clock. They are designed to be as flexible as possible to support many different power-up sequences, however, there are some restrictions on power supply voltage levels, the order in which the power supplies come up and the rate at which it rises.

This document provides an example power-up sequence and timing restrictions for that could be used. For complete information about power supply recommendations and power-up sequences, please refer to the datasheet.

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1 Power-Up Example 1: Power Sequencing with Control Port Availability

Two power rails are provided to the chip as follows:

- VP = 2.5 to 5.5V
- VA = 1.66V to 1.94V

The following diagram shows an example power-up sequence. This should be used in conjunction with Table 1, further below.

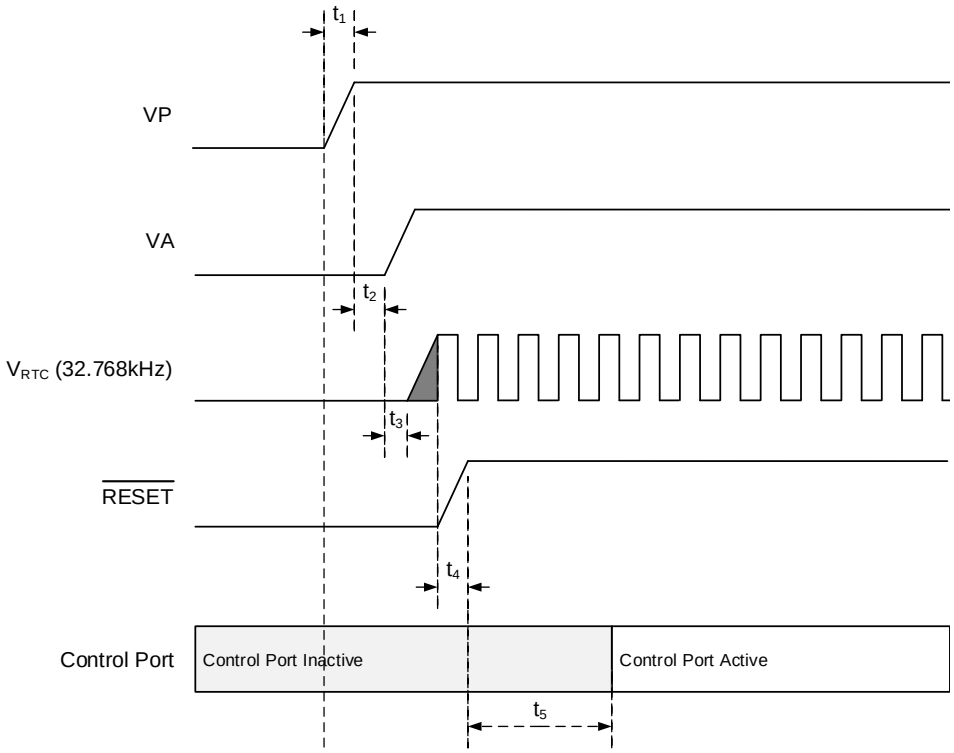

Figure 1: Example Power-Up Sequence 1

Table 1 Timing Restrictions Related to Example Sequence 1

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage ramp up/down (VP) 0-2.5V	t_1	-	-	100	ms
VP high to VA ramp delay	t_2	0			ns
VA high to V_{RTC} (32.768kHz) ramp delay	t_3	0			ns
Delay from 32.768kHz clock source active to RESET_B high	t_4	0			ns
RESET_B High to control port active	t_5			750	us

1. A valid VP voltage must be present whenever a VA voltage is applied.
2. The external 32.768kHz clock source (V_{RTC}) may not be enabled before VA is enabled and must be disabled before VA is disabled.

2 Power-Up Example 2: Boot Buzz Power Up Sequence

Two power rails are provided to the chip as follows:

- VP = 2.5 to 5.5V
- VA = 1.66V to 1.94V

The following diagram shows an example power-up sequence. This should be used in conjunction with Table 2, further below.

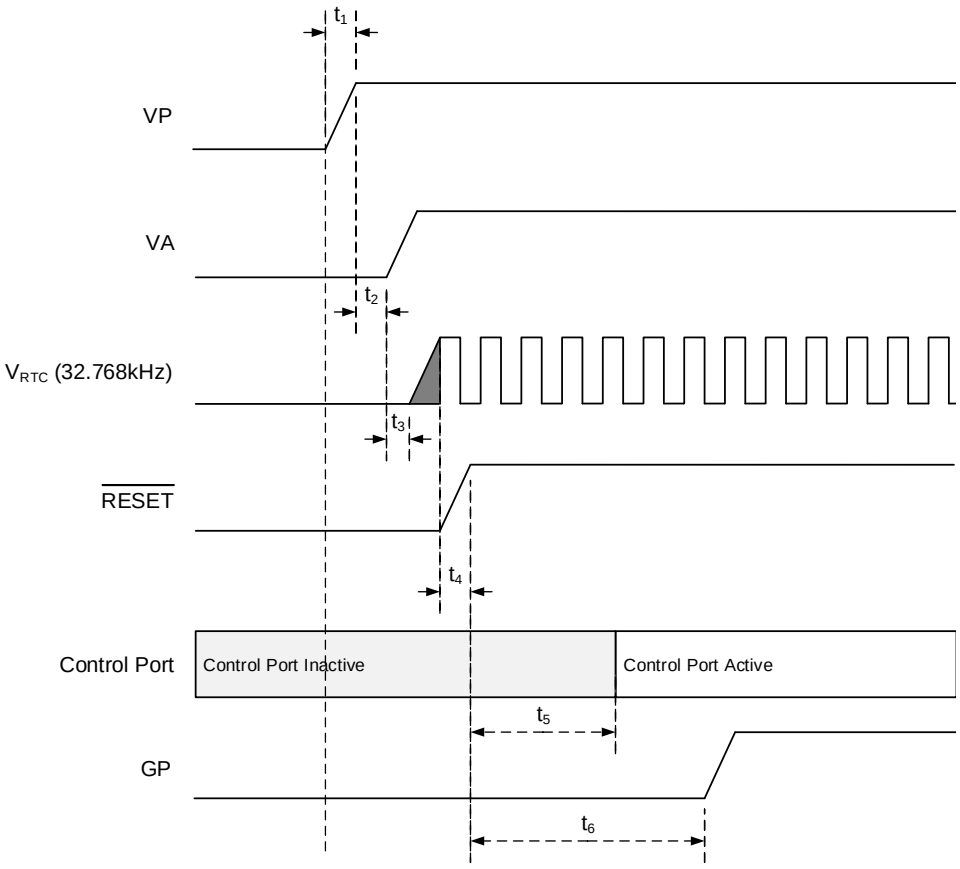

Figure 2: Example Power-Up Sequence 1

Table 2 Timing Restrictions Related to Example Sequence 1

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage ramp up/down (VP) 0-2.5V	t_1	-	-	100	ms
VP high to VA ramp delay	t_2	0			ns
VA high to V_{RTC} (32.768kHz) ramp delay	t_3	0			ns
Delay from 32.768kHz clock source active to RESET_B high	t_4	0			ns
RESET_B High to control port active	t_5			750	us
RESET_B High and V_{RTC} (32.76kHz) to GP ramp delay	t_6			3	s

1. A valid VP voltage must be present whenever a VA voltage is applied.
2. The external 32.768kHz clock source (V_{RTC}) may not be enabled before VA is enabled and must be disabled before VA is disabled.

3 External Reference Clock Guidelines

- The 32.768-kHz reference clock connected to ASP_BCLK/REFCLK or REFCLK/GPIO2 must be enabled and stable after VA is applied and before $\overline{\text{RESET}}$ is de-asserted. The kernel driver de-asserts $\overline{\text{RESET}}$relatively early in its execution, therefore the 32.768-kHz reference clock must be applied before the kernel driver is loaded by the host.
- The CS40L25 and CS40L25B requires a reference clock at all times, even in Always on Haptics (AoH) mode. In AoH mode, the device requires a 32.768-kHz reference clock to process interrupts and render haptic feedback at all times.
- The 32.768-kHz reference clock should not be applied to the device until VA has settled.

4 Revision History

Revision History

Revision	Changes
1.0 JUN 2018	• Initial version.
2.0 SEP 2018	• Timing Diagrams Updated.
3.0 JUL 2020	• Timing Diagrams Updated. • Updated legal boilerplate wording.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.