Q1: If a $0-\Omega$ resistor is placed between the F6 (VDDP) ball and the power supply net (see Fig 1), how much current may pass through it?

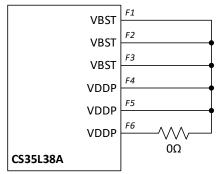


Fig 1: $0-\Omega$ resistor placed on F6 (VDDP)

A1: Each of the VDDP pins are internally connected to the same net on the CS35L38A. There are multiple pins provided on the package to handle the total current demands. In the CS35L38A Schematic and Layout Guidelines (AN0486R1) it is recommended that all VDDP pins are connected together via 8-10 mil traces to a shared copper flood (see Fig 2). That is the expected configuration for the device, and how it has been tested and qualified. Using an alternative configuration such as this proposal has not been tested by Cirrus.

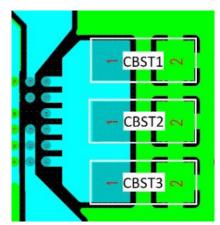


Fig 2: Excerpt from AN0486R1, showing recommended VBST and VDDP routing

The total current drawn by VDDP (balls F4, F5 and F6) will vary according to the maximum power delivery that the system employing CS35L38A has been tuned for. For a first-order approximation, assume half of the total current delivered to the load will flow through F6.

As an example, assuming the output is set to utilise the maximum full-scale input of the IMON path (2.1A), the maximum current flowing into F6 can be assumed to be 1.05A.

As mentioned above, the VDDP pins are expected to be directly connected on the PCB. Adding any component that is unique to one pin only, even a $0-\Omega$ resistor as proposed, may affect the performance of the device. Though it may be rated as $0-\Omega$, it will have a finite resistance that is greater than $0-\Omega$. It will also add some inductance. As a result, it will present different electrical parameters compared to the routing to F4 and F5 and may therefore create a preferential path for the current to flow via F4 and F5 rather than F6. In that scenario, the current is no longer equally shared between the pins as was originally intended.

To ensure each VDDP pin presents a similar electrical path to the shared copper flood, consider using a separate $0-\Omega$ resistor on each trace (F4, F5 and F6) so that the current is shared as intended. Cirrus recommendation remains to connect each VDDP ball as shown in the CS35L38A Schematic and Layout Guidelines (AN0486R1).