CS40L25/B

Boosted Haptics Driver with Integrated DSP and Waveform Memory with Closed Loop Algorithms and LRA Protection

Always on Haptics (AoH) With Ultra Low Latency Wakeup

- Wakeup from AoH Hibernate mode in 5 ms (typ)
- 20 µA in AoH Hibernate mode with RAM retention
- Basic Haptics Mode from ROM at power-on

Haptics Driver Features

- 11 V maximum driver supply voltage for fast startup and braking
- Class-D architecture with adaptive output stage reduces idle power consumption and switching losses
- Compatible with LRA impedances as low as 6 Ω
- Driver short-circuit protection

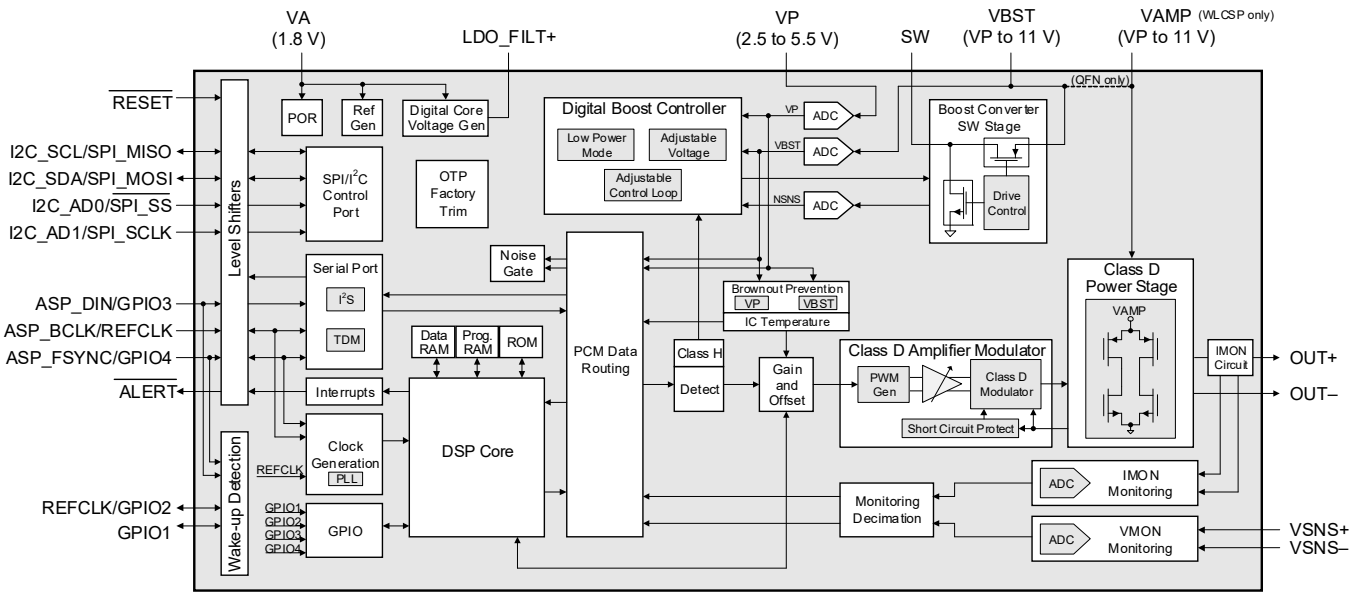
System Protection Features

- IC thermal self-protection against overtemperature
- Battery rail reactive brownout system protection
- Output current sensing via integrated current-monitoring sense resistor
- LRA protection
  - — Coil resistance monitoring
  - — Mass excursion monitoring and over-excursion protection

Cirrus Haptic Suite

- System Level Linear Resonant Actuator (LRA) resonance frequency calibration
- Output voltage and current monitoring for software triggered haptic actuator impedance and resonance frequency reporting
- Pre-stored haptic waveforms triggerable by I²C/GPI for gaming and user interface events
- Flexible haptic waveform generation
  - — I²C/GPI-triggered haptic effects rendered at measured resonant frequency for optimum efficiency
  - — Haptic effects triggered by GPI for home button or side button switch replacement
  - — Compensation in click waveform playback for actuator unit-to-unit variation in resonant frequency and coil resistance

(**Features** continue on p. 2)



Advanced Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

DS1213A4
JUL 2019

Digital Boost Converter Features

- Integrated boost and rectification FETs
- High-bandwidth digital control loop
- 2 MHz switching frequency
- Synchronous rectification in Boost Active Mode
- Programmable boost voltages of up to 11.0 V

Efficiency and Power Consumption

- 85% overall efficiency (boost + driver) at 500 mW output
- Device reset: 2 µA VP supply current (0 µA on VA)
- AoH Hibernate: 20 µA (VA supply current with driver lowest power state, maintaining DSP RAM)

LRA Diagnostic Features

- Coil short detection

Clocking and Data Interface Features

- Haptic data serial port
  - I²S/TDM interface format
  - 48 kHz frame rate
- I²C or SPI control port
  - Programmable I²C slave address
  - Support for I²C Fast Mode Plus (Fm+)
  - Support for 25-MHz SPI

General Description

The CS40L25/B family devices integrate a self-contained haptic signal generator and driver optimized for high performance haptics in switch-replacement type configurations and gaming applications. Hardware and digital signal processing are resonance-aware and designed specifically for optimal drive of highly-resonant linear resonant actuators (LRAs). The CS40L25/B low-power standby and hibernate modes with fast wake upon GPI enable always-available operation.

Both devices integrate a high-performance haptic driver, Halo Core™ DSP, and driver voltage boost converter. The integrated DSP executes all haptic algorithms. The family supports Basic Haptics Mode at power-on with default settings that may be updated by the host. Basic Haptics Mode, which runs from ROM, implements only a subset of the functionality available in the normal configuration executing firmware loaded into RAM by the host. Two device variants are available to support different platform hardware connections. The CS40L25 supports Basic Haptics Mode on hardware platforms with one GPI using the I²S interface. The CS40L25B supports Basic Haptics Mode on hardware platforms which do not use I²S and use four general purpose input pins (GPIs).

The Class D driver features an advanced closed-loop architecture providing superior power supply rejection ratio (PSRR) and a complementary output stage. The digitally controlled boost converter boosts standard-voltage lithium-ion and lithium-polymer battery voltages up to 11 V. The elevated VBST supply generated by the boost converter allows the CS40L25/B to deliver up to 5.3 W into an 6-Ω load at 1% THD+N.

The CS40L25/B family devices include self-protection and system-protection features. The boost and driver stage are protected against short circuits. IC over-temperature shutdown protection is provided in hardware. Battery voltage is continuously monitored. The boost converter and driver gain are automatically adjusted to preserve battery voltage according to programmable voltage/current load-shedding set-points. The battery protection adjustment of the driver is integrated with the IC thermal protection, ensuring seamless coordination of gain rollback if necessary.

The CS40L25/B family devices are available in a commercial-grade 0.4-mm pitch, 30-ball WLCSP chip-scale package or a 32-pin QFN package for operation from -40° to +85°C.

Part Number	Haptic DSP	On-chip ROM inc. Power-On Buzz	RAM download firmware	Core & Digital I/O Power Supply	Boosted Amplifier Power Supply	Boosted Amplifier with Programmable output up to 11.0 V	External Reference Clock	GPI Inputs	Streaming Haptics (I²S)	Control Port	Package	Minimum PCB Layers
CS40L25	✓	✓	✓	1.8 V	2.5 – 5.5 V	✓	32.768 kHz	1 (with I²S/TDM) 3 (w/o I²S/TDM)	✓	SPI or I²C	WLCSP	4
CS40L25B	✓	✓	✓	1.8 V	2.5 – 5.5 V	✓	32.768 kHz	4	×	SPI or I²C	WLCSP, QFN	4 (WLCSP) 2 (QFN)

Table of Contents

1 Pin Descriptions

1.1 Pin Descriptions—30-Ball, 0.40-mm ball-pitch WLCSP (Through-Package View)

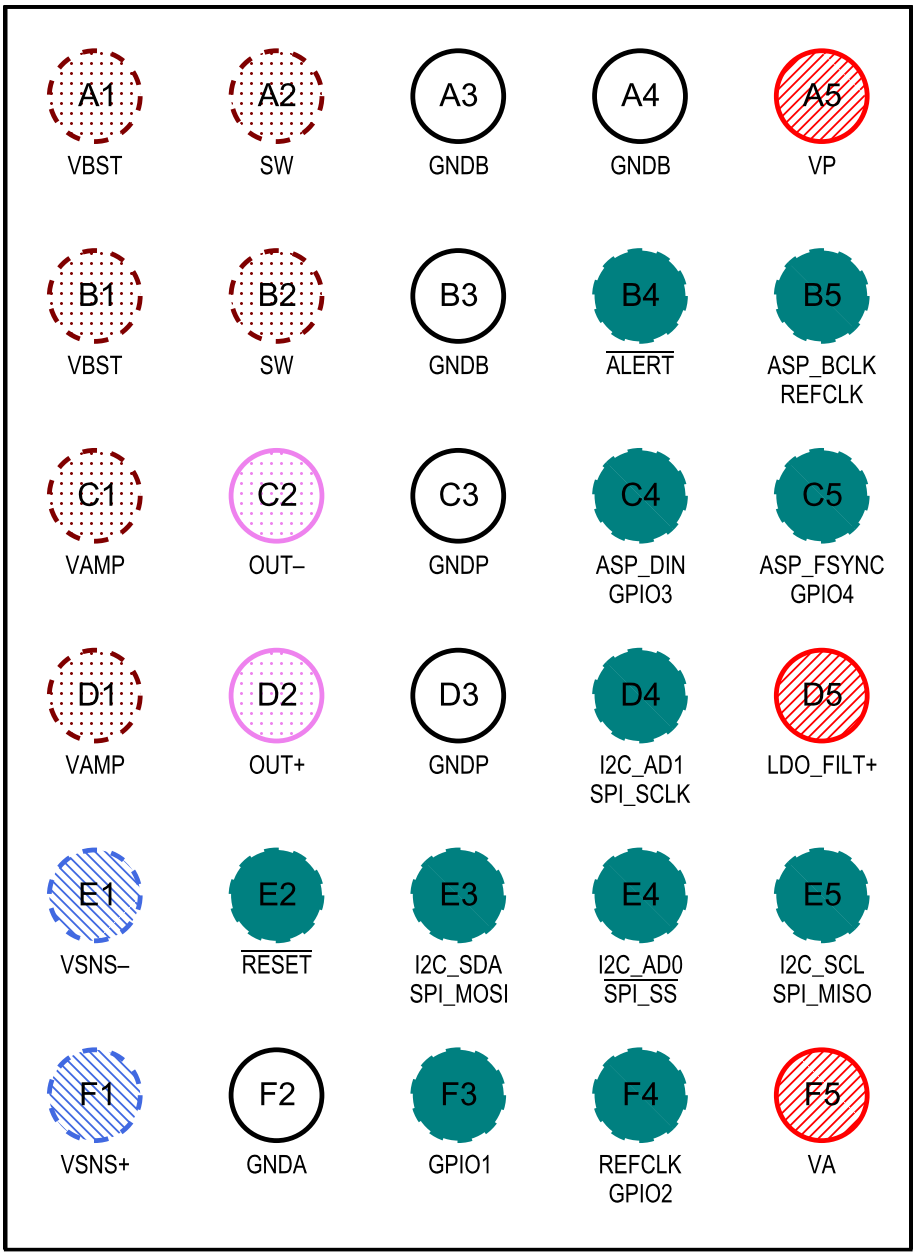


Figure 1-1. Top-Down (Through-Package) View—30-Ball WLCSP Package

Table 1-1. WLCSP Pin Descriptions

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
$\overline{\text{ALERT}}$	B4	VA	O	**Alert.** Active-low, open-drain interrupt output.	Weak pull-down/ Open drain	Weak pull-down
ASP_BCLK/ REFCLK	B5	VA	I	**Serial Clock.** Serial interface bit clock for the CS40L25. **Reference Clock.** Reference Clock input for the CS40L25B.	Weak pull-down	Weak pull-down
ASP_DIN/ GPIO3	C4	VA	I/O	**Serial Data Input.** Serial interface data input for the CS40L25. **General Purpose Input/Output Pin.** Programmable GPIO3 for the CS40L25B (and CS40L25 when using 3 GPIs instead of the serial interface). This input is wake capable in AoH Standby but not in AoH Hibernate.	Weak pull-down	Weak pull-down
ASP_FSYNC/ GPIO4	C5	VA	I/O, I	**Frame Sync.** Serial interface sync input for the CS40L25. **General Purpose Input/Output Pin.** Programmable GPIO4 for the CS40L25B (and CS40L25 when using 3 GPIs instead of the serial interface). This input is wake capable in AoH Standby and AoH Hibernate.	Weak pull-down	Weak pull-down
GNDA	F2	VA	I	**Analog and Digital Ground.** Ground reference for the analog and digital portions of the IC.	—	—
GNDB	A3, A4, B3	VBST	I	**Boost Converter Ground.** Ground reference for the internal boost converter.	—	—
GNDP	C3, D3	VP	I	**Power Ground.** Ground reference for the boost converter and Class-D amplifier's output stage.	—	—
GPIO1	F3	VA	I	**General Purpose Input/Output Pin.** Programmable GPIO, wake capable in AoH Standby and AoH Hibernate. Must be grounded if not used.	—	Hi-Z
I2C_AD0/ $\overline{\text{SPI\_SS}}$	E4	VA	I	**I²C Slave Device Address Select 0.** Used with I2C_AD1, connected to VA or GNDA, to select among four possible addresses. **SPI Control-Port Slave Select.** Active-low SPI Slave Select (SS) input.	—	—
I2C_AD1/ SPI_SCLK	D4	VA	I	**I²C Slave Device Address Select 1.** Used with I2C_AD0, connected to VA or GNDA, to select among four possible addresses. **SPI Control-Port Clock.** SPI clock input.	—	—
I2C_SCL/ SPI_MISO	E5	VA	I, O	**I²C Control Port Clock.** Clock input for the I²C control port. **SPI Control-Port Master In Slave Out.** SPI data output.	—	Hi-Z
I2C_SDA/ SPI_MOSI	E3	VA	I/O, I	**I²C Control-Port Data.** Bidirectional data input/output to/from the I²C control port. **SPI Control-Port Master Out Slave In.** SPI data input.	CMOS/Open drain	Hi-Z
LDO_FILT+	D5	VA	O	**Digital Core LDO Output.** Decoupling point for integrated LDO providing power to the digital core circuitry.	—	—
OUT+	D2	VAMP	O	**Differential Haptic Output, Positive.** Internal Class D amplifier output.	—	—
OUT–	C2	VAMP	O	**Differential Haptic Output, Negative.** Internal Class D amplifier output.	—	—
REFCLK/ GPIO2	F4	VA	I	**Alternate Reference Clock.** Reference Clock input for the CS40L25. **General Purpose Input/Output Pin.** Programmable GPIO2 for the CS40L25B. This input is wake capable in AoH Standby and AoH Hibernate. Must be grounded if not used.	—	—
$\overline{\text{RESET}}$	E2	VA	I	**Reset.** If this pin is driven low, the device enters a low-power mode, all register values are set to their default settings and DSP volatile memory (RAM) contents may be lost.	—	—
SW	A2, B2	VP	I	**Boost Switch.** Input to internal boost FETs. Connect to LBST inductor.	—	—
VA	F5	VA	I	**Analog Power.** Power supply for internal analog and digital sections.	—	—

Table 1-1. WLCSP Pin Descriptions *(Cont.)*

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
VAMP	C1, D1	VAMP	I	**Driver Power.** Power supply input for the Class D amplifier's output stage. Must be connected to VBST externally.	—	—
VBST	A1, B1	VBST	O	**Boosted Supply from Boost Converter.** Internal boost converter output which must be connected to VAMP externally.	—	—
VP	A5	VP	I	**Boost Converter Power.** Power supply for the boost converter and portions of the Class D amplifier.	—	—
VSNS+	F1	VAMP	I	**Voltage Sense Input, Positive.** Sense voltage input for monitoring OUT±.	—	—
VSNS–	E1	VAMP	I	**Voltage Sense Input, Negative.** Sense voltage input for monitoring OUT±.	—	—

1.2 Pin Descriptions—32-Pin, 0.40-mm pitch QFN (Top Down View)

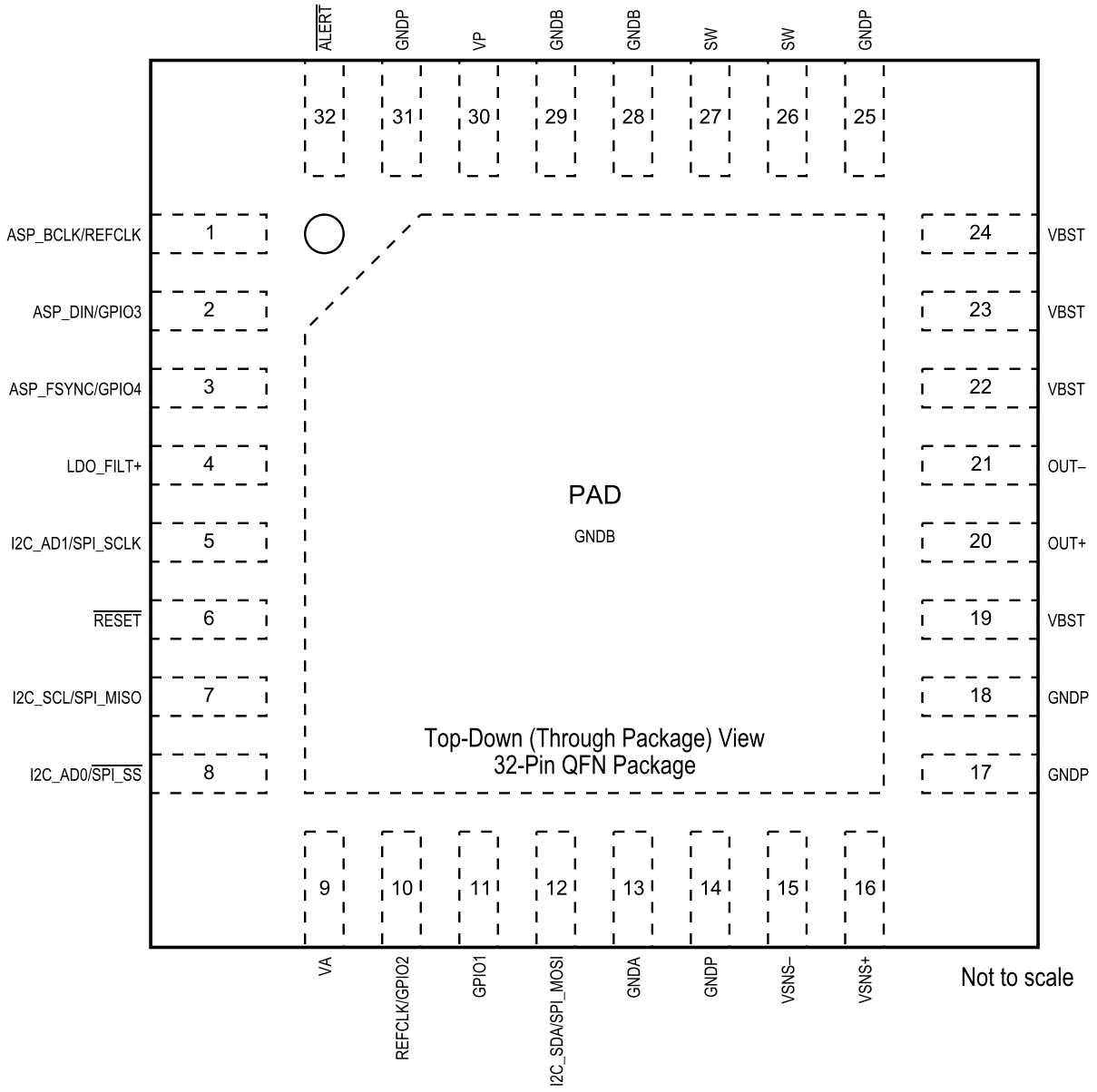


Figure 1-2. Top-Down View—32-Pin QFN Package

Table 1-2. QFN Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description	Internal Connection	State at Reset
$\overline{\text{ALERT}}$	32	VA	O	**Alert.** Active-low, open-drain interrupt output.	Weak pull-down/ Open drain	Weak pull-down
ASP_BCLK/ REFCLK	1	VA	I	**Serial Clock.** Serial interface bit clock for the CS40L25. **Reference Clock.** Reference Clock input for the CS40L25B.	Weak pull-down	Weak pull-down
ASP_DIN/ GPIO3	2	VA	I/O	**Serial Data Input.** Serial interface data input for the CS40L25. **General Purpose Input/Output Pin.** Programmable GPIO3 for the CS40L25B (or CS40L25 when using 3 GPIs instead of the serial interface). This input is wake capable in AoH Standby but not in AoH Hibernate.	Weak pull-down	Weak pull-down
ASP_FSYNC/ GPIO4	3	VA	I/O, I	**Frame Sync.** Serial interface sync input for the CS40L25. **General Purpose Input/Output Pin.** Programmable GPIO4 for the CS40L25B (or CS40L25 when using 3 GPIs instead of the serial interface). This input is wake capable in AoH Standby and AoH Hibernate.	Weak pull-down	Weak pull-down
GNDA	13	VA	I	**Analog and Digital Ground.** Ground reference for the analog and digital portions of the IC.	—	—
GNDB	PAD, 28, 29	VBST	I	**Boost Converter Ground.** Ground reference for the internal boost converter.	—	—
GNDP	14, 17, 18, 25, 31	VP	I	**Power Ground.** Ground reference for the boost converter and Class-D amplifier's output stage.	—	—
GPIO1	11	VA	I	**General Purpose Input/Output Pin.** Programmable GPIO, wake capable in AoH Standby and AoH Hibernate. Must be grounded if not used.	—	Hi-Z
I2C_AD0/ $\overline{\text{SPI\_SS}}$	8	VA	I	**I²C Slave Device Address Select 0.** Used with I2C_AD1, connected to VA or GNDA, to select among four possible addresses. **SPI Control-Port Slave Select.** Active-low SPI Slave Select (SS) input.	—	—
I2C_AD1/ SPI_SCLK	5	VA	I	**I²C Slave Device Address Select 1.** Used with I2C_AD0, connected to VA or GNDA, to select among four possible addresses. **SPI Control-Port Clock.** SPI clock input.	—	—
I2C_SCL/ SPI_MISO	7	VA	I, O	**I²C Control Port Clock.** Clock input for the I²C control port. **SPI Control-Port Master In Slave Out.** SPI data output.	—	Hi-Z
I2C_SDA/ SPI_MOSI	12	VA	I/O, I	**I²C Control-Port Data.** Bidirectional data input/output to/from the I²C control port. **SPI Control-Port Master Out Slave In.** SPI data input.	CMOS/Open drain	Hi-Z
LDO_FILT+	4	VA	O	**Digital Core LDO Output.** Decoupling point for integrated LDO providing power to the digital core circuitry.	—	—
OUT+	20	VBST	O	**Differential Haptic Output, Positive.** Internal Class D amplifier output.	—	—
OUT–	21	VBST	O	**Differential Haptic Output, Negative.** Internal Class D amplifier output.	—	—
REFCLK/ GPIO2	10	VA	I	**Alternate Reference Clock.** Reference Clock input for the CS40L25. **General Purpose Input/Output Pin.** Programmable GPIO2 for the CS40L25B. This input is wake capable in AoH Standby and AoH Hibernate. Must be grounded if not used.	—	—
$\overline{\text{RESET}}$	6	VA	I	**Reset.** If this pin is driven low, the device enters a low-power mode, all register values are set to their default settings and DSP volatile memory (RAM) contents may be lost.	—	—
SW	26, 27	VP	I	**Boost Switch.** Input to internal boost FETs. Connect to LBST inductor.	—	—
VA	9	VA	I	**Analog Power.** Power supply for internal analog and digital sections.	—	—

Table 1-2. QFN Pin Descriptions *(Cont.)*

Pin Name	Pin #	Power Supply	I/O	Description	Internal Connection	State at Reset
VBST	19, 22, 23, 24	VBST	O	**Boosted Supply from Boost Converter.** Internal boost converter output connected to the amplifier supply input inside the package.	—	—
VP	30	VP	I	**Boost Converter Power.** Power supply for the boost converter and portions of the Class D amplifier.	—	—
VSNS+	16	VBST	I	**Voltage Sense Input, Positive.** Sense voltage input for monitoring OUT±.	—	—
VSNS–	15	VBST	I	**Voltage Sense Input, Negative.** Sense voltage input for monitoring OUT±.	—	—

1.3 Termination of Unused Pins

Table 1-3 shows termination requirements for pins while not used in some applications.

Table 1-3. Termination of Unused Pins

Termination	Analog Inputs	Analog Outputs	Digital I/O
Floating	SW	—	$\overline{\text{ALERT}}$, ASP_BCLK/REFCLK, ASP_DIN/GPIO3, ASP_FSYNC/GPIO4
Grounded	—	—	GPIO1, REFCLK/GPIO2

1.4 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS40L25/B is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

2 Typical Connection Diagrams

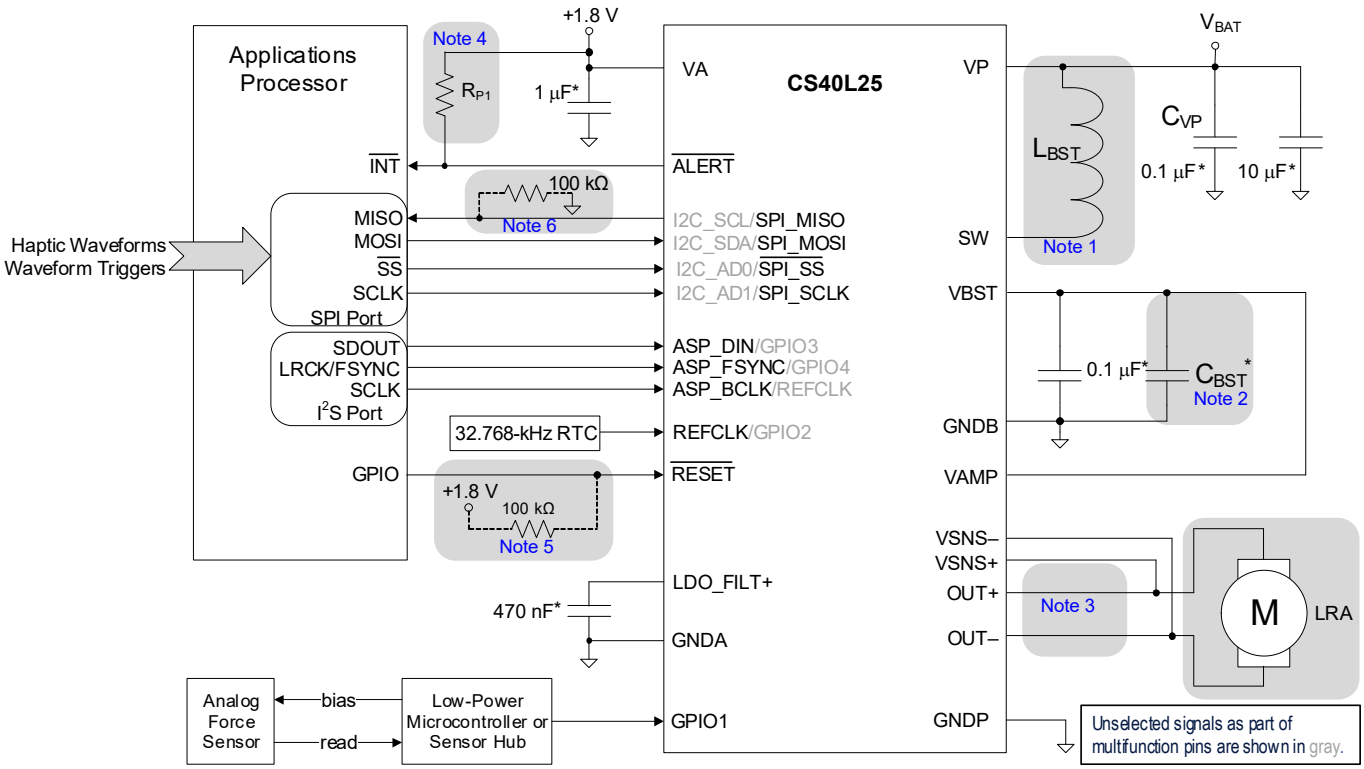


Figure 2-1. Typical Connection Diagram—SPI with GPI and I²S Support

General Notes for Typical Connection Diagrams (see Table 2-1 for specific notes cross-referenced in the figures):

- Fig. 2-1 – Fig. 2-4 are intended to provide a sample of possible connection schemes and does not encompass all variations.
- The CS40L25/B requires a 32.768-kHz clock at all times. Connect the 32.768-kHz clock to the ASP_BCLK/REFCLK or REFCLK/GPIO2 inputs.
- If REFCLK/GPIO2 is used as a playback trigger source, connect the 32.768-kHz clock to the ASP_BCLK/REFCLK input. Note that driving the 32.768-kHz clock into the ASP_BCLK/REFCLK input precludes the use of the auxiliary serial port for I²S.
- All external passive component values listed are nominal values. See Section 5.1 for additional information on recommended external components and derating requirements.
- Use low ESR, X7R/X5R capacitors for capacitors denoted with *.

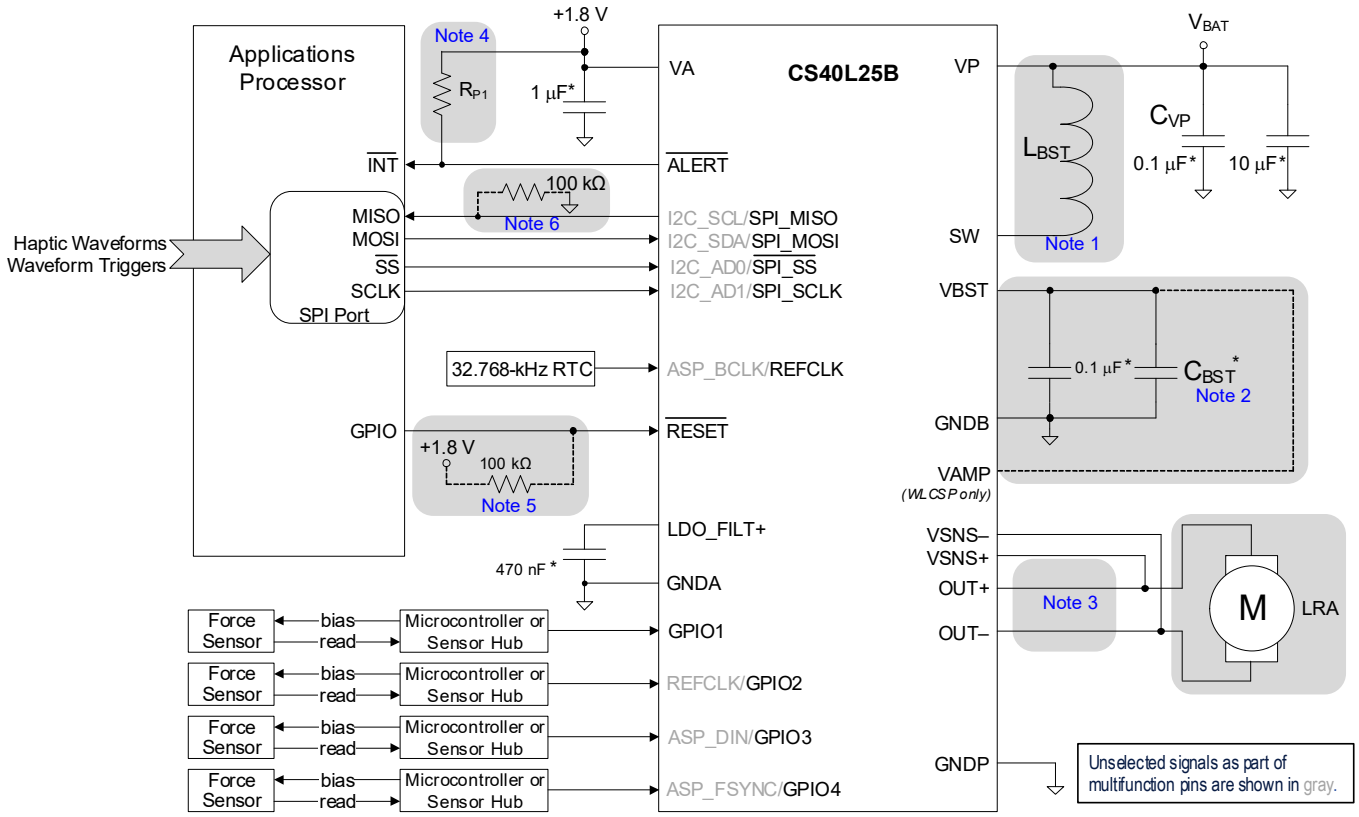


Figure 2-2. Typical Connection Diagram—SPI with Four GPIs and Triggered Waveforms

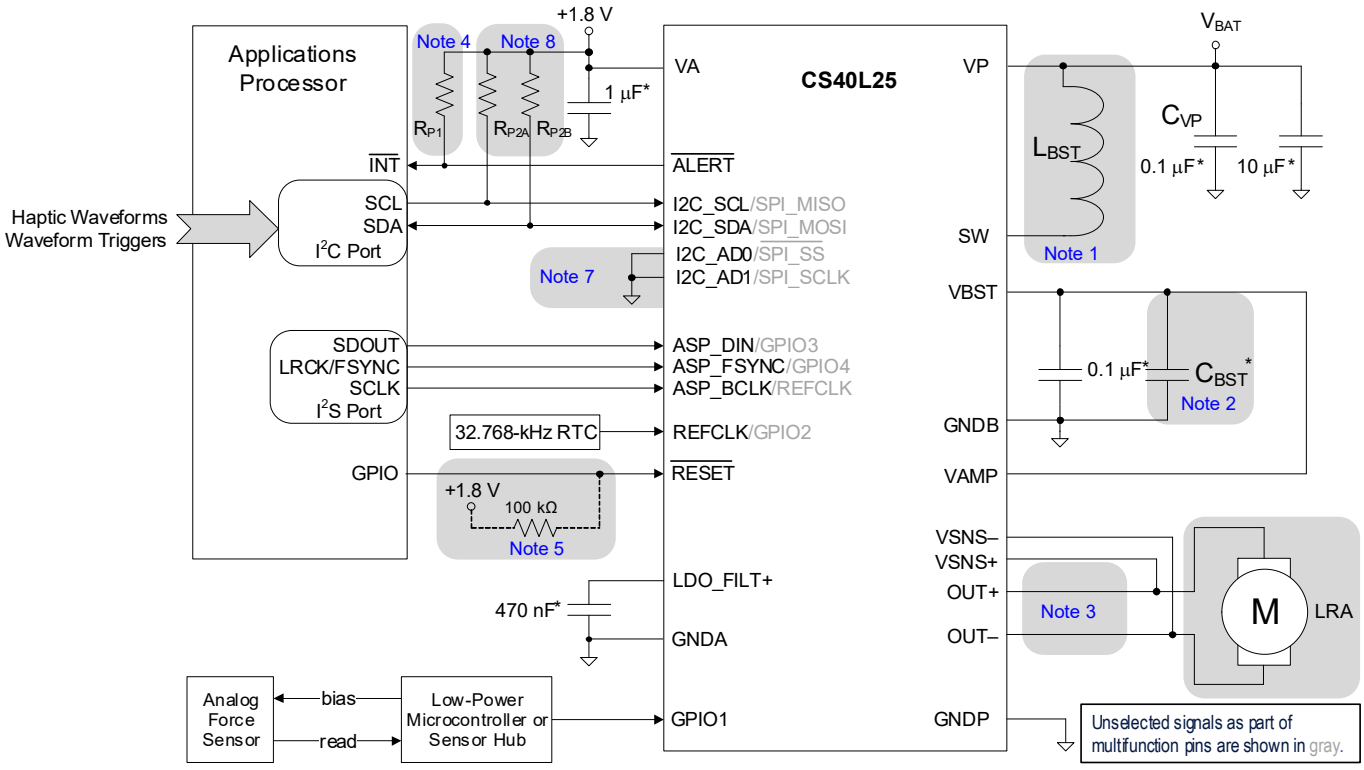


Figure 2-3. Typical Connection Diagram—I²C Interface with GPI and I²S Support

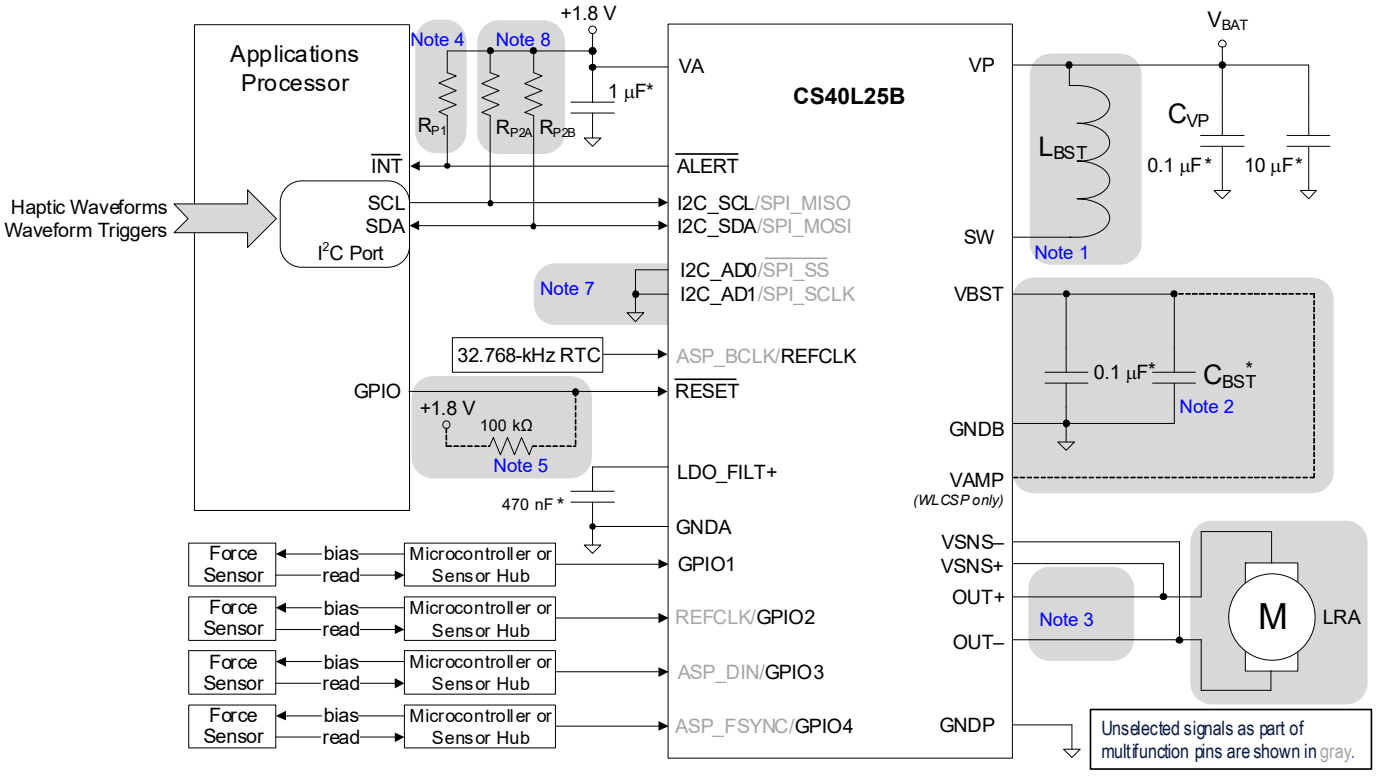


Figure 2-4. Typical Connection Diagram—I²C Interface with Four GPIs and Triggered Waveforms

Table 2-1. Typical Component Values and Types

Module	Description
Boost Converter	1. L_{BST} values of 2.2 to 1.0 µH are supported for typical use operation. See Section 5.1 for more information on component requirements. 2. The C_{BST} capacitor must not derate to a combined capacitance value of less than 3.6 µF with 11.0 VDC applied. The WLCSP package requires a common connection among all VBST and VAMP balls. On the CS40L25B QFN package, there are no external VAMP pins and the amplifier supply input is connected to the boost supply output inside the device. All VBST balls/ pins must be connected together on the PCB and connected to the capacitors shown. See Section 5.1 for more information on component requirements.
Driver	3. Location of optional EMI suppressor capacitors between OUT± and GNDP (typically 470 pF) which may be used in addition to the edge-rate control of the CS40L25/B, depending on the application requirements. It is recommended that the value of these components not exceed 2 nF, as higher capacitances increase switching losses.
Miscellaneous	4. The value for R_{P1} on the $\overline{\text{ALERT}}$ pin may be calculated based on the minimum $\overline{\text{ALERT}}$ pull-down resistance specified in Table 3-12, the minimum level of the 1.8-V supply, and the maximum VIH of the host input driven by the $\overline{\text{ALERT}}$ pin. 5. A pull-up or pull-down on $\overline{\text{RESET}}$ is only required in systems where the $\overline{\text{RESET}}$ pin is not driven continuously from power-on. 6. An external pull-down resistor must be used on the SPI_MISO pin if this pin also connects to the SPI_MISO pin of another SPI slave device in addition to the SPI_MISO pin of the SPI master device.
I²C	7. The CS40L25/B supports four I²C device address options selected by connecting I2C_AD0 and I2C_AD1 to VA or GND. While configured as shown here, the device responds to an address of 0x80 for writes and 0x81 for reads.The I²C address is latched at hardware reset or power-on reset. See Table 4-14 for details. 8. Minimum $R_{P2A/B}$ values may be determined from the maximum VA level, the minimum sink current strength of their respective output, and the maximum low-level output voltage (VOL). Maximum $R_{P2A/B}$ values may be determined by how fast their associated signals must transition, taking into account load capacitance.

3 Characteristics and Specifications

Note: All features and performance specifications here are defined for RAM based operation. ROM based operation in Basic Haptics Mode provides a subset of features and specifications here do not apply unless noted otherwise.

Table 3-1. Recommended Operating Conditions

Test conditions (unless specified otherwise): Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; Device initialization after power-on and reset done as described in Section 4.2.4.

Parameters		Symbol	Minimum	Maximum	Units
DC power supply	Analog (and digital I/O and core) [1]	VA	1.66	1.94	V
	Battery [2]	VP	2.5	5.5	V
	Amplifier with fixed supply voltage [3, 4]	VAMP	VP	11.0	V
	Amplifier with variable supply voltage [4, 5]	VAMP	VP	11.0	V
External voltage applied to analog outputs		V_{INAO}	–0.3	VAMP + 0.3	V
External voltage applied to digital inputs [6]		V_{INDI}	–0.3	VA + 0.3	V
External voltage applied to digital outputs [6]		V_{INDO}	–0.3	VA + 0.3	V
External voltage applied VSNS± pins		$V_{IN-VMON}$	–0.3	VAMP + 0.3	V
Ambient temperature		T_A	–40	+85	°C

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and parametric performance is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. A valid VP voltage must be present whenever a VA voltage is applied. See Table 3-14 for power supply sequencing requirements.
2. Device performance is specified with a VP down to 2.8 V. The CS40L25/B continues to operate functionally down to 2.5 V, but may not meet all parametric specifications.
3. This applies when VAMP is supplied by the on-chip boost converter with a fixed voltage (BST_CTL_SEL = 00).
4. **CAUTION:** To avoid potentially damaging the IC, an external VAMP supply voltage must not be applied on the WLCSP when VP is not present.
5. This applies when VAMP is supplied by the on-chip boost converter with a variable voltage controlled by Class H (BST_CTL_SEL = 01).
6. The maximum over/under voltage is limited by the input current.

Table 3-2. Absolute Maximum Ratings

Test conditions (unless specified otherwise): Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground;

Parameters		Symbol	Minimum	Maximum	Units
DC power supply	Analog	VA	–0.3	2.1	V
	Battery	VP	–0.3	6.0	V
	Amplifier [1]	VAMP	VP–0.3	12.0	V
Input current [2]		I_{in}	—	±10	mA
Ambient operating temperature (local to device, power applied)		T_A	–50	+115	°C
Junction operating temperature (power applied)		T_J	–40	+150	°C
Storage temperature		T_{STG}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-1 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. **CAUTION:** An external VAMP supply voltage must not be applied on the WLCSP when VP is not present.
2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins do not cause SCR latch up.

Table 3-3. Class D Amplifier Load-Independent Output Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show typical connections to, and passive components used with, the CS40L25/B; input test signal is a 24-bit full-scale 997-Hz sine wave with 1 LSB of triangular PDF dither applied; typical performance data taken with VA = 1.8 V, VP = 3.6 V, VAMP = VBST = 11.0 V; min/max performance data taken with VA = 1.80 V, VP = 3.60 V, VAMP is automatically adjusted between VP and 11.0 V by Class H based on signal level; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; T_A = 25°C; AMP_VOL_PCM = 0 dB; AMP_RAMP_PCM = 000; measurement bandwidth is 20 Hz to 20 kHz; Fs = 48 kHz; L_{BST} = 1.0 µH; f_{PLL_OUT} = 196.608 MHz. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameters		Symbol	Minimum	Typical	Maximum	Units
Output switching frequency		f_{AMP_SW}	—	438.857	—	kHz
PFET ON resistance	$I_{OUT(A)}$ = 0.5 A, VBST = 11.0 V[1]	$R_{DSON-AP}$	—	220	—	mΩ
NFET ON resistance	$I_{OUT(A)}$ = 0.5 A, VBST = 11.0 V[1]	$R_{DSON-AN}$	—	130	—	mΩ
Integrated R_{SENSE} resistance[2]		R_{SENSE}	70	100	130	mΩ
Amplifier Low Z to GND detection threshold [3]		Z_{GND_PUP}	1	—	3	Ω

1. VAMP = VBST = 11.0 V supplied by the on-chip boost converter with CLASSH_EN = 1 and BST_CTL_SEL = 01.

2. R_{SENSE} resistance can vary by up to ±30% from typical value. This is also the maximum variation from the typical value that the factory trim can properly compensate for.
3. This detection is in addition to the always-on comparator based amplifier output shorts protection which detects hard shorts to GND, VAMP, and between OUT±. It only occurs on power-up.

Table 3-4. Class D Amplifier Load-Dependent Output Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show typical connections to, and passive components used with, the CS40L25/B; input test signal is a 24-bit full-scale 997-Hz sine wave with 1 LSB of triangular PDF dither applied; typical performance data taken with VA = 1.8 V, VP = 3.6 V, VAMP = VBST = 11.0 V; min/max performance data taken with VA = 1.80 V, VP = 3.60 V, VAMP = 11.0 V; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; T_A = 25°C; measurement bandwidth is 20 Hz–20 kHz AES-17; Fs = 48.0 kHz; L_{BST} = 1.0 µH; f_{PLL_OUT} = 196.608 MHz; simulated load = 8 Ω + 33 µH. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameters				Symbol	Minimum	Typical	Maximum	Units
Power delivered to load @ 1% THD+N (average) [1]		VP = 3.6 V	8-Ω load 6-Ω load	$P_{O@1\%}$	— —	4.3 4.3	— —	W W
Power delivered to load @ 1% THD+N (average) [1]		VP = 4.3 V	8-Ω load 6-Ω load	$P_{O@1\%}$	— —	5.3 5.5	— —	W W
Amplifier operating efficiency[2] @ 10% THD+N		VP = 3.6 V, VAMP = 11.0 V_{DC}	8-Ω load 6-Ω load	η_A	— —	90 89	— —	% %
Total harmonic distortion + noise	P_O = 1.0 W	VAMP = VBST = 11.0 V_{DC} VAMP = VBST = 8.2 V_{DC}	8-Ω load 6-Ω load	THD+N	— —	–74 –71	–61 —	dB dB

1. Powered by the internal boost converter. The amplifier's maximum output power may be limited by the boost converter's maximum load current, $I_{BST\_OUT\_MAX}$ see Table 3-5. This specification assumes BST_IPK = $BST\_IPK_{CTL-MAX}$, and VP voltage is a fixed value as listed in the spec parameters.
2. Amplifier efficiency specified in this table assumes the amplifier output stage is powered from an external voltage supply (on VAMP) instead of the onboard boost converter. This encompasses the power consumption of the amplifier from VAMP as well as the overhead of the IC from VA and VP. See Table 3-7 for the combined efficiency of the entire device, where the amplifier (VAMP) is supplied by the boost converter's output (VBST). Tests for this specification were performed with the generic standard load shown here:

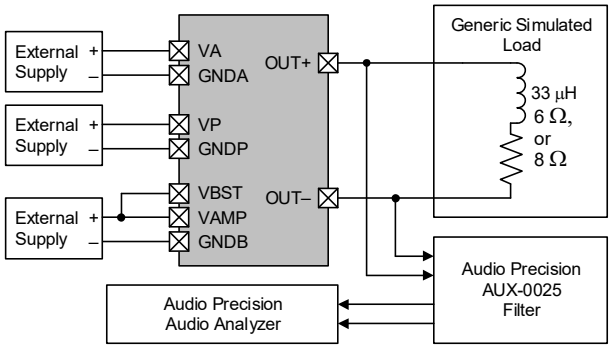


Table 3-5. Boost Converter Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show connections to, and passive components used with, the CS40L25/B; typical performance data taken with VA = 1.8 V, VP = 3.6 V, VAMP = VBST = 11.0 V; min/max performance data taken with VA = 1.80 V VP = 3.60 V, VAMP = VBST = 11.0 V; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; T_A = 25°C; L_{BST} = 1.0 µH; C_{BST} = 3.6 µF; f_{PLL_OUT} = 196.608 MHz. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameters		Symbol	Minimum	Typical	Maximum	Units
L_{BST} shorts inductance threshold		L_{BST_ERR}	—	—	0.16	µH
Power-down time [1]		t_{BST_PDN}	—	0.5	—	ms
Boost output voltage [2]	$VBST_{CTL-MIN}$ $VBST_{CTL-MAX}$ $\Delta VBST_{CTL}$	VBST	— — —	VP 11.0 50	— — —	V V mV
Power-up time [3]	From BST_EN = 00→10 (GLOBAL_EN = 1) From GLOBAL_EN = 0→1 (BST_EN = 10)	t_{BST_PUP}	— —	1 3	— —	ms ms
Operating efficiency [4]	VBST = 11.0 V; VP = 3.6V; I_{BST_OUT} = 500 mA; L_{BST} = 1.0 µH	η_B	—	83	—	%

CAUTION: The maximum allowable discharge depth of the batteries specified by the battery manufacturer must not be exceeded.

1. Power-down time t_{BST_PDN} refers to the time required for the switching on the SW net to stop once the boost converter been transitioned from its powered-up state to a powered-down state.
2. The VBST output level is manually configured via the control port or automatically via the Class H algorithm. However, if configured to generate a VBST output level lower than $VBST_{MIN}$, the VBST level is limited to $VBST_{MIN}$. If configured to generate a VBST voltage less than VP, the boost converter remains in Bypass Mode.
3. Power-up time t_{BST_PUP} refers to the time required for the switching on the SW net to start once the boost converter been transitioned from its powered-down state to its powered-up state.

4. Efficiency specified in this table assumes that the boost converter is driving an external resistive load via the VBST pin, instead of the onboard Class D amplifier. Losses from the boost-converter inductor (L_{BST}) are included in the calculation and are based on the preferred inductor shown in Note 1 in Table 2-1. R_{BST_LOAD} is selected to produce the specified value of $I_{OUT(B)}$.
   For the combined efficiency of the entire device, where the boost converter load is provided by the internal Class D amplifier driving a standard load attached to the OUT± nets; see Table 3-7.

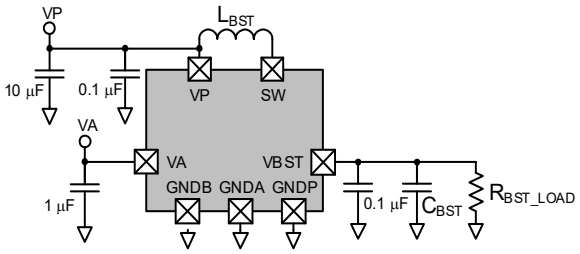


Table 3-6. Device Power Consumption Specifications—Low Power Modes

Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show typical connections; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; VA = 1.8 V, VP = VAMP = VBST = 3.60 V; T_A = 25°C; $\overline{\text{RESET}}$ inactive; control port inactive; DSP disabled and bypassed. Device initialization after power-on and reset done as described in Section 4.2.4.

Use Configuration		Typical	
		I_{VA} (µA)	I_{VP} + I_{SW} (µA)
OFF (VA = 0 V)	No input pins driven externally	0	2
Reset ($\overline{\text{RESET}}$ pin = LOW) [1]	ASP_BCLK, ASP_FSYNC and ASP_DIN driven low externally	0	2
	ASP_BCLK, ASP_FSYNC and ASP_DIN toggled externally	2	2
Always-On Haptic (AoH) Hibernate 32.768 kHz clock applied, DSP initialized and triggerable, no activity on SPI/I²C interface pins, RAM contents preserved.	Wakeup with haptic playback triggerable from GPIO1, GPIO2, and/or GPIO4[2]	20	2
Always-On Haptic (AoH) Standby 32.768 kHz clock applied, DSP initialized and triggerable, no activity on SPI/I²C interface pins, RAM and register contents preserved	Wakeup with haptic playback triggerable only from a GPIO1 low-to-high transition or a control port command	212	8
	Wakeup with haptic playback triggerable from GPIO1 high-to-low transition, any transition of GPIO2, GPIO3 or GPIO4, or a control port command	600	8

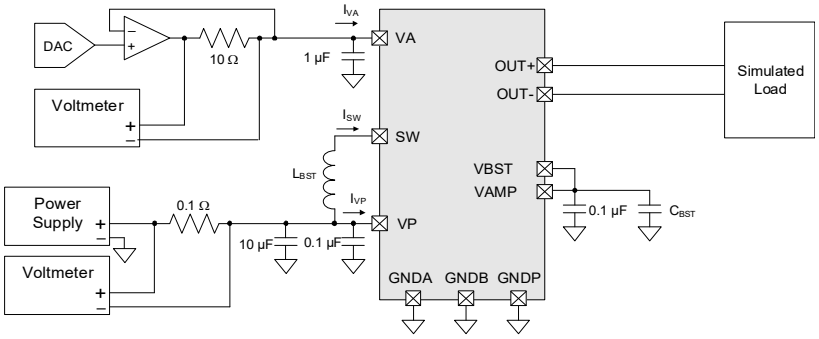
1. VP consumption is due to circuitry which enables an external boost voltage ($VBST_{EXT}$) to be supplied in any of the low power states.
2. During AoH Hibernate, a software-administered handshake can promote the device to AoH Standby, but this wakeup will not trigger haptic playback.

Table 3-7. Device Efficiency (Standard Load)

Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show typical connections; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; VA = 1.8 V, VP = 3.6 V, VAMP sourced from and attached to VBST; T_A = 25°C; $\overline{\text{RESET}}$ inactive; f_{PLL_OUT} = 196.608 MHz; ADSP is in Slave Mode with Fs = 48 kHz; input test signal is a 24-bit 997-Hz sine wave with 1 LSB of triangular PDF dither applied. DSP disabled and bypassed. Device initialization after power-on and reset done as described in Section 4.2.4.

Use Configuration [1]			Minimum	Typical	Maximum	Units
P_{OUT} = 50 mW	VP = 4.3 V VBST = Class H [2]	Amp + Boost + Class H + VP/VBSTMON	—	52	—	%
P_{OUT} = 500 mW			—	85	—	%

1. Tests were performed with the simulated load (33 µH in series with an 8-Ω resistor). Specified testing components are as follows:
   L_{BST} (TDK TFM201610GHM-1R0MTAA).



2. Efficiency for when Class H is enabled is measured using a 100-Hz sine wave at the specified output power when the Class H is configured as follows: CLASSH_EN = 1; all other Class H configurations are default.

Table 3-8. Signal Monitoring Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show typical connections; inputs to VSNS± are 1-kHz sine waves supplied by the CS40L25/B's Class D amplifier; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; typical performance data taken with VA = 1.8 V, VP = 3.6 V, VAMP = VBST = 11.0 V, min/max performance data taken with VA = 1.80 V, VP = 3.60 V, VAMP = VBST = 11.0 V; T_A = 25°C; L_{BST} = 1.0 µH; f_{PLL_OUT} = 196.608 MHz; measurement bandwidth is 20 Hz to 20 kHz; Fs = 48.0 kHz; standard load = 8 Ω + 33 µH. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameters [1]			Symbol	Minimum	Typical	Maximum	Units
Characteristics for all ADCs	Power-up time [2]	GLOBAL_EN = 0→1	t_{PUP_ADC}	—	—	3	ms
	Group delay—VMON, IMON [3]	Fs = 48 kHz Fs = 96 kHz Fs = 192 kHz	$GD_{VMON-IMON}$	— — —	51 42 24	— — —	µs µs µs
VPMON characteristics	Effective number of bits		$VPMON_{ENOB}$	—	8.5	—	Bits
	Voltage resolution		$VPMON_{STEP}$	—	5.94	—	mV
	Nominal 3.6-V voltage measurement		$VPMON_{MEAS}$	3.54	3.60	3.66	V
	Input voltage for 0-dBFS output		$VPMON_{0dBFS}$	—	6.087	—	V
VBSTMON characteristics [4]	Effective number of bits		$VBSTMON_{ENOB}$	—	8.5	—	Bits
	Voltage resolution		$VBSTMON_{STEP}$	—	13.67	—	mV
	Nominal 11.0-V voltage measurement		$VBSTMON_{MEAS}$	10.8	11.00	11.2	V
	Input voltage for 0-dBFS output		$VBSTMON_{0dBFS}$	—	14.00	—	V
VMON characteristics	Dynamic range (unweighted), VSNS± = ±8.0 V (16 V_{PP})		$VMON_{DNR}$	70	74	—	dB
	Total harmonic distortion + noise	5.6 Vpk 8 Vpk	$VMON_{THDN-5p6V}$ $VMON_{THDN-8V}$	— —	–70 –68	–66 –64	dB dB
	Nominal 11.0-V voltage measurement		$VMON_{MEAS}$	10.80	11.00	11.20	V
	Input voltage for 0-dBFS output [5]		$VMON_{0dBFS}$	—	12.30	—	V
	Common mode rejection ratio (217 Hz @ 800 mV_{PP}) [6]		$VMON_{CMRR}$	50	60	—	dB
	Single-ended input impedance [7]		$VMON_{ZIN}$	—	1	—	MΩ
	DC offset error		$VMON_{DC-OFF}$	–10	—	10	mV
IMON characteristics	Dynamic range (unweighted), ±1.0 A (2 A_{PP})		$IMON_{DNR}$	64	69	—	dB
	Total harmonic distortion + noise [8]	700 mApk 1 Apk	$IMON_{THDN-700}$ $IMON_{THDN-1Apk}$	— —	–61 –59	–57 –55	dB dB
	Nominal 1.00-A current measurement		$IMON_{MEAS}$	0.98	1.00	1.02	A
	Input current for 0-dBFS output [5]		$IMON_{0dBFS}$	—	2.1	—	A
	DC offset error		$IMON_{DC-OFF}$	–2	0	2	mA
	Voltage-to-current isolation		$IMON_{V-TO-I}$	56	66	—	dB
	VMON/IMON gain ratio variance [9]		$IMON_{VI-RATIO}$	–0.25	—	0.25	%

1. All parameters given in terms of dB are referred to the applicable typical full-scale voltages. Applies to all THD+N and resolution values in the table.
2. The amount of time measured from the completion (or ACK) of the control port write (GLOBAL_EN = 1) to the time at which the first valid data word is present on the serial port output. GLOBAL_EN represents a full power-down, where VA is present, and $\overline{\text{RESET}}$ is deasserted.
3. xMON group delay is measured from the time a signal is presented on the respective input pins (VP, VBST, OUT+, or VSNS±) until data available.
4. VBST measurements conducted with an external supply, BST_EN = 00, and specified voltage range applied to the VBST/VAMP pins.
5. The full-scale (maximum code) signal refers to the 16-bit or 24-bit scaled xMON D_{OUT}.
6. CMRR test setup for VSNS±.

7. A continuous-time active filter exists between the VSNS± pins and the ADC.
8. The total harmonic distortion of IMON is measured using the CS40L25/B Class D amplifier as the signal source, which is connected to an 8 Ω + 33 µH load, operating under the typical performance test conditions to produce an unclipped sine wave.
9. The VMON/IMON gain ratio variance is tested using 10 averages of a –40-dBFS input pilot tone at 40 Hz to measure impedance. A secondary tone at 2 kHz is swept from –35 dBFS to 0 dBFS.

Table 3-9. Monitoring PSRR Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show typical connections; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; VA = 1.8 V; VP = 3.6 V, VAMP = VBST = VP; L_{BST} = 1.0 µH; f_{PLL_OUT} = 196.608 MHz; unless indicated otherwise, voltages are with respect to ground. T_A = 25°C. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameters	Noise Injected Into	Noise Measured On	Noise Amplitude (mVpk)	Noise Frequency (Hz)	Minimum	Typical	Maximum	Units
VMON PSRR [1]	VA	DSP	100	217 1k 20k	31 31 31	45 45 43	— — —	dB dB dB
IMON PSRR [1]	VA	DSP	100	217 1k 20k	50 40 40	60 50 50	— — —	dB dB dB

1. To isolate VMON and IMON VA PSRR from the signal path while maintaining a connected and sourced operational state, the amplifier signal source is muted.

Table 3-10. VP and VBST Brownout Prevention Monitoring Characteristics

Test conditions (unless specified otherwise): Fig. 2-1–Fig. 2-3 show connections to, and passive components used with, the CS40L25/B; typical performance data taken with VA = 1.8 V, VP = 3.6 V, VAMP = VBST = 11.0 V; min/max performance data taken with VA = 1.80 V, VP = 3.60 V, VAMP = VBST = 11.0 V; Ground = GND = GNDA = GNDB = GNDP = 0 V; voltages are with respect to ground; T_A = 25°C; L_{BST} = 1.0 µH; C_{BST} = 3.6 µF; f_{PLL_OUT} = 196.608 MHz. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameters [1]		Symbol	Minimum	Typical	Maximum	Units
Initial VP brownout response voltage threshold	$VP_{BR1\text{-}MIN}$ $VP_{BR1\text{-}MAX}$ ΔVP_{BR1}	VP_{BR_1}	— — —	2.497 3.874 0.048	— — —	V V V
Initial VP brownout threshold set point variation		$\Delta VPBR_{BR1\text{-}VAR}$	–60	—	+60	mV
Second VP brownout threshold relative to initial threshold [2]	$VP_{BR\_1} – VP_{BR\_2}$	VP_{BR_2}	20	50	80	mV
Third VP brownout threshold relative to second threshold [2]	$VP_{BR\_2} – VP_{BR\_3}$	VP_{BR_3}	20	50	80	mV
Initial VBST brownout response voltage threshold ($VBST_{TARGET} – VBST_{MEAS}$)	$VBST_{BR1\text{-}MIN}$ $VBST_{BR1\text{-}MAX}$ $\Delta VBST_{BR1}$	$VBST_{BR\_1}$	— — —	0.109 3.445 0.055	— — —	V V V
Initial VBST brownout threshold set point variation [2]		$\Delta VBST_{BR1\text{-}VAR}$	–60	—	+60	mV
Second VBST brownout threshold relative to initial threshold [2]	$VBST_{BR\_1} – VBST_{BR\_2}$	$VBST_{BR\_2}$	20	50	80	mV
Third VBST brownout threshold relative to second threshold [2]	$VBST_{BR\_2} – VBST_{BR\_3}$	$VBST_{BR\_3}$	20	50	80	mV
Initial brownout response time		t_{VPBR_INIT}	—	—	10	µs
Attenuation release volume step		VOL_{VxBR_REL}	—	0.0625	—	dB
Attenuation attack volume step [3]	Vx_{BR_1} triggered Vx_{BR_2} triggered Vx_{BR_3} triggered	VOL_{VxBR_ATK}	0.125 0.250 0.500	— — —	1.250 2.500 5.000	dB dB dB
Maximum volume attenuation limit	$VxBR_{ATT\text{-}LIM\text{-}MIN}$ $VxBR_{ATT\text{-}LIM\text{-}MAX}$ $\Delta VxBR_{ATT\text{-}LIM}$	$VxBR_{ATT\text{-}LIM}$	— — —	0 15 1	— — —	dB dB dB

1. All timings are referenced with f_{PLL_OUT} = 196.608 MHz. When using a f_{PLL_OUT} other than 196.608 MHz, all timings scale by 196.608 MHz/f_{PLL_OUT}.
2. t_{VxBR_INIT} is the time required for the system to detect the initial VP or VBST brownout condition, modify the device's operational state, and allow for the initial change in attenuation propagate through the amplifier.
3. The attenuation volume step varies based on the current VP or VBST voltage threshold range. The specified minimum/maximum range is based on the available user configurations. For more information on the multiple VP or VBST voltage thresholds, refer to Section 4.7.2.

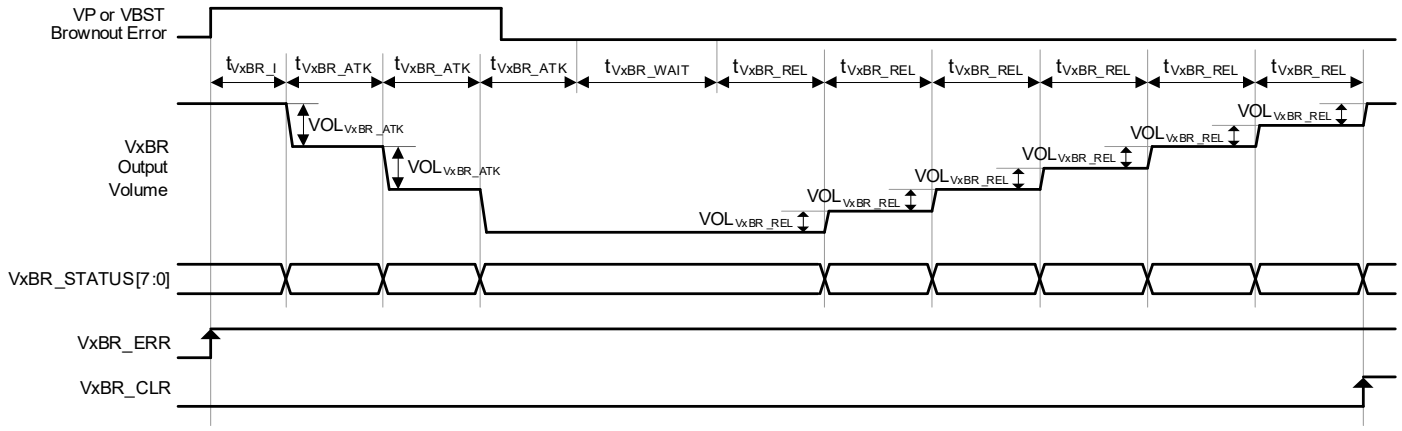


Figure 3-1. VPBR and VBBR Error, Volume Attenuation, Status Reporting, and Interrupts

Table 3-11. Device Temperature Monitoring and Protection Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show connections to, and passive components used with, the CS40L25/B; typical performance data taken with VA = 1.8 V, VP = 3.6 V, VAMP = VBST = 11.0 V; min/max performance data taken with VA = 1.8 V, VP = 3.6 V, VAMP = VBST = 11.0 V; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; T_A = 25°C. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameters		Minimum	Typical	Maximum	Units
Die temperature measurement	Minimum	—	0	—	°C
	Maximum	—	150	—	°C
	Resolution	—	1	—	°C
	Accuracy	-10	—	+10	°C
Overtemperature warning threshold	TEMP_WARN_THLD = 00	—	105	—	°C
	TEMP_WARN_THLD = 01	—	115	—	°C
	TEMP_WARN_THLD = 10	—	125	—	°C
	TEMP_WARN_THLD = 11	—	135	—	°C
Overtemperature error threshold [1]		—	150	—	°C
Overtemperature warning/error threshold deviation [2]		–10	—	+10	°C

1. Because the same internal temperature-measuring circuitry is used to create both the overtemperature warning and error signals, overtemperature warning/error threshold deviation is applied equally to both thresholds, which results in the individual thresholds being inaccurate to the same degree and of the same polarity as all other values. For example, if the overtemperature warning threshold is 10°C below the TEMP_WARN_THLD setting, the overtemperature error threshold is also 10°C below its specified threshold.
2. The overtemperature warning/error threshold deviation specifies the accuracy of the temperature-detection circuitry. This specification relates how many degrees above or below the threshold the overtemperature warning/error circuitry may trigger.

Table 3-12. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show typical connections; VA = 1.66 to 1.94 V, VP = 2.80 to 5.50 V, VBST = $VBST_{MIN}$ to 8.0 V; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; T_A = 25°C. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameters			Symbol	Minimum	Maximum	Units
Digital I/O hysteresis			—	75	—	mV
Input capacitance (per pin)			—	—	10	pF
SDA pull-up resistance [1]			R_P	500	—	Ω
Input leakage current (per pin) [2,3]	ASP_BCLK, ASP_FSYNC, ASP_DIN, $\overline{\text{ALERT}}$		I_{IN}	—	±4000	nA
	All other digital pins			—	±100	nA
Internal weak pull-down	ASP_BCLK, ASP_FSYNC, ASP_DIN, $\overline{\text{ALERT}}$		—	550	—	kΩ
VA logic I/Os	High-level output voltage	I_{OH} = –100 µA	V_{OH}	VA–0.2	—	V
	Low-level output voltage	All outputs, I_{OL} = 100 µA	V_{OL}	—	0.20	V
		SDA, I_{OL} as per $R_{P(min)}$ [1]		—	0.20•VA	V
	High-level input voltage		V_{IH}	0.70•VA	—	V
	Low-level input voltage		V_{IL}	—	0.30•VA	V

1. Minimum R_P values (shown in Fig. 2-1 – Fig. 2-2 and specified in Table 3-12) are determined from the maximum VA level, the minimum sink current strength of their respective output, and the maximum low-level output voltage (V_{OL}). Maximum R_P values may be determined by how fast their associated signals must transition (e.g., the lower the R_P value, the faster the I²C bus can operate for a given bus load capacitance).
2. Specification includes current through internal pull up/down resistors, where applicable (as defined in Section 2).
3. Leakage current is measured with VA = 1.80 V, VP = 3.60 V, VBST = 3.60 V, and $\overline{\text{RESET}}$ asserted. Each pin is tested while being driven high and low.

Table 3-13. DC Characteristics

Test conditions (unless specified otherwise):Fig. 2-1 – Fig. 2-4 show connections to, and passive components used with, the CS40L25/B; typical performance data taken with VA = 1.8 V, VP = 3.6 V, VAMP = VBST = 11.0 V; min/max performance data taken with VA = 1.8 V, VP = 3.6 V, VAMP = VBST = 11.0 V; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; T_A = 25°C. Device initialization after power-on and reset done as described in Section 4.2.4.

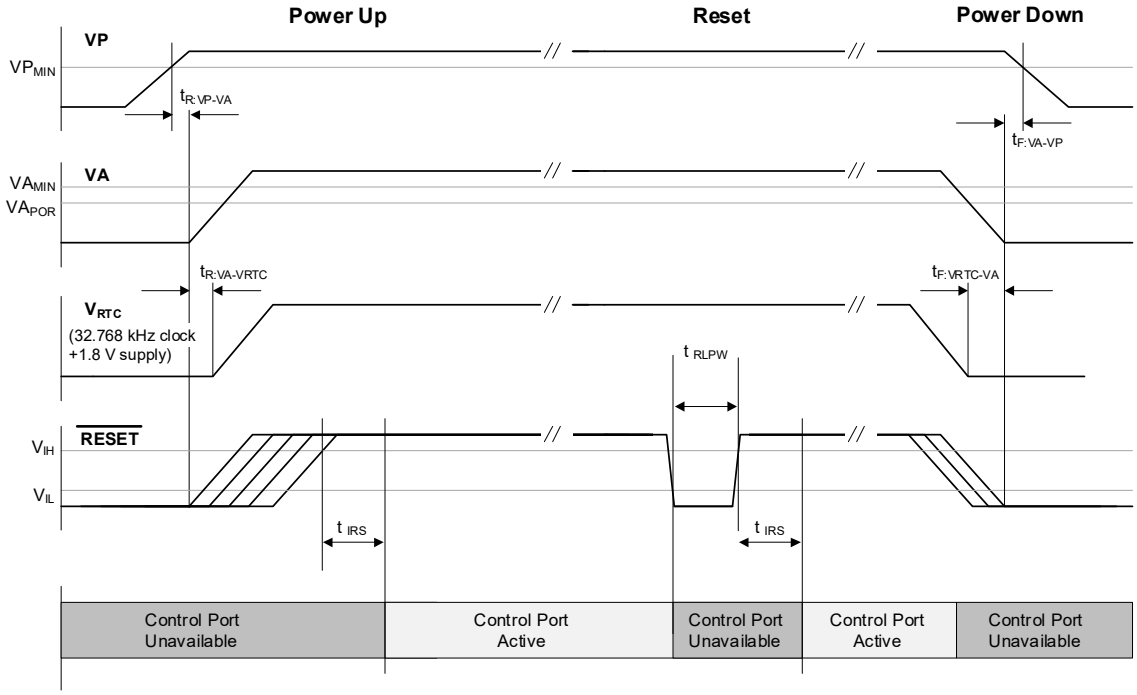
Parameters		Minimum	Typical	Maximum	Units
LDO_FILT+ voltage	$\overline{\text{RESET}}$ = HIGH	—	1.2	—	V
VA power-on reset (POR) threshold (V_{POR})	Up	—	1.2	—	V
	Down	—	1.05	—	V

Table 3-14. Switching Specifications—Power, Reset, Master Clock References

Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show connections to, and passive components used with, the CS40L25/B; typical performance data taken with VA = 1.8 V, VP = 3.6 V, VAMP = VBST = 11.0 V; min/max performance data taken with VA = 1.8 V, VP = 3.6 V, VAMP = VBST = 11.0 V; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; T_A = 25°C. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameters		Symbol	Minimum	Typical	Maximum	Units
Reset	$\overline{\text{RESET}}$ low (logic 0) pulse width	t_{RLPW}	1	—	—	ms
	$\overline{\text{RESET}}$ rising edge to control port active [1]	t_{IRS}	—	—	750	µs
	Delay from 32.768 kHz clock source active to $\overline{\text{RESET}}$ high	t_{CK-R}	0	—	—	µs
GPI Wake-up	GPIO1 Wake trigger to control port active	t_{IW}	—	—	750	µs
Power supplies [2]	Power-supply ramp up/down	$t_{PWR-RUD}$	—	—	100	ms
	Delay from VP valid to VA rising	$t_{R:VP-VA}$	0	—	—	ms
	Delay from VA off to VP falling	$t_{F:VA-VP}$	0	—	—	ms
	Delay from VA valid to V_{RTC} rising [3]	$t_{R:VA-VRTC}$	0	—	—	ms
	Delay from V_{RTC} off to VA falling [3]	$t_{F:VRTC-VA}$	0	—	—	ms

1. Power and reset sequencing with control port availability



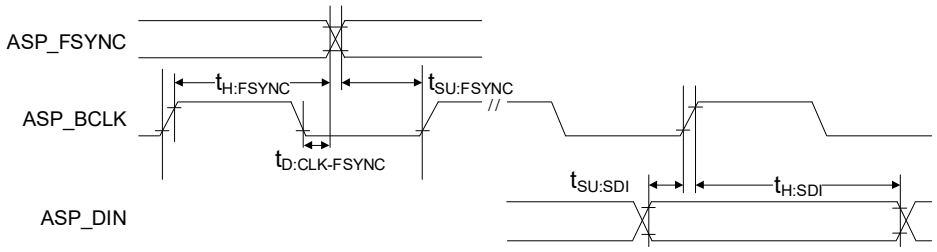
2. A valid VP voltage must be present whenever a VA voltage is applied.
3. The external 32.768 kHz clock source may not be enabled before VA is enabled, and it must be disabled before VA is disabled.

Table 3-15. Switching Specifications—Auxiliary Serial Port (ASP)

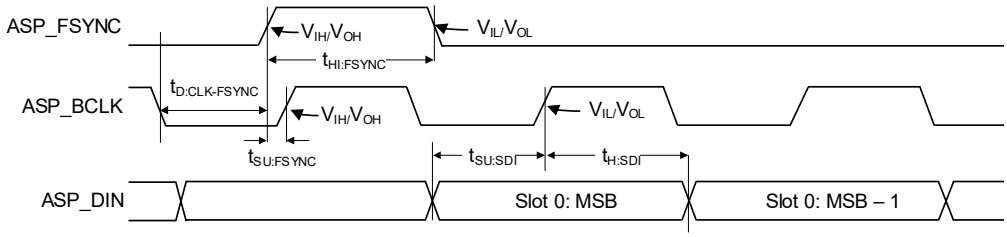
Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show typical connections; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; VA = 1.66–1.94 V, VP = 2.80–5.50 V, VBST = $VBST_{MIN}$ to 11.0 V, Inputs: Logic 0 = 0 V; Logic 1 = VA; output timings are measured at V_{OL} and V_{OH} thresholds for VA logic (as specified in Table 3-12); T_A = 25°C. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameters [1,2,3]		Symbol	Minimum	Maximum	Units
ASP_FSYNC input sample/frame rate [4]		Fs	8	192	kHz
ASP_FSYNC duty cycle	I²S	D_{FSYNC}	45	55	%
FSYNC high period [5]	TDM	$t_{HI:FSYNC}$	$1/f_{ASP\_BCLK}$	$(n–1)/f_{ASP\_BCLK}$	s
ASP_BCLK frequency		f_{ASP_BCLK}	16•Fs	24.576	MHz
ASP_BCLK duty cycle		D_{ASP_BCLK}	45	55	%
ASP_FSYNC setup time before ASP_BCLK latching edge		$t_{SU:FSYNC}$	10	—	ns
ASP_FSYNC hold time after ASP_BCLK latching edge	I²S	$t_{H:FSYNC}$	5	—	ns
ASP_DIN setup time before ASP_BCLK latching edge		$t_{SU:SDI}$	10	—	ns
ASP_DIN hold time after ASP_BCLK latching		$t_{H:SDI}$	5	—	ns

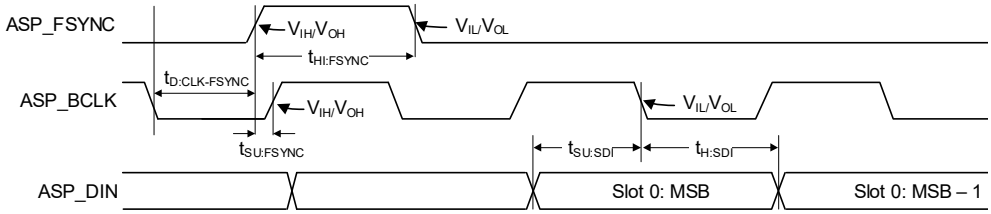
1. ASP timing in I²S Mode (ASP_FMT = 010)



2. ASP timing in TDM 1 Mode (ASP_FMT = 000). Note that ASP_BCLK and ASP_FSYNC can be inverted if required; the figure shows the default, noninverted polarity.



3. ASP timing in TDM 1.5 Mode (ASP_FMT = 100). Note that ASP_BCLK and ASP_FSYNC can be inverted if required; the figure shows the default, noninverted polarity.



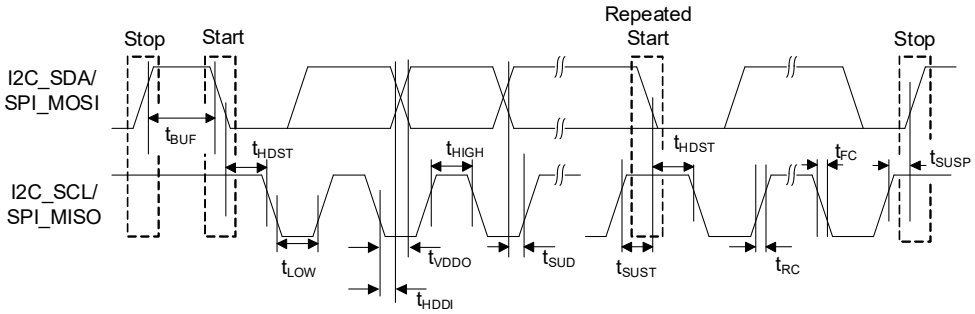
4. Sample rates available are based on a combination of the REFCLK frequency provided and the f_{PLL_OUT} frequency.
5. "n" refers to the total number of ASP_BCLKs in a given FSYNC frame.

Table 3-16. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): Fig. 2-1 – Fig. 2-4 show typical connections; Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; VA = 1.8 V; inputs: Logic 0 = GNDA = 0 V, Logic 1 = VA; T_A = 25°C; SDA load capacitance equal to maximum value of C_B = 400 pF; minimum SDA pull-up resistance, $R_{P(min)}$.[1] All specifications are valid for the signals at the pins of the CS40L25/B with the specified load capacitance. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameter [2]		Symbol [3]	Minimum	Maximum	Units
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	Standard-mode Fast-mode Fast-mode Plus	t_{RC}	— — —	1000 300 120	ns ns ns
Fall time of SCL and SDA	Standard-mode Fast-mode Fast-mode Plus	t_{FC}	— — —	300 300 120	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [4]		t_{HDDI}	0	—	ns
Output data valid (Data/Ack) [5]	Standard-mode Fast-mode Fast-mode Plus	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance		C_B	—	400	pF
SCL/SDA pull-up resistance [1]		R_P	500	—	Ω
Pulse width of spikes to be suppressed		t_{ps}	0	50	ns

1. The minimum R_{P2A} and R_{P2B} resistor values (shown in Fig. 2-3 and Fig. 2-4) are determined by using the maximum level of VA, the minimum sink current strength of its respective output, and the maximum low-level output voltage V_{OL}. The maximum R_{P2A} and R_{P2B} resistor values may be determined by how fast the associated signal must transition (e.g., the lower the value of the resistor, the faster the I²C bus is able to operate for a given bus load capacitance). See I²C bus specification referenced in Section .
2. All timing is relative to thresholds specified in Table 3-12, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.
3. I²C control-port timing.



4. Data must be held long enough to bridge the transition time, t_{FC}, of SCL.
5. Time from falling edge of SCL until data output is valid.

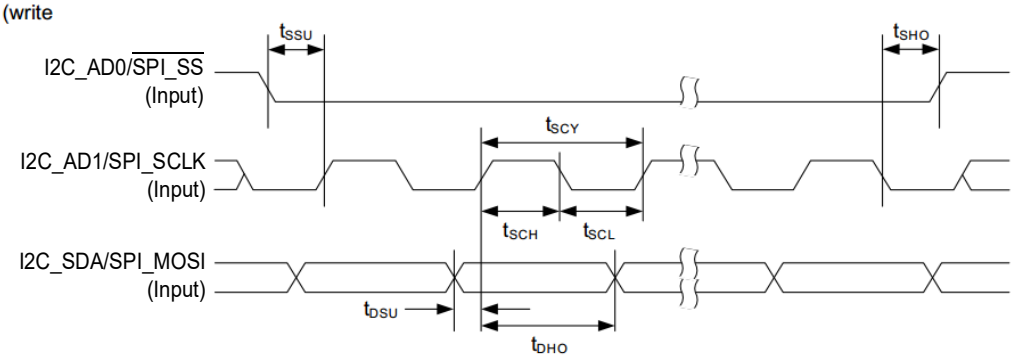
Table 3-17. Switching Specifications—SPI Port

Test conditions (unless specified otherwise): Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; VA = 1.8 V, VP = 3.6 V; T_A = 25°C; Logic 0 = GNDA = GNDB = 0 V, Logic 1 = VA; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds for VA logic (as specified in Table 3-12). Device initialization after power-on and reset done as described in Section 4.2.4.

Parameter	Symbol[1]	Minimum	Typical	Maximum	Units
$\overline{\text{SPI\_SS}}$ falling edge to SPI_SCLK rising edge	t_{SSU}	2.6	—	—	ns
SPI_SCLK falling edge to $\overline{\text{SPI\_SS}}$ rising edge	t_{SHO}	0	—	—	ns
SPI_SCLK pulse cycle time	t_{SCY}	40	—	—	ns
SPI_SCLK pulse width low	t_{SCL}	15.3	—	—	ns
SPI_SCLK pulse width high	t_{SCH}	15.3	—	—	ns
SPI_MOSI to SPI_SCLK setup time	t_{DSU}	1.5	—	—	ns
SPI_MOSI to SPI_SCLK hold time	t_{DHO}	1.7	—	—	ns
SPI_SCLK falling edge to SPI_MISO transition SPI_SCLK slew (90%–10%) = 5 nsC_{LOAD} (SPI_MISO) = 25 pF	t_{DL}	0	—	12.6	ns

1.SPI control-port timing

1. Control interface timing—SPI Mode (write cycle)



2. Control interface timing—SPI Mode (read cycle)

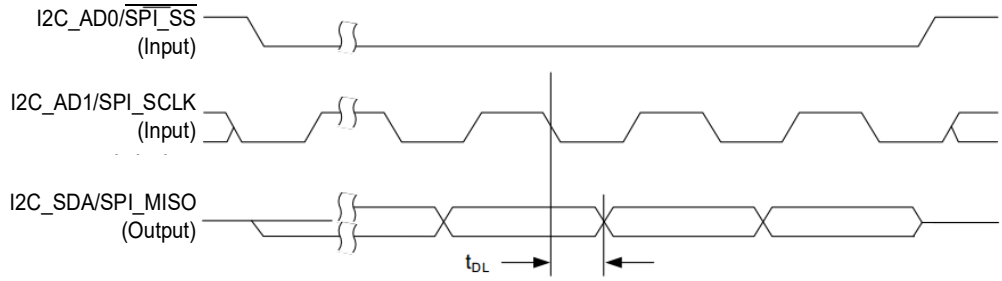
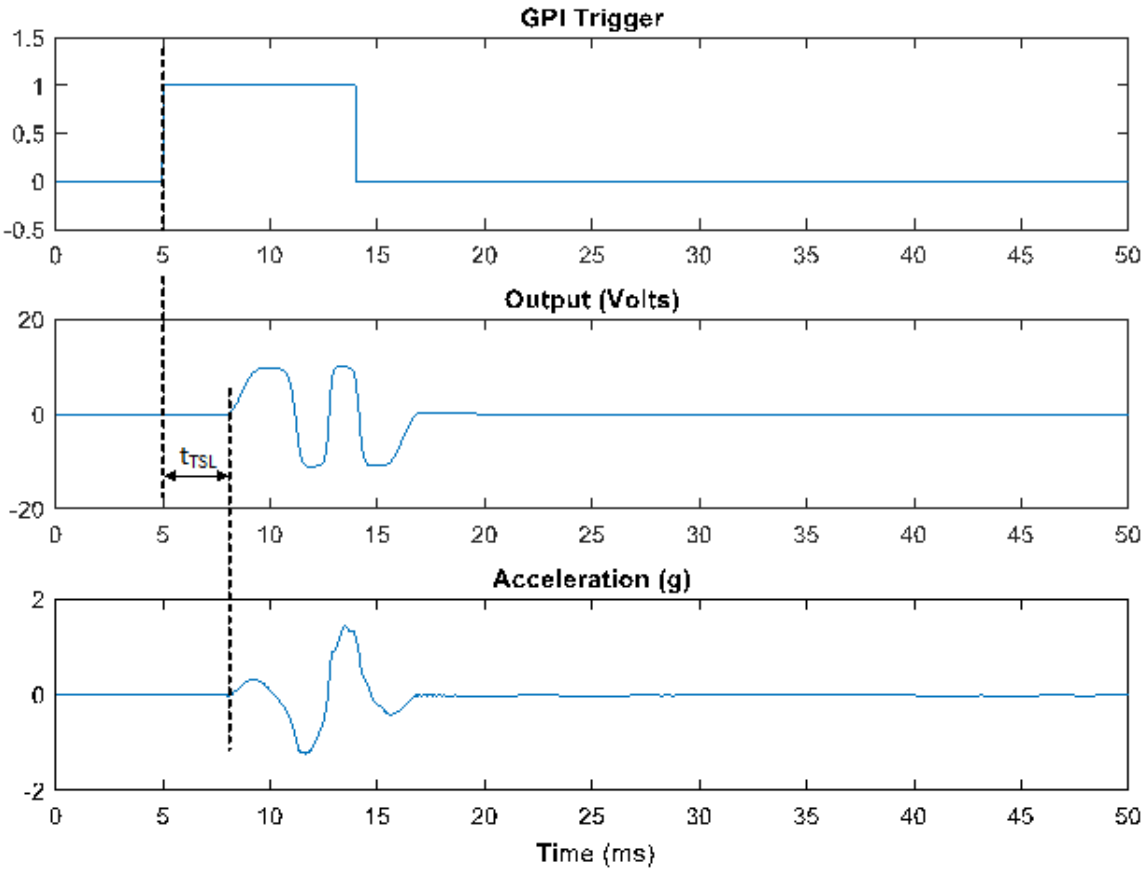


Table 3-18. Latency Specifications

Test conditions (unless specified otherwise): Ground = GND = GNDA = GNDP = 0 V; voltages are with respect to ground; VA = 1.8 V, VP = 3.6 V; T_A = 25°C; Logic 0 = GNDA = GNDB = 0 V, Logic 1 = VA; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds for VA logic (as specified in Table 3-12). Actuator type ELV0815C LRA. Device initialization after power-on and reset done as described in Section 4.2.4.

Parameter[1]		Symbol	Minimum	Typical	Maximum	Units
Trigger-Start Latency[2]	from AoH Standby mode	t_{TSL}	—	3	—	ms
	from AoH Hibernate mode		—	5	—	

1. Latency specification applies for triggers received during Always-on haptic (AoH) Standby or AoH Hibernate mode entered running in normal operation (not in Basic Haptics Mode). A haptic event may be delayed or missed if a trigger is received while the host is initializing device RAM and initiating RAM-based operation.
2. Trigger-Start Latency is the time between the GPIO1 pin rising edge trigger event received in AoH Standby or AoH Hibernate mode and the start of the waveform drive. Measured with all DSP Core algorithms disabled except Vibegen (refer to Firmware Release Notes), BST_CTL_SEL = 01 (Class H tracking value), and CLASSH_EN = 1 (enabled).



4 Functional Description

This document describes features supported by the CS40L25/B hardware architecture including some that require additional firmware and/or device driver software to implement in a system. Please see the software release notes for details about the features which have been integrated and validated in specific releases.

The functional descriptions of the CS40L25/B blocks are listed below:

4.1 Haptics Overview

Haptic technology is an important component of the user interface and overall user experience in many mobile devices. Haptic technology provides the new dimension of tactile sensory stimulation which effectively allows the user to touch and feel the device or the virtual environment. Two common application examples of haptic technology are the replacement of physical buttons or switches in the user interface and force effects and force feedback in gaming applications. The CS40L25/B is an integrated haptic generator and driver for low power mobile devices. The CS40L25/B enables stored waveform/effects playback triggered by a control port command or hardware pin.

4.1.1 Compatible Actuators

The CS40L25/B is intended for driving Linear Resonant Actuator (LRA) devices. The CS40L25/B is compatible with multiple types of LRAs such as X-axis prismatic, Z-axis cylindrical, and Z-axis prismatic. The boost and high power amplifier are designed to drive an LRA with an impedance as low as 6 Ω and a resonant frequency in 50-561 Hz range.

4.1.2 LRA-Driven Haptics

The key component parts of an LRA are the mass, centering spring, and electromotive force transduction mechanism. Fig. 4-1 shows a schematic diagram of an LRA.

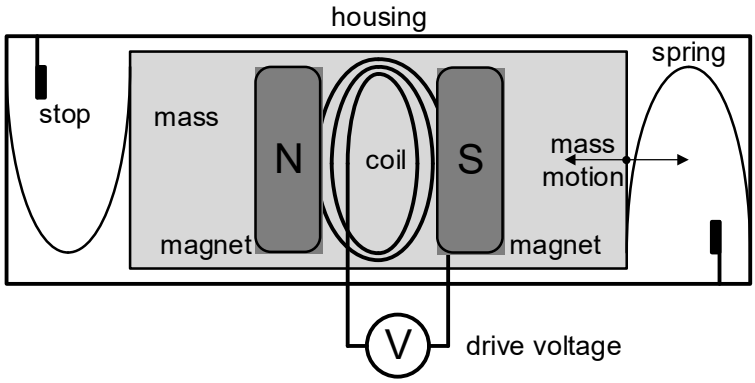


Figure 4-1. LRA Schematic Diagram

Haptic force on the portable device incorporating the LRA is generated by mass reaction due to movement of the LRA mass according to Eq. 4-1.

$$F = M_{LRA} \times a_{LRA} = M_{device} \times a_{device}$$

Equation 4-1. Haptic force on portable device generated by an LRA

Force on the LRA mass at any displacement is a combination of spring force and electromotive force.

In resonant buzz operation, the spring force dominates in a mass-spring system which resonates at a characteristic frequency. Electromotive energy is applied in-phase as needed to maintain oscillation and make up for losses. Resonant buzz operation is useful if the driver is low voltage and highest efficiency is paramount.

In non-resonant applications, the applied electromotive force from the boosted amplifier may be much greater than the spring force. The mass acceleration is primarily due to electromotive force, and affected secondarily by spring force. Drive waveforms may be arbitrary and not necessarily resonant. Non-resonant operation is useful to achieve crisp, distinct haptic effects.

4.1.3 LRA Characteristics Measurement and Unit Calibration

The CS40L25/B supports the ability to measure each individual LRA on the production line following the portable device assembly. Resonance frequency, f_0, and coil electrical resistance, R_e, are measured and their values stored within the host nonvolatile memory. The CS40L25/B algorithm references f_0 to initialize resonant buzz operation as well as to optimize non-resonant drive and braking.

4.1.4 Energizing Versus Braking

For the mass in motion, force in the direction of motion is referred to as energizing force, and force opposite to the direction of motion is referred to as braking force. Likewise, the voltage applied at the actuator terminals may be energizing, which adds to the system energy or braking, which removes energy from the system.

4.1.5 High Performance Haptic Reaction Mass Control

Unlike resonant buzzes, short duration transient haptic effects cannot be described or generated by a single frequency. Strong, high-quality haptic effects require drive synchronization to the LRA motion while energizing and braking, and also require suppression of any after-ringing. The CS40L25/B incorporates high-precision output voltage and current monitoring, allowing the LRA mass motion state to be tracked and controlled. High precision motions are achieved by a combination of user-defined waveform design coupled with precise playback by the CS40L25/B algorithms.

4.1.6 Latency

The overall presentation latency of a crisp feeling haptic effect is the sum of:

- Trigger-start latency, between command and waveform drive start
- Energizing latency between start of the drive and achievement of maximum acceleration
- Braking latency between maximum acceleration and the point at which acceleration is reduced to 10% of the maximum.

See Table 3-18 for latency timing specifications.

4.1.7 User-Defined Haptic Waveform Playback

The CS40L25/B may be configured to play user-defined haptic waveforms (hereafter “waveform” or “waveforms”) when triggered.

Waveforms downloaded from the host processor into the CS40L25/B RAM are triggered by:

- GPI pin transition – rising and falling edges trigger the pre-associated stored waveforms
- I²C/SPI trigger command – triggers stored waveform specified by the command (during playback or in AoH Standby)

Envelope Waveform Commands:

- Envelope command – The on-chip DSP processes a user-defined haptic effect at the specified amplitude. The envelope waveform command may specify the frequency (which may be the resonant frequency measured during the last LRA calibration). Waveform envelope commands include a series of (time, amplitude, and frequency) triplets.

Waveforms may be stored in a range of supported formats, depending on fidelity requirements and waveform time duration as shown in Table 4-1.

Table 4-1. Supported Formats for Waveforms

Type	Where Stored	Transport	Time Domain	Amplitude Domain	Frequency	Usage
PCM waveform	CS40L25/B RAM	I²C/SPI to store into CS40L25/B memory	8 kHz	Waveform Value	Arbitrary waveform, no fixed frequency	Any Waveform is Supported, Typically Short Clicks
PWLE Format	CS40L25/B RAM	I²C/SPI to store into CS40L25/B memory	Time Steps Not Fixed	Envelope Amplitude	Resonant frequency, or frequency as specified	Alert buzzes

Waveform amplitudes are expressed in 2’s complement form, representing a normalized range of ± 1.0 FFS (fraction of full-scale).

The waveform envelope is specified as the normalized 2’s complement peak value envelope of the drive voltage waveform applied as energizing force. Negative envelope numbers represent inverted-phase voltage applied as braking force.

4.1.8 PCM Waveform Storage Limits

The CS40L25/B supports multiple pre-recorded PCM waveforms. PCM Waveforms are stored with 8-bit resolution at 8000 samples/sec. Total PCM waveform storage is approximately 7000 bytes for approximately 800 ms of total waveform duration (depending upon the firmware used). Much longer playback duration are possible using piecewise linear envelope waveform encoding (PWLE), described below, instead of PCM waveforms. Each individual waveform may be arbitrary length, provided that the total duration of all waveforms fits within the storage allocation. PCM allows the highest-fidelity storage of arbitrary waveforms. Longer duration waveform storage is possible using more compact representations. Waveform storage requirements and limitations are subject to change in specific firmware releases.

4.1.9 Piecewise Linear Envelope Waveforms

Long duration waveforms may be represented in the Piece-Wise Linear Envelope (PWLE) format to minimize the storage footprint required in the CS40L25/B. When operating the device from ROM using Basic Haptics Mode, the PWLE waveform is specified by the attributes shown in Table 4-2 . When running downloaded firmware, additional features and options are available using PWLE waveforms.

Table 4-2. PWLE Waveform Attributes

Item	Notes
Event	Serves as an index to a set of 16 event locations, which can all be defined individually, each having a unique set of parameters as defined here.
Repeat	For a given event, sets the number of times that the envelope (as defined by the time / amplitude / frequency triplets) repeats.
Wait Time	For a given event, once the waveform has ended (Last time / amplitude / frequency triplet reached), the synthesis engine waits for this amount of time before any repeat of the waveform (as defined by the Repeat variable).
Time / Amplitude / Frequency triplets: **Time**	Each triplet defines a single piecewise-linear section of the waveform. Up to 64 triplets define a waveform. The time element specifies the length of the section, which can be from 0 to 1023.75 ms.
Time / Amplitude / Frequency triplets: **Amplitude**	Each triplet defines a single piecewise-linear section of the waveform. Up to 32 triplets define a waveform. The amplitude element specifies amplitude of the excitation or breaking. Positive values represent energizing excitation. Negative represents reversed-phase braking excitation. Amplitude is specified in terms of fraction of fullscale (FFS) over the range from (-1.0 to +1.0) and the unloaded output voltage is a function of analog amplifier gain. (At 19.5 dB gain, theoretical output voltage is ~ 12.32 V_{PK}, but is practically limited below VAMP.)
Time / Amplitude / Frequency triplets: **Frequency**	Each triplet defines a single piecewise-linear section of the waveform. Up to 32 triplets define a waveform. The frequency element specifies the frequency of the waveform during the section. The frequency can be the current predetermined resonant frequency, or a value from 50.125 to 561.875 Hz.

Consider an example alert (for a given system) with a 250 Hz sine wave of 2 V_{RMS} amplitude, 700 ms duration, replayed 3 times with 300 ms intervals between; all at sample frequency of Fs = 8 kHz with 8-bit resolution required.

This could be stored as a PCM waveform lasting for the 3 second replay time, but would require a total of 24,000 bytes of storage. A more compact way of storing the alert would be to break it into a set of PWLE parameters.

The following parameters would be needed to be defined for the synthesizer:

- Amplitude = 0.2296 (FFS)
- Frequency = 250 Hz
- On time = 700 ms
- Wait time = 300 ms
- Repeat = 3.

Storing those few parameters needs much less memory than would be required to store the actual waveform samples, but precisely the same output can be synthesized for the alert.

Example 4-1.

The piecewise linear envelope (PWLE) parameters for the synthesizer in this example are given in Table 4-3 below.The first segment is defined by the (time, amplitude, frequency) triplet (120, 0.16234, 200). This triplet represents a waveform segment starting at time 0 at 0V_{PK} and extending to 120 ms at 2.0 V_{PK}. The waveform next segment starts at this time and amplitude and extends 80 ms to a final amplitude of 0.9 V_{PK} at 200 ms given by the triplet (80, 0.07305, 200). The sequence continues for the remaining triplets ending at 540 ms at 0 V_{PK}. The output remains at 0 $V_{PK}$for the 260 ms specified by the wait time and then replays one time.

Table 4-3. PWLE Waveform Example

Item	Value	Units	Notes
Repeat	1	Integer	Repeat once.
Wait Time	260	ms	Restart 260 ms after last point in final segment (800 ms).
Time / Amplitude / Frequency Triplets: Time	120 80 300 40 0	ms	0–120 ms 120–200 ms 200–500 ms 500–540 ms (end of list)
Time / Amplitude / Frequency Triplets: Amplitude	0.16234 0.07305 0.07305 0 0	Fraction of Fullscale (FFS)	Amplifier output voltage ~ 12.32 V x FFS = 2.0 V_{PK} Amplifier output voltage ~ 12.32 V x FFS = 0.9 V_{PK} Amplifier output voltage ~ 12.32 V x FFS = 0.9 V_{PK} Amplifier output voltage ~ 12.32 V x FFS = 2.0 V_{PK} (end of list)
Time / Amplitude / Frequency Triplets: Frequency	200 200 200 200 0	Hz	All segments use a 200 Hz frequency

The piecewise linear envelope template and the ideal synthesized output voltage waveform are shown in Fig. 4-2 below.

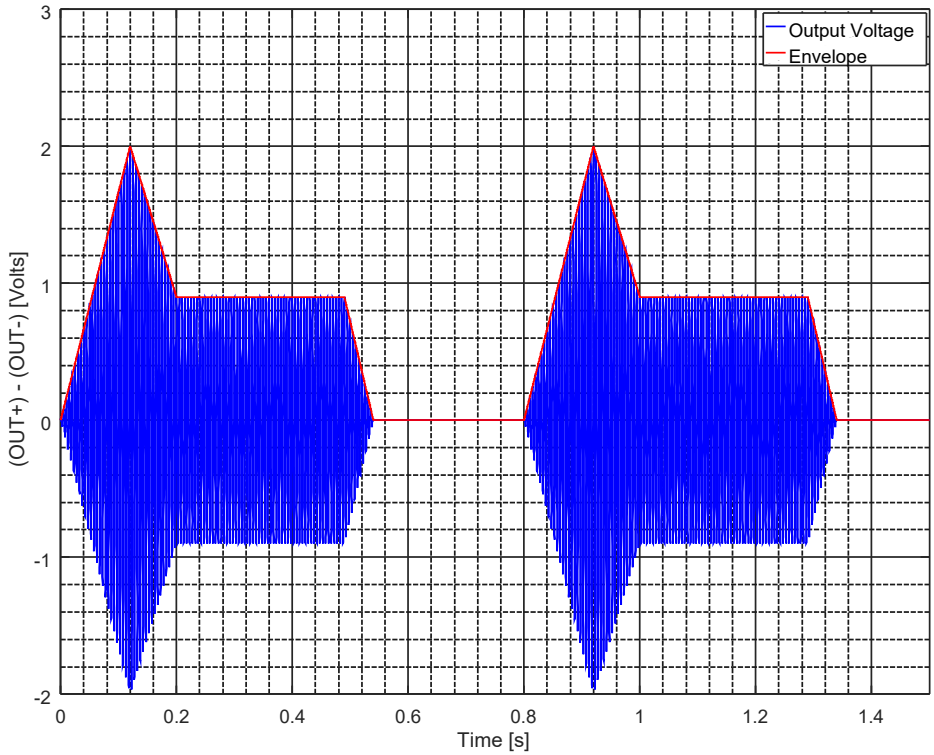


Figure 4-2. PWLE Example

4.1.10 GPI Trigger Inputs

Once initialized, the device enters the low power mode known as Always-on Haptic (AoH) Standby to wait for a haptic trigger event to start waveform playback. From Standby, the CS40L25 can trigger playback on rising or falling edge transitions on GPIO1 if using I2S/TDM, or on GPIO1, GPIO3 and GPIO4 if not using I²S/TDM. From Always-on Haptic (AoH) Hibernate, the CS40L25 can trigger playback on rising or falling edge transitions on GPIO1 and/or GPIO4 if not using I²S/TDM. From Standby, the CS40L25B can trigger playback on rising or falling edge transitions on GPIO1 — GPIO4, and from Hibernate on rising or falling edge transitions on GPIO1, GPIO3, and/or GPIO4. After playing the waveform, the device stays active for a configurable timeout period waiting for the GPI pin opposite edge transition which triggers playback of the other waveform selected for that transition. After playback, the device then returns to AoH Standby. If the opposite edge transition does not occur within the timeout period, the device enters a low power state to wait until the triggered GPI pin transitions inactive. In this case, no waveform playback occurs, but the device returns to AoH Standby ready to detect the next edge trigger event.

4.1.11 Haptic Waveform Priority

Haptic waveform commands may originate from different triggers, e.g GPI versus I²C, and there is the potential that a second waveform command occurs while a first waveform is still playing. Such waveform play conflicts are managed by intelligent replacement and queuing logic, according to the waveform command source and the waveform type.

4.1.12 Alerts to Host

The CS40L25/B $\overline{\text{ALERT}}$ pin provides an active low, open-drain interrupt output for the DSP to use to signal the host upon haptic trigger button events, playback end events, and other hardware related error conditions. Configuration of hardware interrupt events and host alerts using the $\overline{\text{ALERT}}$ pin are managed by DSP firmware in coordination with the host device driver.

4.2 Reset

4.2.1 Control Port Soft Reset

The device soft reset register, asserts and deasserts a device level reset to the CS40L25/B. Upon the completion of the soft reset, all register values are returned to their default state.

If using I²C, note that the device address (from the I2C_AD0/$\overline{\text{SPI\_SS}}$ and I2C_AD1/SPI_SCLK pins) is not updated upon the completion of a soft reset. In order for the I²C device address to be updated, a chip reset from the $\overline{\text{RESET}}$ pin is required.

4.2.2 VA Power on Reset

The CS40L25/B contains a power-on reset (POR) circuit on the VA supply input. This POR circuit holds the device in reset while VA is not present and ensures that the device is initialized in a known state while the VA voltage is applied. All register information is lost when VA is removed and the VA POR is asserted. Refer to Table 3-1 for a valid operating range of VA and Table 3-13 for VA POR specifications.

4.2.3 Chip-Level $\overline{\text{RESET}}$

Asserting and deasserting the $\overline{\text{RESET}}$ pin reinitializes the device, putting all registers and device configurations back to their default values and state. The control ports are not accessible while $\overline{\text{RESET}}$ is asserted.

After $\overline{\text{RESET}}$ is deasserted with the 32.768 kHz reference clock applied, the control ports are active and the device boots from the internal boot ROM into Basic Haptics Mode ready to generate haptic alerts when triggered (see Section 4.4.2).

While $\overline{\text{RESET}}$ is asserted, the amplifier weak-drive FETs to ground are enabled resulting in a typical OUT± pull-down resistance of less than 1.00 Ω. Once $\overline{\text{RESET}}$ is deasserted, the amplifier outputs actively switch driving a modulated zero level (i.e., an idle channel) until triggered in Basic Haptics Mode to generate a waveform or until the device power-up sequence is initiated by the host which disables the output.

4.2.4 Device Initialization Sequence

This device initialization sequence is not required to use Basic Haptics Mode, but must be completed as part of the initialization for normal mode following a power-on reset, the deassertion of the $\overline{\text{RESET}}$ input, or the completion of a control-port soft reset as described in Section 4.2.1, Section 4.2.2 and Section 4.2.3. In all cases, the power-up delay t_{IRS} specified in Table 3-14 must be observed before writing this initialization sequence.

Table 4-4. Device Initialization Sequence

Step	Operation	Address	Value
1	Write	0x0000 3008	0x000C 1837
2	Write	0x0000 3014	0x0300 8E0E
3	Write	0x0000 0040	0x0000 0055
4	Write	0x0000 0040	0x0000 00AA
5	Write	0x0000 4100	0x0000 0000
6	Write	0x0000 4170	0x002F 0065
7	Write	0x0000 4360	0x0000 2B4F
8	Write	0x0000 4310	0x0000 0000
9	Write	0x0000 0040	0x0000 00CC
10	Write	0x0000 0040	0x0000 0033
11	Write	0x0000 4400	0x0000 0000
12	Write	0x02BC 20E0	0x0000 0000
13	Write	0x02BC 2020	0x0000 0000
14	Write	0x02B8 0080	0x0000 0001
15	Write	0x02B8 0088	0x0000 0001
16	Write	0x02B8 0090	0x0000 0001
17	Write	0x02B8 0098	0x0000 0001
18	Write	0x02B8 00A0	0x0000 0001
19	Write	0x02B8 00A8	0x0000 0001
20	Write	0x02B8 00B0	0x0000 0001
21	Write	0x02B8 00B8	0x0000 0001
22	Write	0x02B8 0280	0x0000 0001
23	Write	0x02B8 0288	0x0000 0001
24	Write	0x02B8 0290	0x0000 0001
25	Write	0x02B8 0298	0x0000 0001
26	Write	0x02B8 02A0	0x0000 0001
27	Write	0x02B8 02A8	0x0000 0001
28	Write	0x02B8 02B0	0x0000 0001
29	Write	0x02B8 02B8	0x0000 0001

4.3 Hibernation Mode

The CS40L25/B features a low-power hibernation mode, AoH Hibernate. In this mode, all register contents are lost, but the contents of RAM are retained. During AoH Hibernate, only always-on digital functions to support wake-up from this retention mode are enabled.

Entry to this mode is achieved via the register interface (either by an external driver using the Control Port, or the programmable DSP). Exit from this mode is configurable and may be triggered by activity on GPIO and/or the SDA/MOSI control port pin. Haptic playback is triggered from GPIO1, GPIO2 or GPIO4 transitions when these wakeup events are configured and enabled. However, control port pin activity detected during AoH Hibernate only triggers the transition to AoH Stanby mode without triggering haptic playback or the decoding of the control port command that triggered the wakeup.

Note: To optimize platform battery life by maximizing the time in CS40L25/B AoH Hibernate mode, avoid sharing the control port bus with other high duty cycle sensors. Any control port activity, not just transactions addressed to the CS40L25/B, trigger it to wake from AoH Hibernate and transition to a momentarily active state where it consumes higher current until the DSP firmware determines there is no haptic processing required and triggers the return to AoH hibernate.

Before the always-on hibernation mode circuitry can be used, it must first be configured as described below.

4.3.1 Setup

Configuration of the hibernation logic is done through the register interface on the device. An internal bus is used to transfer register data written to the device into the hibernation logic. While the device is busy processing a write across this internal bus, WR_PEND_STS is set. Any additional writes made to the hibernation mode registers while WR_PEND_STS is set are blocked.

If configuring the device via the I²C Control Port, write blocking is not a concern as the I²C protocol is slower than the maximum time taken by this internal bus. SPI Control Port accesses where the SPI_CLK is faster than 14 MHz may be affected by write blocking, depending on how quickly subsequent writes can be made, so polling WR_PEND_STS is recommended.

Up to four external pins can be monitored while in AoH hibernate mode. These are selected by WKSRC_EN as shown in Table 4-5. Any combination of these four pins may be selected depending on the required use case.

Table 4-5. Hibernation Wakeup Configurations Enabled Using WKSRC_EN

WKSRC_EN	Monitored Pin
xxx1	GPIO1
xx1x	REFCLK/GPIO2
x1xx	ASP_FSYNC/GPIO4
1xxx	I2C_SDA/SPI_MOSI

By default, a rising edge on an enabled pin causes the device to exit hibernation mode. Alternatively, falling-edge sensitivity can be selected by changing WKSRC_POL provided this functionality is enabled by device software.

In order to latch these register settings into the always-on hibernation logic, UPDT_WKCTL must be set. If UPDT_WKCTL is cleared, writes to WKSRC_EN and WKSRC_POL are latched into the device register map (i.e. they can be read-back via the Control Port) but are not latched into the always-on logic.

4.3.2 Memory Ready Flag

The device supports a single bit flag whose value persists while entering and exiting the hibernation state. This flag is configured by MEM_RDY. The value written to MEM_RDY is latched into the always-on hibernation logic, and can be read back using MEM_RDY_STS.

Upon exit from hibernation mode, register settings are set to default values. As a result, the MEM_RDY bit will always read-back 0 in this case. However, the MEM_RDY_STS bit will read back whatever value was programmed into MEM_RDY before hibernation mode was entered.

4.3.3 Entry into Hibernation Mode

Entry into Hibernation Mode is triggered by setting TRIG_HIBER. Entry into hibernation mode must only be triggered by control software once GLOBAL_EN is cleared and the device has fully transitioned into the power-down state (MSM_PDN_DONE_STS1 = 1). Hibernation mode is not supported while WKSRC_EN = 0, so WKSRC_EN must be configured and latched into the always-on logic as described in Section 4.3.1 before setting TRIG_HIBER.

It is recommended to make configuration changes to the PWRMGT_CTL register with TRIG_HIBER = 0 in one write, and then repeat the same write with TRIG_HIBER = 1. This ensures that the configuration of the hibernation logic is completed as expected prior to entering hibernation.

Once TRIG_HIBER is written, the device begins the transition into hibernation. During the transition into hibernation, the device is not capable of capturing pin toggles on the pins being monitored. Once the hibernation mode is reached, the pin transitions are captured.

4.3.4 Exit from Hibernation Mode

Exit from hibernation mode occurs once the first enabled wake source signal defined by WKSRC_EN transitions from low to high (or high to low if the polarity is reversed by WKSRC_POL). The chip transitions from hibernation mode into standby mode, the device registers are reset and the Control Port is available. The time taken for this transition to complete and the device being ready to use is t_{IW} in Table 3-14.

The source responsible for causing the exit from hibernation mode is reflected in the WKSRC_STS field. This field is cleared when the device is commanded to enter hibernation mode by TRIG_HIBER = 1.

If an exit Hibernation event occurs concurrently with an enter Hibernation event, the CS40L25/B nonvolatile memory (RAM) may not be transferred to the control port or the DSP core. To protect against such a collision, the host must administer the following sequence upon every wake-up attempt:

1. Read back the firmware ID[1], FW ID, from register address 0x0280 000C.
2. If firmware ID is the expected value, the device has exited Hibernation mode.
3. If firmware ID is not the expected value, the device must go through another Hibernate cycle as follows:
   a) Write TRIG_HIBER = 1 with MEM_RDY = 1,
   b) Exit from Hibernation Mode.

4.3.5 Example Configuration Sequence

The following sequence shows how to typically enable hibernation mode on the device:

1. Set GLOBAL_EN = 0.
2. Wait t_{AMP_PDN} (see Table 3-4) or until MSM_PDN_DONE_STS1 = 1.
3. Configure WKSRC_EN and WKSRC_POL as required, and set UPDT_WKCTL to latch the values into the hibernation logic.
4. Set MEM_RDY if RAM memory has been initialized and is ready for execution from RAM.
5. Set TRIG_HIBER.

4.4 Basic Haptics Mode Operation

The CS40L25 and CS40L25B provide the ability to play haptic waveforms without initialization of the device RAM memory. This support is provided after RESET deassertion using Basic Haptics Mode. Basic Haptics Mode effects can be triggered by a control port write or GPI transition. Basic Haptics Mode requires only a minimum set of RAM parameter writes to configure haptic effect parameters, and default values for these parameters may be used to enable haptic playback triggered by power management or battery charging circuitry prior to boot-up of the host system main processor and operating system.

Basic Haptics Mode delivers only a subset of the haptic functionality available while running from RAM in Normal Mode, and does not include advanced power saving and standby states. The transition from Basic Haptics Mode to normal mode is done by control port commands. Datasheet specifications for power consumption apply in Normal Mode, not in Basic Haptics Mode.

While using Basic Haptics Mode, the external host processor may not configure any other device registers except those required to exit Basic Haptics Mode. ROM firmware is responsible for all device register configuration in Basic Haptics Mode. Although there is no hardware mechanism to block control port register write accesses by the host processor, they are not permitted in Basic Haptics Mode. Trigger-to-haptic latency specifications apply in Normal Mode, not in Basic Haptics Mode.

1. Refer to firmware release notes.

4.4.1 Entering Basic Haptics Mode

The CS40L25 and CS40L25B enter Basic Haptics Mode operation upon deassertion of the $\overline{\text{RESET}}$ pin. These devices are pre-configured to accept their clock reference from a specific pin, so the device variant (CS40L25 or CS40L25B) must match the pin connection scheme used on the PCB. See the Typical Connection Diagrams in Fig. 2-1 – Fig. 2-4.

Basic Haptics Mode is available following the device initialization interval t_{IRS} (see Table 3-14). Basic Haptics Mode generates an interrupt upon completion of device initialization. The device is ready when Amp_Status (address 0x0280 018C) = 0x1. Refer to Table 4-6.

4.4.2 Using Basic Haptics Mode

Basic Haptics Mode. running from ROM, enables single frequency haptic vibration effects triggered by a GPI transition, or a control port write. Basic Haptics Mode initializes with default parameters which may be used or modified through the control port. Values are read/write accessible in the following control-port addresses shown in Table 4-6.

Table 4-6. Basic Haptics Mode Register Controls

Name	Address	Default Value	Description
GPIO_trigger_edge	00280 0178	0x1 (CS40L25) 0x5 (CS40L25B)	Determines which edge of each available GPIO will trigger haptic playback. • 0x0 All GPIs disabled. • 0x01 GPIO1 rising edge detection enabled. • 0x02, GPIO1 falling edge detection enabled. • 0x04 GPIO2 rising edge detection enabled. • 0x08 GPIO2 falling edge detection enabled. • 0x10 GPIO3 rising edge detection enabled. • 0x20 GPIO3 falling edge detection enabled. • 0x40 GPIO4 rising edge detection enabled. • 0x80 GPIO4 falling edge detection enabled. **Note:** The CS40L25 supports GPIO1 triggering only. **Note:** The CS40L25B supports GPIO1, 2, 3, and 4 triggering with bitwise OR'ed combinations of these enumerated values.
Buzz_Freq	0x0280 017C	160 (160 Hz)	Sets the frequency of the Haptic output.Set in 1 Hz granularity.
Buzz_Level	0x280 0180	200 (2.00 V_{RMS})	Sets the Root Mean Square (RMS) voltage level of the haptic output. Set in 0.01 V_{RMS} granularity.
Buzz_Duration	0x280 0184	125 (0.5 s duration)	Sets the duration of the Haptic effect.Set in 0.004s granularity using the value calculated from: BUZZ_DURATION = duration_in_ms / 4.
Buzz_Trigger	0x0280 0188	0	Set to 0x1 to trigger a haptic effect. This bit is cleared once the request is detected.
Amp_Status	0x0280 018C	0	The run and error state of the amplifier. These error bits are persistent and will remain set even after if the error conditions have cleared. • 0 No status. • 0x1 The device booted correctly. • 0x2 OTP unpacking error detected. • 0x4 Output short error detected. • 0x8 Temperature increase warning detected. • 0x10 Over-temperature error detected.

Note: These registers are not available and may not be accessed after exiting Basic Haptics Mode.

4.4.3 Exiting Basic Haptics Mode

Basic Haptics Mode persists until the host driver configures RAM memory and switches the device to operate from RAM.

4.5 Class D Amplifier

The CS40L25/B amplifier incorporates a high-performance digital PWM generator feeding into a closed-loop Class D modulator.

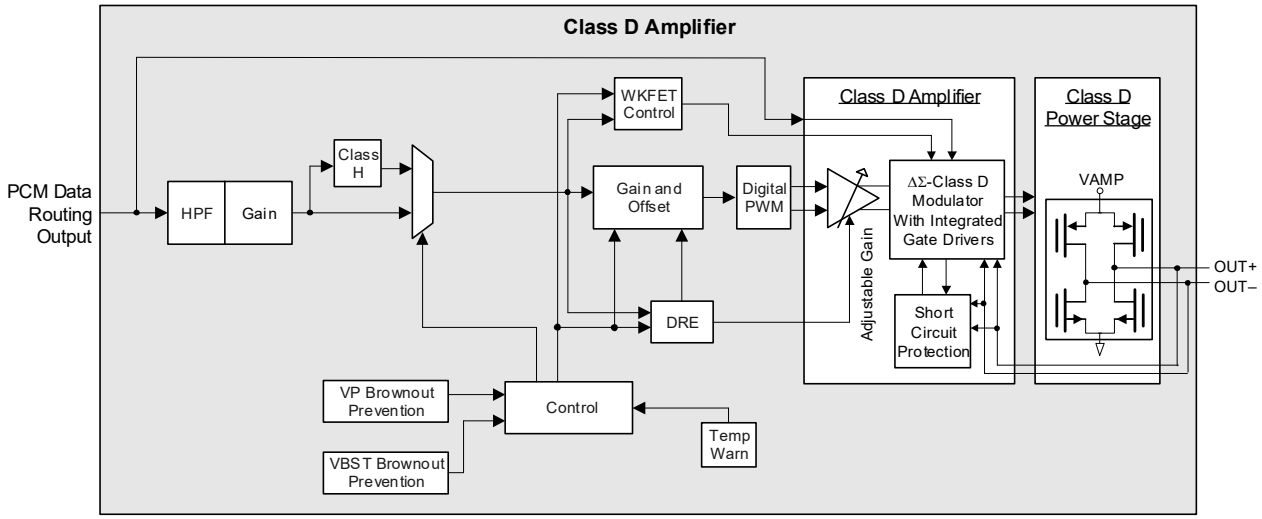


Figure 4-3. Class D Amplifier Block Diagram

4.5.1 Amplifier PWM Output Edge Control

The amplifier's PWM output edge control registers allow configuration of the rise and fall times of the PWM switching on the amplifier's outputs (OUT±).

4.5.2 OUT± Shorts Detection

To determine whether the OUT+ or OUT– pins are shorted together, to GND or to VAMP, a comparison of the expected PWM output is made versus the actual OUT± output. If a large enough difference is detected, an amplifier output short error is reported and the device enters Actuator-Safe Mode to prevent damage to the device or system. For an OUT± short to GND or short to VBST condition, no output signal is required. However, for an OUT+ to OUT– shorts condition to be observed, a large enough, nonzero haptic signal must be applied to produce a measurable difference on the PWM outputs.

Upon detection of an amplifier output short, the amplifier enters Actuator-Safe Mode and optionally asserts an $\overline{\text{ALERT}}$ interrupt to the host.

4.5.3 Amplifier Outputs While in Reset

While $\overline{\text{RESET}}$ is asserted, the CS40L25/B grounds OUT±. Once $\overline{\text{RESET}}$ is released, the amplifier outputs are Hi-Z until the device power-up sequence is initiated.

4.6 Digital Boost Converter

The digital boost converter consists of three ADCs and two digital control loops. The three ADCs measure the VP voltage, VBST voltage, and inductor current through the boost converter's N-FET. This digitized voltage and current information is then provided to the digital boost converter's controller for processing.

This converter uses a digitized control loop based on a current-controlled synchronous boost converter architecture that continually monitors the L_{BST} inductor current during boosted operation. The outer control loop takes the digitized VBST voltage and the digitized current information provided by the inner loop to regulate the boosted voltage to the desired level between $VBST_{MIN}$ and $VBST_{MAX}$ (see Table 3-6).

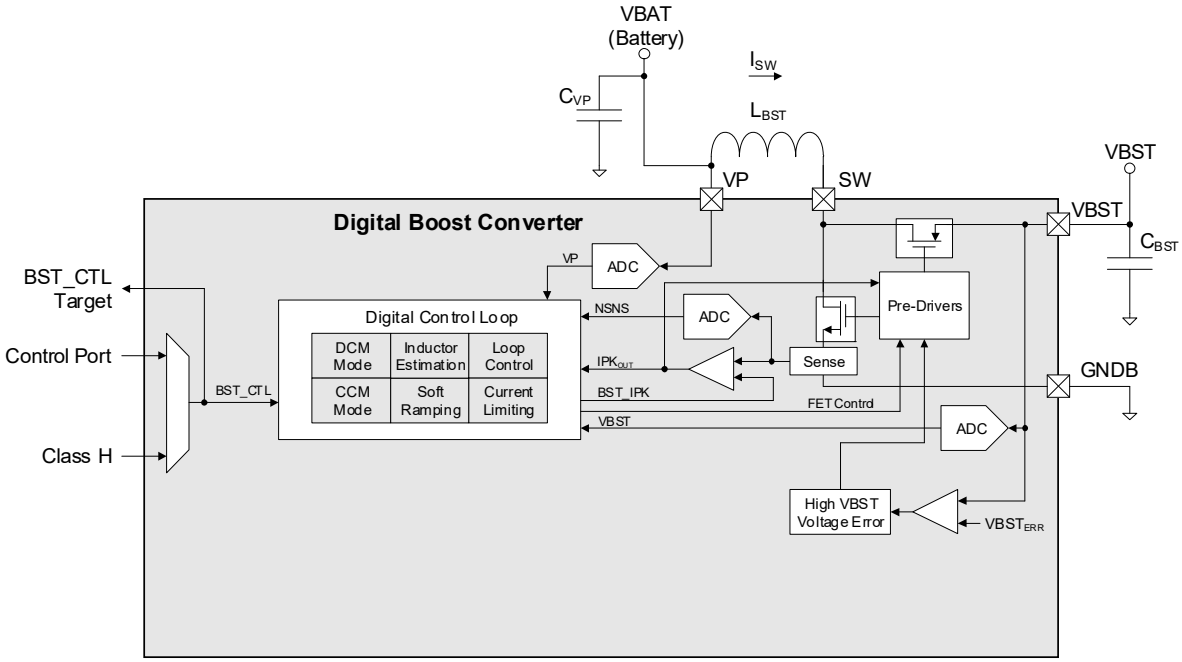


Figure 4-4. Digital Boost Converter Block Diagram

4.6.1 Inductor Current Limiting

The boost FET peak-current limit governs the peak current that is allowed to flow through the inductor during each on cycle of the boost FET. The boost FET is turned off either when the ON time of the boost FET reaches the ON time required by the controller or when it hits the boost peak-current limit. This boost current is quantized and sent to the digital boost converter control block for processing.

4.6.1.1 Peak Current Limiter

If the current demands on the output net of the boost converter (VBST) force the inductor current to reach the configured limit (I_{SW} set by BST_IPK), the boost converter limits the current through the L_{BST} inductor. If the loading on VBST remains while the current is being limited, the boost converter's output voltage may droop below its configured voltage.

4.6.2 VBST Overvoltage and Undervoltage Protection and Errors

The digital boost converter contains integrated monitoring and protection for high VBST voltage conditions. This protects against damage of both the CS40L25/B and its surrounding components.

4.6.2.1 VBST Overvoltage Protection Threshold

If a change in configuration, the system environment, or loading transient causes the VBST voltage to rapidly increase, a safety response is triggered and the controller actively limits the maximum VBST voltage ($VBST_{PROT}$ set by BST_OVP_THLD). After the VBST voltage is reduced back to its configured VBST voltage, the digital boost converter returns to normal operation.

4.6.2.2 VBST Overvoltage Protection Enable

For most operational conditions, it is recommended that the VBST overvoltage protection is enabled (by setting BST_OVP_EN) to help protect external components such as the C_{BST} capacitor.

4.6.3 L_{BST} Selection and Boost Converter Configuration

The CS40L25/B allows the flexibility of using an L_{BST} inductance of 2.2 µH to 1.0 µH. The selected L_{BST} inductor must not derate to a value of less than 0.7-µH under any condition. Depending on the manufacturer, load rating, parasitics, and type of inductor, the derating characteristics of a specific inductor can vary widely. If a given L_{BST} inductor can derate to 0.7-µH or below, it is not considered to be fully compatible with the CS40L25/B.

The digital boost converter contains controls allowing the digital boost converter's control loop to be configured for different boost converter external component configurations (L_{BST} and C_{BST}) or system-level requirements. These configurations are listed in Table 4-7.

Table 4-7. Boost Converter L_{BST} Inductor Configuration Bits

Name	Register Cross-Reference	Field Description
Boost converter coefficient 1	BST_K1	BST_K1 and BST_K2 are used to adjust the boost converter's feedback loop to compensate for the changes produced by using a different L_{BST} inductance or different system requirements. **Note:** Adjusting for a lower inductance reduces the loop bandwidth.
Boost converter coefficient 2	BST_K2	
Boost converter slope compensation	BST_SLOPE	BST_SLOPE allows for adjustment of the boost converter's internal ramp-gen slope to compensate for the changes produced by a using a different L_{BST} inductance.
Boost converter target inductance value	BST_LBST_VAL	BST_LBST_VAL seeds the digital boost converter's inductor estimation block with an initial seeded reference value.
Boost converter switching frequency	BST_CCM_FREQ	BST_CCM_FREQ controls the fundamental output switching frequency of the digital boost converter's SW net.

The recommended configurations for example L_{BST} inductor values are listed in Table 4-8. All configurations assume a maximum of 30% derating below the typical value under all operating conditions.

Table 4-8. Recommended Configurations for Common L_{BST} Values

Typical L_{BST} (µH)	Derated C_{BST} (µF)	BST_K1	BST_K2	BST_SLOPE	BST_CCM_FREQ	BST_LBST_VAL
2.2	<20	0x40	0x48	0x28	0x0	0x3
	20–50	0x32	0x49			
	51–100	0x32	0x66			
	101–200	0x4F	0xA3			
	>200	0x57	0xEA			
1.5	<20	0x40	0x48	0x3B	0x0	0x2
	20–50	0x32	0x49			
	51–100	0x32	0x66			
	101–200	0x4F	0xA3			
	>200	0x57	0xEA			
1.2	<20	0x24	0x24	0x6B	0x0	0x1
	20–50	0x32	0x49			
	51–100	0x32	0x66			
	101–200	0x4F	0xA3			
	>200	0x57	0xEA			
1.0	<20	0x24	0x24	0x75	0x0	0x0
	20–50	0x32	0x49			
	51–100	0x32	0x66			
	101–200	0x4F	0xA3			
	>200	0x57	0xEA			

4.6.3.1 Boost Converter Integrator Gain—K1 Coefficient

The boost converter integrator gain configuration is adjusted using BST_K1. This allows the user to adjust the outer loop (voltage) feedback response of the digital boost converter. It is recommended to use the configuration values listed in Table 4-8 based on the value of the selected L_{BST} inductor.

BST_K1 maintains the relationship in Eq. 4-2.

$$BST\_K1 = \frac{\frac{1}{(R_{IN} \times C_{FB})}}{4096}$$

Equation 4-2. BST_K1 Virtual Circuit Equation

4.6.3.2 Boost Converter Proportional Gain—K2 Coefficient

The boost converter proportional gain configuration is adjusted using BST_K2. This allows the user to adjust the outer loop (voltage) feedback response of the digital boost converter. It is recommended to use the configuration values listed in Table 4-8 based on the value of the selected L_{BST} inductor.

BST_K2 maintains the relationship in Eq. 4-3.

$$BST\_K2 = \frac{R_{FB}}{R_{IN}} \times 16$$

Equation 4-3. BST_K2 Virtual Circuit Equation

4.6.3.3 Boost Converter Slope Compensation

The boost converter's slope compensation is adjusted using BST_SLOPE. It is recommended to use the configuration values listed in Table 4-8 based on the value of the selected L_{BST} inductor.

4.6.3.4 Boost Converter Switching Frequency

The boost converter switching frequency is adjusted using BST_CCM_FREQ and allows the user to adjust the output switching frequency of the boost and rectification FETs.

Eq. 4-4 provides a formula for calculating the $f_{BST\_SW\_FREQ}$. The output switching frequencies will scale with an increased or decreased f_{PLL_OUT}. For most operating conditions it is recommended to leave BST_CCM_FREQ at its default configuration.

$$f_{BST\_SW\_FREQ} = \left(\frac{f_{PLL\_OUT}}{8 \times (12 + BST\_CCM\_FREQ)}\right)$$

Equation 4-4. Boost Converter CCM Switching Frequency

4.7 Signal Monitoring

Signal-monitoring ADCs, shown in Fig. 4-5, allow the internal algorithm to read the amplifier output voltage and current.

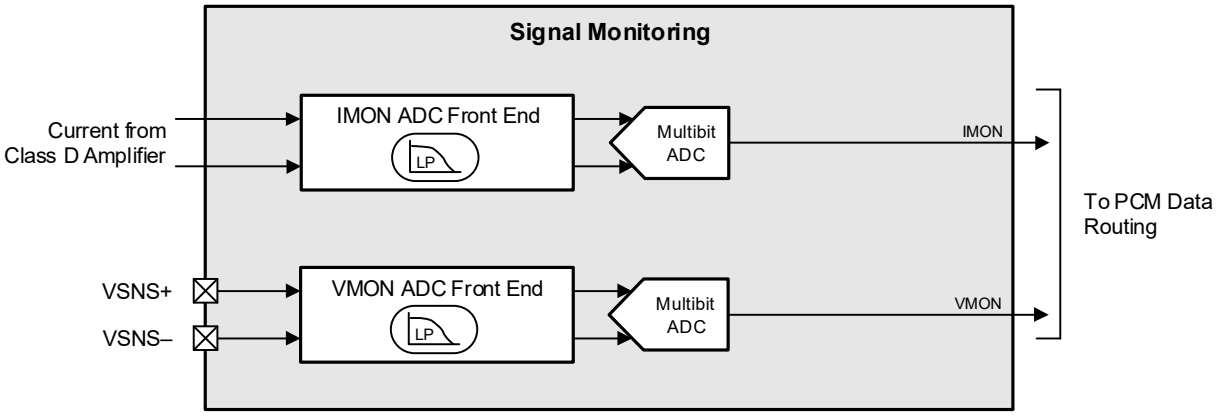


Figure 4-5. Signal Monitoring Block Diagram

The signal and supply monitoring is as follows:

- VMON—Monitors the output voltage of the Class D amplifier via the VSNS± pins.
- IMON—Monitors the current that flows into the load being driven by the Class D amplifier.

An integrated ADC digitizes each of these analog signals. MON_FILT_RESP must be set only while using a sample rate greater than 48 kHz in order to optimize the VMON and IMON signal path filter response.

4.7.1 IMON to VMON Isolation

A high level of IMON-to-VMON isolation is necessary to make sure that the current monitoring circuitry does not report a load voltage signal as a load current. The IMON circuitry is measuring a small differential signal riding on top of a relatively large common mode signal. Good IMON-to-VMON isolation is important for actuator protection accuracy, algorithm robustness, and enables the user to push the performance of the actuator as close to its limits as possible.

4.8 VP and VBST Brownout Prevention

The VP and VBST brownout prevention blocks, shown in Fig. 4-6, are used to help prevent the system battery supply (typically connected to the CS40L25/B VP input) or the VBST voltage from drooping. When enabled, these features detect when the VP or VBST, respectively, fall below error thresholds. Either error triggers attenuation of the output to reduce battery current and/or boost supply current and reduce the risk of browning out the system when the battery is in a weakened condition.

The VP brownout prevention continually monitors the VP voltage through the VPMON supply monitoring block. The VBST brownout prevention continually monitors the VBST voltage through the VBSTMON supply monitoring block. The VP brownout prevention and VBST brownout prevention are independent functional blocks with independent controls (e.g., VPBR_x and VBBR_x). VPMON_EN and VBSTMON_EN do not need to be set in order for the VP and VBST brownout prevention to be functional.

The VBST brownout prevention monitors the actual VBST supply compared against the target VBST supply required for the signal to be reproduced by the amplifier without clipping. If the actual VBST voltage has dropped a user configurable amount below the target VBST voltage, a response is triggered to attenuate the output signal in order to prevent the amplifier's output stage from clipping the waveform.

There are three main states to the VP and VBST brownout prevention block: attack, wait, and release. Fig. 4-7 provides a state diagram for the VP brownout prevention. The VBST brownout prevention is similar, only that the user configurable threshold VBBR_THLD1 is compared against a voltage difference where $VBST_{ACTUAL} - VBST_{TARGET}$ < headroom and $VBST_{ACTUAL} - signal_{TARGET}$ < headroom instead of a raw voltage (see Section 4.8.2.2). The VBST brownout prevention state diagram is shown in Fig. 4-8.

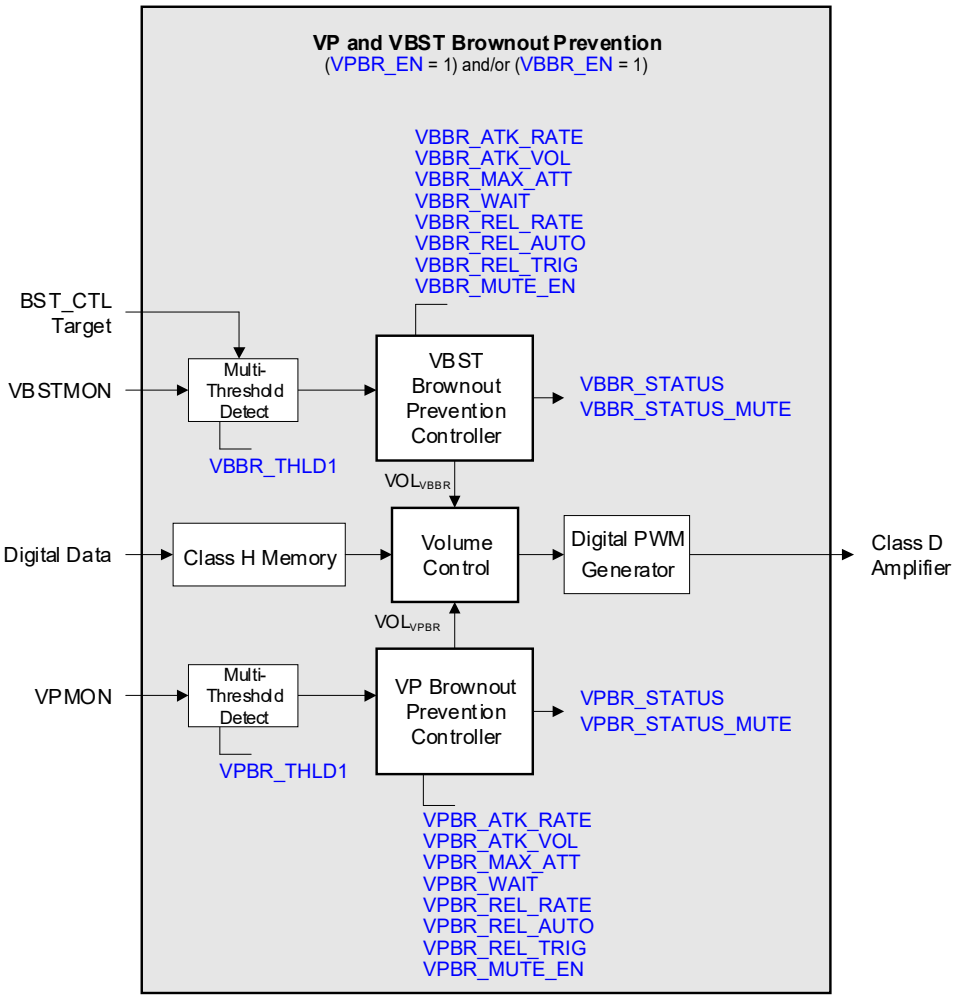


Figure 4-6. VP Brownout Prevention Overview

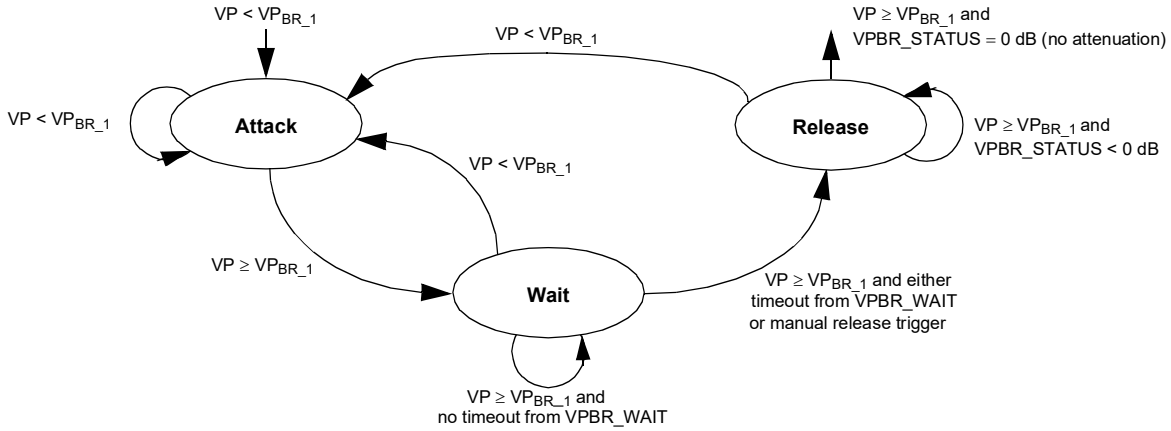


Figure 4-7. VP Brownout Prevention State Diagram

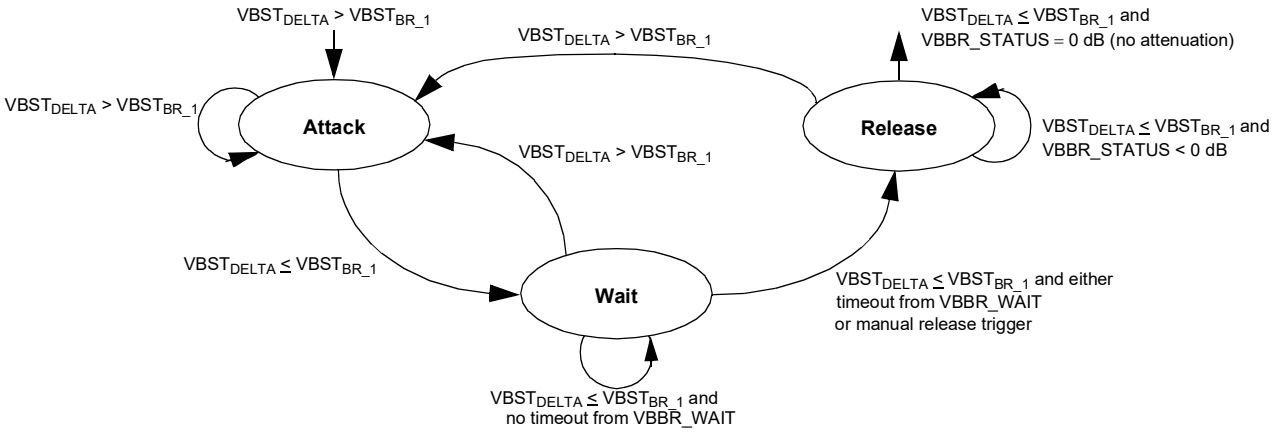


Figure 4-8. VBST Brownout Prevention State Diagram

The attack state is when the measured VP or VBST voltage has violated the initial threshold voltage (VP_{BR_1} or $VBST_{BR\_1}$). This triggers an error condition (VPBR_FLAG_EINT1, or VBBR_FLAG_EINT1), and the output volume is digitally attenuated to rapidly reduce the device power consumption due to the amplifier loading. The initial threshold voltage are set using VPBR_THLD1 and VBBR_THLD1 controlling the state of the VP and VBST brownout prevention respectively. The VP and VBST thresholds are described in more detail in Section 4.8.2.1 and Section 4.8.2.2.

If the VP or VBST supply voltage remains below Vx_{BR_1}, the digital volume is continually reduced by a volume step size of VOL_{VxBR_ATK} at a time rate of t_{VxBR_ATK} until reaching the attenuation limit, as configured by VxBR_MAX_ATT. If the VP or VBST voltage continues to fall below Vx_{BR_2} or Vx_{BR_3}, justifying a more aggressive response, the VOL_{VxBR_ATK} volume step size is automatically increased, as described in Section 4.8.2.3. This independently is applicable to the VBST brownout prevention, with its associated register configurations and thresholds.

A flowchart of the brownout prevention attack state and a description of its stages are shown in Fig. 4-9.

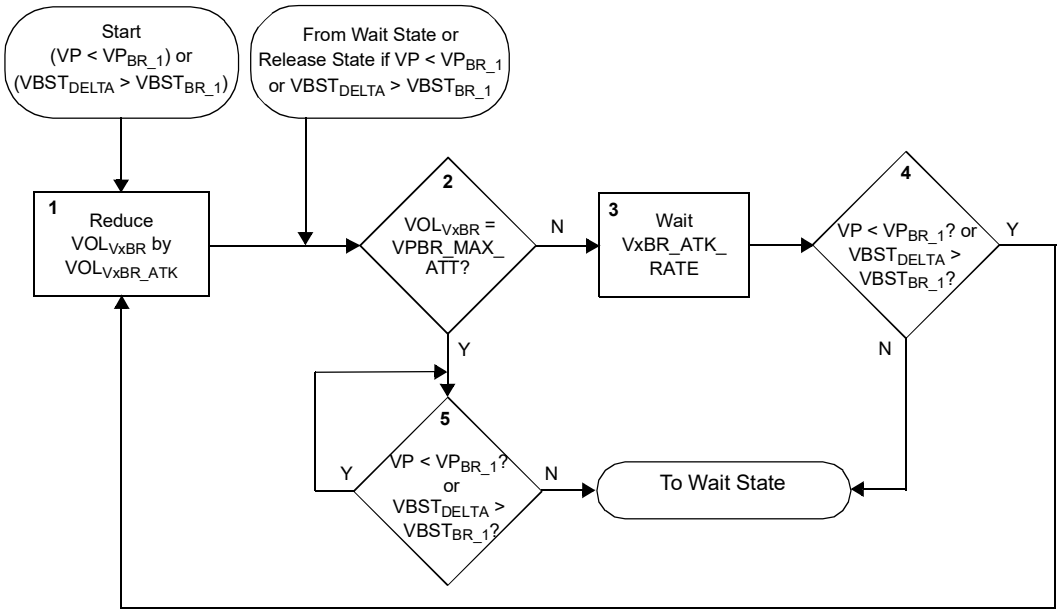


Figure 4-9. Attack State Flowchart

If the brownout prevention error condition clears, the wait state is entered. The wait state allows the supply voltage to settle and possibly recover after the reduction in amplifier loading that was produced by reducing the volume during the attack state. If the error remains cleared for a time, t_{VxBR_WAIT}, the controller exits the wait state and enters the release state. If at any time the brownout prevention error returns, the controller exits the wait state and returns to the attack state.

4.8.1 VP and VBST Brownout Prevention Enables

The VP brownout prevention block can be independently enabled using the VPBR_EN bit and the VBST brownout prevention block can be enabled using the VPBR_EN bit. The brownout blocks must be enabled for action to be taken when either of the supplies' voltage falls below the user configured threshold. The enable state of one supply monitor does not impact the enable state of the other.

If VxBR_EN is cleared to disable the functionality while attenuation is being applied, the attenuation is first completely released prior to the VPBR or VBBR functionality being disabled. When disabled, the attenuation is automatically released back to 0 dB at the configured release rate (VxBR_REL_RATE) for the respective block. The attenuation release on power-down occurs independent of the VxBR_REL_AUTO configuration (see Section 4.8.2.9).

Enabling the VP brownout prevention and VBST brownout prevention automatically enables the VPMON and VBSTMON ADCs respectively.

4.8.2 VP and VBST Brownout Prevention Voltage Thresholds

The VP and VBST brownout prevention threshold configurations are handled independently from each other and are determined by monitoring the absolute VP supply voltage and the VBST supply voltage relative to the output signal, respectively. Both brownout prevention blocks utilize a multi-threshold approach in order to minimize the over-attenuation which can often occur with a single threshold response.

The initial response thresholds VP_{BR_1} and $VBST_{BR\_1}$ thresholds are configured by the user (see Section 4.8.2.1 and Section 4.8.2.2). The second and third brownout thresholds are based on deltas from the user configured VP and VBST thresholds (refer to Table 3-10). As the voltage drop from the initial threshold becomes larger, so does the attenuation step size response.

4.8.2.1 VP Brownout Prevention Initial Voltage Threshold

The VP brownout prevention initial voltage threshold, VPBR_THLD1, configures the VP supply voltage at which the VP brownout initially starts responding (VP_{BR_1}). If the VP supply voltage falls below the configurable threshold, an error condition is triggered and the VP brownout responds by entering an attacking state.

4.8.2.2 VBST Brownout Prevention Initial Voltage Threshold

The VBST brownout prevention initial voltage threshold, VBBR_THLD1, configures the threshold that determines whether the difference between the target VBST supply voltage and the measured VBST supply is large enough to trigger an error condition $VBST_{TARGET} - VBST_{MEAS} = VBST_{DELTA}$. If the $VBST_{DELTA}$ is large enough to exceed the configured VBBR_THLD1 an error condition is triggered and the VBST brownout prevention responds by entering an attacking state.

The VBSTMON is used to determine the $VBST_{MEAS}$, which is compared against the target VBST voltage ($VBST_{TARGET}$).

4.8.2.3 Brownout Prevention Attack Volume/Gain

The VP and VBST brownout prevention attack volume step sizes are configurable via VPBR_ATK_VOL and VBBR_ATK_VOL. The VOL_{VPBR_ATK} and VOL_{VBBR_ATK} responses are listed for each of the voltage thresholds in the Table 4-9.

The VPBR_ATK_VOL configures the amplitude of the attenuation step for each of the three VP voltage thresholds. During an attacking phase, the reactive VP brownout's volume response per step period is controlled by the configurable VPBR_THLD1 and two other preconfigured threshold ranges. This multithreshold approach allows the attenuation response to scale with how far below that user-configurable threshold the VP voltage has dropped.

The multithreshold approach has advantages over a single threshold approach. It reduces the overcorrection that can occur with a larger fixed-amplitude response when triggered by a marginal condition, while still allowing for a more aggressive response when the voltage supply conditions dictate it to be necessary. If the VP or VBST voltage is right at the VxBR_THLD1 voltage and the brownout prevention response triggers a drop in power consumption, the supply voltage can quickly recover. This may lead to a situation where the volume transitions back and forth between an error and non-error conditions with a larger corrective step. The multithreshold approach is designed to reduce this repetitive pumping pattern of attacking and releasing which can occur with single threshold solutions.

Table 4-9. Volume Attack Step Size

VPBR_ATK_VOL or VBBR_ATK_VOL	VOL_{VxBR_1} Attack Attenuation (dB/step)	VOL_{VxBR_2} Attenuation (dB/step)	VOL_{VxBR_3} Attenuation (dB/step)
000	0.0625	0.125	0.250
001	0.125	0.250	0.500
010	0.250	0.500	1.000
011	0.500	1.000	2.000
100	0.750	1.500	3.000
101	1.000	2.000	4.000
110	1.250	2.500	5.000
111	1.500	3.000	6.000

Fig. 4-10 shows an example of the multithreshold VP brownout prevention mechanism's impact on the effective digital volume of the amplifier output path for a relatively slow-falling VP supply.

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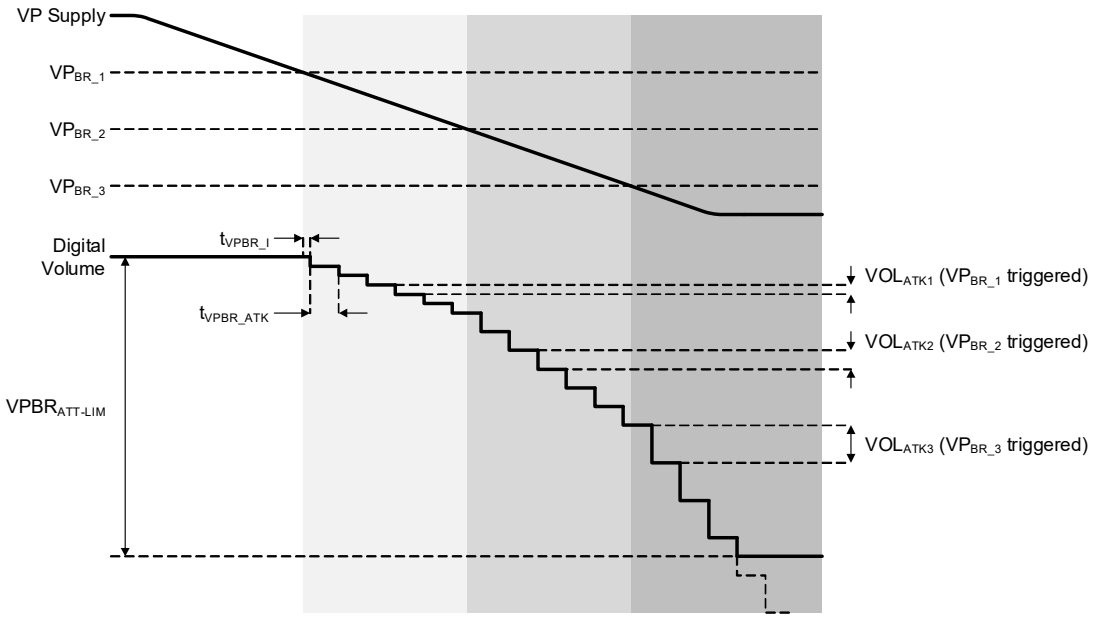


Figure 4-10. Reactive Brownout Prevention Attack — Slow VP

In this case, the VP supply spends multiple attack periods below each VP voltage threshold as the VP supply falls. Once VP falls below VP_{BR_1} (specified in Table 3-10), VOL_{ATK1} attenuation level is applied following the initial response attack time t_{VPBR_I}. Over the course of each subsequent attack time (t_{VPBR_ATK}), the VP brownout prevention mechanism evaluates the VP supply level relative to VP_{BR_1}, VP_{BR_2}, and VP_{BR_3} (specified in Table 3-10) and applies one of three VOL_{ATK} attenuation levels accordingly. As long as the brownout condition persists, attenuation is applied until the maximum allowable attenuation ($VPBR_{ATT-LIM}$, specified in Table 3-10) has been applied. See Section 4.8.2.5 for details.

Fig. 4-11 shows a relatively fast-falling VP supply that drops below the lowest VP voltage threshold (VP_{BR_3}) before the completion of one full attack period (t_{VPBR_ATK}). Following the VP supply falling below VP_{BR_1} such that VOL_{ATK1} attenuation levels is applied, the VP supply rests below VP_{BR_3} for a large enough portion of the first full attack period that the largest of the three VOL_{ATK} attenuation levels is applied. In this case, the VOL_{ATK2} attenuation level is skipped completely.

.

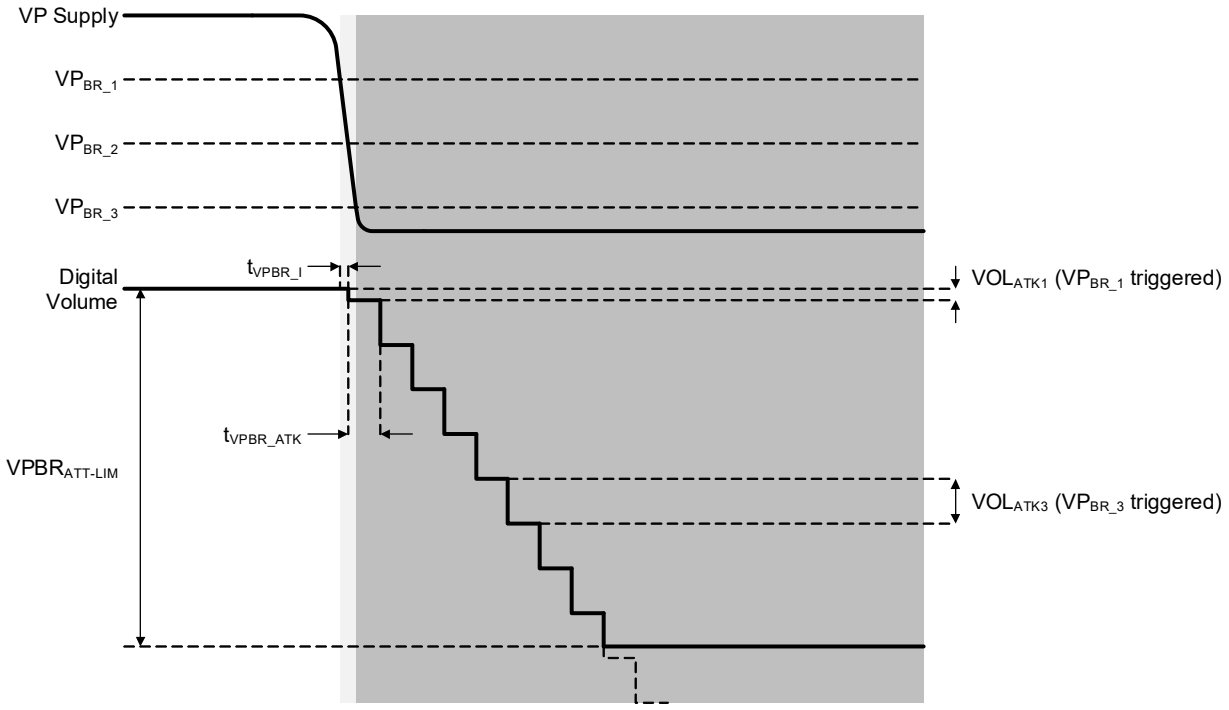


Figure 4-11. Reactive Brownout Prevention Attack — Fast VP

The digital volume may optionally be muted upon the reactive VP brownout attenuation saturating to $VPBR_{ATT-LIM}$; see Section 4.8.2.6 for more information.

Although these examples describe VP brownout sequences, similar behavior occurs with VBST brownout.

4.8.2.4 Brownout Prevention Attack Rates

The attack rate register fields, VPBR_ATK_RATE, and VBBR_ATK_RATE, configure the time between consecutive VP and VBST brownout prevention volume attenuation adjustments when an error condition remains present. The attack rate control does not affect the timing of the initial attacking response (t_{VPBR_I} or t_{VPBR_I}) when a VP or VBST brownout prevention error first occurs, only the time between consecutive attacking volume attenuation adjustments (t_{VxBR_ATK}).

The typical VxBR_ATK_RATE times are based on f_{PLL_OUT} = 192 MHz. The VxBR_ATK_RATE configurations can have a ±1 µs time period error per step relative to their typical configured value. When using an f_{PLL_OUT} other than 192 MHz, the step timings scale by 192 MHz/f_{PLL_OUT}. For more information on the different f_{PLL_OUT} frequencies, refer to Section 4.10.

The VxBR_ATK_RATE, when combined with the dynamic nature of the Digital Mode's multithreshold VOL_{VxBR_ATK} response, allows the VP and VBST brownout prevention responses to be easily tuned for a variety of reactions based on the power supply characteristics of the end system.

4.8.2.5 Brownout Prevention Max Attenuation

The VP and VBST brownout prevention maximum attenuation allows the user to control the maximum attenuation that the VP or VBST brownout can apply to the signal. Even if an error condition remains present, the brownout prevention only attenuates the signal up to the limit configured by VxBR_MAX_ATT. The VPBR_MAX_ATT attenuation and VBBR_MAX_ATT attenuation limits are configurable in increments of 1 dB, from 1 dB up to 15 dB.

4.8.2.6 Brownout Prevention Mute Enable

During the attack state, if the error volume attenuation has reached VxBR_MAX_ATT with the error condition still present, the output is muted if the VPBR_MUTE_EN bit is set for a VP brownout prevention error and the VBBR_MUTE_EN bit is set for a VBST brownout prevention error. The output remains muted until the error condition has cleared and the brownout prevention enters a releasing state.

The VPBR_MUTE_EN and VBBR_MUTE_EN must not be changed after an error condition has occurred and attenuation is present or the signal is being muted.

4.8.2.7 Brownout Prevention Release Volume Steps

The digital volume attenuation produced from a reactive VP or VBST brownout prevention error condition is released at a step size of 0.0625 dB/period (VOL_{VxBR_REL}). The small steps minimize any pumping effects or transients that can occur with larger volume step sizes.

4.8.2.8 Brownout Prevention Release Rates

VPBR_REL_RATE and VBBR_REL_RATE configure the time between consecutive VP and VBST brownout prevention volume attenuation adjustments (t_{VxBR_REL}) while in the release state and when no error conditions are present for each block.

The typical VxBR_REL_RATE times are based on f_{PLL_OUT} = 192 MHz. The VxBR_REL_RATE configurations can have a ±1 ms time period error per step relative to their typical configured value. When using an f_{PLL_OUT} other than 192 MHz, the step timings scale by 192 MHz/f_{PLL_OUT}. For more information on the different f_{PLL_OUT} frequencies, refer to Section 4.10.

4.8.2.9 Brownout Prevention Automatic Release

VPBR_REL_AUTO and VBBR_REL_AUTO configure whether the VP and VBST brownout prevention enter a configurable wait state with an automatic release when no error conditions are present or require the user to manually trigger the respective block's release.

When configured for an automatic release (VxBR_REL_AUTO = 1), the VxBR_WAIT period (see Section 4.8.2.9) is used to determine the amount of time the brownout prevention remains in the wait state before releasing. Otherwise, when configured for a manual release (VxBR_REL_AUTO = 0), the brownout prevention remains in the wait state until the VPBR_REL_TRIG or VBBR_REL_TRIG is triggered (see Section 4.8.2.11) for the respective block.

If a VP brownout error or VBST brownout error condition re-occurs while in the wait state, the brownout prevention returns back to the attack state for the respective block.

4.8.2.10 Brownout Prevention Automatic Wait

VPBR_WAIT and VBBR_WAIT configure the time (t_{VxBR_WAIT}) after the brownout prevention exits the attack state and no error conditions are present, before automatically proceeding to the release state.

The typical VxBR_WAIT times are based on f_{PLL_OUT} = 192 MHz. The VxBR_WAIT configurations can have a ±1 ms time period error relative to their typical configured value. When using an f_{PLL_OUT} other than 192 MHz, the step timings scale by 192 MHz/f_{PLL_OUT}. For more information on the different f_{PLL_OUT} frequencies, refer to Section 4.10.

4.8.2.11 Brownout Prevention Manual Release Trigger

When the VP or VBST brownout prevention is configured for a manual release (VxBR_REL_AUTO = 0), the VPBR_REL_TRIG is used to exit the wait state and enter the release state for VP brownout prevention, and the VBBR_REL_TRIG is used to exit the wait state and enter the release state for VBST brownout prevention. If the manual release is not triggered and no brownout prevention error is present, the brownout prevention will remain in the wait state as long as it is powered up.

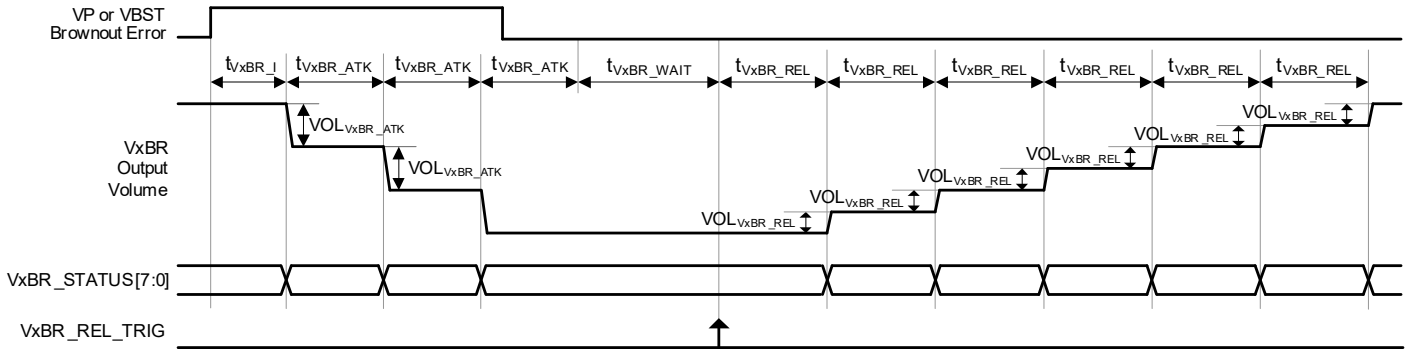


Figure 4-12. VP or VBST Brownout Prevention Manual Release

4.8.2.12 Brownout Prevention Attenuation Status

VPBR_STATUS and VBBR_STATUS are read-only register fields that report how much (if any) attenuation is applied to the output signal by the VP brownout prevention and VBST brownout prevention control. The applied attenuation (VOL_{VxBR}) value is rounded up to the nearest 0.0625 dB increments when reported by the VxBR_STATUS register field. It reports 0 dB attenuation when no attenuation is being applied by the brownout prevention.

4.8.2.13 Brownout Prevention Mute Status

If the VxBR_MUTE_EN option (Section 4.8.2.6) is enabled and the VP or VBST brownout prevention has muted the output, the VPBR_STATUS_MUTE or VBBR_STATUS_MUTE is set, indicating that the output has muted for the respective block.

4.8.2.14 Brownout Prevention Error Conditions and Attenuation Clear

If a VP brownout prevention error or VBST brownout prevention error occurs, the VPBR_FLAG_EINT1 or VBBR_FLAG_EINT1 flags are set. Once the error condition has cleared and any attenuation that has been applied has cleared and returned to 0 dB, the VPBR_ATT_CLR_EINT1 or VBBR_ATT_CLR_EINT1 flags are set indicating that attenuation is no longer being applied to the amplifier's output.

4.8.3 VP and VBST Brownout Prevention Fault/Error Conditions

Table 4-10 lists the available error and flag bits for the VP and VBST brownout prevention.

Table 4-10. VP and VBST Brownout Prevention Error Status and Mask Bits

Error	Cross-Reference to Description
VP brownout prevention error VP brownout prevention error mask	VPBR_FLAG_EINT1 VPBR_FLAG_MASK1
VP brownout prevention attenuation clear VP brownout prevention attenuation clear mask	VPBR_ATT_CLR_EINT1 VPBR_ATT_CLR_MASK1
VBST brownout prevention error VBST brownout prevention error mask	VBBR_FLAG_EINT1 VBBR_FLAG_MASK1
VBST brownout prevention attenuation clear VBST brownout prevention attenuation clear mask	VBBR_ATT_CLR_EINT1 VBBR_ATT_CLR_MASK1

4.9 Die Temperature Monitoring

Onboard monitoring of the die temperature is integrated to prevent the CS40L25/B from reaching a temperature that would compromise reliability or functionality. The CS40L25/B incorporates a two-threshold thermal-monitoring system. When die temperature exceeds the lower threshold, an overtemperature warning event occurs; if it exceeds the second threshold, an overtemperature error condition occurs.

Die over-temperature protection thresholds and protection behavior, including optional generation of alert interrupt, are configured by the device driver and programmable DSP. Additionally, the die temperature can be read-back via the register map.

The controls for the temperature monitoring are shown in Fig. 4-13.

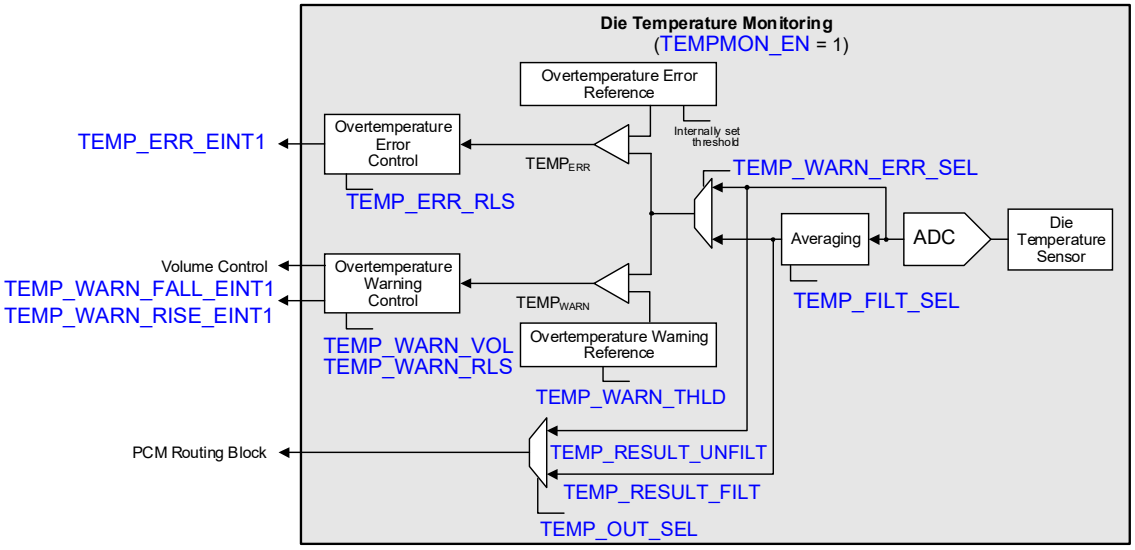


Figure 4-13. Die Temperature Monitoring Block

4.9.1 Temperature Monitoring Enable

The CS40L25/B supports independently enabling or disabling the temperature monitoring via TEMPMON_EN. The temperature monitoring can be enabled when operating in a low power mode. However, whenever the boost converter or amplifier are enabled and operating, the temperature monitoring is automatically enabled for purposes of thermal protection. Both overtemperature warning and error functions, their effects and associated interrupts, are active when the temperature monitoring is enabled either manually or automatically.

The boost converter and amplifier contain large FETs to various supplies and GND. If the die is operating outside of the specified operational temperature (see Table 3-2) and in a thermal error condition, the boost converter and amplifier are not allowed to become active for purposes of device and system level protection.

4.9.2 Die Temperature Measurement Configuration

The die temperature is first digitized by an ADC before being made available for optional averaging. The number of samples used in the moving average filter is configured by TEMP_FILT_SEL. Changes to the depth of the averaging filter will apply to all downstream blocks configured to use the filtered die temperature result.

The overtemperature warning and error blocks can use either the filtered or unfiltered die temperature result using TEMP_WARN_ERR_SEL. Similarly, the die temperature made available to the PCM data routing and selection block using TEMP_OUT_SEL.

The unfiltered result can be read via the control port using TEMP_RESULT_UNFILT. The filtered result can be read via the control port using TEMP_RESULT_FILT.

4.9.3 Die Temperature Overtemperature Warning

An overtemperature warning event occurs when the die temperature exceeds the threshold set by TEMP_WARN_THLD. The programmable die temperature thresholds are described in Table 3-11. When the die temperature exceeds the programmed threshold, a TEMP_WARN_RISE_EINT1 event is registered in the interrupt status and, if TEMP_WARN_RISE_MASK1 = 0, $\overline{\text{ALERT}}$ is asserted.

In addition to TEMP_WARN_RISE_EINT1 being set and the interrupt pin being asserted (if the error is not masked), additional protection attempts to limit further increases in die temperature. This is done by applying a programmable attenuation to the program material being amplified. TEMP_WARN_VOL is provided to program how much attenuation is applied to the signal. The amplifier's output attenuation is applied in accordance with the AMP_RAMP_PCM.

To exit the warning condition, the die temperature must drop below the threshold set by TEMP_WARN_THLD and the release bit, TEMP_WARN_RLS, must be sequenced. This will also remove the attenuation applied during the overtemperature warning event. When the die temperature drops below the programmed threshold, a TEMP_WARN_FALL_EINT1 event is registered in the interrupt status.

4.9.4 Die Temperature Overtemperature Error

An overtemperature error event occurs when the CS40L25/B die temperature exceeds the error threshold shown in Table 3-11. If the die temperature exceeds this threshold, an TEMP_ERR_EINT1 event is registered in the interrupt status register and, if TEMP_ERR_MASK1 = 0, the interrupt pin is asserted.

On an overtemperature error event, the CS40L25/B enters Actuator-Safe Mode, described in Section 4.5.2.

To exit the error condition, the die temperature must drop below the value in Table 3-11 and the release bit, TEMP_ERR_RLS must be toggled.

4.9.5 Die Temperature Monitoring Fault/Error Conditions

Table 4-11 provides links to error status and mask bits associated with components shown in Table 4-11.

Table 4-11. Die Temperature Monitoring Error Status and Mask Bits

Error	Cross-Reference to Description
Overtemperature warning rise Overtemperature warning rise mask Overtemperature warning release	TEMP_WARN_RISE_EINT1 TEMP_WARN_RISE_MASK1 TEMP_WARN_RLS
Overtemperature warning fall Overtemperature warning fall mask Overtemperature warning release	TEMP_WARN_FALL_EINT1 TEMP_WARN_FALL_MASK1 TEMP_WARN_RLS
Overtemperature error Overtemperature error mask Overtemperature error release	TEMP_ERR_EINT1 TEMP_ERR_MASK1 TEMP_ERR_RLS

4.10 Device Clocking and Reference Clock Configurations

The device requires a 32.768 kHz reference clock any time waveforms are being generated. The reference clock is not required in order to read/write registers via the control port. Depending upon system design requirements, this clock source may be provided on one of two input pins. When one GPIO input (to trigger haptic events) and the haptic I²S serial port is required, the clock is provided on the REFCLK/GPIO2 pin as shown in Fig. 2-1 and.Fig. 2-3. When more than one GPIO input to trigger haptic events is required, the clock is provided on the ASP_BCLK/REFCLK pin as shown in Fig. 2-2 and Fig. 2-4.

The reference clock is multiplied up to a 196.6080 MHz main clock by a PLL system. Clocks for all subsystems are generated from the main clock, $MCLK_{INT}$. ($F_{MCLKINT} = F_{PLL} / 16 = 12.288$ MHz). Device software enables the PLL any time that waveforms are being generated. Device software disables the PLL for lowest current consumption during always-on-haptic standby while not generating waveforms.

4.11 Auxiliary Serial Port Data Interface

The CS40L25 provides an auxiliary serial port data interface (ASP), which operates in slave mode supporting I²S and TDM formats.

The serial port interface supports three pins:

- ASP_DIN: serial data input (receive)
- ASP_BCLK: serial data bit clock, for synchronization
- ASP_FSYNC: left/right or frame synchronization alignment clock

The serial interface formats are described in Section 4.11.1. The bit order is MSB-first in each case. Refer to Table 3-18 for signal timing information.

The sample rate for streamed haptic waveforms is fixed at 48 kHz. The ASP configuration is performed by the host.

As shown in Fig. 4-14, the CS40L25's serial port accepts an externally generated clock and frame sync (ASP_BCLK and ASP_FSYNC).

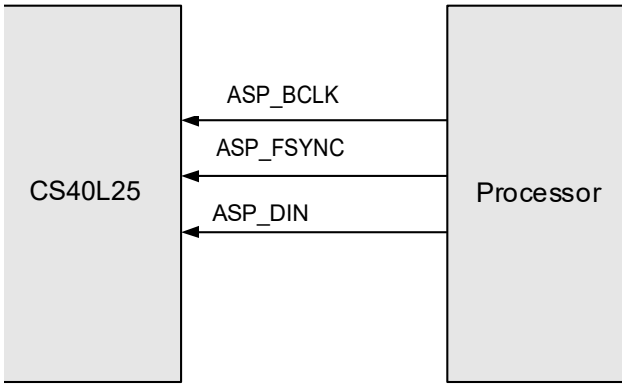


Figure 4-14. ASP_BCLK and ASP_FSYNC Slave Mode

4.11.1 Auxiliary Serial Port Mode Control and Formatting

4.11.1.1 I²S Mode Formatting

For I²S format, the MSB is considered valid on the second rising edge of ASP_BCLK following an ASP_FSYNC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, ASP_BCLK frequency, and sample rate, there may be unused ASP_BCLK cycles between the LSB of one sample and the MSB of the next. I²S format is shown in Fig. 4-15. While ASP_FSYNC is low, it is considered to be the left channel, and while ASP_FSYNC is high, it is considered to be the right channel in I²S Mode.

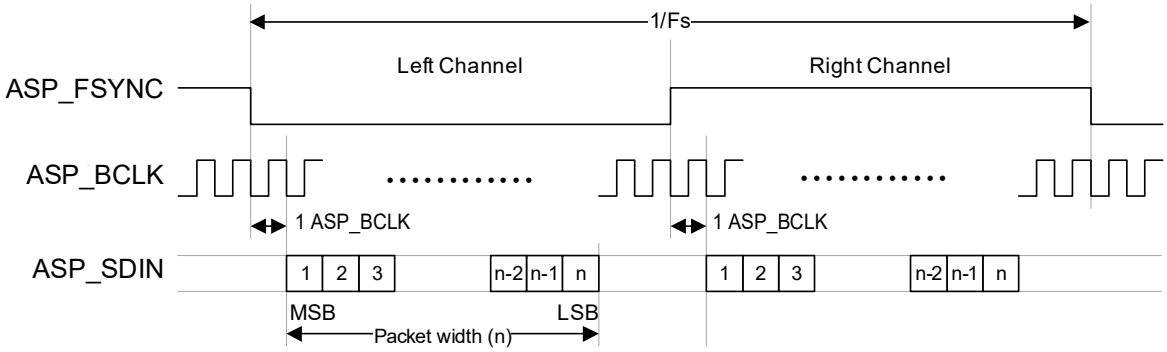


Figure 4-15. I²S Format

The even number slot locations reside on the left channel of the I²S sample period, and the odd number slot locations reside on the right channel of the I²S sample period. The slot locations are organized from lowest to highest on each channel, starting with 0 on the I²S left data channel and 1 on the I²S right data channel.

4.11.1.2 TDM Mode Formatting

The start of the TDM frame is the first rising edge of ASP_BCLK after the rising edge of the frame synchronization (ASP_FSYNC) pulse. When operating in TDM 1 Mode (ASP_FMT = 000), the MSB of the first packet for ASP_DIN is valid 1 full ASP_BCLK period after the start of the frame, as shown in Fig. 4-16. This mode is also known as DSP Mode A. When operating in TDM 1.5 Mode (ASP_FMT = 100), the MSB of the first packet for ASP_DIN is valid 1.5 ASP_BCLK periods after the start of the frame, as shown in Fig. 4-16 (with ASP_BCLK_INV set). If ASP_BCLK_INV is cleared, the ASP_BCLK must be inverted relative to Fig. 4-17 when operating in TDM 1.5 Mode.

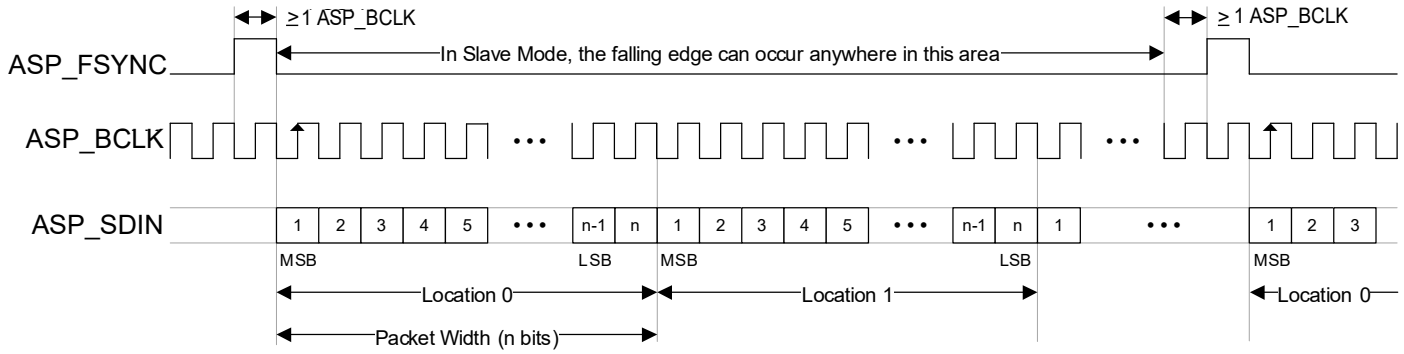


Figure 4-16. TDM 1 (DSP Mode A) Mode Formatting

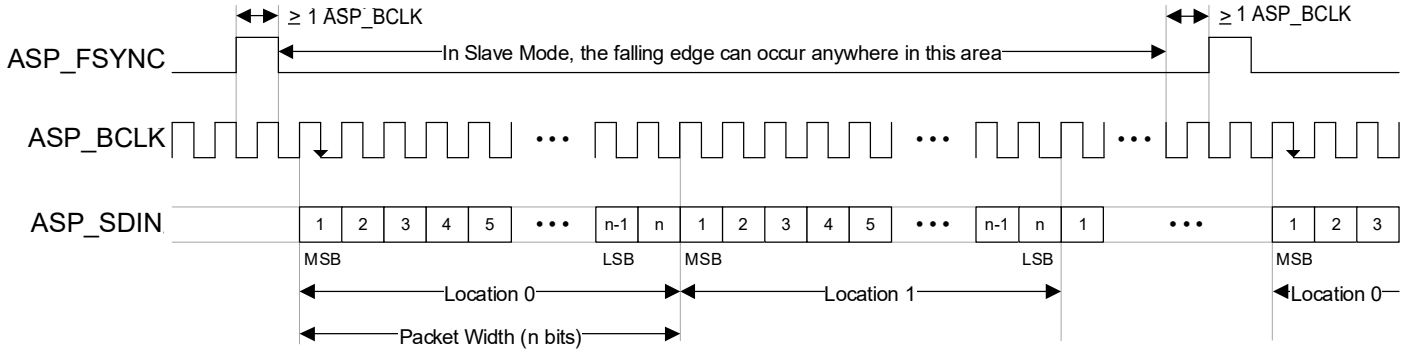


Figure 4-17. TDM 1.5 Mode Formatting

In Master Mode, the ASP_FSYNC output resembles the frame pulse shown in Fig. 4-16 and Fig. 4-17. In Slave Mode, it is possible to use any length of frame pulse less than 1/Fs, providing the falling edge of the frame pulse occurs at least one ASP_BCLK period before the rising edge of the next frame pulse.

4.11.2 Channel Slot Locations

The CS40L25 contains two receiving data packets (ASPRX1 and ASPRX2). Fig. 4-18 shows an example of I²S format where the data received is on the left channel. If the CS40L25 needed to receive the data on the first location of the right channel instead of the left channel, ASP_RX1_SLOT must be configured to slot location 1 instead.

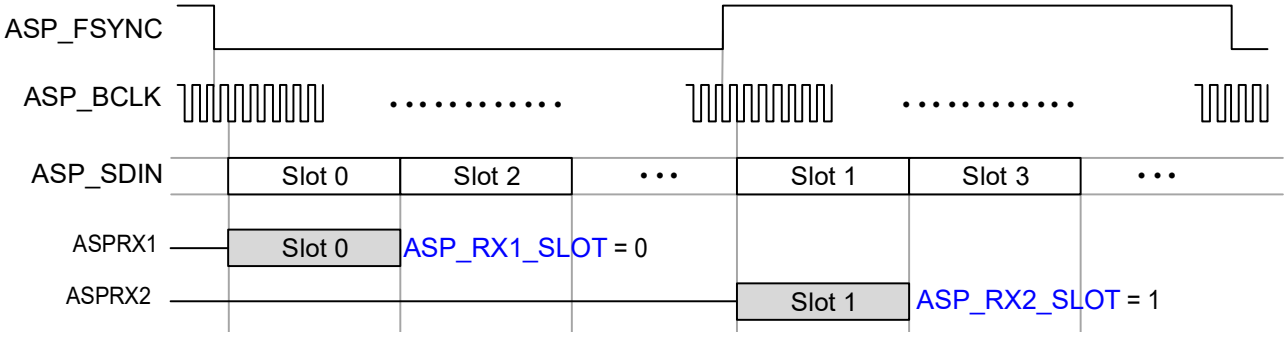


Figure 4-18. I²S Receive Slot Configuration

In the TDM Modes, the receive slot locations are 0 and 1. The data formatting of TDM 1 Mode and TDM 1.5 Mode is the same with the exception of the start location of the data. The start of the data frame is shifted a half of a clock cycle between the two modes. This means that slot location 0 starts one half of an ASP_BCLK period later in TDM 1.5 Mode than in TDM 1 Mode. This shift translates to the start location of slot 1.

The example in Fig. 4-19 illustrates receiving data in TDM 1 Mode from slots 0 and 1 using register configuration ASP_RX1_SLOT = 0 and ASP_RX2_SLOT = 1. The slot locations are shifted later by one-half clock cycle in TDM 1.5 Mode.

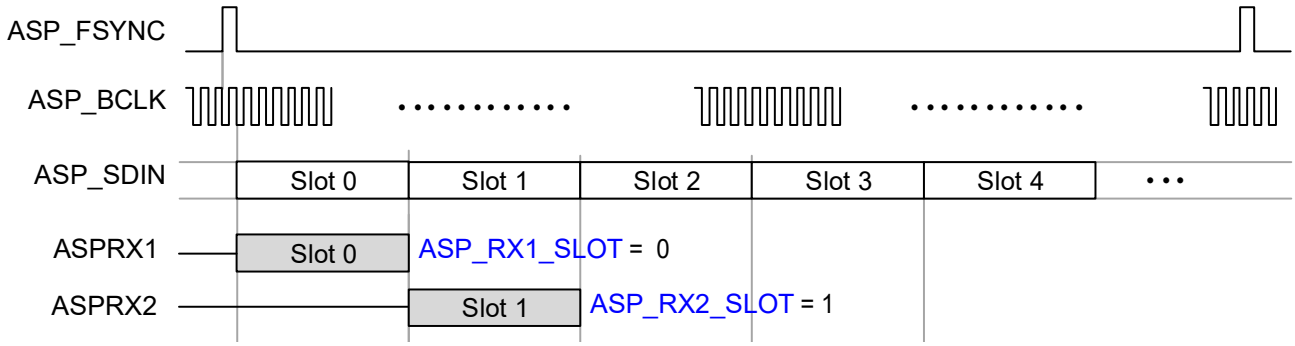


Figure 4-19. TDM 1 Mode (DSP Mode A) Receive Slot Example

4.11.3 Audio Serial Port Channel Enables

Each receive data channel has an enable and disable control (ASP_RX1_EN and ASP_RX2_EN). When the ASPRX1 and ASPRX2 input audio receive channels are disabled (ASP_RX1_EN = 0 and ASP_RX2_EN = 0), the ASP input receives zero-fill data, regardless of what data is present on the ASP_DIN pin. To put the serial port in Low Power Mode, it must be configured in Slave Mode and ASP_RX1_EN and ASP_RX2_EN must be cleared to disable both channels.

4.11.4 Serial Port ASP_BCLK and ASP_FSYNC Invert

The ASP_BCLK signal can be inverted in Slave Mode using the ASP_BCLK_INV bit. The ASP_FSYNC signal can be inverted using the ASP_FSYNC_INV bit. These bits do not move the location of the ASP_DIN data, but simply invert the polarity of the ASP_BCLK and ASP_FSYNC respectively.

4.11.5 ASP Configuration Sequence

With the device already disabled (GLOBAL_EN = 0), ASP configuration is done in the following sequence.

1. Configure the ASP by programming ASP_BCLK_FREQ, ASP_FMT, ASP_RX_WIDTH, ASP_RX_WL, ASP_RX1_SLOT, ASP_BCLK_INV, ASP_FSYNC_INV and clearing ASP_BCLK_MSTR and ASP_FSYNC_MSTR (to select external clock and sync).
2. Set ASP_RX1_EN to enable the ASP receive data path.
3. Write the appropriate value from Table 4-12 below to address 0x0000 2D10.

Table 4-12. Register Value for 0x0000 2D10

ASP_BCLK_FREQ	ASP_BCLK Frequency [MHz]	0x0000 2D10 Write Value
110011	12.288	0x0002 4010
110000	9.600	0x0002 4010
101000	6.144	0x0001 8010
100001	3.072	0x0002 C01C
011011	1.536	0x0005 4034

4. Enable the amplifier and other enabled subsystems using the global enable, GLOBAL_EN.

Note: Writing GLOBAL_EN requires coordination between the host device driver and the DSP firmware.

4.12 Programmable DSP

A DSP controls core functionality of the CS40L25/B. The Cirrus Logic DSP software consists of a real-time core and a selection of library modules accomplishing the haptic functionality.

Cirrus Logic configuration tools are used to establish the device software configuration, adapting it to the customer hardware configuration and I²S setup. These choices are compiled into the DSP program binary and data files. The DSP program binary and data files are loaded by the host. The host configures hardware and software registers affecting the haptic generator operation.

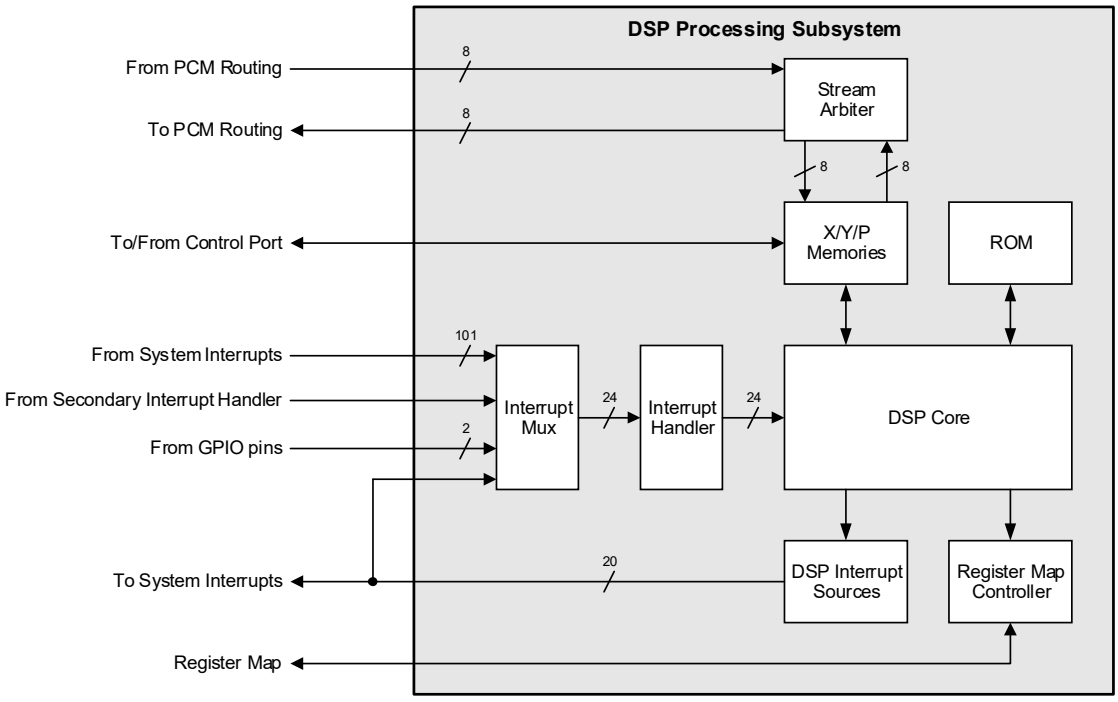


Figure 4-20. DSP Processing Subsystem

4.12.1 DSP Mailbox Registers

To facilitate direct messaging between the DSP core and the host processor, a shared register space is available. Both the Control Port and the DSP can write into this register space and, optionally, an interrupt can be generated to the hardware interrupt pin and/or the DSP core after each write. This enables an event-driven prompt to the host processor or the DSP to check the contents of the registers for new information, and perform some software-defined reconfiguration as a result.

There are three register groups - DSP_MBOX, DSP_VIRTUAL1_MBOX and DSP_VIRTUAL2_MBOX. Each register group accesses the same physical location in the hardware, but are intended for different functions.

DSP_MBOX registers, when written to, will not generate any interrupt and therefore provide silent updates.

DSP_VIRTUAL1_MBOX registers, when written to, generate an interrupt request that is intended to be seen by the DSP subsystem. The primary use case is to enable the Driver to write into the registers and inform the DSP that there is something for it to fetch.

DSP_VIRTUAL2_MBOX registers, when written to, generate an interrupt request that is intended to be output to the $\overline{\text{ALERT}}$ pin. The primary use case is to enable the DSP to write into the registers and inform the Driver that there is something for the Driver to fetch.

No interrupts are generated when any space is 'read'.

Fig. 4-21 shows the DSP Mailbox Register Groups.

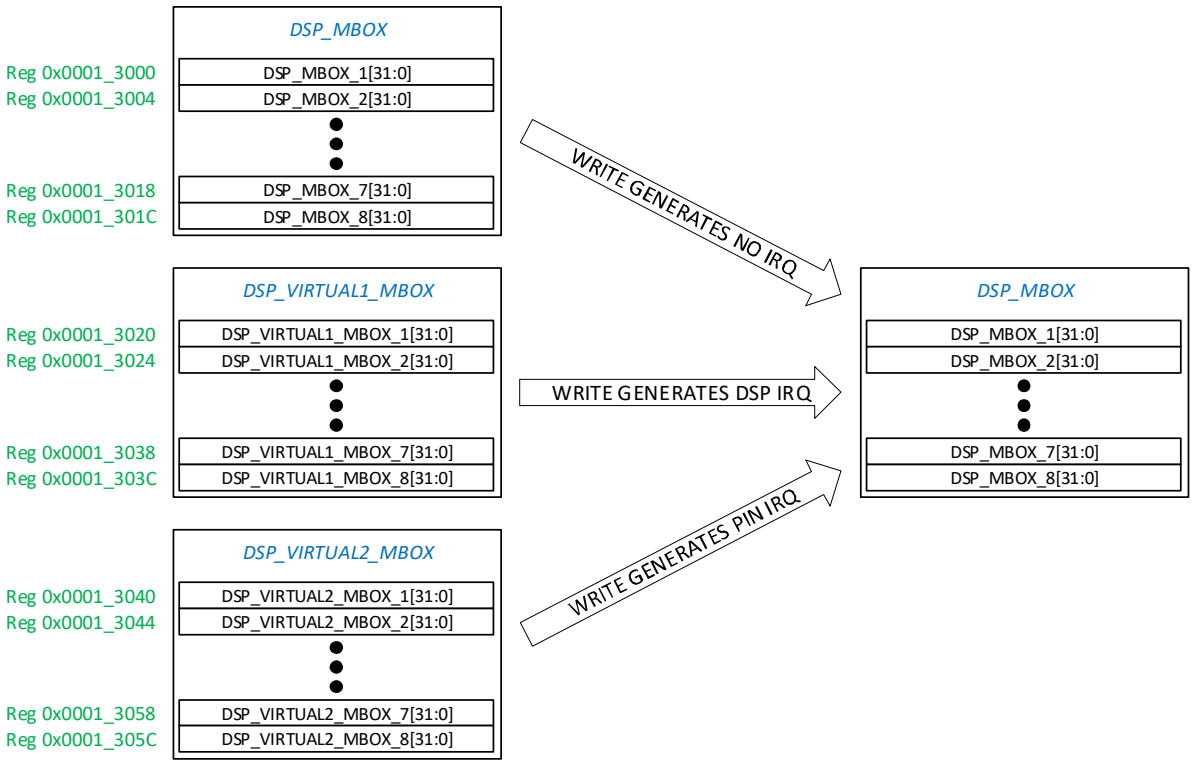


Figure 4-21. DSP Mailbox Register Groups

4.13 I²C/SPI Control Port

The host interacts with the CS40L25/B via the control port. The host device is the master port and the CS40L25/B is the slave port. Host control is implemented in the device driver. Communication constructs include a command/status channel and waveform FIFOs.

Note: The control interface function can be supported with or without system clocking; there is no requirement for MCLK, or any other system clock, to be enabled while transacting I²C.

The control port interface gives the host processor the capability to:

- read device status,
- download DSP firmware and system parameters,
- download stored haptic waveforms,
- start the execution of DSP firmware,
- trigger playback of stored haptic waveforms, and
- initiate an LRA calibration sequence.

4.13.1 Control Port Selection and Address Setting

4.13.1.1 I²C or SPI Selection

Selection of I²C or SPI mode requires no configuration from the user. By default, the device exits from reset in I²C mode. The device latches I²C mode when it receives a matching chip slave address access. If the CS40L25/B control port pins are connected to an SPI source, any SPI behavior on the bus will cause the device to latch into SPI control mode. Once the control port mode is latched, the device will stay in the chosen mode until the $\overline{\text{RESET}}$ pin is asserted or the power supplies are removed.

Table 4-13 shows the signals active on the shared Control Port pins for each mode of operation. For clarity, in subsequent sections the signal function, rather than the full pin name, is used.

Table 4-13. Control Interface Pin Functions

PIN	I²C Function	SPI Function
I2C_SCL/SPI_MISO	I2C_SCL — clock input	SPI_MISO — data output
I2C_SDA/SPI_MOSI	I2C_SDA — data input/output	SPI_MOSI — data input
I2C_AD0/$\overline{\text{SPI\_SS}}$	I2C_AD0 — address select 0	$\overline{\text{SPI\_SS}}$ — slave select
I2C_AD1/SPI_SCLK	I2C_AD1 — address select 1	SPI_SCLK — clock input

4.13.1.2 I²C Address Selection

The CS40L25/B supports four I²C slave device addresses, controlled by the logic levels on the I2C_AD0 and I2C_AD1 pins. These pins must be tied directly to VA and/or GND as close to the CS40L25/B device as possible. Table 4-14 below shows these settings.

Table 4-14. I²C Address Table

I2C_AD1	I2C_AD0	I²C Slave Device Address	
		Write	Read
GND	GND	0x80	0x81
GND	VA	0x82	0x83
VA	GND	0x84	0x85
VA	VA	0x86	0x87

A software reset will not change the CS40L25/B address. For this reason, dynamic addressing is not supported. The chip address configuration will not be ready until t_{IRS} after the hardware reset event. During this period, the CS40L25/B does not respond to any host-issued commands.

4.13.2 I2C Control

The I²C control port operates exclusively in Slave Mode. To allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit chip I²C address. All I²C transactions use the four LSB of the address to specify a read or write as indicated in Table 4-14.

SCL is a clock input, while SDA is a bidirectional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the CS40L25/B transmits logic 1 by tri-stating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the logic 1 can be recognized by the master.

The I²C control port supports START and STOP conditions, acknowledge, and standard format. It can operate in Standard-mode (Sm) with a bit rate of up to 100 kbit/s, Fast-mode (Fm) with a bit rate of up to 400 kbit/s, and Fast-mode plus (FM+) with a bit rate of up to 1 Mbit/s.

4.13.2.1 I²C Write

In an I²C write transaction, any number of data bytes is sent to the CS40L25/B. Fig. 4-22 shows the format of an I²C write command.

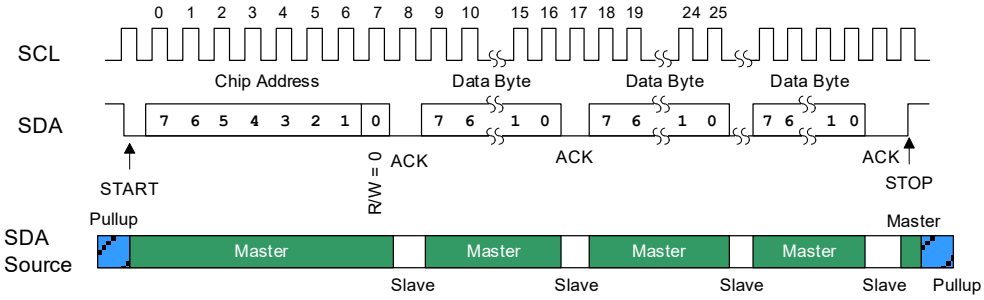


Figure 4-22. I²C Write Waveform

4.13.2.2 I²C Read

In a simple read, the CS40L25/B can receive any number of data bytes from a slave device. Fig. 4-23 shows the format of an I²C read command.

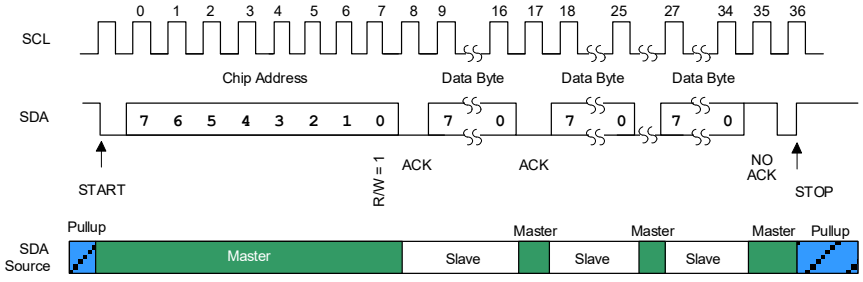


Figure 4-23. I²C Read Waveform

4.13.2.3 I²C Write-Then-Read (with Repeated Start Condition)

In a write-then-read operation (e.g., register read), the Master first sends the CS40L25/B a 4-byte register address followed by a repeated start condition, and then the CS40L25/B responds returning read data. Fig. 4-24 shows how an I²C read is performed with repeated start condition after the write operation finishes.

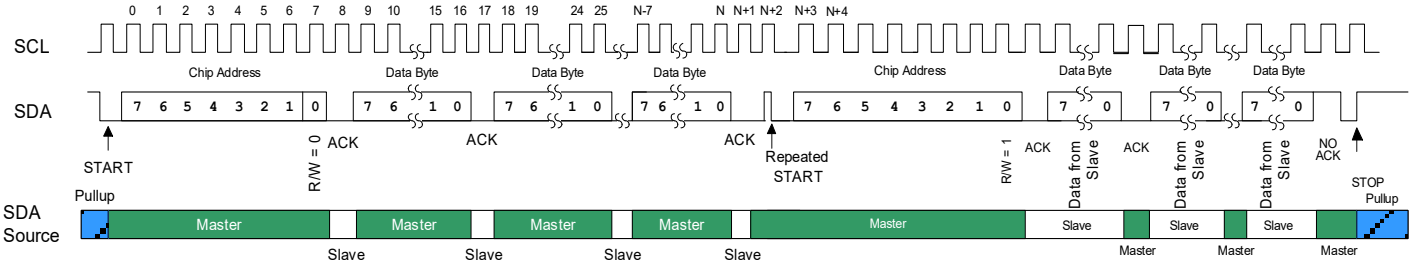


Figure 4-24. I²C Write-Then-Read Waveform (with Repeated Start Condition)

4.13.2.4 Transaction Types

The standard transaction supports a 32-bit register address and 32-bit data width. The register address must be word aligned, i.e. the two LSBs must be 0, for 32-bit transactions.

The legend shown in Fig. 4-25 is used in the following transaction examples.

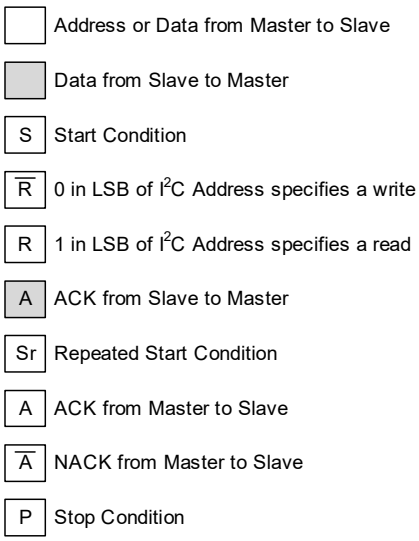


Figure 4-25. Transaction Example Legend

Fig. 4-26 shows a single 32-bit register write to a specified address.

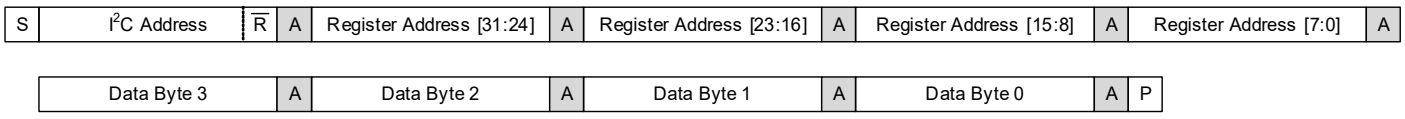


Figure 4-26. Single 32-bit Register Write Transaction

Fig. 4-27 shows a single 32-bit register read from a specified address. After the 32-bit register address is written, reading data bytes is initiated by repeated start condition followed by the chip address directly.

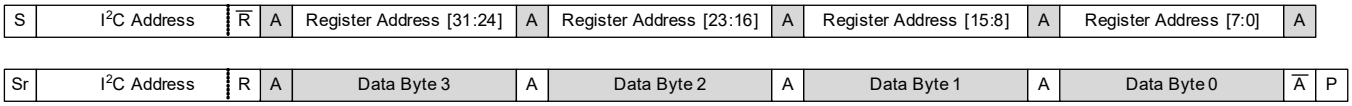


Figure 4-27. Single 32-bit Register Read Transaction

Fig. 4-28 shows multiple 32-bit register writes to a specified address. Multiple 32-bit writes may be submitted sequentially without sending the register address again. Each is submitted to the internal control bus during the ACK after every fourth data byte. If the multiple write goes past the end of the 32-bit address space, then those writes shall be discarded.

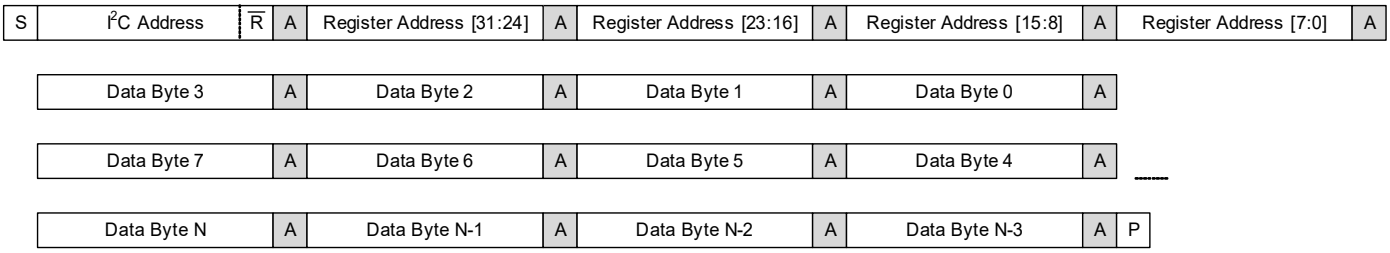


Figure 4-28. Multiple 32-bit Register Write Transaction

Fig. 4-29 shows multiple 32-bit register read to a specified address. Multiple 32-bit registers may be fetched sequentially without sending the register address again. After the first read, each subsequent read is prefetched from the internal control bus during the MSB of the first read being shifted onto the I2C bus. If the multiple read goes past the end of the 32-bit address space, then those reads will return all 0's data.

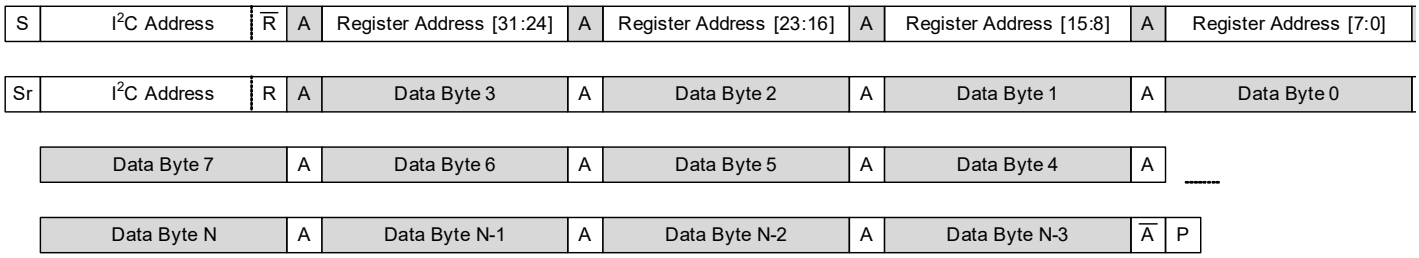


Figure 4-29. Multiple 32-bit Register Read Transaction (with Repeated Start Condition)

4.13.3 SPI Control

In write operations (R/W = 0), the SPI_MOSI pin input is driven by the controlling device. In read operations (R/W = 1), the SPI_MOSI pin is ignored following receipt of the valid register address.

If $\overline{\text{SPI\_SS}}$ is asserted (Logic 0), the SPI_MISO output is actively driven while outputting data and is high impedance at other times. If $\overline{\text{SPI\_SS}}$ is not asserted, the SPI_MISO output is high impedance.

The high-impedance state of the MISO output allows the pin to be shared with other slaves. An external pull-down resistor must be used on the SPI_MISO pin when this pin also connects to the SPI_MISO pin of another SPI slave device in addition to the SPI_MISO pin of the SPI master device.

Data transfers in SPI mode consists of a single read/write bit, followed by a 31-bit register address, 16-bits of padding, then 32-bit data words.

Fig. 4-30 shows a single register read operation.

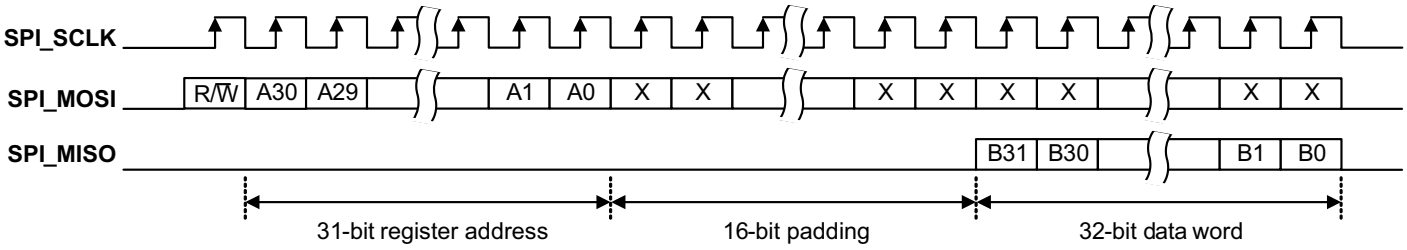


Figure 4-30. Single Register Read Operation

Fig. 4-31 shows a single register write operation.

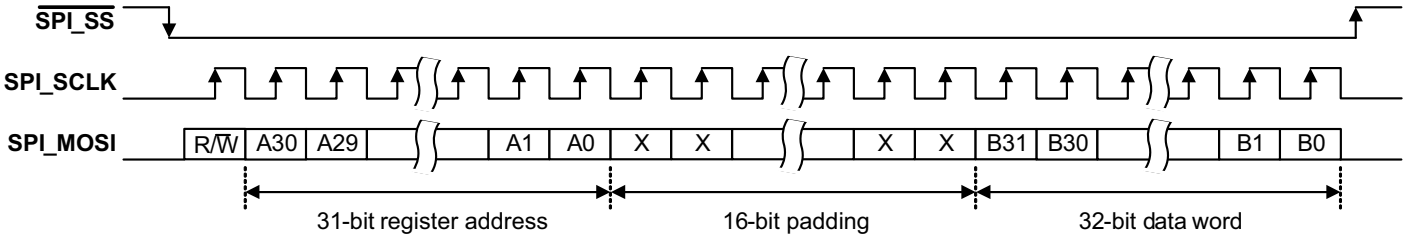


Figure 4-31. Single Register Write Operation

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS40L25/B automatically increments the register address at the end of each data word, for as long as SPI_SS is held low and SPI_SCLK is toggled. Successive data words can be input/output every 32 clock cycles. The 16-bit padding phase may only be placed between the initial register address and the first 32-bit data word - subsequent data words do not (and must not) contain padding.

Fig. 4-32 shows a continuous register write operation.

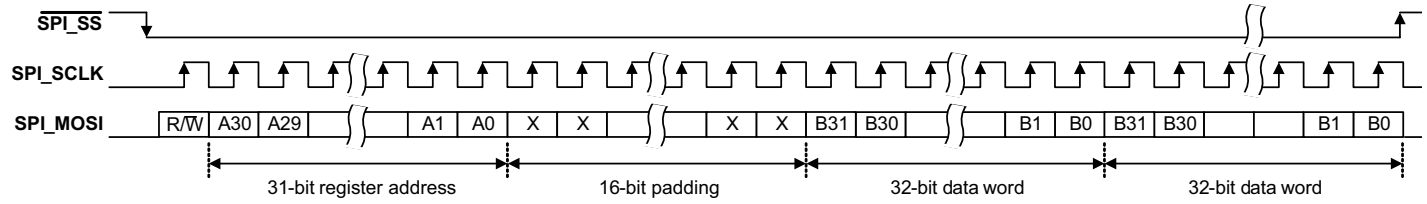


Figure 4-32. Continuous Register Write Operation

Fig. 4-33 shows a continuous register read operation.

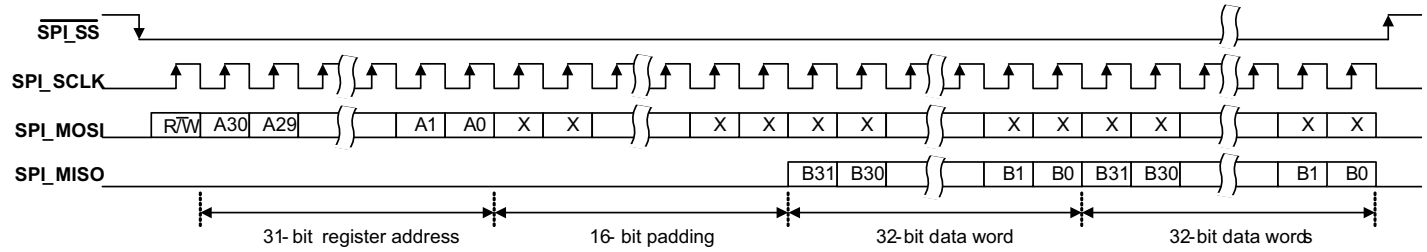


Figure 4-33. Continuous Register Read Operation

4.14 LRA Calibration and Factory Trim

During final test and calibration of the system, e.g. mobile phone, which includes the CS40L25/B, internal calibration routines shall be called via the host. The CS40L25/B runs the self-calibration routine which reports the LRA winding resistance (R_e), resonant frequency (f_0), and Q-Factor (quality factor) parameters to the driver.

The system final test and calibration utility shall check that the R_e and f_0 values are within acceptable tolerances. Assuming that the LRA is found to be normal, these values are used to calibrate the CS40L25/B to the associated LRA during normal system operation.

Resonant frequency and coil resistance f_0 and R_e calibration values may be stored by the system in its own configuration space memory, and the host programs those values into the CS40L25/B at the point of boot and general initialization.

5 Applications

5.1 Recommended External Components

This section provides information on the recommended external components for use with the CS40L25/B.Typical connection diagrams in Section 2 illustrate typical haptic application use cases. Circuit connections depend on a number of system design choices or requirements including:

- I²C or SPI connection for control port
- Pin-configured I²C address selection (while using I²C)
- One GPI trigger plus I²S haptic port, or four GPI triggers without I²S
- Haptic output power level and choice of boost inductor and capacitor

The device operates from power on running from its boot ROM in Basic Haptics Mode without host intervention. Using the full CS40L25/B feature set (running the DSP from RAM) requires host configuration of registers and loading DSP firmware and custom waveforms. The device configuration, including circuit connection options are compiled into the DSP program binary and data files loaded by the host device driver.

Fig. 5-1 and Table 5-1 show part numbers and specifications for boost converter and supply decoupling components used in several Cirrus Logic board designs. These are provided for reference only. Component tolerance and derating requirements are platform specific and must be validated in each product design.

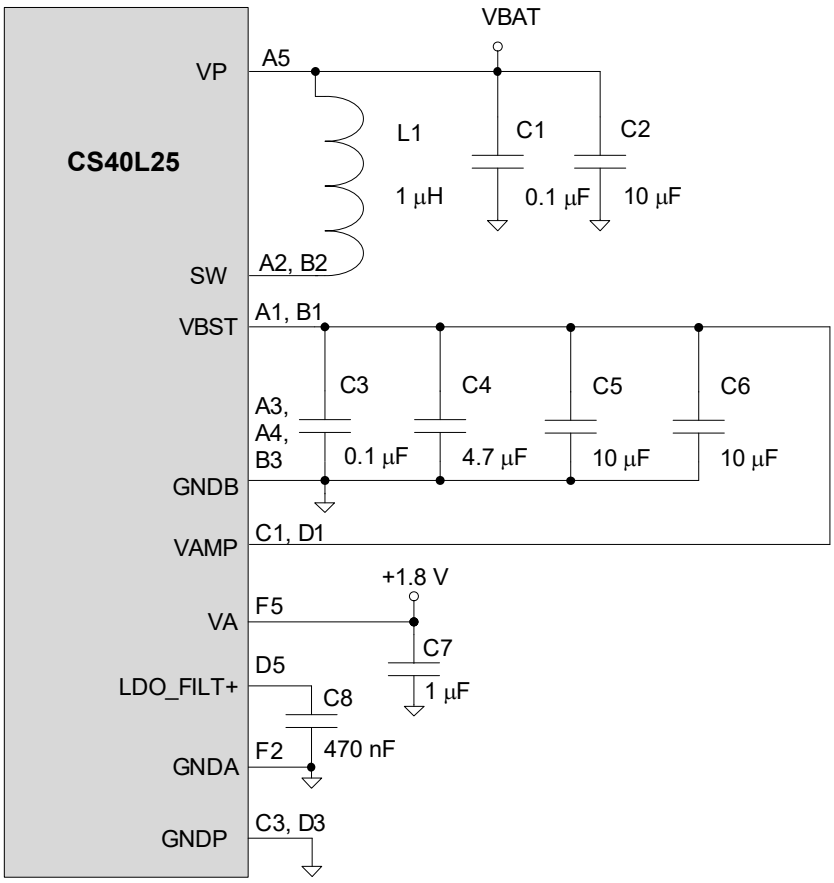


Figure 5-1. Boost Converter and Power Supply Decoupling Components (WLCSP)

Table 5-1. Recommended Components

Reference Designator	Description	Manufacturer	Manufacturer Part Number
C1	CAP 0.1 µF ±10% 10V X5R NPb 0201	TAIYO YUDEN	LMK063BJ104KP-F
C2	CAP 10 µF ±20% 10V X5R NPb 0402	SAMSUNG	CL05A106MP5NUNC
C3	CAP 0.1 µF ±10% 16V X5R NPb 0201	SAMSUNG	CL03A104KO3NNNC
C4	CAP 4.7 µF ±20% 16V X5R NPb 0402	SAMSUNG	CL05A475MO5NUNC
C5, C6	CAP 10 µF ±20% 16V X5R NPb 0603	TAIYO YUDEN	EMK107BBJ106MA-T
C7	CAP 1 µF ±10% 6.3V X5R NPb 0201	AVX	02016D105KAT2A
C8	CAP 0.47 µF ±10% 6.3V NPb X5R 0201	TDK	C0603X5R0J474K030BC
L1	IND 1 µH 3.1 A ±20% 56 mΩ SHLD NPb 0806	TDK	TFM201610ALM-1R0MTAA

5.1.1 Boost Converter

The CS40L25/B supports L7 boost inductor values of 1.0 to 2.2 µH. The inductor value must not derate below 0.7 µH during device operation. The combined boost capacitance of C300—C303 (in parallel) must not derate to less than 3.6 µF at 11 V and must not exceed 50 µF with the default BST_K1 and BST_K2 coefficients. Refer to Table 4-8 in Section 4.6.3 for supported boost inductor and capacitor combinations with different BST_K1 and BST_K2 coefficient values.

5.1.2 Power Supply/Reference Decoupling

Decoupling capacitors are required on the CS40L25/B VA and VP power supply rails. Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges of the intended application. For most applications, the use of ceramic capacitors with X5R dielectric is recommended.

5.2 Hardware Generated Haptic Alerts at Power On

The CS40L25/B boot ROM and internal power-on reset circuit enable the device to generate simple haptic alerts at power on before firmware and waveform downloads from the applications processor. The capability to boot from ROM in Basic Haptics Mode and generate an alert requires the $\overline{\text{RESET}}$ pin to be driven high (or pulled up to VA), the reference clock to run when VA is enabled, and a hardware rising edge transition on the GPIO1 pin.

Basic Haptics Mode register defaults should be acceptable for many applications, but these may also be overridden by the host through the control port to adjust the alert duration and intensity. Table 4-6 describes the Basic Haptics Mode configuration parameters.Basic Haptics Mode does not require the register initialization sequence in Section 4.2.4.

5.3 PCB Layout Guidelines

This section provides general guidelines for PCB design to ensure the best performance of the CS40L25/B and minimize the potential for EMI/EMC issues in the end product. Refer to AN444, CS40L25/B Schematic and Layout Guidelines, for more information and PCB artwork examples when using the WLCSP package. The corresponding PCB layout information for the QFN package is provided in AN472, CS40L25B QFN Schematic & Layout Guidelines.

No particular PCB stackup or PCB fabrication technology is required for the CS40L25/B, although most designs using the WLCSP package will use a 6-layer or 8-layer PCB to achieve end product size and cost requirements. Using a 6- or 8-layer PCB provides the flexibility to use large traces and copper floods on the component side routing together with power and ground planes separating signal routing layers. Track routing from the QFN package is simpler than the WLCSP package allowing the use of a 4-layer PCB. A 2-layer PCB may even be designed for the QFN package if attention is paid to the power routing, but must be fully tested to understand any performance degradation due to compromises made in the PCB layout.

5.3.1 Boost Converter Placement and Routing Requirements

Boost converter component placement and routing must adhere to the following requirements:

- The boost inductor must be placed on the component side of the PCB with the CS40L25/B.

  - One side of the boost inductor must be routed on the same layer to the CS40L25/B SW pins (WLCSP balls A2 and B2, QFN pins 26 and 27).
  - The other side of the inductor must be routed on the same layer to the CS40L25/B VP pin (WLCSP ball A5, QFN pin 30). This route must be connected to the battery supply routing plane directly or using multiple parallel vias capable of handling up to 4.5 A (if the battery supply is on an inner layer plane connected to the outside layer route).
- The connection between the VBST output (WLCSP balls A1 and B1, QFN pins 19, 22, 23 and 24) and the VAMP input (WLCSP balls C1 and D1) must be made on the component layer (without being connected through any vias) and capable of handling currents of 2 A.
  - Note: On the QFN package, there are no external VAMP pins and the amplifier supply input is connected to the boost supply output inside the device.
  - All VBST balls/pins must be connected together on the PCB and connected to the capacitors shown in the Typical Connection diagrams.
- The capacitors on VBST must be close to the CS40L25/B and routed on the same layer.
  - Use a copper flood for the connection between the VBST pins (WLCSP balls A1, B1, C1 and D1, or QFN pins 19, 22, 23 and 24) to the VBST capacitors to minimize the parasitic inductance. Bring the copper flood as close to WLCSP balls A1 and B1 and QFN pins 22, 23 and 24 as the manufacturing process allows.
  - The other side of the VBST capacitors must have an excellent low impedance connection to ground.

5.3.2 Power Supply Placement and Routing Requirements

Power supply decoupling placement and routing requirements:

- Place the local supply decoupling caps on the same layer as the CS40L25/B as close to the device as possible.
- To minimize inductance effects, the low-value ceramic capacitor must be closest to the supply ball.
- Extensive use of power and ground planes, ground-plane fill in unused areas, and surface-mount decoupling capacitors are recommended.
- The VA and VP ball supply routes must be designed to handle currents of 20 mA each.
- All ground traces should connect to a common ground plane which should handle a current of 4.5 A.
- To avoid unwanted coupling into the modulator, all signals, especially clocks, must be isolated from the LDO_FILT+ pin.
- The LDO_FILT+ capacitor must be positioned to minimize the electrical path from the pin to GNDA.
- The QFN package includes a ground pad that must be connected to the ground plane with multiple vias. The ground pad provides thermal dissipation as well as ground connection.

5.3.3 Amplifier Output Placement and Routing Requirements

Amplifier output to LRA placement and routing requirements:

- The OUT± traces (WLCSP balls C2 and D2, QFN pins 20 and 21) must be routed differentially on a layer that is separated from the power supply circuits by a ground plane and must be > 25 mils wide and designed to handle currents of 2 A.
- EMI filtering at the amplifier output is optional, and may use a capacitor of 470 pF or less.
- VSNS± should be routed differentially away from the power circuits and connected as close to the LRA terminals as possible.
- Provide GND shielding around VSNS±.

Note: The CS40L25/B performs actuator current sensing using the integrated current-monitoring sense resistor. The measurement of ReDC relies on accurately capturing the current through the load. Additional components added in the actuator path may reduce the accuracy of the ReDC measurement.

6 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

Table 6-1. Block Base Addresses

Base Address	Block Name	Register Quick Reference	Register Description Reference
0x0000 0000	Software Reset and Hardware ID (SW_RESET)	Section 6.1	Section 7.1
0x0000 2000	Power, Global, and Release Control (MSM)	Section 6.2	Section 7.2
0x0000 2400	Digital I/O Pad Control (PAD_INTF)	Section 6.3	Section 7.3
0x0000 2900	Hibernation Power Management (PWRMGT)	Section 6.4	Section 7.4
0x0000 2C00	Device Clocking and Sample Rate Control (CCM)	Section 6.5	Section 7.5
0x0000 3800	Digital Boost Converter (BOOST)	Section 6.6	Section 7.6
0x0000 4000	VMON and IMON Signal Monitoring (VIMON)	Section 6.7	Section 7.7
0x0000 4200	Die Temperature Monitoring (TEMPMON)	Section 6.8	Section 7.8
0x0000 4800	ASP Data Interface (DATAIF)	Section 6.9	Section 7.9
0x0000 4C00	Data Routing (MIXER)	Section 6.10	Section 7.10
0x0000 6000	Amplifier Volume Control (INTP)	Section 6.11	Section 7.11
0x0000 6400	VP and VBST Brownout Prevention + Temp Warning (ERROR_ VOLUME)	Section 6.12	Section 7.12
0x0000 6800	Power Management - Class H, Weak-FET, and Noise Gating (PWRMGMT)	Section 6.13	Section 7.13
0x0000 6C00	Dynamic Range Enhancement (DRE)	Section 6.14	Section 7.14
0x0001 0000	Interrupt Status and Mask Control (IRQ1)	Section 6.15	Section 7.15
0x0001 0800	Interrupt Status and Mask Control (IRQ2)	Section 6.16	Section 7.16
0x0001 1000	GPIO Control (GPIO)	Section 6.17	Section 7.17
0x0001 3000	DSP scratch space (DSP_MBOX)	Section 6.18	Section 7.18
0x0001 3020	DSP virtual 1 scratch space (DSP_VIRTUAL1_MBOX)	Section 6.19	Section 7.19
0x0001 3040	DSP virtual 2 scratch space (DSP_VIRTUAL2_MBOX)	Section 6.20	Section 7.20
0x0001 4000	Clock Presence Detect (CLOCK_DETECT)	Section 6.21	Section 7.21

6.1 Software Reset and Hardware ID (SW_RESET)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0000	DEVID	—								DEVID[23:16]							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
p. 77		DEVID[15:0]															
		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0
0x0000 0004	REVID	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
p. 77		—								AREVID				MTLREVID			
		0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
0x0000 000C	RELID	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
p. 77		—								RELID							
		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0010	OTPID	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—												OTPID			
p. 77		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0020	SFT_RESET	SFT_RESET								—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
p. 78		0	0	0	0	0	0	0	0	—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.2 Power, Global, and Release Control (MSM)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2014	GLOBAL_ ENABLES	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															GLOBAL_ EN
p. 78		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2018	BLOCK_ ENABLES	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—		IMON_EN	VMON_ EN	—	TEMPMON_EN	VBSTMON_EN	VPMON_ EN	—		BST_EN		—			AMP_EN
p. 78		0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1
0x0000 201C	BLOCK_ ENABLES2	—							WKFET_ AMP_EN	—			AMP_ DRE_EN	—			
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
		—		VBBR_ EN	VPBR_ EN	—							CLASSH_ EN	—			
p. 79		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0x0000 2020	GLOBAL_ OVERRIDES	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—												TEMPMON_ GLOBAL_ OVR	—		BST_ GLOBAL_ OVR
p. 80		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0x0000 2034	ERROR_ RELEASE	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—									TEMP_ ERR_ RLS	TEMP_ WARN_ RLS	BST_ UVP_ ERR_ RLS	BST_ OVP_ ERR_ RLS	BST_ SHORT_ ERR_ RLS	AMP_ SHORT_ ERR_ RLS	—
p. 80		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.3 Digital I/O Pad Control (PAD_INTF)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2418	LRCK_PAD_ CONTROL	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—											GP4_ CTRL	—			
p. 82		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2420	SDIN_PAD_CONTROL	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—												GP3_CTRL	—		
p. 82		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0x0000 242C	GPIO_PAD_CONTROL	—					GP2_CTRL			—					GP1_CTRL		
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															
p. 82		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.4 Hibernation Power Management (PWRMGT)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2900	PWRMGT_CTL	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—														MEM_RDY	TRIG_HIBER
p. 83		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 2904	WAKESRC_CTL	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—							UPDT_WKCTL	WKSRC_EN				WKSRC_POL			
p. 83		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0x0000 2908	PWRMGT_STS	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—								WKSRC_STS				—		WR_PEND_STS	MEM_RDY_STS
p. 83		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.5 Device Clocking and Sample Rate Control (CCM)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2C04	REFCLK_INPUT	—															PLL_FORCE_EN
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—				PLL_OPEN_LOOP	PLL_REFCLK_FREQ						PLL_REFCLK_EN	—	PLL_REFCLK_SEL		
p. 84		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0x0000 2C0C	GLOBAL_SAMPLE_RATE	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—											GLOBAL_FS				
p. 85		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

6.6 Digital Boost Converter (BOOST)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3800	VBST_CTL_1	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—								BST_CTL							
p. 85		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3804	VBST_CTL_2	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—													BST_CTL_LIM_EN	BST_CTL_SEL	
p. 85		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0000 3808	BST_IPK_CTL	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—									BST_IPK						
p. 86		0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0
0x0000 380C	SOFT_RAMP	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—												BST_SFT_RAMP			
p. 86		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0x0000 3810	BST_LOOP_COEFF	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		BST_K2								BST_K1							
p. 86		0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0
0x0000 3814	LBST_SLOPE	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		BST_SLOPE								—						BST_LBST_VAL	
p. 87		0	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0
0x0000 3818	BST_SW_FREQ	BST_DCM_FREQ_MIN								—						BST_DCM_FREQ[9:8]	
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
		BST_DCM_FREQ[7:0]								—				BST_CCM_FREQ			
p. 87		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 381C	BST_DCM_CTL	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—								BST_DCM_EXIT_SEL		BST_DCM_ENTRY_SEL		—			BST_DCM_EN
p. 88		0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1
0x0000 3820	DCM_FORCE	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—														BST_DCM_FRC_EN	BST_DCM_FRC
p. 88		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 3830	VBST_OVP	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—							BST_OVP_EN	—		BST_OVP_THLD					
p. 89		0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0

6.7 VMON and IMON Signal Monitoring (VIMON)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 4008	MONITOR_FILT	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															MON_FILT_RESP
p. 89		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.8 Die Temperature Monitoring (TEMPMON)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 4220	WARN_LIMIT_THRESHOLD	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—														TEMP_WARN_THLD	
p. 89		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0x0000 4224	CONFIGURATION	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—												TEMP_OUT_SEL	TEMP_WARN_ERR_SEL	TEMP_FILT_SEL	
p. 90		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 4308	ENABLES_AND_CODES_DIG	—							TEMP_RESULT_FILT								
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—							TEMP_RESULT_UNFILT								
p. 90		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.9 ASP Data Interface (DATAIF)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 4800	ASP_ENABLES1	—														ASP_RX2_EN	ASP_RX1_EN
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															
p. 91		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 4804	ASP_CONTROL1	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—										ASP_BCLK_FREQ					
p. 91		0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
0x0000 4808	ASP_CONTROL2	ASP_RX_WIDTH								—							
		0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0
		—					ASP_FMT			—	ASP_BCLK_INV	ASP_BCLK_FRC	ASP_BCLK_MSTR	—	ASP_FSYNC_INV	ASP_FSYNC_FRC	ASP_FSYNC_MSTR
p. 91		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0x0000 4820	ASP_FRAME_CONTROL5	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—		ASP_RX2_SLOT						—		ASP_RX1_SLOT					
p. 92		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0x0000 4840	ASP_DATA_CONTROL5	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—										ASP_RX_WL					
p. 93		0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

6.10 Data Routing (MIXER)

Address	Register	31 ... 8	7	6	5	4	3	2	1	0
0x0000 4C00	DACPCM1_INPUT	—	—	DACPCM1_SRC						
p. 93		0x0000 00	0	0	0	0	1	0	0	0
0x0000 4C40	DSP1RX1_INPUT	—	—	DSP1RX1_SRC						
p. 93		0x0000 00	0	0	0	0	1	0	0	0
0x0000 4C44	DSP1RX2_INPUT	—	—	DSP1RX2_SRC						
p. 94		0x0000 00	0	0	0	0	1	0	0	1

Address	Register	31 ... 8	7	6	5	4	3	2	1	0
0x0000 4C48	DSP1RX3_	—	—				DSP1RX3_SRC			
p. 94	INPUT	0x0000 00	0	0	0	1	1	0	0	0
0x0000 4C4C	DSP1RX4_	—	—				DSP1RX4_SRC			
p. 94	INPUT	0x0000 00	0	0	0	1	1	0	0	1
0x0000 4C50	DSP1RX5_	—	—				DSP1RX5_SRC			
p. 95	INPUT	0x0000 00	0	0	1	0	0	0	0	0
0x0000 4C54	DSP1RX6_	—	—				DSP1RX6_SRC			
p. 95	INPUT	0x0000 00	0	0	1	0	0	0	0	1
0x0000 4C58	DSP1RX7_	—	—				DSP1RX7_SRC			
p. 95	INPUT	0x0000 00	0	0	1	1	1	0	1	0
0x0000 4C5C	DSP1RX8_	—	—				DSP1RX8_SRC			
p. 96	INPUT	0x0000 00	0	0	1	1	1	0	1	1
0x0000 4C60	NGATE1_	—	—				NGATE1_SRC			
p. 96	INPUT	0x0000 00	0	0	0	0	1	0	0	0
0x0000 4C64	NGATE2_	—	—				NGATE2_SRC			
p. 96	INPUT	0x0000 00	0	0	0	0	1	0	0	1

6.11 Amplifier Volume Control (INTP)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 6000	AMP_CTRL									—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		AMP_HPF_PCM_EN	AMP_INV_PCM	AMP_VOL_PCM											AMP_RAMP_PCM		
p. 97		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.12 VP and VBST Brownout Prevention + Temp Warning (ERROR_VOLUME)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 6404	VPBR_CONFIG			—			VPBR_REL_TRIG	VPBR_REL_AUTO	VPBR_MUTE_EN	VPBR_REL_RATE			VPBR_WAIT		VPBR_ATK_RATE		
		0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0
		VPBR_ATK_VOL				VPBR_MAX_ATT				—			VPBR_THLD1				
p. 97		0	0	0	1	1	0	0	1	0	0	0	0	0	1	0	1
0x0000 6408	VBBR_CONFIG			—			VBBR_REL_TRIG	VBBR_REL_AUTO	VBBR_MUTE_EN	VBBR_REL_RATE			VBBR_WAIT		VBBR_ATK_RATE		
		0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0
		VBBR_ATK_VOL				VBBR_MAX_ATT				—			VBBR_THLD1				
p. 99		0	0	0	1	1	0	0	1	0	0	0	0	0	1	0	1
0x0000 640C	VPBR_STATUS									—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
					—				VPBR_STATUS_MUTE	VPBR_STATUS							
p. 100		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 6410	VBBR_STATUS									—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
					—				VBBR_STATUS_MUTE	VBBR_STATUS							
p. 100		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 6414	OTW_CONFIG	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—													TEMP_WARN_VOL		
p. 100		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0000 6418	AMP_ERROR_VOL_SEL	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															AMP_ERR_VOL_SEL
p. 101		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 6450	VOL_STATUS_TO_DSP	—														FINAL_ERROR_VOL[8:7]	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		FINAL_ERROR_VOL[6:0]							—								
p. 101		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.13 Power Management - Class H, Weak-FET, and Noise Gating (PWRMGMT)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 6800	CLASSH_CONFIG	—									CH_HD_RM						
		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
		CH_REL_RATE								—					CH_MEM_DEPTH		
p. 101		0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
0x0000 6804	WKFET_AMP_CONFIG	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—				WKFET_AMP_THLD				—			WKFET_AMP_DLY			WKFET_AMP_FRC_EN	WKFET_AMP_FRC
p. 102		0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1
0x0000 6808	NG_CONFIG	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—		NG_EN_SEL						—	NG_DELAY			—	NG_PCM_THLD		
p. 102		0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1

6.14 Dynamic Range Enhancement (DRE)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 6C04	AMP_GAIN	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—					AMP_GAIN_ZC	AMP_GAIN_PCM							—		
p. 103		0	0	0	0	0	0	1	0	0	1	1	1	0	0	1	1

6.15 Interrupt Status and Mask Control (IRQ1)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 0000	IRQ1_CFG	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—												IRQ1_DB_TIME			
p. 103		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 0004	IRQ1_STATUS	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															IRQ1_STS1
p. 103		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0010	IRQ1_EINT_1	AMP_ERR_EINT1	VBBR_ATT_CLR_EINT1	VBBR_FLAG_EINT1	IMON_CLIPPED_EINT1	VMON_CLIPPED_EINT1	VBSTMON_CLIPPED_EINT1	VPMON_CLIPPED_EINT1	MSM_PUP_DONE_EINT1	MSM_PDN_DONE_EINT1	MSM_GLOBAL_EN_ASSERT_EINT1	—				TEMP_ERR_EINT1	TEMP_WARN_FALL_EINT1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		TEMP_WARN_RISE_EINT1	VPBR_ATT_CLR_EINT1	—	VPBR_FLAG_EINT1	REFCLK_STOP_EINT1	REFCLK_START_EINT1	BST_IPK_FLAG_EINT1	BST_SHORT_ERR_EINT1	BST_DCM_UVP_ERR_EINT1	BST_OVP_ERR_EINT1	BST_OVP_FLAG_FALL_EINT1	BST_OVP_FLAG_RISE_EINT1	GPIO2_FALL_EINT1	GPIO2_RISE_EINT1	GPIO1_FALL_EINT1	GPIO1_RISE_EINT1
p. 104		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0014	IRQ1_EINT_2	—		AMP_NG_ON_FALL_EINT1	AMP_NG_ON_RISE_EINT1	—						DSP_VIRTUAL2_MBOX_WR_EINT1	DSP_VIRTUAL1_MBOX_WR_EINT1	—			
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															
p. 105		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0018	IRQ1_EINT_3	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—					ASP_RXSLOT_CFG_ERR_EINT1	ASP_TXSLOT_CFG_ERR_EINT1	REFCLK_IN_FLAG_FALL_EINT1	REFCLK_IN_FLAG_RISE_EINT1	—	PLL_UNLOCK_FLAG_FALL_EINT1	PLL_UNLOCK_FLAG_RISE_EINT1	PLL_FREQ_LOCK_EINT1	PLL_PHASE_LOCK_EINT1	PLL_LOCK_EINT1	INTP_VC_DONE_EINT1
p. 106		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 001C	IRQ1_EINT_4	—	GPIO4_FALL_EINT1	GPIO4_RISE_EINT1	GPIO3_FALL_EINT1	GPIO3_RISE_EINT1	—			MEM_RD_EINT1	—						
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															
p. 106		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0090	IRQ1_STS_1	AMP_ERR_STS1	VBBR_ATT_CLR_STS1	VBBR_FLAG_STS1	IMON_CLIPPED_STS1	VMON_CLIPPED_STS1	VBSTMON_CLIPPED_STS1	VPMON_CLIPPED_STS1	MSM_PUP_DONE_STS1	MSM_PDN_DONE_STS1	MSM_GLOBAL_EN_ASSERT_STS1	—				TEMP_ERR_STS1	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		TEMP_WARN_STS1	VPBR_ATT_CLR_STS1	—	VPBR_FLAG_STS1	REFCLK_STOP_STS1	REFCLK_START_STS1	BST_IPK_FLAG_STS1	BST_SHORT_ERR_STS1	BST_DCM_UVP_ERR_STS1	BST_OVP_ERR_STS1	—	BST_OVP_FLAG_STS1	—	GPIO2_STS1	—	GPIO1_STS1
p. 107		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0094	IRQ1_STS_2	—			AMP_NG_ON_STS1						—						
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															
p. 108		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 0098	IRQ1_STS_3	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—					ASP_RXSLOT_CFG_ERR_STS1	—		REFCLK_IN_FLAG_STS1	—		PLL_UNLOCK_FLAG_STS1	PLL_FREQ_LOCK_STS1	PLL_PHASE_LOCK_STS1	PLL_LOCK_STS1	INTP_VC_DONE_STS1
p. 108		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 009C	IRQ1_STS_4	—		GPIO4_STS1	—	GPIO3_STS1		—		MEM_RD_STS1				—			
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
p. 109		—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0110	IRQ1_MASK_1	AMP_ERR_MASK1	VBBR_ATT_CLR_MASK1	VBBR_FLAG_MASK1	IMON_CLIPPED_MASK1	VMON_CLIPPED_MASK1	VBSTMON_CLIPPED_MASK1	VPMON_CLIPPED_MASK1	MSM_PUP_DONE_MASK1	MSM_PDN_DONE_MASK1	MSM_GLOBAL_EN_ASSERT_MASK1	—				TEMP_ERR_MASK1	TEMP_WARN_FALL_MASK1
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		TEMP_WARN_RISE_MASK1	VPBR_ATT_CLR_MASK1	—	VPBR_FLAG_MASK1	REFCLK_STOP_MASK1	REFCLK_START_MASK1	BST_IPK_FLAG_MASK1	BST_SHORT_ERR_MASK1	BST_DCM_UVP_ERR_MASK1	BST_OVP_ERR_MASK1	BST_OVP_FLAG_FALL_MASK1	BST_OVP_FLAG_RISE_MASK1	GPIO2_FALL_MASK1	GPIO2_RISE_MASK1	GPIO1_FALL_MASK1	GPIO1_RISE_MASK1
p. 109		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x0001 0114	IRQ1_MASK_2	—		AMP_NG_ON_FALL_MASK1	AMP_NG_ON_RISE_MASK1	—											
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
p. 111		—															
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x0001 0118	IRQ1_MASK_3	—															
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		—					ASP_RXSLOT_CFG_ERR_MASK1	—	REFCLK_IN_FLAG_FALL_MASK1	REFCLK_IN_FLAG_RISE_MASK1	—	PLL_UNLOCK_FLAG_FALL_MASK1	PLL_UNLOCK_FLAG_RISE_MASK1	PLL_FREQ_LOCK_MASK1	PLL_PHASE_LOCK_MASK1	PLL_LOCK_MASK1	INTP_VC_DONE_MASK1
p. 111		1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
0x0001 011C	IRQ1_MASK_4	—	GPIO4_FALL_MASK1	GPIO4_RISE_MASK1	GPIO3_FALL_MASK1	GPIO3_RISE_MASK1		—		MEM_RD_MASK1				—			
		1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
p. 112		—															
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x0001 0210	IRQ1_EDGE_1	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—												GPIO2_FALL_EDGE1	GPIO2_RISE_EDGE1	GPIO1_FALL_EDGE1	GPIO1_RISE_EDGE1
p. 113		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
0x0001 021C	IRQ1_EDGE_4	—	GPIO4_FALL_EDGE1	GPIO4_RISE_EDGE1	GPIO3_FALL_EDGE1	GPIO3_RISE_EDGE1						—					
		0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0
p. 113		—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 0290	IRQ1_POL_1									—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
										—				GPIO2_FALL_POL1	GPIO2_RISE_POL1	GPIO1_FALL_POL1	GPIO1_RISE_POL1
p. 114		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 029C	IRQ1_POL_4	—	GPIO4_FALL_POL1	GPIO4_RISE_POL1	GPIO3_FALL_POL1	GPIO3_RISE_POL1						—					
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
										—							
p. 114		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0318	IRQ1_DB_3									—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
						—				REFCLK_IN_FLAG_DB1			—				
p. 115		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.16 Interrupt Status and Mask Control (IRQ2)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 0800	IRQ2_CFG									—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
										—				IRQ2_DB_TIME			
p. 115		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0804	IRQ2_STATUS									—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
										—							IRQ2_STS2
p. 115		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0810	IRQ2_EINT_1	AMP_ERR_EINT2	VBBR_ATT_CLR_EINT2	VBBR_FLAG_EINT2	IMON_CLIPPED_EINT2	VMON_CLIPPED_EINT2	VBSTMON_CLIPPED_EINT2	VPMON_CLIPPED_EINT2	MSM_PUP_DONE_EINT2	MSM_PDN_DONE_EINT2	MSM_GLOBAL_EN_ASSERT_EINT2	—				TEMP_ERR_EINT2	TEMP_WARN_FALL_EINT2
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		TEMP_WARN_RISE_EINT2	VPBR_ATT_CLR_EINT2	—	VPBR_FLAG_EINT2	REFCLK_STOP_EINT2	REFCLK_START_EINT2	BST_IPK_FLAG_EINT2	BST_SHORT_ERR_EINT2	BST_DCM_UVP_ERR_EINT2	BST_OVP_ERR_EINT2	BST_OVP_FLAG_FALL_EINT2	BST_OVP_FLAG_RISE_EINT2	GPIO2_FALL_EINT2	GPIO2_RISE_EINT2	GPIO1_FALL_EINT2	GPIO1_RISE_EINT2
p. 116		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0814	IRQ2_EINT_2	—		AMP_NG_ON_FALL_EINT2	AMP_NG_ON_RISE_EINT2					—		DSP_VIRTUAL2_MBOX_WR_EINT2	DSP_VIRTUAL1_MBOX_WR_EINT2				
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
										—							
p. 117		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 0818	IRQ2_EINT_3	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—					ASP_RXSLOT_CFG_ERR_EINT2	—	REFCLK_IN_FLAG_FALL_EINT2	REFCLK_IN_FLAG_RISE_EINT2	—	PLL_UNLOCK_FLAG_FALL_EINT2	PLL_UNLOCK_FLAG_RISE_EINT2	PLL_FREQ_LOCK_EINT2	PLL_PHASE_LOCK_EINT2	PLL_LOCK_EINT2	INTP_VC_DONE_EINT2
p. 118		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 081C	IRQ2_EINT_4	—	GPIO4_FALL_EINT2	GPIO4_RISE_EINT2	GPIO3_FALL_EINT2	GPIO3_RISE_EINT2		—		MEM_RD_EINT2				—			
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															
p. 118		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0890	IRQ2_STS_1	AMP_ERR_STS2	VBBR_ATT_CLR_STS2	VBBR_FLAG_STS2	IMON_CLIPPED_STS2	VMON_CLIPPED_STS2	VBSTMON_CLIPPED_STS2	VPMON_CLIPPED_STS2	MSM_PUP_DONE_STS2	MSM_PDN_DONE_STS2	MSM_GLOBAL_EN_ASSERT_STS2	—				TEMP_ERR_STS2	—
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		TEMP_WARN_STS2	VPBR_ATT_CLR_STS2	—	VPBR_FLAG_STS2	REFCLK_STOP_STS2	REFCLK_START_STS2	BST_IPK_FLAG_STS2	BST_SHORT_ERR_STS2	BST_DCM_UVP_ERR_STS2	BST_OVP_ERR_STS2	—	BST_OVP_FLAG_STS2	—	GPIO2_STS2	—	GPIO1_STS2
p. 119		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0894	IRQ2_STS_2	—			AMP_NG_ON_STS2							—					
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															
p. 120		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0898	IRQ2_STS_3	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—					ASP_RXSLOT_CFG_ERR_STS2	ASP_TXSLOT_CFG_ERR_STS2	—	REFCLK_IN_FLAG_STS2	—		PLL_UNLOCK_FLAG_STS2	PLL_FREQ_LOCK_STS2	PLL_PHASE_LOCK_STS2	PLL_LOCK_STS2	INTP_VC_DONE_STS2
p. 120		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 089C	IRQ2_STS_4	—		GPIO4_STS2	—	GPIO3_STS2		—		MEM_RD_STS2				—			
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—															
p. 121		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0910	IRQ2_MASK_1	AMP_ERR_MASK2	VBBR_ATT_CLR_MASK2	VBBR_FLAG_MASK2	IMON_CLIPPED_MASK2	VMON_CLIPPED_MASK2	VBSTMON_CLIPPED_MASK2	VPMON_CLIPPED_MASK2	MSM_PUP_DONE_MASK2	MSM_PDN_DONE_MASK2	MSM_GLOBAL_EN_ASSERT_MASK2	—				TEMP_ERR_MASK2	TEMP_WARN_FALL_MASK2
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
		TEMP_WARN_RISE_MASK2	VPBR_ATT_CLR_MASK2	—	VPBR_FLAG_MASK2	REFCLK_STOP_MASK2	REFCLK_START_MASK2	BST_IPK_FLAG_MASK2	BST_SHORT_ERR_MASK2	BST_DCM_UVP_ERR_MASK2	BST_OVP_ERR_MASK2	BST_OVP_FLAG_FALL_MASK2	BST_OVP_FLAG_RISE_MASK2	GPIO2_FALL_MASK2	GPIO2_RISE_MASK2	GPIO1_FALL_MASK2	GPIO1_RISE_MASK2
p. 121		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 0914	IRQ2_MASK_2	—		AMP_NG_ON_FALL_MASK2	AMP_NG_ON_RISE_MASK2				—			DSP_VIRTUAL2_MBOX_WR_MASK2	DSP_VIRTUAL1_MBOX_WR_MASK2			—	
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
p. 123		1	1	1	1	1	1	1	1	— 1	1	1	1	1	1	1	1
0x0001 0918	IRQ2_MASK_3	1	1	1	1	1	1	1	1	— 1	1	1	1	1	1	1	1
		—					ASP_RXSLOT_CFG_ERR_MASK2	ASP_TXSLOT_CFG_ERR_MASK2	REFCLK_IN_FLAG_FALL_MASK2	REFCLK_IN_FLAG_RISE_MASK2	—	PLL_UNLOCK_FLAG_FALL_MASK2	PLL_UNLOCK_FLAG_RISE_MASK2	PLL_FREQ_LOCK_MASK2	PLL_PHASE_LOCK_MASK2	PLL_LOCK_MASK2	INTP_VC_DONE_MASK2
p. 123		1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
0x0001 091C	IRQ2_MASK_4	—	GPIO4_FALL_MASK2	GPIO4_RISE_MASK2	GPIO3_FALL_MASK2	GPIO3_RISE_MASK2		—		MEM_RD_MASK2				—			
		1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
p. 124		1	1	1	1	1	1	1	1	— 1	1	1	1	1	1	1	1
0x0001 0A10	IRQ2_EDGE_1	0	0	0	0	0	0	0	0	— 0	0	0	0	0	0	0	0
		—												GPIO2_FALL_EDGE2	GPIO2_RISE_EDGE2	GPIO1_FALL_EDGE2	GPIO1_RISE_EDGE2
p. 125		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
0x0001 0A1C	IRQ2_EDGE_4	—	GPIO4_FALL_EDGE2	GPIO4_RISE_EDGE2	GPIO3_FALL_EDGE2	GPIO3_RISE_EDGE2						—					
		0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0
p. 125		0	0	0	0	0	0	0	0	— 0	0	0	0	0	0	0	0
0x0001 0A90	IRQ2_POL_1	0	0	0	0	0	0	0	0	— 0	0	0	0	0	0	0	0
		—												GPIO2_FALL_POL2	GPIO2_RISE_POL2	GPIO1_FALL_POL2	GPIO1_RISE_POL2
p. 126		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 0A9C	IRQ2_POL_4	—	GPIO4_FALL_POL2	GPIO4_RISE_POL2	GPIO3_FALL_POL2	GPIO3_RISE_POL2						—					
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
p. 126		0	0	0	0	0	0	0	0	— 0	0	0	0	0	0	0	0
0x0001 0B18	IRQ2_DB_3	0	0	0	0	0	0	0	0	— 0	0	0	0	0	0	0	0
		—								REFCLK_IN_FLAG_DB2				—			
p. 127		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.17 GPIO Control (GPIO)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 1000	GPIO_ STATUS1									—							
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
								—						GP4_STS	GP3_STS	GP2_STS	GP1_STS
p. 127		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 1008	GPIO1_CTRL1	GP1_DIR						—							GP1_DBTIME		
		1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
		GP1_LVL	—	GP1_DB	GP1_POL							—					
p. 127		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0001 100C	GPIO2_CTRL1	GP2_DIR						—							GP2_DBTIME		
		1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
		GP2_LVL	—	GP2_DB	GP2_POL							—					
p. 128		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0001 1010	GPIO3_CTRL1	GP3_DIR						—							GP3_DBTIME		
		1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
		GP3_LVL	—	GP3_DB	GP3_POL							—					
p. 129		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0001 1014	GPIO4_CTRL1	GP4_DIR						—							GP4_DBTIME		
		1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
		GP4_LVL	—	GP4_DB	GP4_POL							—					
p. 129		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

6.18 DSP scratch space (DSP_MBOX)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 3000	DSP_MBOX_1	DSP_MBOX_1[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_MBOX_1[15:0]															
p. 130		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3004	DSP_MBOX_2	DSP_MBOX_2[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_MBOX_2[15:0]															
p. 130		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3008	DSP_MBOX_3	DSP_MBOX_3[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_MBOX_3[15:0]															
p. 130		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 300C	DSP_MBOX_4	DSP_MBOX_4[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_MBOX_4[15:0]															
p. 131		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3010	DSP_MBOX_5	DSP_MBOX_5[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_MBOX_5[15:0]															
p. 131		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3014	DSP_MBOX_6	DSP_MBOX_6[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_MBOX_6[15:0]															
p. 131		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3018	DSP_MBOX_7	DSP_MBOX_7[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_MBOX_7[15:0]															
p. 131		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 301C	DSP_MBOX_8	DSP_MBOX_8[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_MBOX_8[15:0]															
p. 131		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.19 DSP virtual 1 scratch space (DSP_VIRTUAL1_MBOX)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 3020	DSP_ VIRTUAL1_ MBOX_1	DSP_VIRTUAL1_MBOX_1[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL1_MBOX_1[15:0]															
p. 131		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3024	DSP_ VIRTUAL1_ MBOX_2	DSP_VIRTUAL1_MBOX_2[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL1_MBOX_2[15:0]															
p. 132		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3028	DSP_ VIRTUAL1_ MBOX_3	DSP_VIRTUAL1_MBOX_3[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL1_MBOX_3[15:0]															
p. 132		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 302C	DSP_ VIRTUAL1_ MBOX_4	DSP_VIRTUAL1_MBOX_4[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL1_MBOX_4[15:0]															
p. 132		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3030	DSP_ VIRTUAL1_ MBOX_5	DSP_VIRTUAL1_MBOX_5[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL1_MBOX_5[15:0]															
p. 132		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3034	DSP_ VIRTUAL1_ MBOX_6	DSP_VIRTUAL1_MBOX_6[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL1_MBOX_6[15:0]															
p. 132		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3038	DSP_ VIRTUAL1_ MBOX_7	DSP_VIRTUAL1_MBOX_7[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL1_MBOX_7[15:0]															
p. 132		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 303C	DSP_ VIRTUAL1_ MBOX_8	DSP_VIRTUAL1_MBOX_8[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL1_MBOX_8[15:0]															
p. 133		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.20 DSP virtual 2 scratch space (DSP_VIRTUAL2_MBOX)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 3040	DSP_ VIRTUAL2_ MBOX_1	DSP_VIRTUAL2_MBOX_1[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL2_MBOX_1[15:0]															
p. 133		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3044	DSP_ VIRTUAL2_ MBOX_2	DSP_VIRTUAL2_MBOX_2[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL2_MBOX_2[15:0]															
p. 133		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 3048	DSP_ VIRTUAL2_ MBOX_3	DSP_VIRTUAL2_MBOX_3[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL2_MBOX_3[15:0]															
p. 133		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 304C	DSP_ VIRTUAL2_ MBOX_4	DSP_VIRTUAL2_MBOX_4[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL2_MBOX_4[15:0]															
p. 133		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3050	DSP_ VIRTUAL2_ MBOX_5	DSP_VIRTUAL2_MBOX_5[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL2_MBOX_5[15:0]															
p. 133		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3054	DSP_ VIRTUAL2_ MBOX_6	DSP_VIRTUAL2_MBOX_6[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL2_MBOX_6[15:0]															
p. 134		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 3058	DSP_ VIRTUAL2_ MBOX_7	DSP_VIRTUAL2_MBOX_7[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL2_MBOX_7[15:0]															
p. 134		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0001 305C	DSP_ VIRTUAL2_ MBOX_8	DSP_VIRTUAL2_MBOX_8[31:16]															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		DSP_VIRTUAL2_MBOX_8[15:0]															
p. 134		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.21 Clock Presence Detect (CLOCK_DETECT)

Address	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001 4000	CLOCK_ DETECT_1	—															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		—										CLK_DET_FREQ		—			CLK_ DET_EN
p. 134		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7 Register Descriptions

This section describes each of the control port registers.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

7.1 Software Reset and Hardware ID (SW_RESET)

7.1.1 DEVID

Address: 0x0000 0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	—								DEVID																							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0

Bits	Name	Description
31:24	—	Reserved
23:0	DEVID	A value of 0x40A25A indicates a CS40L25 device. A value of 0x40A25B indicates a CS40L25B device.

7.1.2 REVID

Address: 0x0000 0004

	31...8	7	6	5	4	3	2	1	0
RO	—	AREVID				MTLREVID			
Default	0x00 0000	X	X	X	X	X	X	X	X

Bits	Name	Description
31:8	—	Reserved
7:4	AREVID	Alpha revision. Device alpha revision level. AREVID and MTLREVID from the complete device revision ID (e.g., A0, B2).
3:0	MTLREVID	Metal revision. Device metal revision level. AREVID and MTLREVID from the complete device revision ID (e.g., A0, B2).

7.1.3 RELID

Address: 0x0000 000C

	31...8	7	6	5	4	3	2	1	0
RO	—	RELID							
Default	0x00 0000	0	0	0	1	0	0	0	0

Bits	Name	Description
31:8	—	Reserved
7:0	RELID	Software Device revision. (incremented if software driver compatibility or software feature support is changed)

7.1.4 OTPID

Address: 0x0000 0010

	31...8	7	6	5	4	3	2	1	0
RO	—	—				OTPID			
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:4	—	Reserved
3:0	OTPID	OTP revision and additional device ID. A unique code for additional qualification of device ID and the OTP revision programmed into the device. OTPID of 0x0 is Reserved.

7.1.5 SFT_RESET

Address: 0x0000 0020

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	SFT_RESET								—																							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:24	SFT_RESET	Software Reset Write Only Register. Writing to this register resets all registers to their default state. Reading from this register will indicate 00000000. **Note:** Writing 0x5A00_0000 to this register triggers a soft reset.
23:0	—	Reserved

7.2 Power, Global, and Release Control (MSM)

7.2.1 GLOBAL_ENABLES

Address: 0x0000 2014

	31...8	7	6	5	4	3	2	1	0
RW	—	—							GLOBAL_EN
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:1	—	Reserved
0	GLOBAL_EN	Global device enable. Enables and disables all functionality of the device. When GLOBAL_EN = 0, it is equivalent to disabling all of the sub-blocks and their associated circuitry. When GLOBAL_EN = 1, if all of the subblocks are enabled (x_EN = 1), the entire device will power up. Individual sub-blocks may be disabled using their respective enable control bits. If a functional block contains a global override (x_GLOBAL_OVR), setting the x_GLOBAL_OVR = 1 allows that block to remain enabled when GLOBAL_EN = 0. This permits various low power and fast power up modes of operation. 0 = (Default) Device is disabled and put into a power down state (unless one or more x_GLOBAL_OVR is set) 1 = Device is enabled

7.2.2 BLOCK_ENABLES

Address: 0x0000 2018

	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—	—		IMON_EN	VMON_EN	—	TEMPMON_EN	VBSTMON_EN	VPMON_EN	—		BST_EN		—			AMP_EN
Default	0x0000	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1

Bits	Name	Description
31:14	—	Reserved
13	IMON_EN	IMON actuator current monitoring enable. Configures whether the IMON actuator current monitoring is disabled or enabled. 0 = IMON monitoring disabled 1 = (Default) IMON monitoring enabled
12	VMON_EN	VMON actuator voltage monitoring enable. Configures whether the VMON actuator voltage monitoring is disabled or enabled. 0 = VMON monitoring disabled 1 = (Default) VMON monitoring enabled
11	—	Reserved
10	TEMPMON_EN	TEMPMON chip temperature monitoring enable. Configures whether the TEMPMON chip temperature monitoring is enabled. 0 = (Default) TEMPMON monitoring disabled 1 = TEMPMON monitoring enabled
9	VBSTMON_EN	VBSTMON supply voltage monitoring enable. Configures whether the VBSTMON supply monitoring is enabled. Other subblocks that require the VBSTMON (e.g. boost converter) can automatically enable the VBSTMON ADC even when VBSTMON_EN = 0. 0 = VBSTMON monitoring disabled (if no other block is requesting VBSTMON to be enabled) 1 = (Default) VBSTMON monitoring enabled

Bits	Name	Description
8	VPMON_EN	VPMON supply voltage monitoring enable. Configures whether the VPMON supply monitoring is enabled. Other subblocks that require the VPMON (e.g. boost converter) can automatically enable the VPMON ADC even when VPMON_EN = 0. 0 = VPMON monitoring disabled (if no other block requesting VPMON to be enabled) 1 = (Default) VPMON monitoring enabled
7:6	—	Reserved
5:4	BST_EN	Digital boost converter enable/disable control. Configures the power state of the boost converter and bypass FET. When GLOBAL_EN=0 and BST_GLOBAL_OVR = 0, the boost converter's bypass FET is off. 00 = Boost converter disabled with bypass FET off (VBST = VP – diode drop) 01 = Boost converter disabled with bypass FET on (VBST = VP) 10 = (Default) Boost converter enabled 11 = Reserved (Boost converter enabled)
3:1	—	Reserved
0	AMP_EN	Class D amplifier enable/disable control. Configures the operational power state of the Class D amplifier and most of the amplifier's signal path (channel select, diagnostic signal generator, digital gain, modulator, and output stage). 0 = Amplifier functionality disabled 1 = (Default) Amplifier functionality enabled

7.2.3 BLOCK_ENABLES2

Address: 0x0000 201C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—							WKFET_AMP_EN	—			AMP_DRE_EN	—			
Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—		VBBR_EN	VPBR_EN	—							CLASSH_EN	—			
Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Name	Description
31:25	—	Reserved
24	WKFET_AMP_EN	Amplifier weak-FET automatic tracking enable. Configures whether the weak-FET signal based tracking and automatic management for the amplifier's switching outputs is enabled or disabled. 0 = Amplifier weak-FET tracking disabled 1 = (Default) Amplifier weak-FET tracking enabled
23:21	—	Reserved
20	AMP_DRE_EN	Amplifier dynamic range enhancement enable. Configures whether the dynamic range enhancement is enabled and automatically managing the analog gain of the amplifier in order to reduce the noise floor of the amplifier. 0 = (Default) DRE disabled 1 = DRE enabled
19:14	—	Reserved
13	VBBR_EN	VBST brownout prevention enable. Configures whether the VBST brownout prevention algorithm is enabled or disabled. 0 = (Default) VBST brownout prevention disabled 1 = VBST brownout prevention enabled
12	VPBR_EN	VP brownout prevention enable. Configures whether the VP brownout prevention algorithm is enabled or disabled. 0 = (Default) VP brownout prevention disabled 1 = VP brownout prevention enabled
11:5	—	Reserved
4	CLASSH_EN	Class H enable. Configures whether the Class H tracking is enabled or disabled (and the memory buffer bypassed). When the Class H is enabled, the BST_CTL_SEL must be configured to use the Class H target in order for VBST tracking to occur. 0 = Class H disabled 1 = (Default) Class H enabled
3:0	—	Reserved

7.2.4 GLOBAL_OVERRIDES

Address: 0x0000 2020

RW	31...8	7	6	5	4	3	2	1	0
	—	—				TEMPMON_GLOBAL_OVR	—		BST_GLOBAL_OVR
Default	0x00 0000	0	0	0	0	0	0	1	0

Bits	Name	Description
31:4	—	Reserved
3	TEMPMON_GLOBAL_OVR	TEMPMON global enable override. Setting TEMPMON_GLOBAL_OVR allows the TEMPMON to continue to function and remain in an operational state while GLOBAL_EN = 0. 0 = (Default) The TEMPMON is disabled when GLOBAL_EN = 0 1 = Assumes the configuration of TEMPMON_EN, regardless of the state of GLOBAL_EN
2:1	—	Reserved
0	BST_GLOBAL_OVR	Boost converter global enable override. Setting BST_GLOBAL_OVR allows the boost converter's enable control (BST_EN) to operate independently from the GLOBAL_EN control. This allows the boost converter to be powered up when GLOBAL_EN = 0 and the rest of the IC is disabled. 0 = (Default) The boost converter is disabled when GLOBAL_EN = 0 1 = The configuration of BST_EN is applied, regardless of the state of GLOBAL_EN

7.2.5 ERROR_RELEASE

Address: 0x0000 2034

RW	31...8	7	6	5	4	3	2	1	0
	—	—	TEMP_ERR_RLS	TEMP_WARN_RLS	BST_UVP_ERR_RLS	BST_OVP_ERR_RLS	BST_SHORT_ERR_RLS	AMP_SHORT_ERR_RLS	—
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:7	—	Reserved
6	TEMP_ERR_RLS	Overtemperature error protection release. Releases overtemperature error protection that places the device into Actuator-Safe Mode if the overtemperature error condition is no longer present. The present overtemperature error condition can be determined by reading the TEMP_ERR_STS1 bit twice. At the end of the protection release sequence (0 –> 1 –> 0), if the overtemperature error condition is no longer present, then the overtemperature error-caused Actuator-Safe Mode is cleared (the device may remain in Actuator-Safe Mode if another error is present). **Note:** For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the potential protection release sequence, then protection is not removed, the related interrupt status bit is set again and, if unmasked, a new interrupt is generated. 0 = (Default) Release0. After 0 –> 1 –> 0 sequence, if the overtemperature error condition is present, Actuator-Safe is applied 1 = Release1
5	TEMP_WARN_RLS	Overtemperature warning release. Releases overtemperature warning if the overtemperature warning condition is no longer present. The present overtemperature warning condition can be determined by reading the TEMP_WARN_STS1 bit twice. At the end of the warning release sequence (0 –> 1 –> 0), if the overtemperature warning condition is no longer present, then the overtemperature warning is cleared (the device may remain in Actuator-Safe Mode if another error is present). **Note:** For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the potential protection release sequence, then protection is not removed, the related interrupt status bit is set again and, if unmasked, a new interrupt is generated. 0 = (Default) Release0. After 0 –> 1 –> 0 sequence, if the overtemperature warning condition is present, the protection is not removed 1 = Release1

Bits	Name	Description
4	BST_UVP_ERR_RLS	Boost converter undervoltage error protection release. Releases boost converter undervoltage error protection that places the device into Actuator-Safe Mode if the boost converter undervoltage error condition is no longer present. The present boost converter undervoltage error condition can be determined by reading the BST_DCM_UVP_ERR_EINT1 bit twice. At the end of the protection release sequence (0 –> 1 –> 0), if the boost converter undervoltage error condition is no longer present, then the boost converter undervoltage error-caused Actuator-Safe Mode is cleared (the device may remain in Actuator-Safe Mode if another error is present). **Note:** For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the potential protection release sequence, then protection is not removed, the related interrupt status bit is set again and, if unmasked, a new interrupt is generated. 0 = (Default) Release0. After 0 –> 1 –> 0 sequence, if the undervoltage error condition is present, Actuator-Safe Mode is applied 1 = Release1
3	BST_OVP_ERR_RLS	Boost converter overvoltage error protection release. Releases boost converter overvoltage error protection that places the device into Actuator-Safe Mode if the boost converter overvoltage error condition is no longer present. The present boost converter overvoltage error condition can be determined by reading the BST_OVP_ERR_EINT1 bit twice. At the end of the protection release sequence (0 –> 1 –> 0), if the boost converter overvoltage error condition is no longer present, then the boost converter overvoltage error-caused Actuator-Safe Mode is cleared (the device may remain in Actuator-Safe Mode if another error is present). **Note:** For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the potential protection release sequence, then protection is not removed, the related interrupt status bit is set again and, if unmasked, a new interrupt is generated. 0 = (Default) Release0. After 0 –> 1 –> 0 sequence, if the overvoltage error condition is present, Actuator-Safe Mode is applied 1 = Release1
2	BST_SHORT_ERR_RLS	Boost converter inductor short error protection release. Releases boost converter inductor short error protection that places the device into Actuator-Safe Mode if the boost converter inductor short error condition is no longer present. The present boost converter inductor short error condition can be determined by reading the BST_SHORT_ERR_EINT1 bit twice. At the end of the protection release sequence (0 –> 1 –> 0), if the boost converter inductor short error condition is no longer present, then the boost converter inductor short error-caused Actuator-Safe Mode is cleared (the device may remain in Actuator-Safe Mode if another error is present). **Note:** For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the potential protection release sequence, then protection is not removed, the related interrupt status bit is set again and, if unmasked, a new interrupt is generated. 0 = (Default) Release0. After 0 –> 1 –> 0 sequence, if the inductor short error condition is present, Actuator-Safe Mode is applied 1 = Release1
1	AMP_SHORT_ERR_RLS	Amplifier short protection release. Releases amplifier short protection that places the device into Actuator-Safe Mode if the amplifier short condition is no longer present. The present amplifier short condition can be determined by reading the AMP_ERR_EINT1 bit twice. At the end of the protection release sequence (0 –> 1 –> 0), if the amplifier short condition is no longer present, the amplifier short-caused Actuator-Safe Mode is cleared (the device may remain Actuator-Safe Mode if another error is present). **Note:** For the protection release bits (x_RLS), if the condition that causes automatic protection becomes true again during the protection potential release sequence, protection is not removed, the related interrupt status bit is set again, and, if unmasked, a new interrupt is generated. 0 = (Default) Release0. After 0 –> 1 –> 0 sequence, if the amplifier short error condition is present, Actuator-Safe Mode is applied 1 = Release1
0	—	Reserved

7.3 Digital I/O Pad Control (PAD_INTF)

7.3.1 LRCK_PAD_CONTROL

Address: 0x0000 2418

	31...8	7	6	5	4	3	2	1	0
RW	—	—			GP4_CTRL	—			
Default	0x00 0000	0	0	0	0	0	1	1	1

Bits	Name	Description
31:5	—	Reserved
4	GP4_CTRL	Defines the function of the ASP_FYSNC/GPIO4 pin: 0 = (Default) Pin acts as ASP_FSYNC input/output 1 = Pin acts as a GPIO, direction controlled by the GP4_DIR register.
3:0	—	Reserved

7.3.2 SDIN_PAD_CONTROL

Address: 0x0000 2420

	31...8	7	6	5	4	3	2	1	0
RW	—	—				GP3_CTRL	—		
Default	0x00 0000	0	0	0	0	0	1	1	1

Bits	Name	Description
31:4	—	Reserved
3	GP3_CTRL	Defines the function of the ASP_DIN/GPIO3 pin: 0 = (Default) Pin acts as ASP_DIN input 1 = Pin acts as a GPIO, direction controlled by the GP3_DIR register.
2:0	—	Reserved

7.3.3 GPIO_PAD_CONTROL

Address: 0x0000 242C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—				GP2_CTRL				—				GP1_CTRL				—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:27	—	Reserved
26:24	GP2_CTRL	Defines the function of the REFCLK/GPIO2 pin: 000 = (Default) High Impedance input 001 = Pin acts as a GPIO, direction controlled by the GP2_DIR register. 010 = Reserved 011 = Pin acts as REFCLK (MCLK) Input 100–111 = Reserved
23:19	—	Reserved
18:16	GP1_CTRL	Defines the function of the GPIO1 pin: 000 = (Default) High Impedance input 001 = Pin acts as a GPIO, direction controlled by the GP1_DIR register. 010–111 = Reserved
15:0	—	Reserved

7.4 Hibernation Power Management (PWRMGT)

7.4.1 PWRMGT_CTL

Address: 0x0000 2900

	31...8	7	6	5	4	3	2	1	0
	—	—						MEM_RDY	TRIG_HIBER
Access	—	—						RW	WO
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:2	—	Reserved
1	MEM_RDY	Setting for the memory ready bit. The status of this bit is reported into MEM_RDY_STS and persists across hibernation modes. 0 = (Default) MEM_RDY_STS cleared 1 = MEM_RDY_STS set
0	TRIG_HIBER	Triggers entry into hibernation mode. Will only take effect if WKSRC_EN has at least one pin enabled. 0 = (Default) No effect. 1 = Enter hibernation mode

7.4.2 WAKESRC_CTL

Address: 0x0000 2904

	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—							UPDT_WKCTL	WKSRC_EN				WKSRC_POL			
Access	—	—							WO	RW				RW			
Default	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Name	Description
31:9	—	Reserved
8	UPDT_WKCTL	Updates the always-on hibernation logic with the current values of WKSRC_EN and WKSRC_POL when set. 0 = (Default) Do not latch values 1 = Latch values
7:4	WKSRC_EN	Configures external pin sources to be monitored to trigger exit from hibernation mode. Must be set to a non-zero value before entry to hibernation mode is permitted using TRIG_HIBER. When enabled, a rising edge on the pin will trigger an exit from hibernation mode. xxx1 – GPIO1 enabled xx1x – REFCLK/GPIO2 enabled x1xx – ASP_FSYNC/GPIO4 enabled 1xxx – I2C_SDA/SPI_MOSI enabled
3:0	WKSRC_POL	Enables the polarity on wake sources to be inverted. xxx1 – GPIO1 falling edge triggered xx1x – REFCLK/GPIO2 falling edge triggered x1xx – ASP_FSYNC/GPIO4 falling edge triggered 1xxx – I2C_SDA/SPI_MOSI falling edge triggered

7.4.3 PWRMGT_STS

Address: 0x0000 2908

RO	31...8	7	6	5	4	3	2	1	0
	—	WKSRC_STS				—		WR_PEND_STS	MEM_RDY_STS
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:8	—	Reserved
7:4	WKSRC_STS	Readback from always-on hibernation logic on the source that caused the exit from hibernation mode. 0000 = (Default) No sources 0001 = GPIO1 triggered 0010 = REFCLK/GPIO2 triggered 0011 = Reserved 0100 = ASP_FSYNC/GPIO4 triggered 0101–0111 = Reserved 1000 = I2C_SDA/SPI_MOSI triggered 1001–1111 = Reserved

Bits	Name	Description
3:2	—	Reserved
1	WR_PEND_STS	Indicates a write is in-progress over the internal bus between the register space and the hibernation logic. Any new writes to the hibernation logic registers will silently fail. 0 = (Default) No write in progress 1 = Write in progress
0	MEM_RDY_STS	Readback status of value previously written to MEM_RDY prior to entry of hibernation mode. 0 = (Default) RAM is not initialised 1 = RAM is initialised

7.5 Device Clocking and Sample Rate Control (CCM)

7.5.1 REFCLK_INPUT

Address: 0x0000 2C04

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	—															PLL_FORCE_EN
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—				PLL_OPEN_LOOP	PLL_REFCLK_FREQ						PLL_REFCLK_EN	—	PLL_REFCLK_SEL		
Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Name	Description
31:17	—	Reserved
16	PLL_FORCE_EN	PLL force enable. Forces the PLL to remain on and selected as the clock source during operational states instead of using the internal oscillator. 0 = (Default) Normal operation (PLL not forced on/selected) 1 = PLL is forced as the internal clock selection source instead of the internal oscillator for low power modes.
15:12	—	Reserved
11	PLL_OPEN_LOOP	PLL closed loop operation control. Configures whether the PLL is operating in an open loop or closed loop configuration. The PLL must be configured to operate open loop if the REFCLK source or frequency is being reconfigured. After the REFCLK has been reconfigured and is stable, the PLL can be set back to a closed loop configuration to resume normal operation. 0 = (Default) Closed loop (PLL is locked to REFCLK) 1 = Open loop (PLL unlocked)
10:5	PLL_REFCLK_FREQ	PLL input reference clock frequency. This value must match the input frequency present at the selected REFCLK source in order to properly configure the internal clocking of the device. 000000 = (Default) 32768Hz 000001–011010 = Reserved 011011 = 1536000 Hz 011100–100000 = Reserved 100001 = 3072000 Hz 100010–100111 = Reserved 101000 = 6144000 Hz 101001–101111 = Reserved 110000 = 9600000 Hz 110001–110010 = Reserved 110011 = 12288000 Hz 110100–111111 = Reserved
4	PLL_REFCLK_EN	Input reference clock enable. Enables the selected reference input clock for purposes of power savings when the device is on a shared bus. 0 = Reference clock input disabled 1 = (Default) Enabled (normal mode)
3	—	Reserved
2:0	PLL_REFCLK_SEL	Device reference clock input select. Selects the reference clock the device uses to generate an internal master clock. 000 = (Default) BCLK input 001 = FSYNC input 010–100 = Reserved 101 = MCLK input 110–111 = Reserved

7.5.2 GLOBAL_SAMPLE_RATE

Address: 0x0000 2C0C

RW	31...8	7	6	5	4	3	2	1	0
	—	—				GLOBAL_FS			
Default	0x00 0000	0	0	0	0	0	0	1	1

Bits	Name	Description
31:5	—	Reserved
4:0	GLOBAL_FS	Serial port sample rate frequency. Configures the global sample rate of the serial port (I²S/TDM). 00000–00010 = Reserved 00011 = (Default) 48.0 kHz 00100–11111 = Reserved

7.6 Digital Boost Converter (BOOST)

7.6.1 VBST_CTL_1

Address: 0x0000 3800

RW	31...8	7	6	5	4	3	2	1	0
	—	BST_CTL							
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:8	—	Reserved
7:0	BST_CTL	Boost converter target control word. Configures the boost converter's output mode and voltage when BST_CTL_SEL is configured to use the control port value. When Class H is enabled and BST_CTL_LIM_EN = 1, configures the maximum allowable VBST voltage for when the target boost voltage is controlled by Class H. When the BST_CTL target is less than VP, the boost converter remains in bypass mode (VBST = VP). Step size is 50 mV. 00000000 = (Default) VBST = VP 00000001 = 2.55 V 00000010 = 2.60 V … 10101001 = 10.95 V 10101010 = 11.00 V … 10101011–11111111 = Reserved

7.6.2 VBST_CTL_2

Address: 0x0000 3804

RW	31...8	7	6	5	4	3	2	1	0
	—	—					BST_CTL_LIM_EN	BST_CTL_SEL	
Default	0x00 0000	0	0	0	0	0	0	0	1

Bits	Name	Description
31:3	—	Reserved
2	BST_CTL_LIM_EN	Class H boost control maximum limit. Controls whether the Class H's maximum generated boost control voltage is limited by the BST_CTL configuration. 0 = (Default) No user-configured limit 1 = Maximum Class H BST_CTL generation is limited by BST_CTL configuration
1:0	BST_CTL_SEL	Boost converter control source selection. Selects the source of the BST_CTL target VBST voltage for the boost converter to generate. This allows the user to select how to manage the control of the target VBST voltage without enabling and disabling other functional blocks, potentially changing the signal path (i.e. Class H tracking). **Note:** When Class H tracking is selected as the BST_CTL target source, and the Class H is disabled (CLASSH_EN = 0) the boost converter remains in bypass mode (VBST = VP). 00 = Control port BST_CTL register value 01 = (Default) Class H tracking value 10–11 = Reserved

7.6.3 BST_IPK_CTL

Address: 0x0000 3808

RW	31...8	7	6	5	4	3	2	1	0
	—	—	BST_IPK						
Default	0x00 0000	0	1	0	0	1	0	1	0

Bits	Name	Description
31:7	—	Reserved
6:0	BST_IPK	Boost converter peak current limit. Configures the peak current by monitoring the current through the boost FET. If the amplifier attempts to draw enough power to where the boost FET reaches the configured IMAX(B) limit, only the set limit current is provided and, consequently, the boosted VBST voltage droops. Step size is 50 mA. 0000000–0001111 = Reserved 0010000 = 1.60 A 0010001 = 1.65 A 0010010 = 1.70 A … 1001000 = 4.40 A 1001001 = 4.45 A 1001010 = (Default) 4.50 A 1001011–1111111 = Reserved

7.6.4 SOFT_RAMP

Address: 0x0000 380C

RW	31...8	7	6	5	4	3	2	1	0
	—	—				BST_SFT_RAMP			
Default	0x00 0000	0	0	0	0	0	0	1	1

Bits	Name	Description
31:4	—	Reserved
3:0	BST_SFT_RAMP	Boost converter VBST voltage soft ramp. Configures how quickly the VBST voltage is allowed to change in response to a BST_CTL or target VBST voltage configuration change. This limits the amount of inrush or backpowering current associated with charging or discharging the CBST capacitor. Absolute time is based on a fPLL_OUT = 192 MHz. Larger values produce a slower change in voltage and are intended for use cases with large CBST values. 0000 = 50.0 mV/µs 0001 = 33.3 mV/µs 0010 = 25.0 mV/µs 0011 = (Default) 18.8 mV/µs 0100 = 12.5 mV/µs 0101 = 9.4 mV/µs 0110 = 4.7 mV/µs 0111 = 2.3 mV/µs 1000 = 1.2 mV/µs 1001 = 585 mV/ms 1010 = 292 mV/ms 1011 = 146 mV/ms 1100 = 73 mV/ms 1101 = 36 mV/ms 1110 = 18 mV/ms 1111 = 9 mV/ms

7.6.5 BST_LOOP_COEFF

Address: 0x0000 3810

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	BST_K2								BST_K1							
Default	0x0000	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0

Bits	Name	Description
31:16	—	Reserved
15:8	BST_K2	Along with BST_K1, adjusts the boost converter's feedback loop to compensate for the changes produced by using a different LBST inductance or different system requirements. **Note:** Adjusting for a lower inductance reduces the loop bandwidth.
7:0	BST_K1	Along with BST_K2, adjusts the boost converter's feedback loop to compensate for the changes produced by using a different LBST inductance or different system requirements. **Note:** Adjusting for a lower inductance reduces the loop bandwidth.

7.6.6 LBST_SLOPE

Address: 0x0000 3814

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	BST_SLOPE								—						BST_LBST_VAL	
Default	0x0000	0	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description
31:16	—	Reserved
15:8	BST_SLOPE	Allows for adjustment of the boost converter's internal ramp-gen slope to compensate for the changes produced by using a different LBST inductance.
7:2	—	Reserved
1:0	BST_LBST_VAL	Inductor estimation LBST reference value. Seeds the digital boost converter's inductor estimation block with the initial inductance value to reference. 00 = (Default) 1.0 µH 01 = 1.2 µH 10 = 1.5 µH 11 = 2.2 µH

7.6.7 BST_SW_FREQ

Address: 0x0000 3818

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BST_DCM_FREQ_MIN								—								BST_DCM_FREQ								—				BST_CCM_FREQ			
Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:24	BST_DCM_FREQ_MIN	Boost converter's minimum DCM mode switching frequency. Configures the minimum allowable SW net switching frequency the boost converter can produce while operating in DCM Mode. The maximum allowable number of consecutive skipped periods is set by BST_DCM_FREQ_MIN. If the BST_DCM_FREQ_MIN = 0, then no switching period is allowed to be skipped; if BST_DCM_FREQ_MIN = 1, then 1 switching period is allowed to be skipped, etc. The minimum allowable switching period = BST_DCM_FREQ/(BST_DCM_FREQ_MIN+1) MHz. 00000000 = DCM mode frequency skipping disabled (BST_DCM_FREQ/1) 00000001 = (Default) BST_DCM_FREQ/2 00000010 = BST_DCM_FREQ/3 00000011 = BST_DCM_FREQ/4 … 11111110 = BST_DCM_FREQ/255 11111111 = BST_DCM_FREQ/256
23:18	—	Reserved
17:8	BST_DCM_FREQ	Boost converter's DCM mode switching frequency. Configures the base rate SW net switching frequency when operating in DCM Mode. All frequencies listed with a fPLL_OUT of 192 MHz. Other fPLL_OUT frequencies scale ratiometrically. Step size: fPLL_OUT/(8*(12+n)) MHz. 0x000 = 2,000.00 kHz 0x001 = 1,846.15 kHz 0x002 = 1,714.29 kHz … 0x080 = (Default) 171.43 kHz … 0x3FE = 23.21 kHz 0x3FF = 23.19 kHz
7:4	—	Reserved
3:0	BST_CCM_FREQ	Boost converter's CCM mode switching frequency. Controls the fundamental output switching frequency of the digital boost converter's SW net when operating in CCM mode. The frequency listed is based on a f_{PLL_OUT} = 192 MHz. Other f_{PLL_OUT} frequencies scale ratiometrically. 0000 = (Default) 2.000 MHz 0001 = 1.846 MHz 0010 = 1.714 MHz 0011 = 1.600 MHz 0100 = 1.500 MHz 0101 = 1.412 MHz 0110 = 1.333 MHz 0111 = 1.263 MHz 1000 = 1.200 MHz 1001 = 1.143 MHz 1010 = 1.091 MHz 1011 = 1.043 MHz 1100 = 1.000 MHz 1101 = 0.960 MHz 1110 = 0.923 MHz 1111 = 0.889 MHz

7.6.8 BST_DCM_CTL

Address: 0x0000 381C

RW	31...8	7	6	5	4	3	2	1	0
	—	BST_DCM_EXIT_SEL		BST_DCM_ENTRY_SEL		—			BST_DCM_EN
Default	0x00 0000	0	1	0	1	0	0	0	1

Bits	Name	Description
31:8	—	Reserved
7:6	BST_DCM_EXIT_SEL	Boost converter DCM exit source selection. Selects the signal source for the automatic DCM exit to CCM Mode. 00 = Reserved 01 = (Default) Noise gating control triggers DCM Mode exit 10 = Reserved 11 = Automatic load detection disabled. User must manually force in/out of DCM Mode via BST_DCM_FORCE registers.
5:4	BST_DCM_ENTRY_SEL	Boost converter DCM entry source selection. Selects the signal source for the automatic DCM entry from CCM Mode. 00 = Reserved 01 = (Default) Noise gating control triggers DCM Mode entry 10 = Reserved 11 = Automatic load detection disabled. User must manually force in/out DCM Mode via BST_DCM_FORCE registers.
3:1	—	Reserved
0	BST_DCM_EN	Boost converter automatic DCM Mode enable. This enables the digital boost converter to operate in a low power (DCM) mode during low loading conditions. 0 = Boost converter automatic low power mode disabled 1 = (Default) Boost converter automatic low power mode enabled

7.6.9 DCM_FORCE

Address: 0x0000 3820

RW	31...8	7	6	5	4	3	2	1	0
	—	—						BST_DCM_FRC_EN	BST_DCM_FRC
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:2	—	Reserved
1	BST_DCM_FRC_EN	Boost converter DCM force mode control enable. Setting this field enables the DCM/CCM control functionality of BST_DCM_FRC. Do not force the boost converter in to DCM Mode when there is a load greater than 8 mA on the VBST supply. Device damage may occur. 0 = (Default) BST_DCM_FORCE control disabled 1 = BST_DCM_FORCE control enabled
0	BST_DCM_FRC	Force the boost converter to operate in DCM Mode. When enabled by BST_DCM_FRC_EN, manually puts the boost converter in either DCM Mode or CCM Mode. When BST_DCM_FRC_EN = 0, this control has no functionality. [Sequence: 0 –> 1]: Force transition to DCM Mode [Sequence: 1 –> 0]: Force transition to CCM mode 0 = (Default) Remain in CCM mode when automatic control is disabled (BST_DCM_EN = 0) 1 = Remain in DCM mode if no error condition is present and automatic control disabled (BST_DCM_EN = 0).

7.6.10 VBST_OVP

Address: 0x0000 3830

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—							BST_OVP_EN	—		BST_OVP_THLD					
Default	0x0000	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0

Bits	Name	Description
31:9	—	Reserved
8	BST_OVP_EN	Boost converter overvoltage protection enable. Clearing this bit disables the boost converter active protection limit (configured by BST_OVP_THLD). This setting has no impact on the VBST overvoltage error protection (BST_VBST_ERR). 0 = Overvoltage protection disabled 1 = (Default) (Default) Overvoltage protection enabled
7:6	—	Reserved
5:0	BST_OVP_THLD	Boost converter overvoltage protection limit. Threshold to actively limit any VBST voltage overshoot caused by a rapid load change. Intended to allow for the protection of external components such as CBST. Step size: 0.0625V. 000000 = 9.0000 V 000001 = 9.0625 V 000010 = 9.1250 V … 110000 = (Default) 12.0000 V … 111110 = 12.8750 V 111111 = 12.9375 V

7.7 VMON and IMON Signal Monitoring (VIMON)

7.7.1 MONITOR_FILT

Address: 0x0000 4008

RW	31...8	7	6	5	4	3	2	1	0
	—	—							MON_FILT_RESP
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:1	—	Reserved
0	MON_FILT_RESP	Selects filter response for VMON and IMON paths. 0 = (Default) Optimized for sample rates of 48 kHz and below 1 = Optimized for sample rates greater than 48 kHz

7.8 Die Temperature Monitoring (TEMPMON)

7.8.1 WARN_LIMIT_THRESHOLD

Address: 0x0000 4220

RW	31...8	7	6	5	4	3	2	1	0
	—	—						TEMP_WARN_THLD	
Default	0x00 0000	0	0	0	0	0	0	1	0

Bits	Name	Description
31:2	—	Reserved
1:0	TEMP_WARN_THLD	Amplifier overtemperature warning threshold. Configures the threshold at which the overtemperature warning condition occurs. When the threshold is met, the overtemperature warning attenuation is applied and the TEMP_WARN_RISE_EINT1 interrupt status bit is set. If TEMP_WARN_RISE_MASK1 = 0, ALERT is asserted. 00 = 105 C 01 = 115 C 10 = (Default) 125 C 11 = 135 C

7.8.2 CONFIGURATION

Address: 0x0000 4224

RW	31...8	7	6	5	4	3	2	1	0
	—	—				TEMP_OUT_SEL	TEMP_WARN_ERR_SEL	TEMP_FILT_SEL	
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:4	—	Reserved
3	TEMP_OUT_SEL	Selects the source of the temperature measurement passed to the PCM Data Routing block. 0 = (Default) Unfiltered 1 = Filtered
2	TEMP_WARN_ERR_SEL	Selects the source of the temperature measurement passed to the overtemperature warning and error blocks. 0 = (Default) Unfiltered 1 = Filtered
1:0	TEMP_FILT_SEL	Selects the depth of the running average filter used on the raw temperature value. 00 = (Default) 1 sample (no filtering) 01 = 2 samples 10 = 4 samples 11 = 8 samples

7.8.3 ENABLES_AND_CODES_DIG

Address: 0x0000 4308

RO	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—								TEMP_RESULT_FILT								—								TEMP_RESULT_UNFILT							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:25	—	Reserved
24:16	TEMP_RESULT_FILT	Filtered die temperature result. 2's complement, 1 LSB = 1 °C. 0x000 = (Default) 0 °C 0x001 = 1 °C 0x002 = 2 °C … 0x0AF = 175 °C 0x0B0 = 176 °C 0x0B1–0x1BF = Reserved 0x1C0 = –64 °C 0x1C1 = –63 °C … 0x1FE = –2 °C 0x1FF = –1 °C
15:9	—	Reserved
8:0	TEMP_RESULT_UNFILT	Unfiltered die temperature result. 2's complement, 1 LSB = 1 °C. 0x000 = (Default) 0 °C 0x001 = 1 °C 0x002 = 2 °C … 0x0AF = 175 °C 0x0B0 = 176 °C 0x0B1–0x1BF = Reserved 0x1C0 = –64 °C 0x1C1 = –63 °C … 0x1FE = –2 °C 0x1FF = –1 °C

7.9 ASP Data Interface (DATAIF)

7.9.1 ASP_ENABLES1

Address: 0x0000 4800

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	—														ASP_RX2_EN	ASP_RX1_EN
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:18	—	Reserved
17	ASP_RX2_EN	ASP Interface RX Channel 2 Enable 0 = (Default) Disabled 1 = Enabled
16	ASP_RX1_EN	ASP Interface RX Channel 1 Enable 0 = (Default) Disabled 1 = Enabled
15:0	—	Reserved

7.9.2 ASP_CONTROL1

Address: 0x0000 4804

	31...8	7	6	5	4	3	2	1	0
RW	—	—		ASP_BCLK_FREQ					
Default	0x00 0000	0	0	1	0	1	0	0	0

Bits	Name	Description
31:6	—	Reserved
5:0	ASP_BCLK_FREQ	ASP_BCLK freq. This field must be set to match the frequency of the ASP_BCLK clock source. 000000–011010 = Reserved 011011 = 1.536 MHz 011100–100000 = Reserved 100001 = 3.072 MHz 100010–100111 = Reserved 101000 = (Default) 6.144 MHz 101001–101111 = Reserved 110000 = 9.600 MHz 110001–110010 = Reserved 110011 = 12.288 MHz 110100–111111 = Reserved

7.9.3 ASP_CONTROL2

Address: 0x0000 4808

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	ASP_RX_WIDTH								—							
Default	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—				ASP_FMT				—	ASP_BCLK_INV	ASP_BCLK_FRC	ASP_BCLK_MSTR	—	ASP_FSYNC_INV	ASP_FSYNC_FRC	ASP_FSYNC_MSTR
Default	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:24	ASP_RX_WIDTH	ASP RX data pin (ASP_DIN) slot width and data width. Sets the total number of ASP_BCLK cycles per Rx slot. The number of ASP_BCLK cycles per Rx slot that contains valid data is controlled by ASP_RX_WL. Integer (LSB = 1); Valid from 12 to 128. 00000000–00001011 = Reserved 00001100 = 12 cycles per slot … 00010000 = 16 cycles per slot 00010001 = 17 cycles per slot 00010010 = 18 cycles per slot … 00011000 = (Default) 24 cycles per slot 00011001 = 25 cycles per slot … 01111111 = 127 cycles per slot 10000000 = 128 cycles per slot 10000001–11111111 = Reserved
23:11	—	Reserved

Bits	Name	Description
10:8	ASP_FMT	ASP Interface Format. This field should only be changed when all ASP channels are disabled. 000 = TDM 1 (DSP Mode A) 001 = Reserved 010 = (Default) I²S mode 011 = Reserved 100 = TDM 1.5 101–111 = Reserved
7	—	Reserved
6	ASP_BCLK_INV	ASP Interface ASP_BCLK Invert 0 = (Default) ASP_BCLK not inverted 1 = ASP_BCLK inverted
5	ASP_BCLK_FRC	ASP Interface ASP_BCLK Output Control 0 = (Default) Normal 1 = ASP_BCLK always enabled in Master mode
4	ASP_BCLK_MSTR	ASP Interface ASP_BCLK Master Select 0 = (Default) ASP_BCLK Slave mode 1 = ASP_BCLK Master mode
3	—	Reserved
2	ASP_FSYNC_INV	ASP Interface FSYNC Invert 0 = (Default) ASP_FSYNC not inverted 1 = ASP_FSYNC inverted
1	ASP_FSYNC_FRC	ASP Interface FSYNC Output Control 0 = (Default) Normal 1 = ASP_FSYNC always enabled in Master mode
0	ASP_FSYNC_MSTR	ASP Interface FSYNC Master Select 0 = (Default) ASP_FSYNC Slave mode 1 = ASP_FSYNC Master mode

7.9.4 ASP_FRAME_CONTROL5

Address: 0x0000 4820

	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—	—		ASP_RX2_SLOT						—		ASP_RX1_SLOT					
Default	0x0000	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Name	Description
31:14	—	Reserved
13:8	ASP_RX2_SLOT	ASP RX Channel 2 Slot position Defines the RX timeslot position of the Channel 2 sample Integer (LSB=1); Valid from 0 to 63. 000000 = Slot 0 000001 = (Default) Slot 1 000010 = Slot 2 … 111101 = Slot 61 111110 = Slot 62 111111 = Slot 63
7:6	—	Reserved
5:0	ASP_RX1_SLOT	ASP RX Channel 1 Slot position Defines the RX timeslot position of the Channel 1 sample Integer (LSB=1); Valid from 0 to 63. 000000 = (Default) Slot 0 000001 = Slot 1 000010 = Slot 2 … 111101 = Slot 61 111110 = Slot 62 111111 = Slot 63

7.9.5 ASP_DATA_CONTROL5

Address: 0x0000 4840

RW	31...8	7	6	5	4	3	2	1	0
	—	—				ASP_RX_WL			
Default	0x00 0000	0	0	0	1	1	0	0	0

Bits	Name	Description
31:6	—	Reserved
5:0	ASP_RX_WL	ASP RX (ASP_DIN) active data width. Sets the number of ASP_BCLK cycles of valid data per Rx slot. Defines number of active MSBs at start of slot. The total number of ASP_BCLK cycles per Rx slot is controlled by ASP_RX_WIDTH. If ASP_RX_WL < ASP_RX_WIDTH, any data after the active width will be cropped to 0. If ASP_RX_WL >= ASP_RX_WIDTH, all data bits in slot are active. Integer (LSB=1); Valid from 12 to 24. 000000–001011 = Reserved 001100 = 12 cycles per slot 001101 = 13 cycles per slot 001110 = 14 cycles per slot … 010110 = 22 cycles per slot 010111 = 23 cycles per slot 011000 = (Default) 24 cycles per slot 011001–111111 = Reserved

7.10 Data Routing (MIXER)

7.10.1 DACPCM1_INPUT

Address: 0x0000 4C00

RW	31...8	7	6	5	4	3	2	1	0
	—	—				DACPCM1_SRC			
Default	0x00 0000	0	0	0	0	1	0	0	0

Bits	Name	Description
31:7	—	Reserved
6:0	DACPCM1_SRC	DACPCM1 input source 0000000 = ZERO_FILL 0000001–0000111 = Reserved 0001000 = (Default) ASPRX1 0001001 = ASPRX2 0001010–0110001 = Reserved 0110010 = DSP1TX1 0110011 = DSP1TX2 0110100 = DSP1TX3 0110101 = DSP1TX4 0110110 = DSP1TX5 0110111 = DSP1TX6 0111000 = DSP1TX7 0111001 = DSP1TX8 0111010–1111111 = Reserved

7.10.2 DSP1RX1_INPUT

Address: 0x0000 4C40

RW	31...8	7	6	5	4	3	2	1	0
	—	—				DSP1RX1_SRC			
Default	0x00 0000	0	0	0	0	1	0	0	0

Bits	Name	Description
31:7	—	Reserved
6:0	DSP1RX1_SRC	DSP1RX1 input source 0000000 = ZERO_FILL 0000001–0000111 = Reserved 0001000 = (Default) ASPRX1 0001001 = ASPRX2 0001010–0010111 = Reserved 0011000 = VMON 0011001 = IMON 0011010–0011111 = Reserved 0100000 = ERR_VOL 0100001 = CLASSH_TGT 0100010–0100111 = Reserved 0101000 = VPMON 0101001 = VBSTMON 0101010–0110001 = Reserved 0110010 = DSP1TX1 0110011 = DSP1TX2 0110100 = DSP1TX3 0110101 = DSP1TX4 0110110 = DSP1TX5 0110111 = DSP1TX6 0111000 = DSP1TX7 0111001 = DSP1TX8 0111010 = TEMP_MON 0111011–1111111 = Reserved

7.10.3 DSP1RX2_INPUT

Address: 0x0000 4C44

RW	31...8	7	6	5	4	3	2	1	0
	—	—	DSP1RX2_SRC						
Default	0x00 0000	0	0	0	0	1	0	0	1

Bits	Name	Description
31:7	—	Reserved
6:0	DSP1RX2_SRC	DSP1RX2 input source 0000000 = ZERO_FILL 0000001–0000111 = Reserved 0001000 = ASPRX1 0001001 = (Default) ASPRX2 0001010–0010111 = Reserved 0011000 = VMON 0011001 = IMON 0011010–0011111 = Reserved 0100000 = ERR_VOL 0100001 = CLASSH_TGT 0100010–0100111 = Reserved 0101000 = VPMON 0101001 = VBSTMON 0101010–0110001 = Reserved 0110010 = DSP1TX1 0110011 = DSP1TX2 0110100 = DSP1TX3 0110101 = DSP1TX4 0110110 = DSP1TX5 0110111 = DSP1TX6 0111000 = DSP1TX7 0111001 = DSP1TX8 0111010 = TEMP_MON 0111011–1111111 = Reserved

7.10.4 DSP1RX3_INPUT

Address: 0x0000 4C48

RW	31...8	7	6	5	4	3	2	1	0
	—	—	DSP1RX3_SRC						
Default	0x00 0000	0	0	0	1	1	0	0	0

Bits	Name	Description
31:7	—	Reserved
6:0	DSP1RX3_SRC	DSP1RX3 input source 0000000 = ZERO_FILL 0000001–0000111 = Reserved 0001000 = ASPRX1 0001001 = ASPRX2 0001010–0010111 = Reserved 0011000 = (Default) VMON 0011001 = IMON 0011010–0011111 = Reserved 0100000 = ERR_VOL 0100001 = CLASSH_TGT 0100010–0100111 = Reserved 0101000 = VPMON 0101001 = VBSTMON 0101010–0110001 = Reserved 0110010 = DSP1TX1 0110011 = DSP1TX2 0110100 = DSP1TX3 0110101 = DSP1TX4 0110110 = DSP1TX5 0110111 = DSP1TX6 0111000 = DSP1TX7 0111001 = DSP1TX8 0111010 = TEMP_MON 0111011–1111111 = Reserved

7.10.5 DSP1RX4_INPUT

Address: 0x0000 4C4C

RW	31...8	7	6	5	4	3	2	1	0
	—	—	DSP1RX4_SRC						
Default	0x00 0000	0	0	0	1	1	0	0	1

Bits	Name	Description
31:7	—	Reserved
6:0	DSP1RX4_SRC	DSP1RX4 input source 0000000 = ZERO_FILL 0000001–0000111 = Reserved 0001000 = ASPRX1 0001001 = ASPRX2 0001010–0010111 = Reserved 0011000 = VMON 0011001 = (Default) IMON 0011010–0011111 = Reserved 0100000 = ERR_VOL 0100001 = CLASSH_TGT 0100010–0100111 = Reserved 0101000 = VPMON 0101001 = VBSTMON 0101010–0110001 = Reserved 0110010 = DSP1TX1 0110011 = DSP1TX2 0110100 = DSP1TX3 0110101 = DSP1TX4 0110110 = DSP1TX5 0110111 = DSP1TX6 0111000 = DSP1TX7 0111001 = DSP1TX8 0111010 = TEMP_MON 0111011–1111111 = Reserved

7.10.6 DSP1RX5_INPUT

Address: 0x0000 4C50

RW	31...8	7	6	5	4	3	2	1	0
	—	—	DSP1RX5_SRC						
Default	0x00 0000	0	0	1	0	0	0	0	0

Bits	Name	Description
31:7	—	Reserved
6:0	DSP1RX5_SRC	DSP1RX5 input source 0000000 = ZERO_FILL 0000001–0000111 = Reserved 0001000 = ASPRX1 0001001 = ASPRX2 0001010–0010111 = Reserved 0011000 = VMON 0011001 = IMON 0011010–0011111 = Reserved 0100000 = (Default) ERR_VOL 0100001 = CLASSH_TGT 0100010–0100111 = Reserved 0101000 = VPMON 0101001 = VBSTMON 0101010–0110001 = Reserved 0110010 = DSP1TX1 0110011 = DSP1TX2 0110100 = DSP1TX3 0110101 = DSP1TX4 0110110 = DSP1TX5 0110111 = DSP1TX6 0111000 = DSP1TX7 0111001 = DSP1TX8 0111010 = TEMP_MON 0111011–1111111 = Reserved

7.10.7 DSP1RX6_INPUT

Address: 0x0000 4C54

RW	31...8	7	6	5	4	3	2	1	0
	—	—	DSP1RX6_SRC						
Default	0x00 0000	0	0	1	0	0	0	0	1

Bits	Name	Description
31:7	—	Reserved
6:0	DSP1RX6_SRC	DSP1RX6 input source 0000000 = ZERO_FILL 0000001–0000111 = Reserved 0001000 = ASPRX1 0001001 = ASPRX2 0001010–0010111 = Reserved 0011000 = VMON 0011001 = IMON 0011010–0011111 = Reserved 0100000 = ERR_VOL 0100001 = (Default) CLASSH_TGT 0100010–0100111 = Reserved 0101000 = VPMON 0101001 = VBSTMON 0101010–0110001 = Reserved 0110010 = DSP1TX1 0110011 = DSP1TX2 0110100 = DSP1TX3 0110101 = DSP1TX4 0110110 = DSP1TX5 0110111 = DSP1TX6 0111000 = DSP1TX7 0111001 = DSP1TX8 0111010 = TEMP_MON 0111011–1111111 = Reserved

7.10.8 DSP1RX7_INPUT

Address: 0x0000 4C58

RW	31...8	7	6	5	4	3	2	1	0
	—	—	DSP1RX7_SRC						
Default	0x00 0000	0	0	1	1	1	0	1	0

Bits	Name	Description
31:7	—	Reserved
6:0	DSP1RX7_SRC	DSP1RX7 input source 0000000 = ZERO_FILL 0000001–0000111 = Reserved 0001000 = ASPRX1 0001001 = ASPRX2 0001010–0010111 = Reserved 0011000 = VMON 0011001 = IMON 0011010–0011111 = Reserved 0100000 = ERR_VOL 0100001 = CLASSH_TGT 0100010–0100111 = Reserved 0101000 = VPMON 0101001 = VBSTMON 0101010–0110001 = Reserved 0110010 = DSP1TX1 0110011 = DSP1TX2 0110100 = DSP1TX3 0110101 = DSP1TX4 0110110 = DSP1TX5 0110111 = DSP1TX6 0111000 = DSP1TX7 0111001 = DSP1TX8 0111010 = (Default) TEMP_MON 0111011–1111111 = Reserved

7.10.9 DSP1RX8_INPUT

Address: 0x0000 4C5C

RW	31...8	7	6	5	4	3	2	1	0
	—	—	DSP1RX8_SRC						
Default	0x00 0000	0	0	1	1	1	0	1	1

Bits	Name	Description
31:7	—	Reserved
6:0	DSP1RX8_SRC	DSP1RX8 input source 0000000 = ZERO_FILL 0000001–0000111 = Reserved 0001000 = ASPRX1 0001001 = ASPRX2 0001010–0010111 = Reserved 0011000 = VMON 0011001 = IMON 0011010–0011111 = Reserved 0100000 = ERR_VOL 0100001 = CLASSH_TGT 0100010–0100111 = Reserved 0101000 = VPMON 0101001 = VBSTMON 0101010–0110001 = Reserved 0110010 = DSP1TX1 0110011 = DSP1TX2 0110100 = DSP1TX3 0110101 = DSP1TX4 0110110 = DSP1TX5 0110111 = DSP1TX6 0111000 = DSP1TX7 0111001 = DSP1TX8 0111010 = TEMP_MON 0111011–1111111 = (Default) Reserved

7.10.10 NGATE1_INPUT

Address: 0x0000 4C60

RW	31...8	7	6	5	4	3	2	1	0
	—	—	NGATE1_SRC						
Default	0x00 0000	0	0	0	0	1	0	0	0

Bits	Name	Description
31:7	—	Reserved
6:0	NGATE1_SRC	NGATE1 input source 0000000 = ZERO_FILL 0000001–0000111 = Reserved 0001000 = (Default) ASPRX1 0001001 = ASPRX2 0001010–0010111 = Reserved 0011000 = VMON 0011001 = IMON 0011010–0110001 = Reserved 0110010 = DSP1TX1 0110011 = DSP1TX2 0110100 = DSP1TX3 0110101 = DSP1TX4 0110110 = DSP1TX5 0110111 = DSP1TX6 0111000 = DSP1TX7 0111001 = DSP1TX8 0111010–1111111 = Reserved

7.10.11 NGATE2_INPUT

Address: 0x0000 4C64

RW	31...8	7	6	5	4	3	2	1	0
	—	—	NGATE2_SRC						
Default	0x00 0000	0	0	0	0	1	0	0	1

Bits	Name	Description
31:7	—	Reserved
6:0	NGATE2_SRC	NGATE2 input source 0000000 = ZERO_FILL 0000001–0000111 = Reserved 0001000 = ASPRX1 0001001 = (Default) ASPRX2 0001010–0010111 = Reserved 0011000 = VMON 0011001 = IMON 0011010–0110001 = Reserved 0110010 = DSP1TX1 0110011 = DSP1TX2 0110100 = DSP1TX3 0110101 = DSP1TX4 0110110 = DSP1TX5 0110111 = DSP1TX6 0111000 = DSP1TX7 0111001 = DSP1TX8 0111010–1111111 = Reserved

7.11 Amplifier Volume Control (INTP)

7.11.1 AMP_CTRL

Address: 0x0000 6000

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	AMP_HPF_PCM_EN	AMP_INV_PCM	AMP_VOL_PCM										AMP_RAMP_PCM			
Default	0x0000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:16	—	Reserved
15	AMP_HPF_PCM_EN	Amplifier PCM path high-pass filter enable. Enables the internal high-pass filter at the input of the PCM path. The corner frequency of the HPF is 0.94 Hz. 0 = Disabled 1 = (Default) Enabled
14	AMP_INV_PCM	Amplifier PCM inversion. Inverts the polarity of the data output from the Class-D amplifier. 0 = (Default) PCM data not inverted 1 = PCM data inverted
13:3	AMP_VOL_PCM	Amplifier digital gain control. Sets the gain of the amplifier's digital PCM data path. Register configuration values beyond listed range are clamped to the corresponding min/max values. Step size: 0.125 dB. Range +12.0 dB to –102 dB. Values below –102 dB digitally mute the output. 0x400–0x4CF = Mute 0x4D0 = –102.0 dB 0x4D1 = –101.875 dB … 0x7FE = –0.25 dB 0x7FF = –0.125 dB 0x000 = (Default) 0.0 dB 0x001 = 0.125 dB … 0x05E = 11.75 dB 0x05F = 11.875 dB 0x060–0x3FF = 12.0 dB
2:0	AMP_RAMP_PCM	Amplifier PCM soft-ramp rate. Selects the soft-ramp rate for all digital gain changes. This register must not be changed during a gain change. 000 = (Default) No Ramp 001 = 0.5 ms/6 dB 010 = 1 ms/6 dB 011 = 2 ms/6 dB 100 = 4 ms/6 dB 101 = 8 ms/6 dB 110 = 15 ms/6 dB 111 = 30 ms/6 dB

7.12 VP and VBST Brownout Prevention + Temp Warning (ERROR_VOLUME)

7.12.1 VPBR_CONFIG

Address: 0x0000 6404

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—					VPBR_REL_TRIG	VPBR_REL_AUTO	VPBR_MUTE_EN	VPBR_REL_RATE			VPBR_WAIT		VPBR_ATK_RATE		
Default	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VPBR_ATK_VOL				VPBR_MAX_ATT				—			VPBR_THLD1				
Default	0	0	0	1	1	0	0	1	0	0	0	0	0	1	0	1

Bits	Name	Description
31:27	—	Reserved
26	VPBR_REL_TRIG	VP brownout prevention manual release trigger. When sequencing when configured in manual release mode (VPBR_REL_AUTO = 0), triggers the VP brownout prevention to enter the release state. **Note:** VPBR_REL_TRIG has no effect if VPBR_REL_AUTO = 1. 0 –> 1 –> 0 sequence. At the end of the sequence, if the VP brownout prevention is in the manual wait state and no VPBR_FLAG condition is present, triggers it to enter the release state. 0 = (Default) No action 1 = When in a wait state with no VPBR_FLAG, waits indefinitely for a manual trigger to occur
25	VPBR_REL_AUTO	VP brownout prevention automatic wait and release. Configures whether the automatic VPBR_WAIT timer or the manual VPBR_REL_TRIG determines when the wait state is exited and the release state is entered. 0 = Manual mode; requires VPBR_REL_TRIG to be sequenced to enter release 1 = (Default) Automatic wait period based on VPBR_WAIT

Bits	Name	Description
24	VPBR_MUTE_EN	During the attack state, if the VPBR_MAX_ATT value is reached, the error condition still remains, and this bit is set, the signal is muted. The signal remains muted until the error condition has cleared and the VP brownout prevention enters a releasing state. 0 = (Default) Mute disabled 1 = Mute enabled
23:21	VPBR_REL_RATE	Attenuation release step rate (tVPBR_REL). Configures the delay between consecutive volume attenuation release steps (VOLREL) when a brownout condition is no longer present and the VP brownout is in an attenuation release state. 000 = 5 ms 001 = 10 ms 010 = 25 ms 011 = 50 ms 100 = 100 ms 101 = (Default) 250 ms 110 = 500 ms 111 = 1000 ms
20:19	VPBR_WAIT	Configures the delay between a brownout condition no longer being present and the VP brownout prevention entering an attenuation release state. 00 = 10 ms 01 = (Default) 100 ms 10 = 250 ms 11 = 500 ms
18:16	VPBR_ATK_RATE	Attenuation attack step rate (tVPBR_ATK). Configures the amount delay between consecutive volume attenuation steps (VOLATK) when a brownout condition is present and the VP brownout condition is in an attacking state. 000 = 2.5 µs 001 = 5 µs 010 = (Default) 10 µs 011 = 25 µs 100 = 50 µs 101 = 100 µs 110 = 250 µs 111 = 500 µs
15:12	VPBR_ATK_VOL	VP brownout prevention attack step size. Configures the VP brownout prevention attacking attenuation step size when operating in either digital volume or analog gain modes. Attenuation values listed are relative to triggering VPBR_THLD1 / VP_{BR_2} / VP_{BR_3} per attack time period (VPBR_ATK_RATE). 0000 = 0.0625 dB / 0.125 dB / 0.250 dB 0001 = (Default) 0.125 dB / 0.250 dB / 0.500 dB 0010 = 0.250 dB / 0.500 dB / 1.000 dB 0011 = 0.500 dB / 1.000 dB / 2.000 dB 0100 = 0.750 dB / 1.500 dB / 3.000 dB 0101 = 1.000 dB / 2.000 dB / 4.000 dB 0110 = 1.250 dB / 2.500 dB / 5.000 dB 0111 = 1.500 dB / 3.000 dB / 6.000 dB 1000–1111 = Reserved
11:8	VPBR_MAX_ATT	Maximum attenuation that the VP brownout prevention can apply to the signal. Even if an error condition remains present, the VP brownout prevention only attenuates the signal up to the limit configured by VPBR_MAX_ATT. Step size: 1 dB. **Note:** VPBR_MAX_ATT should not be adjusted when attenuation is being applied by the VP brownout prevention. 0000 = 0 dB 0001 = 1 dB 0010 = 2 dB … 1001 = (Default) 9 dB … 1110 = 14 dB 1111 = 15 dB
7:5	—	Reserved
4:0	VPBR_THLD1	Initial VPBR_1 threshold. Configures the VP brownout threshold voltage. 00000–00001 = Reserved 00010 = 2.497 V 00011 = 2.544 V 00100 = 2.592 V 00101 = (Default) 2.639 V … 11111 = 3.874 V

7.12.2 VBBR_CONFIG

Address: 0x0000 6408

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW						VBBR_REL_TRIG	VBBR_REL_AUTO	VBBR_MUTE_EN								
	—								VBBR_REL_RATE			VBBR_WAIT		VBBR_ATK_RATE		
Default	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																
	VBBR_ATK_VOL				VBBR_MAX_ATT				—		VBBR_THLD1					
Default	0	0	0	1	1	0	0	1	0	0	0	0	0	1	0	1

Bits	Name	Description
31:27	—	Reserved
26	VBBR_REL_TRIG	VBST brownout prevention manual release trigger. When sequencing when configured in manual release mode (VBBR_REL_AUTO = 0), triggers the VBST brownout prevention to enter the release state. **Note:** VBBR_REL_TRIG has no effect if VBBR_REL_AUTO = 1. 0 –> 1 –> 0 sequence. At the end of the sequence, if the VBST brownout prevention is in the manual wait state and no VBBR_FLAG condition is present, triggers it to enter the release state. 0 = (Default) No action 1 = When in a wait state with no VBBR_FLAG, waits indefinitely for a manual trigger to occur
25	VBBR_REL_AUTO	VBST brownout prevention automatic wait and release. Configures whether the automatic VBBR_WAIT timer or the manual VBBR_REL_TRIG determines when the wait state is exited and the release state is entered. 0 = Manual mode; requires VBBR_REL_TRIG to be sequenced to enter release 1 = (Default) Automatic wait period based on VBBR_WAIT
24	VBBR_MUTE_EN	During the attack state, if the VBBR_MAX_ATT value is reached, the error condition still remains, and this bit is set, the output is muted. The output remains muted until the error condition has cleared and the VBST brownout prevention enters a releasing state. 0 = (Default) Mute disabled 1 = Mute enabled
23:21	VBBR_REL_RATE	Attenuation release step rate (tVBBR_REL). Configures the delay between consecutive volume attenuation release steps (VOLREL) when a brownout condition is no longer present and the VBST brownout prevention is in an attenuation release state. 000 = 5 ms 001 = 10 ms 010 = 25 ms 011 = 50 ms 100 = 100 ms 101 = (Default) 250 ms 110 = 500 ms 111 = 1000 ms
20:19	VBBR_WAIT	Configures the delay between a brownout condition no longer being present and the VBST brownout prevention entering an attenuation release state. 00 = 10 ms 01 = (Default) 100 ms 10 = 250 ms 11 = 500 ms
18:16	VBBR_ATK_RATE	Attenuation attack step rate (tVBBR_ATK). Configures the amount delay between consecutive volume attenuation steps (VOLATK) when a brownout condition is present and the VP brownout condition is in an attacking state. 000 = 2.5 µs 001 = 5 µs 010 = (Default) 10 µs 011 = 25 µs 100 = 50 µs 101 = 100 µs 110 = 250 µs 111 = 500 µs
15:12	VBBR_ATK_VOL	VBST brownout prevention attack step size. Configures the VBST brownout prevention attacking attenuation step size when operating in either digital volume or analog gain modes. Attenuation values listed are relative to triggering VBBR_THLD1 / $VBST_{BR\_2}$ / $VBST_{BR\_3}$ per attack time period (VBBR_ATK_RATE). 0000 = 0.0625 dB / 0.125 dB / 0.250 dB 0001 = (Default) 0.125 dB / 0.250 dB / 0.500 dB 0010 = 0.250 dB / 0.500 dB / 1.000 dB 0011 = 0.500 dB / 1.000 dB / 2.000 dB 0100 = 0.750 dB / 1.500 dB / 3.000 dB 0101 = 1.000 dB / 2.000 dB / 4.000 dB 0110 = 1.250 dB / 2.500 dB / 5.000 dB 0111 = 1.500 dB / 3.000 dB / 6.000 dB 1000–1111 = Reserved
11:8	VBBR_MAX_ATT	Maximum attenuation that the reactive VP brownout can apply to the signal. Even if an error condition remains present, the VBST brownout prevention only attenuates the signal up to the limit configured by VBBR_MAX_ATT. Step size: 1 dB. **Note:** VBBR_MAX_ATT should not be adjusted when attenuation is being applied by the VBST brownout prevention. 0000 = 0 dB 0001 = 1 dB 0010 = 2 dB … 1001 = (Default) 9 dB … 1110 = 14 dB 1111 = 15 dB

Bits	Name	Description
7:6	—	Reserved
5:0	VBBR_THLD1	VBST brownout prevention delta voltage threshold. Configures the VBST brownout voltage. VBST(target) – VBST(actual) <= threshold setting 000000–000001 = Reserved 000010 = 0.109 V 000011 = 0.164 V 000100 = 0.219 V 000101 = (Default) 0.273 V … 111110 = 3.391 V 111111 = 3.445 V

7.12.3 VPBR_STATUS

Address: 0x0000 640C

	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	—	—							VPBR_STATUS_MUTE	VPBR_STATUS							
Default	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:9	—	Reserved
8	VPBR_STATUS_MUTE	VP brownout prevention mute status. If VPBR_MUTE_EN is set and the reactive VP brownout has muted the output, this bit is set, indicating that the output has been muted.
7:0	VPBR_STATUS	Reports how much (if any) attenuation is applied to the output by the VP brownout prevention control. This field only reports 0 dB attenuation when no attenuation is being applied by the VP brownout prevention. Step size: 0.0625 dB 00000000 = (Default) 0.0 dB 00000001 = 0.0625 dB … 11101111 = 14.9375 dB 11110000 = 15.0 dB 11110001–11111111 = Reserved

7.12.4 VBBR_STATUS

Address: 0x0000 6410

	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	—	—							VBBR_STATUS_MUTE	VBBR_STATUS							
Default	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:9	—	Reserved
8	VBBR_STATUS_MUTE	VBST brownout prevention mute status (READ ONLY). If VBBR_MUTE_EN is set and the VBST brownout prevention has muted the output, this bit is set, indicating that the output has been muted.
7:0	VBBR_STATUS	Reports how much (if any) attenuation is applied to the output by the VBST brownout prevention control. This field only reports 0 dB attenuation when no attenuation is being applied by the VP brownout prevention. Step size: 0.0625 dB 00000000 = (Default) 0.0 dB 00000001 = 0.0625 dB … 11101111 = 14.9375 dB 11110000 = 15.0 dB 11110001–11111111 = Reserved

7.12.5 OTW_CONFIG

Address: 0x0000 6414

	31...8	7	6	5	4	3	2	1	0
RW	—	—						TEMP_WARN_VOL	
Default	0x00 0000	0	0	0	0	0	0	0	1

Bits	Name	Description
31:3	—	Reserved
2:0	TEMP_WARN_VOL	Overtemperature warning attenuation. Configures the digital volume attenuation of the amplifier that is applied to the signal in response to an overtemperature warning condition. This attenuation is applied until TEMP_WARN_RLS is sequenced and the overtemperature warning condition is no longer present. 000 = 0 dB (disabled) 001 = (Default) 3 dB 010 = 6 dB 011 = 9 dB 100–111 = Reserved

7.12.6 AMP_ERROR_VOL_SEL

Address: 0x0000 6418

RW	31...8	7	6	5	4	3	2	1	0
	—	—							AMP_ERR_VOL_SEL
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:1	—	Reserved
0	AMP_ERR_VOL_SEL	ERR_VOL source select. Configures the ERR_VOL attenuation to the amplifier to be sourced locally from the VP brownout prevention, VBST brownout prevention, and thermal warning. 0 = (Default) Only local ERR_VOL applied 1 = Rserved.

7.12.7 VOL_STATUS_TO_DSP

Address: 0x0000 6450

RO	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—														FINAL_ERROR_VOL										—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:18	—	Reserved
17:9	FINAL_ERROR_VOL	Final error volume.
8:0	—	Reserved

7.13 Power Management - Class H, Weak-FET, and Noise Gating (PWRMGMT)

7.13.1 CLASSH_CONFIG

Address: 0x0000 6800

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—								CH_HD_RM								CH_REL_RATE								—						CH_MEM_DEPTH	
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1

Bits	Name	Description
31:23	—	Reserved
22:16	CH_HD_RM	Class H algorithm headroom. Controls VBST headroom in the max detection path of the Class H algorithm. Step size: 0.1 V 0000000 = 0.0 V 0000001 = 0.1 V 0000010 = 0.2 V … 0001011 = (Default) 1.1 V … 0111110 = 6.2 V 0111111 = 6.3 V 1000000 = –6.4 V 1000001 = –6.3 V … 1111110 = –0.2 V 1111111 = –0.1 V
15:8	CH_REL_RATE	Class H release rate. Controls the amount of time required before allowing consecutive release condition VBST supply tracking updates. 00000000–00000011 = Reserved 00000100 = (Default) 20 µs 00000101 = 25 µs … 11111110 = 1,270 µs 11111111 = 1,275 µs
7:3	—	Reserved
2:0	CH_MEM_DEPTH	Class H memory depth. Controls the memory depth used in the Class H algorithm for data buffering and analysis. Listed configuration range is based on time and varies based on the memory update rate. 000 = 20.83 – 23.4 µs 001 = 41.67 – 46.88 µs 010 = 83.33 – 85.94 µs 011 = 166.67 – 171.88 µs 100 = 250.00 – 255.10 µs 101 = (Default) 333.33 – 335.93 µs 110–111 = Reserved

7.13.2 WKFET_AMP_CONFIG

Address: 0x0000 6804

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—				WKFET_AMP_THLD				—			WKFET_AMP_DLY			WKFET_AMP_FRC_EN	WKFET_AMP_FRC
Default	0x0000	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1

Bits	Name	Description
31:12	—	Reserved
11:8	WKFET_AMP_THLD	Weak-FET amplifier drive threshold. Configures the signal threshold at which the PWM output stage enters weak-FET operation. 0000 = Reserved 0001 = (Default) 0.05 V 0010 = 0.1 V 0011 = 0.15 V 0100 = 0.2 V 0101 = 0.25 V 0110 = 0.3 V 0111 = 0.35 V 1000 = 0.4 V 1001 = 0.45 V 1010 = 0.5 V 1011 = 0.55 V 1100 = 0.6 V 1101 = 0.65 V 1110 = 0.7 V 1111 = Reserved
7:5	—	Reserved
4:2	WKFET_AMP_DLY	Weak-FET entry delay. Controls the delay (in ms) before the Class H algorithm switches to the weak-FET voltage (after the signal falls and remains below the value specified in WKFET_AMP_THLD). 000 = 0 ms 001 = 5 ms 010 = 10 ms 011 = 50 ms 100 = (Default) 100 ms 101 = 200 ms 110 = 500 ms 111 = 1000 ms
1	WKFET_AMP_FRC_EN	Weak-FET amplifier force control enable. Enables the functionality of WKFET_AMP_FRC to manually force the amplifier to be configured into Weak-FET mode. 0 = (Default) WKFET_AMP_FORCE functionality disabled 1 = WKFET_AMP_FORCE functionality enabled
0	WKFET_AMP_FRC	Weak-FET amplifier mode force. Manually configures the amplifier into Weak-FET or normal operation mode when WKFET_AMP_FRC_EN is set. If WKFET_AMP_FORCE_EN is cleared, this register has no functionality. 0 = Amplifier power FETs are not manually put into weak-FET mode 1 = (Default) Amplifier power FETs are put into weak-FET mode

7.13.3 NG_CONFIG

Address: 0x0000 6808

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—		NG_EN_SEL						—	NG_DELAY			—	NG_PCM_THLD		
Default	0x0000	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1

Bits	Name	Description
31:14	—	Reserved
13:8	NG_EN_SEL	Amplifier noise gate enable mode selection. Configures whether the amplifier noise gating is enabled for the various blocks when the signal has been below the AMP_NG_THLD for a period of time configured by AMP_NG_DELAY. If any bit is enabled, the amplifier will stop switching when the source is below the threshold for the time configured. 000000 – All noise gating functionality disabled xxxxx1 – Amplifier noise gating detection enabled (OUT+/-; switching) xxxx1x – Boost converter DCM detection enabled xxx1xx – VMON low power mode detection enabled xx1xxx – IMON low power mode detection enabled x1xxxx – VP brownout prevention detection enabled 1xxxxx – VBST brownout prevention detection enabled
7	—	Reserved
6:4	NG_DELAY	Amplifier noise gate entry delay. Time that the signal must be below the NG_THLD prior to entering a noise gated state. 000 = 5 ms 001 = 10 ms 010 = 25 ms 011 = (Default) 50 ms 100 = 100 ms 101 = 250 ms 110 = 500 ms 111 = 1000 ms

Bits	Name	Description
3	—	Reserved
2:0	NG_PCM_THLD	Amplifier noise gate threshold. Threshold at which the amplifier's noise gating activates. Levels are output-referred. 000 = 0.654 mVpk 001 = 0.328 mVpk 010 = 0.164 mVpk 011 = (Default) 0.082 mVpk 100 = 0.041 mVpk 101 = 0.021 mVpk 110 = 0.010 mVpk 111 = True zero data (no LSB dither)

7.14 Dynamic Range Enhancement (DRE)

7.14.1 AMP_GAIN

Address: 0x0000 6C04

	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—	—					AMP_GAIN_ZC	AMP_GAIN_PCM						—			
Default	0x0000	0	0	0	0	0	0	1	0	0	1	1	1	0	0	1	1

Bits	Name	Description
31:11	—	Reserved
10	AMP_GAIN_ZC	Amplifier gain change at zero-cross. 0 = (Default) No zero cross 1 = Zero cross
9:5	AMP_GAIN_PCM	Amplifier analog gain. 00000 – 10010 Reserved 10011 19.5 dB 10100 – 11111 Reserved
4:0	—	Reserved

7.15 Interrupt Status and Mask Control (IRQ1)

7.15.1 IRQ1_CFG

Address: 0x0001 0000

	31...8	7	6	5	4	3	2	1	0
RW	—	—				IRQ1_DB_TIME			
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:4	—	Reserved
3:0	IRQ1_DB_TIME	Debounce time for IRQ Debouncer 0000 = (Default) x 8192 0001 = Default val x 16 0010 = Default val x 32 0011 = Default val x 64 0100 = Default val x 128 0101 = Default val x 256 0110 = Default val x 512 0111 = Default val x 1024 1000 = Default val x 2048 1001 = Default val x 4096 1010 = Default val x 8192 1011–1111 = Reserved

7.15.2 IRQ1_STATUS

Address: 0x0001 0004

	31...8	7	6	5	4	3	2	1	0
RO	—	—							IRQ1_STS1
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:1	—	Reserved
0	IRQ1_STS1	Status bit to indicate if the IRQ1 pin is currently asserted – useful flag to see if any other interrupts are pending.

7.15.3 IRQ1_EINT_1

Address: 0x0001 0010

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AMP_ERR_EINT1	VBBR_ATT_CLR_EINT1	VBBR_FLAG_EINT1	IMON_CLIPPED_EINT1	VMON_CLIPPED_EINT1	VBSTMON_CLIPPED_EINT1	VPMON_CLIPPED_EINT1	MSM_PUP_DONE_EINT1	MSM_PDN_DONE_EINT1	MSM_GLOBAL_EN_ASSERT_EINT1	—				TEMP_ERR_EINT1	TEMP_WARN_FALL_EINT1
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TEMP_WARN_RISE_EINT1	VPBR_ATT_CLR_EINT1	—	VPBR_FLAG_EINT1	REFCLK_STOP_EINT1	REFCLK_START_EINT1	BST_IPK_FLAG_EINT1	BST_SHORT_ERR_EINT1	BST_DCM_UVP_ERR_EINT1	BST_OVP_ERR_EINT1	BST_OVP_FLAG_FALL_EINT1	BST_OVP_FLAG_RISE_EINT1	GPIO2_FALL_EINT1	GPIO2_RISE_EINT1	GPIO1_FALL_EINT1	GPIO1_RISE_EINT1
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31	AMP_ERR_EINT1	Amplifier Short Error Interrupt Rising edge triggered. Write '1' to clear.
30	VBBR_ATT_CLR_EINT1	VBST Brownout Attenuation Cleared Interrupt Rising edge triggered. Write '1' to clear.
29	VBBR_FLAG_EINT1	VBST Brownout Threshold Flag Interrupt Rising edge triggered. Write '1' to clear.
28	IMON_CLIPPED_EINT1	IMON Overflow Error Interrupt Rising edge triggered. Write '1' to clear.
27	VMON_CLIPPED_EINT1	VMON Overflow Error Interrupt Rising edge triggered. Write '1' to clear.
26	VBSTMON_CLIPPED_EINT1	VBSTMON Overflow Error Interrupt Rising edge triggered. Write '1' to clear.
25	VPMON_CLIPPED_EINT1	VPMON Overflow Error Interrupt Rising edge triggered. Write '1' to clear.
24	MSM_PUP_DONE_EINT1	Global Power up Done Flag Interrupt Rising edge triggered. Write '1' to clear.
23	MSM_PDN_DONE_EINT1	Global Power down Done Flag Interrupt Rising edge triggered. Write '1' to clear.
22	MSM_GLOBAL_EN_ASSERT_EINT1	Global Enable Assert Flag Interrupt Rising edge triggered. Write '1' to clear.
21:18	—	Reserved
17	TEMP_ERR_EINT1	Overtemperature Error Interrupt Rising edge triggered. Write '1' to clear.
16	TEMP_WARN_FALL_EINT1	Overtemperature Warning Interrupt Falling edge triggered. Write '1' to clear.
15	TEMP_WARN_RISE_EINT1	Overtemperature Warning Interrupt Rising edge triggered. Write '1' to clear.
14	VPBR_ATT_CLR_EINT1	VP Brownout Attenuation Cleared Interrupt Rising edge triggered. Write '1' to clear.
13	—	Reserved
12	VPBR_FLAG_EINT1	VP Brownout Threshold Flag Interrupt Rising edge triggered. Write '1' to clear.
11	REFCLK_STOP_EINT1	DPLL Reference clock absence detected Interrupt Rising edge triggered. Write '1' to clear.
10	REFCLK_START_EINT1	DPLL Reference clock presence detected Interrupt Rising edge triggered. Write '1' to clear.
9	BST_IPK_FLAG_EINT1	Boost Peak Current Limit Flag Interrupt Rising edge triggered. Write '1' to clear.

Bits	Name	Description
8	BST_SHORT_ERR_EINT1	Boost Inductor Short Error Interrupt Rising edge triggered. Write '1' to clear.
7	BST_DCM_UVP_ERR_EINT1	Boost Undervoltage Error Interrupt Rising edge triggered. Write '1' to clear.
6	BST_OVP_ERR_EINT1	Boost Overvoltage Error Interrupt Rising edge triggered. Write '1' to clear.
5	BST_OVP_FLAG_FALL_EINT1	Boost Overvoltage Warning Interrupt Falling edge triggered. Write '1' to clear.
4	BST_OVP_FLAG_RISE_EINT1	Boost Overvoltage Warning Interrupt Rising edge triggered. Write '1' to clear.
3	GPIO2_FALL_EINT1	GPIO2 Pin Status Interrupt Falling edge triggered. Write '1' to clear.
2	GPIO2_RISE_EINT1	GPIO2 Pin Status Interrupt Rising edge triggered. Write '1' to clear.
1	GPIO1_FALL_EINT1	GPIO1 Pin Status Interrupt Falling edge triggered. Write '1' to clear.
0	GPIO1_RISE_EINT1	GPIO1 Pin Status Interrupt Rising edge triggered. Write '1' to clear.

7.15.4 IRQ1_EINT_2

Address: 0x0001 0014

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	—		AMP_NG_ON_FALL_EINT1	AMP_NG_ON_RISE_EINT1	—						DSP_VIRTUAL2_MBOX_WR_EINT1	DSP_VIRTUAL1_MBOX_WR_EINT1	—			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:30	—	Reserved
29	AMP_NG_ON_FALL_EINT1	Amplifier Noise Gate Entry Interrupt Falling edge triggered. Write '1' to clear.
28	AMP_NG_ON_RISE_EINT1	Amplifier Noise Gate Entry Interrupt Rising edge triggered. Write '1' to clear.
27:22	—	Reserved
21	DSP_VIRTUAL2_MBOX_WR_EINT1	DSP Virtual Mailbox 2 Write Flag Interrupt Rising edge triggered. Write '1' to clear.
20	DSP_VIRTUAL1_MBOX_WR_EINT1	DSP Virtual Mailbox 1 Write Flag Interrupt Rising edge triggered. Write '1' to clear.
19:0	—	Reserved

7.15.5 IRQ1_EINT_3

Address: 0x0001 0018

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—					ASP_RXSLOT_CFG_ERR_EINT1	ASP_TXSLOT_CFG_ERR_EINT1	REFCLK_IN_FLAG_FALL_EINT1	REFCLK_IN_FLAG_RISE_EINT1	—	PLL_UNLOCK_FLAG_FALL_EINT1	PLL_UNLOCK_FLAG_RISE_EINT1	PLL_FREQ_LOCK_EINT1	PLL_PHASE_LOCK_EINT1	PLL_LOCK_EINT1	INTP_VC_DONE_EINT1
Default	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:11	—	Reserved
10	ASP_RXSLOT_CFG_ERR_EINT1	ASP Rx Slot Configuration Error Interrupt Rising edge triggered. Write '1' to clear.
9	ASP_TXSLOT_CFG_ERR_EINT1	ASP Tx Slot Configuration Error Interrupt Rising edge triggered. Write '1' to clear.
8	REFCLK_IN_FLAG_FALL_EINT1	Input REFCLK Missing Flag Interrupt Falling edge triggered. Write '1' to clear.
7	REFCLK_IN_FLAG_RISE_EINT1	Input REFCLK Missing Flag Interrupt Rising edge triggered. Write '1' to clear.
6	—	Reserved
5	PLL_UNLOCK_FLAG_FALL_EINT1	PLL Unlock Flag Interrupt Falling edge triggered. Write '1' to clear.
4	PLL_UNLOCK_FLAG_RISE_EINT1	PLL Unlock Flag Interrupt Rising edge triggered. Write '1' to clear.
3	PLL_FREQ_LOCK_EINT1	PLL Frequency Lock Flag Interrupt Rising edge triggered. Write '1' to clear.
2	PLL_PHASE_LOCK_EINT1	PLL Phase Lock Flag Interrupt Rising edge triggered. Write '1' to clear.
1	PLL_LOCK_EINT1	PLL Lock Flag Interrupt Rising edge triggered. Write '1' to clear.
0	INTP_VC_DONE_EINT1	Amplifier Interpolator Volume Control Ramp Done Interrupt Rising edge triggered. Write '1' to clear.

7.15.6 IRQ1_EINT_4

Address: 0x0001 001C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	GPIO4_FALL_EINT1	GPIO4_RISE_EINT1	GPIO3_FALL_EINT1	GPIO3_RISE_EINT1	—			MEM_RD_EINT1	—						
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31	—	Reserved
30	GPIO4_FALL_EINT1	GPIO4 Pin Status Interrupt Falling edge triggered. Write '1' to clear.
29	GPIO4_RISE_EINT1	GPIO4 Pin Status Interrupt Rising edge triggered. Write '1' to clear.
28	GPIO3_FALL_EINT1	GPIO3 Pin Status Interrupt Falling edge triggered. Write '1' to clear.
27	GPIO3_RISE_EINT1	GPIO3 Pin Status Interrupt Rising edge triggered. Write '1' to clear.

Bits	Name	Description
26:24	—	Reserved
23	MEM_RD_EINT1	Memory Ready Interrupt Rising edge triggered. Write '1' to clear.
22:0	—	Reserved

7.15.7 IRQ1_STS_1

Address: 0x0001 0090

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RO	AMP_ERR_STS1	VBBR_ATT_CLR_STS1	VBBR_FLAG_STS1	IMON_CLIPPED_STS1	VMON_CLIPPED_STS1	VBSTMON_CLIPPED_STS1	VPMON_CLIPPED_STS1	MSM_PUP_DONE_STS1	MSM_PDN_DONE_STS1	MSM_GLOBAL_EN_ASSERT_STS1	—				TEMP_ERR_STS1	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	TEMP_WARN_STS1	VPBR_ATT_CLR_STS1	—	VPBR_FLAG_STS1	REFCLK_STOP_STS1	REFCLK_START_STS1	BST_IPK_FLAG_STS1	BST_SHORT_ERR_STS1	BST_DCM_UVP_ERR_STS1	BST_OVP_ERR_STS1	—	BST_OVP_FLAG_STS1	—	GPIO2_STS1	—	GPIO1_STS1
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31	AMP_ERR_STS1	Amplifier Short Error Status
30	VBBR_ATT_CLR_STS1	VBST Brownout Attenuation Cleared Status
29	VBBR_FLAG_STS1	VBST Brownout Threshold Flag Status
28	IMON_CLIPPED_STS1	IMON Overflow Error Status
27	VMON_CLIPPED_STS1	VMON Overflow Error Status
26	VBSTMON_CLIPPED_STS1	VBSTMON Overflow Error Status
25	VPMON_CLIPPED_STS1	VPMON Overflow Error Status
24	MSM_PUP_DONE_STS1	Global Power up Done Flag Status
23	MSM_PDN_DONE_STS1	Global Power down Done Flag Status
22	MSM_GLOBAL_EN_ASSERT_STS1	Global Enable Assert Flag Status
21:18	—	Reserved
17	TEMP_ERR_STS1	Overtemperature Error Status
16	—	Reserved
15	TEMP_WARN_STS1	Overtemperature Warning Status
14	VPBR_ATT_CLR_STS1	VP Brownout Attenuation Cleared Status
13	—	Reserved
12	VPBR_FLAG_STS1	VP Brownout Threshold Flag Status
11	REFCLK_STOP_STS1	DPLL Reference clock absence detected Status
10	REFCLK_START_STS1	DPLL Reference clock presence detected Status
9	BST_IPK_FLAG_STS1	Boost Peak Current Limit Flag Status
8	BST_SHORT_ERR_STS1	Boost Inductor Short Error Status

Bits	Name	Description
7	BST_DCM_UVP_ERR_STS1	Boost Undervoltage Error Status
6	BST_OVP_ERR_STS1	Boost Overvoltage Error Status
5	—	Reserved
4	BST_OVP_FLAG_STS1	Boost Overvoltage Warning Status
3	—	Reserved
2	GPIO2_STS1	GPIO2 Pin Interrupt Status
1	—	Reserved
0	GPIO1_STS1	GPIO1 Pin Interrupt Status

7.15.8 IRQ1_STS_2

Address: 0x0001 0094

RO	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—			AMP_NG_ON_STS1	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:29	—	Reserved
28	AMP_NG_ON_STS1	Amplifier Noise Gate Entry Status
27:0	—	Reserved

7.15.9 IRQ1_STS_3

Address: 0x0001 0098

RO	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—					ASP_RXSLOT_CFG_ERR_STS1	—		REFCLK_IN_FLAG_STS1	—		PLL_UNLOCK_FLAG_STS1	PLL_FREQ_LOCK_STS1	PLL_PHASE_LOCK_STS1	PLL_LOCK_STS1	INTP_VC_DONE_STS1
Default	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:11	—	Reserved
10	ASP_RXSLOT_CFG_ERR_STS1	ASP Rx Slot Configuration Error Status
9:8	—	Reserved
7	REFCLK_IN_FLAG_STS1	Input REFCLK Missing Flag Status
6:5	—	Reserved
4	PLL_UNLOCK_FLAG_STS1	PLL Unlock Flag Status
3	PLL_FREQ_LOCK_STS1	PLL Frequency Lock Status
2	PLL_PHASE_LOCK_STS1	PLL Phase Lock Status
1	PLL_LOCK_STS1	PLL Lock Status
0	INTP_VC_DONE_STS1	Amplifier Interpolator Volume Control Ramp Done Status

7.15.10 IRQ1_STS_4

Address: 0x0001 009C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RO	—		GPIO4_STS1	—	GPIO3_STS1	—			MEM_RD_STS1	—						
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:30	—	Reserved
29	GPIO4_STS1	GPIO4 Pin Interrupt Status
28	—	Reserved
27	GPIO3_STS1	GPIO3 Pin Interrupt Status
26:24	—	Reserved
23	MEM_RD_STS1	Memory Ready Status
22:0	—	Reserved

7.15.11 IRQ1_MASK_1

Address: 0x0001 0110

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	AMP_ERR_MASK1	VBBR_ATT_CLR_MASK1	VBBR_FLAG_MASK1	IMON_CLIPPED_MASK1	VMON_CLIPPED_MASK1	VBSTMON_CLIPPED_MASK1	VPMON_CLIPPED_MASK1	MSM_PUP_DONE_MASK1	MSM_PDN_DONE_MASK1	MSM_GLOBAL_EN_ASSERT_MASK1	—				TEMP_ERR_MASK1	TEMP_WARN_FALL_MASK1
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	TEMP_WARN_RISE_MASK1	VPBR_ATT_CLR_MASK1	—	VPBR_FLAG_MASK1	REFCLK_STOP_MASK1	REFCLK_START_MASK1	BST_IPK_FLAG_MASK1	BST_SHORT_ERR_MASK1	BST_DCM_UVP_ERR_MASK1	BST_OVP_ERR_MASK1	BST_OVP_FLAG_FALL_MASK1	BST_OVP_FLAG_RISE_MASK1	GPIO2_FALL_MASK1	GPIO2_RISE_MASK1	GPIO1_FALL_MASK1	GPIO1_RISE_MASK1
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description
31	AMP_ERR_MASK1	Amplifier Short Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
30	VBBR_ATT_CLR_MASK1	VBST Brownout Attenuation Cleared Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
29	VBBR_FLAG_MASK1	VBST Brownout Threshold Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
28	IMON_CLIPPED_MASK1	IMON Overflow Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
27	VMON_CLIPPED_MASK1	VMON Overflow Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
26	VBSTMON_CLIPPED_MASK1	VBSTMON Overflow Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
25	VPMON_CLIPPED_MASK1	VPMON Overflow Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt

Bits	Name	Description
24	MSM_PUP_DONE_MASK1	Global Power up Done Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
23	MSM_PDN_DONE_MASK1	Global Power down Done Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
22	MSM_GLOBAL_EN_ASSERT_MASK1	Global Enable Assert Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
21:18	—	Reserved
17	TEMP_ERR_MASK1	Overtemperature Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
16	TEMP_WARN_FALL_MASK1	Overtemperature Warning Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
15	TEMP_WARN_RISE_MASK1	Overtemperature Warning Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
14	VPBR_ATT_CLR_MASK1	VP Brownout Attenuation Cleared Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
13	—	Reserved
12	VPBR_FLAG_MASK1	VP Brownout Threshold Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
11	REFCLK_STOP_MASK1	DPLL Reference clock absence detected Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
10	REFCLK_START_MASK1	DPLL Reference clock presence detected Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
9	BST_IPK_FLAG_MASK1	Boost Peak Current Limit Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
8	BST_SHORT_ERR_MASK1	Boost Inductor Short Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
7	BST_DCM_UVP_ERR_MASK1	Boost Undervoltage Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
6	BST_OVP_ERR_MASK1	Boost Overvoltage Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
5	BST_OVP_FLAG_FALL_MASK1	Boost Overvoltage Warning Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
4	BST_OVP_FLAG_RISE_MASK1	Boost Overvoltage Warning Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
3	GPIO2_FALL_MASK1	GPIO2 Pin Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt

Bits	Name	Description
2	GPIO2_RISE_MASK1	GPIO2 Pin Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
1	GPIO1_FALL_MASK1	GPIO1 Pin Interrupt Status Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
0	GPIO1_RISE_MASK1	GPIO1 Pin Interrupt Status Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt

7.15.12 IRQ1_MASK_2

Address: 0x0001 0114

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW																
	—		AMP_NG_ON_FALL_MASK1	AMP_NG_ON_RISE_MASK1	—											
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																
	—															
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description
31:30	—	Reserved
29	AMP_NG_ON_FALL_MASK1	Amplifier Noise Gate Entry Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
28	AMP_NG_ON_RISE_MASK1	Amplifier Noise Gate Entry Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
27:0	—	Reserved

7.15.13 IRQ1_MASK_3

Address: 0x0001 0118

	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW																	
	—	—					ASP_RXSLOT_CFG_ERR_MASK1	—	REFCLK_IN_FLAG_FALL_MASK1	REFCLK_IN_FLAG_RISE_MASK1	—	PLL_UNLOCK_FLAG_FALL_MASK1	PLL_UNLOCK_FLAG_RISE_MASK1	PLL_FREQ_LOCK_MASK1	PLL_PHASE_LOCK_MASK1	PLL_LOCK_MASK1	INTP_VC_DONE_MASK1
Default	0xFFFF	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description
31:11	—	Reserved
10	ASP_RXSLOT_CFG_ERR_MASK1	ASP Rx Slot Configuration Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
9	—	Reserved
8	REFCLK_IN_FLAG_FALL_MASK1	Input REFCLK Missing Flag Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
7	REFCLK_IN_FLAG_RISE_MASK1	Input REFCLK Missing Flag Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
6	—	Reserved
5	PLL_UNLOCK_FLAG_FALL_MASK1	PLL Unlock Flag Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt

Bits	Name	Description
4	PLL_UNLOCK_FLAG_RISE_MASK1	PLL Unlock Flag Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
3	PLL_FREQ_LOCK_MASK1	PLL Frequency Lock Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
2	PLL_PHASE_LOCK_MASK1	PLL Phase Lock Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
1	PLL_LOCK_MASK1	PLL Lock Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
0	INTP_VC_DONE_MASK1	Amplifier Interpolator Volume Control Ramp Done Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt

7.15.14 IRQ1_MASK_4

Address: 0x0001 011C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	—	GPIO4_FALL_MASK1	GPIO4_RISE_MASK1	GPIO3_FALL_MASK1	GPIO3_RISE_MASK1	—			MEM_RD_MASK1	—						
Default	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—															
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description
31	—	Reserved
30	GPIO4_FALL_MASK1	GPIO4 Pin Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
29	GPIO4_RISE_MASK1	GPIO4 Pin Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
28	GPIO3_FALL_MASK1	GPIO3 Pin Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
27	GPIO3_RISE_MASK1	GPIO3 Pin Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
26:24	—	Reserved
23	MEM_RD_MASK1	Memory Ready Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
22:0	—	Reserved

7.15.15 IRQ1_EDGE_1

Address: 0x0001 0210

RW	31...8	7	6	5	4	3	2	1	0
	—	—				GPIO2_FALL_EDGE1	GPIO2_RISE_EDGE1	GPIO1_FALL_EDGE1	GPIO1_RISE_EDGE1
Default	0x00 0000	0	0	0	0	1	1	1	1

Bits	Name	Description
31:4	—	Reserved
3	GPIO2_FALL_EDGE1	GPIO2 Pin Falling Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
2	GPIO2_RISE_EDGE1	GPIO2 Pin Rising Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
1	GPIO1_FALL_EDGE1	GPIO1 Pin Falling Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
0	GPIO1_RISE_EDGE1	GPIO1 Pin Rising Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive

7.15.16 IRQ1_EDGE_4

Address: 0x0001 021C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	GPIO4_FALL_EDGE1	GPIO4_RISE_EDGE1	GPIO3_FALL_EDGE1	GPIO3_RISE_EDGE1	—										
Default	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31	—	Reserved
30	GPIO4_FALL_EDGE1	GPIO4 Pin Falling Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
29	GPIO4_RISE_EDGE1	GPIO4 Pin Rising Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
28	GPIO3_FALL_EDGE1	GPIO3 Pin Falling Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
27	GPIO3_RISE_EDGE1	GPIO3 Pin Rising Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
26:0	—	Reserved

7.15.17 IRQ1_POL_1

Address: 0x0001 0290

	31...8	7	6	5	4	3	2	1	0
RW	—	—				GPIO2_FALL_POL1	GPIO2_RISE_POL1	GPIO1_FALL_POL1	GPIO1_RISE_POL1
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:4	—	Reserved
3	GPIO2_FALL_POL1	GPIO2 Pin Interrupt Status Fall Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
2	GPIO2_RISE_POL1	GPIO2 Pin Interrupt Status Rise Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
1	GPIO1_FALL_POL1	GPIO1 Pin Interrupt Status Fall Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
0	GPIO1_RISE_POL1	GPIO1 Pin Interrupt Status Rise Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity

7.15.18 IRQ1_POL_4

Address: 0x0001 029C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	—	GPIO4_FALL_POL1	GPIO4_RISE_POL1	GPIO3_FALL_POL1	GPIO3_RISE_POL1	—										
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31	—	Reserved
30	GPIO4_FALL_POL1	GPIO4 Pin Falling Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
29	GPIO4_RISE_POL1	GPIO4 Pin Rising Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
28	GPIO3_FALL_POL1	GPIO3 Pin Falling Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
27	GPIO3_RISE_POL1	GPIO3 Pin Rising Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
26:0	—	Reserved

7.15.19 IRQ1_DB_3

Address: 0x0001 0318

	31...8	7	6	5	4	3	2	1	0
RW	—	REFCLK_IN_FLAG_DB1				—			
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:8	—	Reserved
7	REFCLK_IN_FLAG_DB1	Input REFCLK Missing Flag Debounce Enable 0 = (Default) Debounce Disabled 1 = Debounce Enabled
6:0	—	Reserved

7.16 Interrupt Status and Mask Control (IRQ2)

7.16.1 IRQ2_CFG

Address: 0x0001 0800

	31...8	7	6	5	4	3	2	1	0
RW	—	—				IRQ2_DB_TIME			
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:4	—	Reserved
3:0	IRQ2_DB_TIME	Debounce time for IRQ Debouncer 0000 = (Default) x 8192 0001 = Default val x 16 0010 = Default val x 32 0011 = Default val x 64 0100 = Default val x 128 0101 = Default val x 256 0110 = Default val x 512 0111 = Default val x 1024 1000 = Default val x 2048 1001 = Default val x 4096 1010 = Default val x 8192 1011–1111 = Reserved

7.16.2 IRQ2_STATUS

Address: 0x0001 0804

	31...8	7	6	5	4	3	2	1	0
RO	—				—				IRQ2_STS2
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:1	—	Reserved
0	IRQ2_STS2	Status bit to indicate if the IRQ2 pin is currently asserted – useful flag to see if any other interrupts are pending.

7.16.3 IRQ2_EINT_1

Address: 0x0001 0810

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AMP_ERR_EINT2	VBBR_ATT_CLR_EINT2	VBBR_FLAG_EINT2	IMON_CLIPPED_EINT2	VMON_CLIPPED_EINT2	VBSTMON_CLIPPED_EINT2	VPMON_CLIPPED_EINT2	MSM_PUP_DONE_EINT2	MSM_PDN_DONE_EINT2	MSM_GLOBAL_EN_ASSERT_EINT2	—				TEMP_ERR_EINT2	TEMP_WARN_FALL_EINT2
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TEMP_WARN_RISE_EINT2	VPBR_ATT_CLR_EINT2	—	VPBR_FLAG_EINT2	REFCLK_STOP_EINT2	REFCLK_START_EINT2	BST_IPK_FLAG_EINT2	BST_SHORT_ERR_EINT2	BST_DCM_UVP_ERR_EINT2	BST_OVP_ERR_EINT2	BST_OVP_FLAG_FALL_EINT2	BST_OVP_FLAG_RISE_EINT2	GPIO2_FALL_EINT2	GPIO2_RISE_EINT2	GPIO1_FALL_EINT2	GPIO1_RISE_EINT2
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31	AMP_ERR_EINT2	Amplifier Short Error Interrupt Rising edge triggered. Write '1' to clear.
30	VBBR_ATT_CLR_EINT2	VBST Brownout Attenuation Cleared Interrupt Rising edge triggered. Write '1' to clear.
29	VBBR_FLAG_EINT2	VBST Brownout Threshold Flag Interrupt Rising edge triggered. Write '1' to clear.
28	IMON_CLIPPED_EINT2	IMON Overflow Error Interrupt Rising edge triggered. Write '1' to clear.
27	VMON_CLIPPED_EINT2	VMON Overflow Error Interrupt Rising edge triggered. Write '1' to clear.
26	VBSTMON_CLIPPED_EINT2	VBSTMON Overflow Error Interrupt Rising edge triggered. Write '1' to clear.
25	VPMON_CLIPPED_EINT2	VPMON Overflow Error Interrupt Rising edge triggered. Write '1' to clear.
24	MSM_PUP_DONE_EINT2	Global Power up Done Flag Interrupt Rising edge triggered. Write '1' to clear.
23	MSM_PDN_DONE_EINT2	Global Power down Done Flag Interrupt Rising edge triggered. Write '1' to clear.
22	MSM_GLOBAL_EN_ASSERT_EINT2	Global Enable Assert Flag Interrupt Rising edge triggered. Write '1' to clear.
21:18	—	Reserved
17	TEMP_ERR_EINT2	Overtemperature Error Interrupt Rising edge triggered. Write '1' to clear.
16	TEMP_WARN_FALL_EINT2	Overtemperature Warning Interrupt Falling edge triggered. Write '1' to clear.
15	TEMP_WARN_RISE_EINT2	Overtemperature Warning Interrupt Rising edge triggered. Write '1' to clear.
14	VPBR_ATT_CLR_EINT2	VP Brownout Attenuation Cleared Interrupt Rising edge triggered. Write '1' to clear.
13	—	Reserved
12	VPBR_FLAG_EINT2	VP Brownout Threshold Flag Interrupt Rising edge triggered. Write '1' to clear.
11	REFCLK_STOP_EINT2	DPLL Reference clock absence detected Interrupt Rising edge triggered. Write '1' to clear.
10	REFCLK_START_EINT2	DPLL Reference clock presence detected Interrupt Rising edge triggered. Write '1' to clear.
9	BST_IPK_FLAG_EINT2	Boost Peak Current Limit Flag Interrupt Rising edge triggered. Write '1' to clear.

Bits	Name	Description
8	BST_SHORT_ERR_EINT2	Boost Inductor Short Error Interrupt Rising edge triggered. Write '1' to clear.
7	BST_DCM_UVP_ERR_EINT2	Boost Undervoltage Error Interrupt Rising edge triggered. Write '1' to clear.
6	BST_OVP_ERR_EINT2	Boost Overvoltage Error Interrupt Rising edge triggered. Write '1' to clear.
5	BST_OVP_FLAG_FALL_EINT2	Boost Overvoltage Warning Interrupt Falling edge triggered. Write '1' to clear.
4	BST_OVP_FLAG_RISE_EINT2	Boost Overvoltage Warning Interrupt Rising edge triggered. Write '1' to clear.
3	GPIO2_FALL_EINT2	GPIO2 Pin Interrupt Status Interrupt Falling edge triggered. Write '1' to clear.
2	GPIO2_RISE_EINT2	GPIO2 Pin Interrupt Status Interrupt Rising edge triggered. Write '1' to clear.
1	GPIO1_FALL_EINT2	GPIO1 Pin Interrupt Status Interrupt Falling edge triggered. Write '1' to clear.
0	GPIO1_RISE_EINT2	GPIO1 Pin Interrupt Status Interrupt Rising edge triggered. Write '1' to clear.

7.16.4 IRQ2_EINT_2

Address: 0x0001 0814

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	—		AMP_NG_ON_FALL_EINT2	AMP_NG_ON_RISE_EINT2	—						DSP_VIRTUAL2_MBOX_WR_EINT2	DSP_VIRTUAL1_MBOX_WR_EINT2	—			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:30	—	Reserved
29	AMP_NG_ON_FALL_EINT2	Amplifier Noise Gate Entry Interrupt Falling edge triggered. Write '1' to clear.
28	AMP_NG_ON_RISE_EINT2	Amplifier Noise Gate Entry Interrupt Rising edge triggered. Write '1' to clear.
27:22	—	Reserved
21	DSP_VIRTUAL2_MBOX_WR_EINT2	DSP Virtual Mailbox 2 Write Flag Interrupt Rising edge triggered. Write '1' to clear.
20	DSP_VIRTUAL1_MBOX_WR_EINT2	DSP Virtual Mailbox 1 Write Flag Interrupt Rising edge triggered. Write '1' to clear.
19:0	—	Reserved

7.16.5 IRQ2_EINT_3

Address: 0x0001 0818

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—					ASP_RXSLOT_CFG_ERR_EINT2	—	REFCLK_IN_FLAG_FALL_EINT2	REFCLK_IN_FLAG_RISE_EINT2	—	PLL_UNLOCK_FLAG_FALL_EINT2	PLL_UNLOCK_FLAG_RISE_EINT2	PLL_FREQ_LOCK_EINT2	PLL_PHASE_LOCK_EINT2	PLL_LOCK_EINT2	INTP_VC_DONE_EINT2
Default	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:11	—	Reserved
10	ASP_RXSLOT_CFG_ERR_EINT2	ASP Rx Slot Configuration Error Interrupt Rising edge triggered. Write '1' to clear.
9	—	Reserved
8	REFCLK_IN_FLAG_FALL_EINT2	Input REFCLK Missing Flag Interrupt Falling edge triggered. Write '1' to clear.
7	REFCLK_IN_FLAG_RISE_EINT2	Input REFCLK Missing Flag Interrupt Rising edge triggered. Write '1' to clear.
6	—	Reserved
5	PLL_UNLOCK_FLAG_FALL_EINT2	PLL Unlock Flag Interrupt Falling edge triggered. Write '1' to clear.
4	PLL_UNLOCK_FLAG_RISE_EINT2	PLL Unlock Flag Interrupt Rising edge triggered. Write '1' to clear.
3	PLL_FREQ_LOCK_EINT2	PLL Frequency Lock Flag Interrupt Rising edge triggered. Write '1' to clear.
2	PLL_PHASE_LOCK_EINT2	PLL Phase Lock Flag Interrupt Rising edge triggered. Write '1' to clear.
1	PLL_LOCK_EINT2	PLL Lock Flag Interrupt Rising edge triggered. Write '1' to clear.
0	INTP_VC_DONE_EINT2	Amplifier Interpolator Volume Control Ramp Done Interrupt Rising edge triggered. Write '1' to clear.

7.16.6 IRQ2_EINT_4

Address: 0x0001 081C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	GPIO4_FALL_EINT2	GPIO4_RISE_EINT2	GPIO3_FALL_EINT2	GPIO3_RISE_EINT2	—			MEM_RD_EINT2	—						
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31	—	Reserved
30	GPIO4_FALL_EINT2	GPIO4 Pin Falling Edge Interrupt Rising edge triggered. Write '1' to clear.
29	GPIO4_RISE_EINT2	GPIO4 Pin Rising Edge Interrupt Rising edge triggered. Write '1' to clear.
28	GPIO3_FALL_EINT2	GPIO3 Pin Falling Edge Interrupt Falling edge triggered. Write '1' to clear.
27	GPIO3_RISE_EINT2	GPIO3 Pin Rising Edge Interrupt Rising edge triggered. Write '1' to clear.

Bits	Name	Description
26:24	—	Reserved
23	MEM_RD_EINT2	Memory Ready Interrupt Rising edge triggered. Write '1' to clear.
22:0	—	Reserved

7.16.7 IRQ2_STS_1

Address: 0x0001 0890

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RO	AMP_ERR_STS2	VBBR_ATT_CLR_STS2	VBBR_FLAG_STS2	IMON_CLIPPED_STS2	VMON_CLIPPED_STS2	VBSTMON_CLIPPED_STS2	VPMON_CLIPPED_STS2	MSM_PUP_DONE_STS2	MSM_PDN_DONE_STS2	MSM_GLOBAL_EN_ASSERT_STS2	—				TEMP_ERR_STS2	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	TEMP_WARN_STS2	VPBR_ATT_CLR_STS2	—	VPBR_FLAG_STS2	REFCLK_STOP_STS2	REFCLK_START_STS2	BST_IPK_FLAG_STS2	BST_SHORT_ERR_STS2	BST_DCM_UVP_ERR_STS2	BST_OVP_ERR_STS2	—	BST_OVP_FLAG_STS2	—	GPIO2_STS2	—	GPIO1_STS2
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31	AMP_ERR_STS2	Amplifier Short Error Status
30	VBBR_ATT_CLR_STS2	VBST Brownout Attenuation Cleared Status
29	VBBR_FLAG_STS2	VBST Brownout Threshold Flag Status
28	IMON_CLIPPED_STS2	IMON Overflow Error Status
27	VMON_CLIPPED_STS2	VMON Overflow Error Status
26	VBSTMON_CLIPPED_STS2	VBSTMON Overflow Error Status
25	VPMON_CLIPPED_STS2	VPMON Overflow Error Status
24	MSM_PUP_DONE_STS2	Global Power up Done Flag Status
23	MSM_PDN_DONE_STS2	Global Power down Done Flag Status
22	MSM_GLOBAL_EN_ASSERT_STS2	Global Enable Assert Flag Status
21:18	—	Reserved
17	TEMP_ERR_STS2	Overtemperature Error Status
16	—	Reserved
15	TEMP_WARN_STS2	Overtemperature Warning Status
14	VPBR_ATT_CLR_STS2	VP Brownout Attenuation Cleared Status
13	—	Reserved
12	VPBR_FLAG_STS2	VP Brownout Threshold Flag Status
11	REFCLK_STOP_STS2	DPLL Reference clock absence detected Status
10	REFCLK_START_STS2	DPLL Reference clock presence detected Status
9	BST_IPK_FLAG_STS2	Boost Peak Current Limit Flag Status
8	BST_SHORT_ERR_STS2	Boost Inductor Short Error Status

Bits	Name	Description
7	BST_DCM_UVP_ERR_STS2	Boost Undervoltage Error Status
6	BST_OVP_ERR_STS2	Boost Overvoltage Error Status
5	—	Reserved
4	BST_OVP_FLAG_STS2	Boost Overvoltage Warning Status
3	—	Reserved
2	GPIO2_STS2	GPIO2 Pin Interrupt Status
1	—	Reserved
0	GPIO1_STS2	GPIO1 Pin Interrupt Status

7.16.8 IRQ2_STS_2

Address: 0x0001 0894

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RO		—		AMP_NG_ON_STS2						—						
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO								—								
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:29	—	Reserved
28	AMP_NG_ON_STS2	Amplifier Noise Gate Entry Status
27:0	—	Reserved

7.16.9 IRQ2_STS_3

Address: 0x0001 0898

	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	—	—					ASP_RXSLOT_CFG_ERR_STS2	ASP_TXSLOT_CFG_ERR_STS2	—	REFCLK_IN_FLAG_STS2	—		PLL_UNLOCK_FLAG_STS2	PLL_FREQ_LOCK_STS2	PLL_PHASE_LOCK_STS2	PLL_LOCK_STS2	INTP_VC_DONE_STS2
Default	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:11	—	Reserved
10	ASP_RXSLOT_CFG_ERR_STS2	ASP Rx Slot Configuration Error Status
9	ASP_TXSLOT_CFG_ERR_STS2	ASP Tx Slot Configuration Error Status
8	—	Reserved
7	REFCLK_IN_FLAG_STS2	Input REFCLK Missing Flag Status
6:5	—	Reserved
4	PLL_UNLOCK_FLAG_STS2	PLL Unlock Flag Status
3	PLL_FREQ_LOCK_STS2	PLL Frequency Lock Status
2	PLL_PHASE_LOCK_STS2	PLL Phase Lock Status
1	PLL_LOCK_STS2	PLL Lock Status
0	INTP_VC_DONE_STS2	Amplifier Interpolator Volume Control Ramp Done Status

7.16.10 IRQ2_STS_4

Address: 0x0001 089C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RO	—		GPIO4_STS2	—	GPIO3_STS2	—			MEM_RD_STS2	—						
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:30	—	Reserved
29	GPIO4_STS2	GPIO4 Pin Status
28	—	Reserved
27	GPIO3_STS2	GPIO3 Pin Status
26:24	—	Reserved
23	MEM_RD_STS2	Memory Ready Status
22:0	—	Reserved

7.16.11 IRQ2_MASK_1

Address: 0x0001 0910

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	AMP_ERR_MASK2	VBBR_ATT_CLR_MASK2	VBBR_FLAG_MASK2	IMON_CLIPPED_MASK2	VMON_CLIPPED_MASK2	VBSTMON_CLIPPED_MASK2	VPMON_CLIPPED_MASK2	MSM_PUP_DONE_MASK2	MSM_PDN_DONE_MASK2	MSM_GLOBAL_EN_ASSERT_MASK2	—				TEMP_ERR_MASK2	TEMP_WARN_FALL_MASK2
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	TEMP_WARN_RISE_MASK2	VPBR_ATT_CLR_MASK2	—	VPBR_FLAG_MASK2	REFCLK_STOP_MASK2	REFCLK_START_MASK2	BST_IPK_FLAG_MASK2	BST_SHORT_ERR_MASK2	BST_DCM_UVP_ERR_MASK2	BST_OVP_ERR_MASK2	BST_OVP_FLAG_FALL_MASK2	BST_OVP_FLAG_RISE_MASK2	GPIO2_FALL_MASK2	GPIO2_RISE_MASK2	GPIO1_FALL_MASK2	GPIO1_RISE_MASK2
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description
31	AMP_ERR_MASK2	Amplifier Short Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
30	VBBR_ATT_CLR_MASK2	VBST Brownout Attenuation Cleared Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
29	VBBR_FLAG_MASK2	VBST Brownout Threshold Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
28	IMON_CLIPPED_MASK2	IMON Overflow Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
27	VMON_CLIPPED_MASK2	VMON Overflow Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
26	VBSTMON_CLIPPED_MASK2	VBSTMON Overflow Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
25	VPMON_CLIPPED_MASK2	VPMON Overflow Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt

Bits	Name	Description
24	MSM_PUP_DONE_MASK2	Global Power up Done Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
23	MSM_PDN_DONE_MASK2	Global Power down Done Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
22	MSM_GLOBAL_EN_ASSERT_MASK2	Global Enable Assert Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
21:18	—	Reserved
17	TEMP_ERR_MASK2	Overtemperature Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
16	TEMP_WARN_FALL_MASK2	Overtemperature Warning Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
15	TEMP_WARN_RISE_MASK2	Overtemperature Warning Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
14	VPBR_ATT_CLR_MASK2	VP Brownout Attenuation Cleared Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
13	—	Reserved
12	VPBR_FLAG_MASK2	VP Brownout Threshold Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
11	REFCLK_STOP_MASK2	DPLL Reference clock absence detected Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
10	REFCLK_START_MASK2	DPLL Reference clock presence detected Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
9	BST_IPK_FLAG_MASK2	Boost Peak Current Limit Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
8	BST_SHORT_ERR_MASK2	Boost Inductor Short Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
7	BST_DCM_UVP_ERR_MASK2	Boost Undervoltage Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
6	BST_OVP_ERR_MASK2	Boost Overvoltage Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
5	BST_OVP_FLAG_FALL_MASK2	Boost Overvoltage Warning Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
4	BST_OVP_FLAG_RISE_MASK2	Boost Overvoltage Warning Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
3	GPIO2_FALL_MASK2	GPIO2 Pin Interrupt Status Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt

Bits	Name	Description
2	GPIO2_RISE_MASK2	GPIO2 Pin Interrupt Status Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
1	GPIO1_FALL_MASK2	GPIO1 Pin Interrupt Status Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
0	GPIO1_RISE_MASK2	GPIO1 Pin Interrupt Status Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt

7.16.12 IRQ2_MASK_2

Address: 0x0001 0914

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—		AMP_NG_ON_FALL_MASK2	AMP_NG_ON_RISE_MASK2	—						DSP_VIRTUAL2_MBOX_WR_MASK2	DSP_VIRTUAL1_MBOX_WR_MASK2	—			
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description
31:30	—	Reserved
29	AMP_NG_ON_FALL_MASK2	Amplifier Noise Gate Entry Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
28	AMP_NG_ON_RISE_MASK2	Amplifier Noise Gate Entry Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
27:22	—	Reserved
21	DSP_VIRTUAL2_MBOX_WR_MASK2	DSP Virtual Mailbox 2 Write Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
20	DSP_VIRTUAL1_MBOX_WR_MASK2	DSP Virtual Mailbox 1 Write Flag Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
19:0	—	Reserved

7.16.13 IRQ2_MASK_3

Address: 0x0001 0918

RW	31...16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—					ASP_RXSLOT_CFG_ERR_MASK2	ASP_TXSLOT_CFG_ERR_MASK2	REFCLK_IN_FLAG_FALL_MASK2	REFCLK_IN_FLAG_RISE_MASK2	—	PLL_UNLOCK_FLAG_FALL_MASK2	PLL_UNLOCK_FLAG_RISE_MASK2	PLL_FREQ_LOCK_MASK2	PLL_PHASE_LOCK_MASK2	PLL_LOCK_MASK2	INTP_VC_DONE_MASK2
Default	0xFFFF	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description
31:11	—	Reserved
10	ASP_RXSLOT_CFG_ERR_MASK2	ASP Rx Slot Configuration Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
9	ASP_TXSLOT_CFG_ERR_MASK2	ASP Tx Slot Configuration Error Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt

Bits	Name	Description
8	REFCLK_IN_FLAG_FALL_MASK2	Input REFCLK Missing Flag Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
7	REFCLK_IN_FLAG_RISE_MASK2	Input REFCLK Missing Flag Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
6	—	Reserved
5	PLL_UNLOCK_FLAG_FALL_MASK2	PLL Unlock Flag Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
4	PLL_UNLOCK_FLAG_RISE_MASK2	PLL Unlock Flag Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
3	PLL_FREQ_LOCK_MASK2	PLL Frequency Lock Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
2	PLL_PHASE_LOCK_MASK2	PLL Phase Lock Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
1	PLL_LOCK_MASK2	PLL Lock Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
0	INTP_VC_DONE_MASK2	Amplifier Interpolator Volume Control Ramp Done Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt

7.16.14 IRQ2_MASK_4

Address: 0x0001 091C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	GPIO4_FALL_MASK2	GPIO4_RISE_MASK2	GPIO3_FALL_MASK2	GPIO3_RISE_MASK2	—			MEM_RD_MASK2	—						
Default	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Name	Description
31	—	Reserved
30	GPIO4_FALL_MASK2	GPIO4 Pin Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
29	GPIO4_RISE_MASK2	GPIO4 Pin Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
28	GPIO3_FALL_MASK2	GPIO3 Pin Falling Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
27	GPIO3_RISE_MASK2	GPIO3 Pin Rising Edge Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
26:24	—	Reserved
23	MEM_RD_MASK2	Memory Ready Interrupt Mask 0 = Do not mask interrupt 1 = (Default) Mask interrupt
22:0	—	Reserved

7.16.15 IRQ2_EDGE_1

Address: 0x0001 0A10

	31...8	7	6	5	4	3	2	1	0
RW	—	—				GPIO2_FALL_EDGE2	GPIO2_RISE_EDGE2	GPIO1_FALL_EDGE2	GPIO1_RISE_EDGE2
Default	0x00 0000	0	0	0	0	1	1	1	1

Bits	Name	Description
31:4	—	Reserved
3	GPIO2_FALL_EDGE2	GPIO2 Pin Falling Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
2	GPIO2_RISE_EDGE2	GPIO2 Pin Rising Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
1	GPIO1_FALL_EDGE2	GPIO1 Pin Falling Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
0	GPIO1_RISE_EDGE2	GPIO1 Pin Rising Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive

7.16.16 IRQ2_EDGE_4

Address: 0x0001 0A1C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	—	GPIO4_FALL_EDGE2	GPIO4_RISE_EDGE2	GPIO3_FALL_EDGE2	GPIO3_RISE_EDGE2	—										
Default	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31	—	Reserved
30	GPIO4_FALL_EDGE2	GPIO4 Pin Falling Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
29	GPIO4_RISE_EDGE2	GPIO4 Pin Rising Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
28	GPIO3_FALL_EDGE2	GPIO3 Pin Falling Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
27	GPIO3_RISE_EDGE2	GPIO3 Pin Rising Interrupt Edge/Level Select 0 = Level sensitive 1 = (Default) Edge sensitive
26:0	—	Reserved

7.16.17 IRQ2_POL_1

Address: 0x0001 0A90

	31...8	7	6	5	4	3	2	1	0
RW	—	—				GPIO2_FALL_POL2	GPIO2_RISE_POL2	GPIO1_FALL_POL2	GPIO1_RISE_POL2
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:4	—	Reserved
3	GPIO2_FALL_POL2	GPIO2 Pin Falling Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
2	GPIO2_RISE_POL2	GPIO2 Pin Rising Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
1	GPIO1_FALL_POL2	GPIO1 Pin Falling Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
0	GPIO1_RISE_POL2	GPIO1 Pin Rising Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity

7.16.18 IRQ2_POL_4

Address: 0x0001 0A9C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	—	GPIO4_FALL_POL2	GPIO4_RISE_POL2	GPIO3_FALL_POL2	GPIO3_RISE_POL2	—										
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	—															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31	—	Reserved
30	GPIO4_FALL_POL2	GPIO4 Pin Falling Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
29	GPIO4_RISE_POL2	GPIO4 Pin Rising Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
28	GPIO3_FALL_POL2	GPIO3 Pin Falling Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
27	GPIO3_RISE_POL2	GPIO3 Pin Rising Interrupt Polarity Select 0 = (Default) Preserve polarity 1 = Invert polarity
26:0	—	Reserved

7.16.19 IRQ2_DB_3

Address: 0x0001 0B18

	31...8	7	6	5	4	3	2	1	0
RW	—	REFCLK_IN_FLAG_DB2				—			
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:8	—	Reserved
7	REFCLK_IN_FLAG_DB2	Input REFCLK Missing Flag Debounce Enable 0 = (Default) Debounce Disabled 1 = Debounce Enabled
6:0	—	Reserved

7.17 GPIO Control (GPIO)

7.17.1 GPIO_STATUS1

Address: 0x0001 1000

	31...8	7	6	5	4	3	2	1	0
RO	—	—				GP4_STS	GP3_STS	GP2_STS	GP1_STS
Default	0x00 0000	0	0	0	0	0	0	0	0

Bits	Name	Description
31:4	—	Reserved
3	GP4_STS	GPIO4 status. Valid only when GP4_CTRL = 0x1 and GP4_DIR = 1. This reflects the status of the GPIO4 input pin when configured as an input.
2	GP3_STS	GPIO3 status. Valid only when GP3_CTRL = 0x1 and GP3_DIR = 1. This reflects the status of the GPIO3 input pin when configured as an input.
1	GP2_STS	GPIO2 status. Valid only when GP2_CTRL = 0x1 and GP2_DIR = 1. This reflects the status of the GPIO2 input pin when configured as an input.
0	GP1_STS	GPIO1 status. Valid only when GP1_CTRL = 0x1 and GP1_DIR = 1. This reflects the status of the GPIO1 input pin when configured as an input.

7.17.2 GPIO1_CTRL1

Address: 0x0001 1008

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	GP1_DIR	—											GP1_DBTIME			
Default	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	GP1_LVL	—	GP1_DB	GP1_POL	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description
31	GP1_DIR	GPIO1 pin direction. Valid only when GP1_CTRL = 0x1. 0 = Output 1 = (Default) Input
30:20	—	Reserved
19:16	GP1_DBTIME	GPIO1 input debounce time setting. Valid only when GP1_CTRL = 0x1, GP1_DIR = 1 and GP1_DB = 1. GPIO debounce filtering happens only when GLOBAL_EN = 1. Although GPIO debounce may remain enabled when the device enters Standby, no debounce filtering is done in Standby mode. 0000 = (Default) 93.75 µs 0001 = 1.5 ms 0010 = 3 ms 0011 = 6 ms 0100 = 12 ms 0101 = 24 ms 0110 = 48 ms 0111 = 96 ms 1000 = 192 ms 1001 = 384 ms 1010 = 768 ms 1011–1111 = Reserved

Bits	Name	Description
15	GP1_LVL	GPIO1 level. Valid only when GP1_CTRL = 0x1 and GP1_DIR = 0. Write to this bit to set a GPIO output. When GP1_POL is set, the register is the opposite logic level to the external pin. This register is write only. 0 = (Default) Low 1 = High
14	—	Reserved
13	GP1_DB	GPIO1 input debounce enable. Debounce may be enabled when GP1_CTRL = 0x1, GP1_DIR = 1 and GLOBAL_EN = 1. GPIO debounce filtering happens only when GLOBAL_EN = 1. Although GPIO debounce may remain enabled when the device enters Standby, no debounce filtering is done in Standby mode. 0 = (Default) Disabled 1 = Enabled
12	GP1_POL	GPIO1 output polarity select. Valid only when GP1_CTRL = 0x1, GP1_DIR = 0. 0 = (Default) Non-inverted (Active High) 1 = Inverted (Active Low)
11:0	—	Reserved

7.17.3 GPIO2_CTRL1

Address: 0x0001 100C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP2_DIR	—											GP2_DBTIME			
Default	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP2_LVL	—	GP2_DB	GP2_POL	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description
31	GP2_DIR	GPIO2 pin direction. Valid only when GP2_CTRL = 0x1. 0 = Output 1 = (Default) Input
30:20	—	Reserved
19:16	GP2_DBTIME	GPIO2 input debounce time setting. Valid only when GP2_CTRL = 0x1, GP2_DIR = 1 and GP2_DB = 1. GPIO debounce filtering happens only when GLOBAL_EN = 1. Although GPIO debounce may remain enabled when the device enters Standby, no debounce filtering is done in Standby mode. 0000 = (Default) 93.75 µs 0001 = 1.5 ms 0010 = 3 ms 0011 = 6 ms 0100 = 12 ms 0101 = 24 ms 0110 = 48 ms 0111 = 96 ms 1000 = 192 ms 1001 = 384 ms 1010 = 768 ms 1011–1111 = Reserved
15	GP2_LVL	GPIO2 level. Valid only when GP2_CTRL = 0x1, GP2_DIR = 0. Write to this bit to set a GPIO output. When GP2_POL is set, the register is the opposite logic level to the external pin. This register is write only. 0 = (Default) Low 1 = High
14	—	Reserved
13	GP2_DB	GPIO2 input debounce enable. Valid only when GP2_CTRL = 0x1, GP2_DIR = 1 and GLOBAL_EN = 1. GPIO debounce filtering happens only when GLOBAL_EN = 1. Although GPIO debounce may remain enabled when the device enters Standby, no debounce filtering is done in Standby mode. 0 = (Default) Disabled 1 = Enabled
12	GP2_POL	GPIO2 output polarity select. Valid only when GP2_CTRL = 0x1, GP2_DIR = 0. 0 = (Default) Non-inverted (Active High) 1 = Inverted (Active Low)
11:0	—	Reserved

7.17.4 GPIO3_CTRL1

Address: 0x0001 1010

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	GP3_DIR	—											GP3_DBTIME			
Default	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	GP3_LVL	—	GP3_DB	GP3_POL	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description
31	GP3_DIR	GPIO3 pin direction. Valid only when GP3_CTRL = 0x1. 0 = Output 1 = (Default) Input
30:20	—	Reserved
19:16	GP3_DBTIME	GPIO3 input debounce time setting. Valid only when GP3_CTRL = 0x1, GP3_DIR = 1 and GP3_DB = 1. GPIO debounce filtering happens only when GLOBAL_EN = 1. Although GPIO debounce may remain enabled when the device enters Standby, no debounce filtering is done in Standby mode. 0000 = (Default) 93.75 µs 0001 = 1.5 ms 0010 = 3 ms 0011 = 6 ms 0100 = 12 ms 0101 = 24 ms 0110 = 48 ms 0111 = 96 ms 1000 = 192 ms 1001 = 384 ms 1010 = 768 ms 1011–1111 = Reserved
15	GP3_LVL	GPIO3 level. Valid only when GP3_CTRL = 0x1, GP3_DIR = 0. Write to this bit to set a GPIO output. When GP3_POL is set, the register is the opposite logic level to the external pin. This register is write only. 0 = (Default) Low 1 = High
14	—	Reserved
13	GP3_DB	GPIO3 input debounce enable. Debounce may be enabled when GP3_CTRL = 0x1, GP3_DIR = 1 and GLOBAL_EN = 1. GPIO debounce filtering happens only when GLOBAL_EN = 1. Although GPIO debounce may remain enabled when the device enters Standby, no debounce filtering is done in Standby mode. 0 = (Default) Disabled 1 = Enabled
12	GP3_POL	GPIO3 output polarity select. Valid only when GP3_CTRL = 0x1, GP3_DIR = 0. 0 = (Default) Non-inverted (Active High) 1 = Inverted (Active Low)
11:0	—	Reserved

7.17.5 GPIO4_CTRL1

Address: 0x0001 1014

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RW	GP4_DIR	—											GP4_DBTIME			
Default	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	GP4_LVL	—	GP4_DB	GP4_POL	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Description
31	GP4_DIR	GPIO4 pin direction. Valid only when GP4_CTRL = 0x1. 0 = Output 1 = (Default) Input
30:20	—	Reserved

Bits	Name	Description
19:16	GP4_DBTIME	GPIO4 input debounce time setting. Valid only when GP4_CTRL = 0x1, GP4_DIR = 1 and GP4_DB = 1. GPIO debounce filtering happens only when GLOBAL_EN = 1. Although GPIO debounce may remain enabled when the device enters Standby, no debounce filtering is done in Standby mode. 0000 = (Default) 93.75 µs 0001 = 1.5 ms 0010 = 3 ms 0011 = 6 ms 0100 = 12 ms 0101 = 24 ms 0110 = 48 ms 0111 = 96 ms 1000 = 192 ms 1001 = 384 ms 1010 = 768 ms 1011–1111 = Reserved
15	GP4_LVL	GPIO4 level. Valid only when GP4_CTRL = 0x1, GP4_DIR = 0. Write to this bit to set a GPIO output. When GP4_POL is set, the register is the opposite logic level to the external pin. This register is write only. 0 = (Default) Low 1 = High
14	—	Reserved
13	GP4_DB	GPIO4 input debounce enable. Debounce may be enabled when GP4_CTRL = 0x1, GP4_DIR = 1 and GLOBAL_EN = 1. GPIO debounce filtering happens only when GLOBAL_EN = 1. Although GPIO debounce may remain enabled when the device enters Standby, no debounce filtering is done in Standby mode. 0 = (Default) Disabled 1 = Enabled
12	GP4_POL	GPIO4 output polarity select. Valid only when GP4_CTRL = 0x1, GP4_DIR = 0. 0 = (Default) Non-inverted (Active High) 1 = Inverted (Active Low)
11:0	—	Reserved

7.18 DSP scratch space (DSP_MBOX)

7.18.1 DSP_MBOX_1

Address: 0x0001 3000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	DSP_MBOX_1																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_MBOX_1	DSP Mailbox Space 1. Intended, alongside the Virtual 1 and Virtual 2 mailbox fields, to provide direct messaging to and from the DSP core and the driver.

7.18.2 DSP_MBOX_2

Address: 0x0001 3004

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	DSP_MBOX_2																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_MBOX_2	DSP Mailbox Space 2. Intended, alongside the Virtual 1 and Virtual 2 mailbox fields, to provide direct messaging to and from the DSP core and the driver.

7.18.3 DSP_MBOX_3

Address: 0x0001 3008

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	DSP_MBOX_3																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_MBOX_3	DSP Mailbox Space 3. Intended, alongside the Virtual 1 and Virtual 2 mailbox fields, to provide direct messaging to and from the DSP core and the driver.

7.18.4 DSP_MBOX_4

Address: 0x0001 300C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_MBOX_4																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_MBOX_4	DSP Mailbox Space 4. Intended, alongside the Virtual 1 and Virtual 2 mailbox fields, to provide direct messaging to and from the DSP core and the driver.

7.18.5 DSP_MBOX_5

Address: 0x0001 3010

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_MBOX_5																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_MBOX_5	DSP Mailbox Space 5. Intended, alongside the Virtual 1 and Virtual 2 mailbox fields, to provide direct messaging to and from the DSP core and the driver.

7.18.6 DSP_MBOX_6

Address: 0x0001 3014

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_MBOX_6																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_MBOX_6	DSP Mailbox Space 6. Intended, alongside the Virtual 1 and Virtual 2 mailbox fields, to provide direct messaging to and from the DSP core and the driver.

7.18.7 DSP_MBOX_7

Address: 0x0001 3018

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_MBOX_7																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_MBOX_7	DSP Mailbox Space 7. Intended, alongside the Virtual 1 and Virtual 2 mailbox fields, to provide direct messaging to and from the DSP core and the driver.

7.18.8 DSP_MBOX_8

Address: 0x0001 301C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_MBOX_8																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_MBOX_8	DSP Mailbox Space 8. Intended, alongside the Virtual 1 and Virtual 2 mailbox fields, to provide direct messaging to and from the DSP core and the driver.

7.19 DSP virtual 1 scratch space (DSP_VIRTUAL1_MBOX)

7.19.1 DSP_VIRTUAL1_MBOX_1

Address: 0x0001 3020

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_VIRTUAL1_MBOX_1																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL1_MBOX_1	DSP Virtual 1 Mailbox Space 1. A write to this space will assert the DSP_VIRTUAL1_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.19.2 DSP_VIRTUAL1_MBOX_2

Address: 0x0001 3024

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	DSP_VIRTUAL1_MBOX_2																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL1_MBOX_2	DSP Virtual 1 Mailbox Space 2. A write to this space will assert the DSP_VIRTUAL1_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.19.3 DSP_VIRTUAL1_MBOX_3

Address: 0x0001 3028

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	DSP_VIRTUAL1_MBOX_3																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL1_MBOX_3	DSP Virtual 1 Mailbox Space 3. A write to this space will assert the DSP_VIRTUAL1_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.19.4 DSP_VIRTUAL1_MBOX_4

Address: 0x0001 302C

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	DSP_VIRTUAL1_MBOX_4																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL1_MBOX_4	DSP Virtual 1 Mailbox Space 4. A write to this space will assert the DSP_VIRTUAL1_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.19.5 DSP_VIRTUAL1_MBOX_5

Address: 0x0001 3030

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	DSP_VIRTUAL1_MBOX_5																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL1_MBOX_5	DSP Virtual 1 Mailbox Space 5. A write to this space will assert the DSP_VIRTUAL1_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.19.6 DSP_VIRTUAL1_MBOX_6

Address: 0x0001 3034

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	DSP_VIRTUAL1_MBOX_6																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL1_MBOX_6	DSP Virtual 1 Mailbox Space 6. A write to this space will assert the DSP_VIRTUAL1_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.19.7 DSP_VIRTUAL1_MBOX_7

Address: 0x0001 3038

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RW	DSP_VIRTUAL1_MBOX_7																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL1_MBOX_7	DSP Virtual 1 Mailbox Space 7. A write to this space will assert the DSP_VIRTUAL1_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.19.8 DSP_VIRTUAL1_MBOX_8

Address: 0x0001 303C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_VIRTUAL1_MBOX_8																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL1_MBOX_8	DSP Virtual 1 Mailbox Space 8. A write to this space will assert the DSP_VIRTUAL1_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.20 DSP virtual 2 scratch space (DSP_VIRTUAL2_MBOX)

7.20.1 DSP_VIRTUAL2_MBOX_1

Address: 0x0001 3040

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_VIRTUAL2_MBOX_1																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL2_MBOX_1	DSP Virtual 2 Mailbox Space 1. A write to this space will assert the DSP_VIRTUAL2_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.20.2 DSP_VIRTUAL2_MBOX_2

Address: 0x0001 3044

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_VIRTUAL2_MBOX_2																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL2_MBOX_2	DSP Virtual 2 Mailbox Space 2. A write to this space will assert the DSP_VIRTUAL2_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.20.3 DSP_VIRTUAL2_MBOX_3

Address: 0x0001 3048

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_VIRTUAL2_MBOX_3																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL2_MBOX_3	DSP Virtual 2 Mailbox Space 3. A write to this space will assert the DSP_VIRTUAL2_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.20.4 DSP_VIRTUAL2_MBOX_4

Address: 0x0001 304C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_VIRTUAL2_MBOX_4																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL2_MBOX_4	DSP Virtual 2 Mailbox Space 4. A write to this space will assert the DSP_VIRTUAL2_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.20.5 DSP_VIRTUAL2_MBOX_5

Address: 0x0001 3050

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_VIRTUAL2_MBOX_5																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL2_MBOX_5	DSP Virtual 2 Mailbox Space 5. A write to this space will assert the DSP_VIRTUAL2_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.20.6 DSP_VIRTUAL2_MBOX_6

Address: 0x0001 3054

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_VIRTUAL2_MBOX_6																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL2_MBOX_6	DSP Virtual 2 Mailbox Space 6. A write to this space will assert the DSP_VIRTUAL2_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.20.7 DSP_VIRTUAL2_MBOX_7

Address: 0x0001 3058

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_VIRTUAL2_MBOX_7																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL2_MBOX_7	DSP Virtual 2 Mailbox Space 7. A write to this space will assert the DSP_VIRTUAL2_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.20.8 DSP_VIRTUAL2_MBOX_8

Address: 0x0001 305C

RW	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSP_VIRTUAL2_MBOX_8																															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	DSP_VIRTUAL2_MBOX_8	DSP Virtual 2 Mailbox Space 8. A write to this space will assert the DSP_VIRTUAL2_MBOX_WR signal into IRQ1 and IRQ2 interrupt controllers.

7.21 Clock Presence Detect (CLOCK_DETECT)

7.21.1 CLOCK_DETECT_1

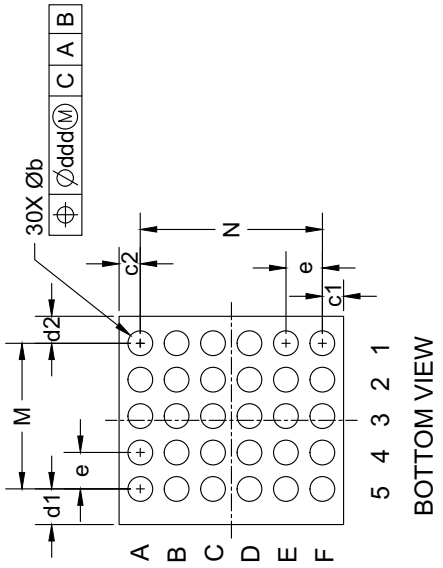
Address: 0x0001 4000

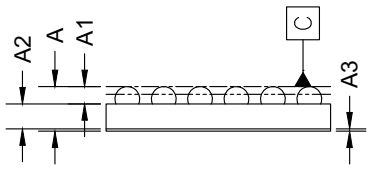
RW	31...8	7	6	5	4	3	2	1	0
	—	—		CLK_DET_FREQ		—			CLK_DET_EN
Default	0x00 0000	0	0	0	0	0	0	0	0

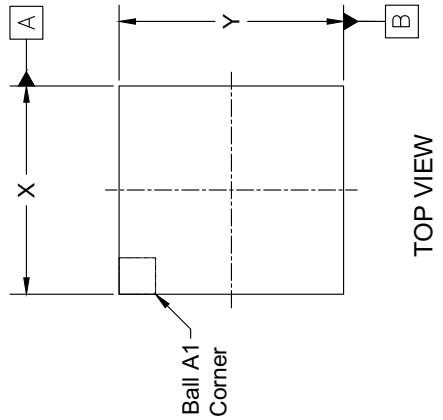
Bits	Name	Description
31:6	—	Reserved
5:4	CLK_DET_FREQ	Clock detection frequency threshold multiplier. Raises the minimum frequency required to start up the chip. The minimum frequency will vary depending on the oscillator frequency. By default, the exit hysteresis is enabled. Therefore, the clock frequency would need to be half of the detection frequency, in order to trigger a lost clock. 00 = (Default) Detect frequencies from 256 – 384 kHz 01 = Detect frequencies from 512 – 768 kHz 10 = Detect frequencies from 1.000 – 1.536 MHz 11 = Detect frequencies from 2.000 MHz and above
3:1	—	Reserved
0	CLK_DET_EN	Clock presence detection enable. 0 = (Default) Disabled 1 = Enabled

8 Package Dimensions

8.1 WLCSP Package Dimensions







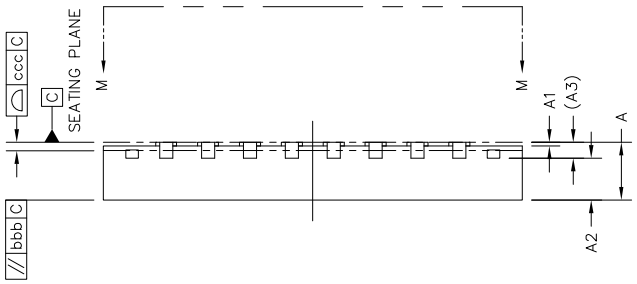
Dimension	Millimeters		
	Minimum	Nominal	Maximum
A	0.46	0.49	0.52
A1	0.175	0.19	0.205
A2	0.26	0.275	0.29
A3	REF	0.025	REF
b	0.24	0.27	0.3
c1	0.20764	0.23264	0.25764
c2	0.20804	0.23304	0.25804
d1	0.36747	0.39247	0.41747
d2	0.27091	0.29591	0.32091
e	BSC	0.4	BSC
M	BSC	1.6	BSC
N	BSC	2	BSC
X	2.26338	2.28838	2.31338
Y	2.44068	2.46568	2.49068
ddd=0.015			

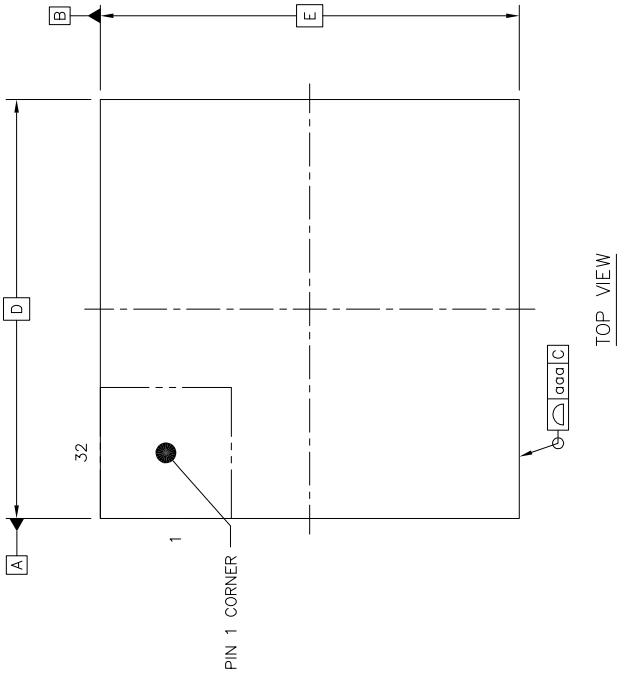
Notes: Controlling dimension is millimeters.
Dimensioning and tolerances per ASME Y 14.5-2009. The Ball A1 position indicator is for illustration purposes only. Dimension "b" applies to the solder sphere diameter and is measured at the maximum solder sphere diameter, parallel to primary Datum C.
X/Y Tolerances can apply to an individual edge increasing or decreasing by 25um.

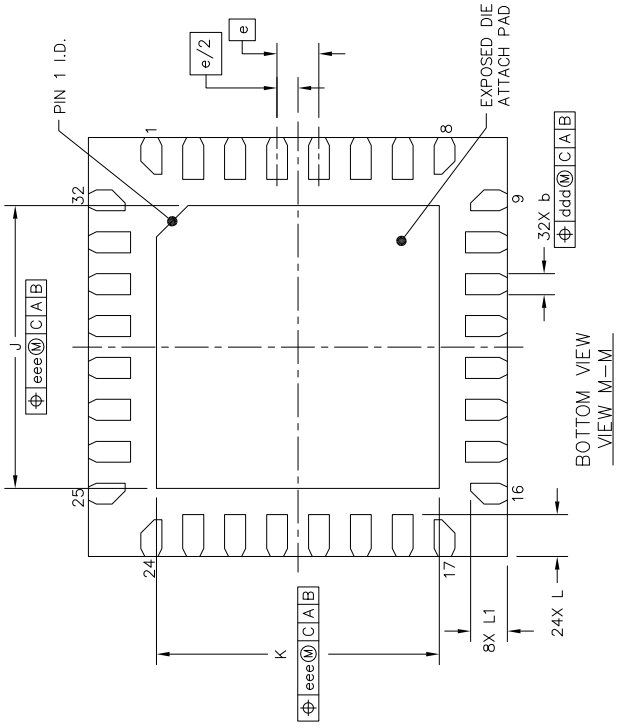
8.2 QFN Package Dimensions

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.5	0.55	0.6
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	---	0.4	---
L/F THICKNESS	A3		0.152 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		4 BSC	
BODY SIZE Y	E		4 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	J	2.6	2.7	2.8
EP SIZE Y	K	2.6	2.7	2.8
LEAD LENGTH	L	0.35	0.4	0.45
	L1	0.25	0.35	0.4
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ccc		0.08	
LEAD OFFSET	ddd		0.1	
EXPOSED PAD OFFSET	eee		0.1	

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 TOTAL THICKNESS NOT INCLUDE SAW BURR.







9 Thermal Characteristics

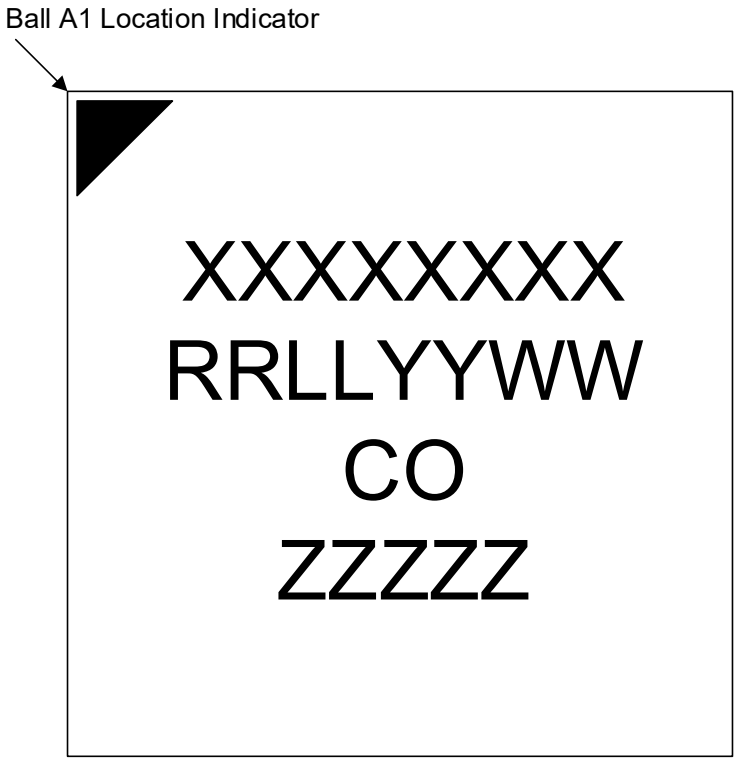
9.1 Typical Thermal Characteristics—JEDEC Four-Layer 2s2p Board

Table 9-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	WLCSP	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	60.0	40.3	°C/W
Junction-to-board thermal resistance	θ_{JB}	22.4	12.5	°C/W
Junction-to-case thermal resistance	θ_{JC}	2.6	60.7	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	11.9	11.9	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	1.0	2.4	°C/W

Notes:
- Natural convection at the maximum recommended operating temperature T_A
- Four-layer, 2s2p PCB as specified by JESD51-9 and JESD51-11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51-12
- The CS40L25B QFN package option uses a 3x3 via array (with 0.8 mm pitch) to ground the thermal pad.

10 Package Marking



Top Side Brand
Line 1: Part Number (8 characters max.)
Line 2: Package Mark (8 characters)
Line 3: Country of Origin (2 characters)
Line 4: Encoded Wafer/Die ID (5 characters)

Package Mark Fields
RR = Device Revision Code
LL = Lot Sequence Code
YY = Year of manufacture
WW = Work Week of manufacture

Figure 10-1. Package Marking

11 Ordering Information

Table 11-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Order Number
CS40L25	Boosted Haptics Driver with integrated DSP supporting one GPI + I²S.	30-ball WLCSP	Yes	Commercial	–40°C to +85°C	Tape and Reel	CS40L25-CWZR
CS40L25B	Boosted Haptics Driver with integrated DSP supporting four GPIs.	30-ball WLCSP	Yes	Commercial	–40°C to +85°C	Tape and Reel	CS40L25B-CWZR
		32-pin QFN	Yes	Commercial	–40°C to +85°C	Tape and Reel	CS40L25B-CNZ

12 References

- International Electrotechnical Commission*, IEC60958-3 Digital Audio Interface—Consumer, http://www.ansi.org/*
- JEDEC Solid State Technology Association, *Test Boards for Area Array Surface Mount Package Thermal Measurements*, *JEDEC Standard No. JESD51-9*, July 2000, http://www.jedec.org/
- JEDEC Solid State Technology Association, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*, *JEDEC Standard No. JESD51-11*, June 2001, http://www.jedec.org/
- JEDEC Solid State Technology Association, *Guidelines for Reporting and Using Electronic Package Thermal Information*, *JEDEC Standard No. JESD51-12*, May 2005, http://www.jedec.org/
- Joint Electron Device Engineering Council, *J-STD-033B.1 Handling of Moisture Sensitive Surface Mount Devices*, http://www.jedec.org/
- NXP Semiconductors, UM10204 Rev. 06, April 2014, *The I²C-Bus Specification and User Manual*, http://www.nxp.com

13 Revision History

Table 13-1. Revision History

Revision	Change
A1 MAR 2018	Initial revision.
A2 JUL 2018	• Updated part numbers globally and in Ordering Information. • Updated Typical Connection Diagrams. • Added Basic Haptics Mode registers. • Updated Package Mechanical Drawing.
A3 SEP 2018	• Updated Typical Connection Diagrams in Fig. 2-1, Fig. 2-2, and Fig. 2-3. • Updated Table 2-1. • Updated Table 3-6 to split AoH Standby current specification for CS40L25 and CS40L25B.
A4 JUN 2019	• Added QFN package and PCB layout information. • Updated register descriptions.

Important:

Please check with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.