# Daughter Card for the CS35L36

## Features

- Digital inputs
  - External PCM/PDM/SoundWire, Lochnagar I/O, and direct CODEC audio interface
  - Compatible with ADSP2 Codecs
- Two CS35L36 devices support stereo mode
- External VP, VBST, and VA via stake headers
- GPIO header
- WISCE™ software control
  - Windows® compatible
  - Predefined and user-configurable settings

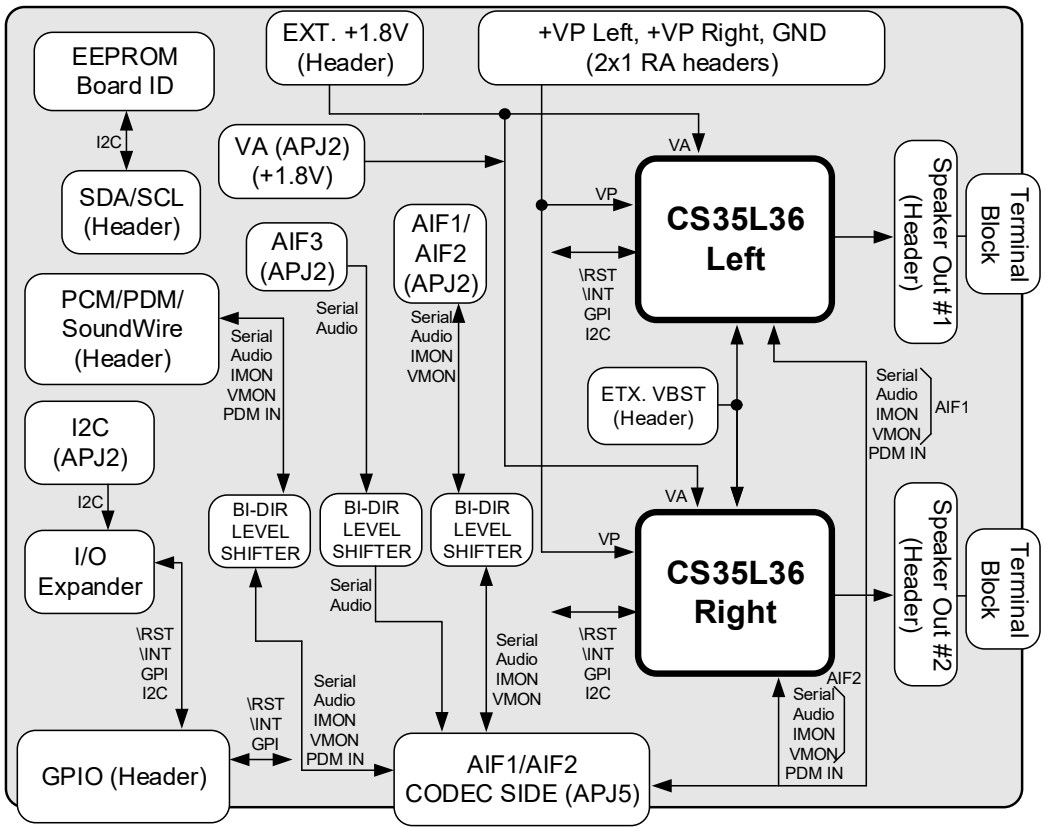
## Description

The DC35L36 board is a dedicated platform for testing and evaluating the CS35L36, mono hybrid Class D amplifier with integrated boost and monitoring. To allow comprehensive testing of CS35L36 features and performance, extensive software-configurable options are available on the DC35L36.

The DC35L36 is intended to be used in conjunction with ADSP2 CODECS, using Lochnagar platform as their baseboard. Software options, such as register settings for the CS35L36, are configured with the WISCE™ software, which communicates with the DC35L36 via an Aardvark™ USB adapter or via direct USB connection to a PC. The DC35L36 also serves as the component and layout reference for the CS35L36.

Ordering information

DC35L36-CSP Evaluation Board



## Table of Contents



# 1 DC35L36 System Overview

The DC35L36 evaluation board is a convenient platform for evaluating the CS35L36, a mono hybrid Class D amplifier with integrated boost and monitoring. It supports multiple power supply and signal I/O configurations. To evaluate stereo and shared boost modes, the DC35L36 incorporates two CS35L36 devices. It also serves as the component and layout reference for the CS35L36.

The DC35L36 is intended to be used with the Lochnagar 2 baseboard as shown in Fig. 1-1.

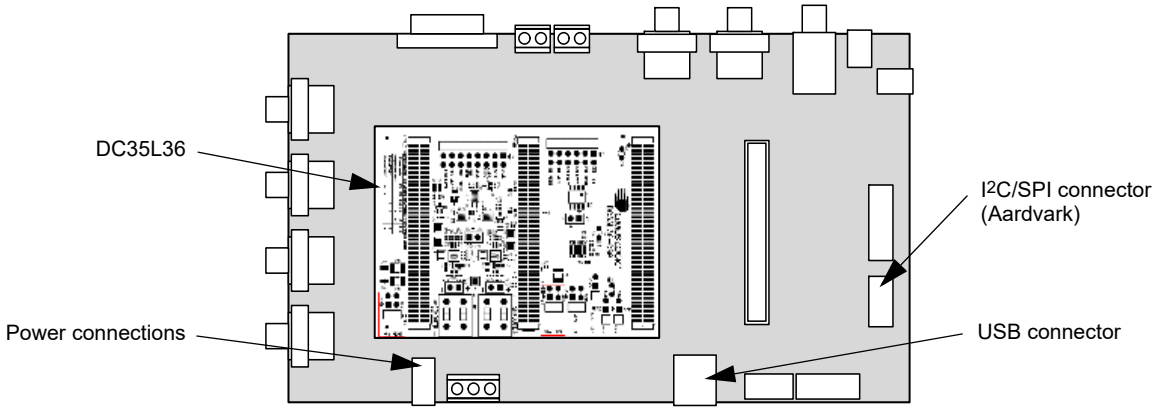



**Figure 1-1. Lochnagar 2 Baseboard with DC35L36 Installed**

The following subsections describe the features of the DC35L36 evaluation board in detail.

## 1.1 Power-Supply Circuitry

The DC35L36 requires several supply rails for proper operation, which are provided by the Lochnagar platform by default. VP_LEFT and VP_RIGHT are tied to PWR_SYSVDD supply. These two amplifier rails can be tied together by installing a 0-Ω shunt on R12. Alternatively, VP can also be supplied externally via J10 and J5. The supply-current limit is set accordingly. For example, for a stereo setup delivering 4.3 W into 8 Ω at 1% THD+N and playing a 1-kHz tone at VP = 4 V, the supply must provide at least 3 A. The VP supply current limit is set to at least 5.0 A. For a mono setup, the supply-current limit requirement is half that of the stereo mode. More details are provided in Section 2.

## 1.2 PCM/PDM Header

Header J9 provides an interface for the PDM, I²S, and SoundWire serial audio clocks and data. The header signals are described in Table 1-1. The logic level for all serial I/O is +1.8 V. When a CODEC board such as the CDB47L90 is plugged onto the DC35L36, the level shifters passing the signals from the external headers to the amps are disabled.

**Table 1-1. J9 - Serial Header Signal Descriptions**

| Pin Number | Signal Name | Direction | Description |
|---|---|---|---|
| 2 | MCLK | Input | Master clock |
| 4 | SCLK | Input/Output | I²S bit clock |
| 6 | AMP2 SDOUT | Output | I²S data out (right amp) |
| 8 | LRCK | Input/Output | I²S frame clock |
| 10 | AMP SDIN | Input | I²S data in (right and left amps) |
| 12 | AMP1 SDOUT | Output | I²S data out (left amp) |
| 14 | PDM_SWIRE_CLK_IN | Input | PDM/SoundWire clock input (right and left amps) |
| 16 | PDM_SWIRE_DATA_IN | Input | PDM/SoundWire data in (right and left amps) |
| 1,3,5,7,9,11,13,15 | GND | N/A | Ground |

## 1.3 GPIO Header

Header J11 provides an interface for the amplifier's I/O pins. The header signals are described in Table 1-2. The logic level for all I/O is +1.8 V.

**Table 1-2. GPIO Signal Descriptions**

| Pin Number | Signal Name | Direction | Description |
|---|---|---|---|
| 2 | $\overline{\text{RST\_LEFT\_AMP}}$ | Input | Left amplifier reset |
| 4 | $\overline{\text{RST\_RIGHT\_AMP}}$ | Input | Right amplifier reset |
| 6 | GPI_LEFT | Output | Left amplifier programmable interrupt output |
| 8 | GPI_RIGHT | Output | Right amplifier programmable interrupt output |
| 10 | $\overline{\text{INT\_LEFT}}$ | Output | Left amplifier interrupt |
| 12 | $\overline{\text{INT\_RIGHT}}$ | Output | Right amplifier interrupt |
| 1,3,5,7,9,11 | GND | N/A | Ground |

## 1.4 SYNC Header

Header J12 configures SYNC settings for the amplifiers. Refer to Table 1-3 for SYNC configuration options.

**Table 1-3. SYNC Pin Configuration**

| Header | Signal Name | Direction | Description |
|---|---|---|---|
| J12 | SYNC L/R | Input | Tie Left and Right Sync pins for stereo mode |

## 1.5 I²C Headers

Headers J8-A and J10-A provide access to the I²C bus as described in Table 1-4.

**Table 1-4. I²C Headers**

| Header | Signal Name | Direction | Description |
|---|---|---|---|
| J8-A | SCL | Input/Output | I²C SCL pin |
| J10-A | SDA | Input/Output | I²C SDA pin |

## 1.6 Compatibility with WISCE

Settings for both C35L36 devices and the I/O expander can be configured by interfacing with WISCE (downloadable from http://www.cirrus.com/support/wisce), which provides an easy, intuitive way to configure the DC35L36. A Windows-compatible PC, Aardvark USB bundle, and Lochnagar board are required to run WISCE.

## 1.7 Layout Reference

The DC35L36 uses a ten-layer PCB that allows for optimal trace and power routing to the CS35L36 devices and surrounding circuitry. Local decoupling capacitors for the CS35L36 are placed as close as possible to the device. Double-sided component and ground fill is used extensively on the component layer of the DC35L36 to isolate critical nets where possible.

# 2 System Connections

Table 2-1 lists all power and signal I/O connections.

**Table 2-1. External System Connections**

| Reference Designator | Connection | Input/Output | Description |
|---|---|---|---|
| J7 | EXT. +1.8 V | Input | External +1.8-V VA supply to both CS35L36 devices |
| J10 | VP+ LEFT | Input | Left CS35L36 VP |
| J5 | VP+ RIGHT | Input | Right CS35L36 VP |
| J1, J2 | SPKOUTL | Output | Left CS35L36 speaker output |
| J3, J4 | SPKOUTR | Output | Right CS35L36 speaker output |
| J6 | EXT. VBST | Input | External VBST input to the CS35L36s |
| J9 | PCM/PDM | Input/Output | External PCM/PDM header |
| J11 | GPIO | Input/Output | External Amplifier GPIO |
| TP2, TP4, TP6 | GND | GND | GND test loops |
| J12 | SYNC_L/R | Input | Ties SYNC_L and SYNC_R for stereo operation |
| J8-A | SCL | Input/Output | I²C SCL pin |
| J10-A | SDA | Input/Output | I²C SDA pin |
| J8 | WP | Input | EEPROM Write protect pin |

## 2.1 External VA and VP supplies

In some cases (e.g. amplifier performance measurements vs. VP voltage, or device input power measurements), it may be necessary to power one or both CS35L36 devices from external VP and VA power sources rather than from Lochnagar. The information in the following subsections describes what modifications should be performed on the daughter card in this case.

Table 2-2 provides an overview of the resistor modifications that are described in the following sub-sections.

**Table 2-2. Resistor Modifications for Using External VA and VP Supplies**

| Configuration | | R25 | R59 | R60 | R11 | R16 | R17 | R18 |
|---|---|---|---|---|---|---|---|---|
| Default | Both VA and VP powered from Lochnagar | Installed 0Ω | Installed 0Ω | Installed 0Ω | Installed 0Ω | Installed 0Ω | Installed 0Ω | Installed 0Ω |
| External VA | Left amplifier only | Remove | Remove | Default | Default | Default | Default | Default |
| | Right amplifier only | Remove | Default | Remove | Default | Default | Default | Default |
| | Both amplifiers | Remove | Remove | Remove | Default | Default | Default | Default |
| External VP | Both amplifiers | Default | Default | Default | Remove | Remove | Remove | Remove |

### 2.1.1 External power supply for VA (1.8V)

Follow these steps to use an external power supply for VA.

1. Remove R25 on the bottom side of the PCB (Fig. 2-2).
2. If testing is to be performed on the Left amplifier channel only, remove R59. If testing is done only on the Right amplifier channel, remove R60. This disconnects 1.8V from the respective amplifier IC. Both resistors are located on the bottom side of the PCB (Fig. 2-2).
3. Connect the external 1.8-V power source to connector J7 (Fig. 2-3). The external power supply must provide at least 100 mA.

**Note:** VA power must be applied only after VP (external or from Lochnagar) is applied.

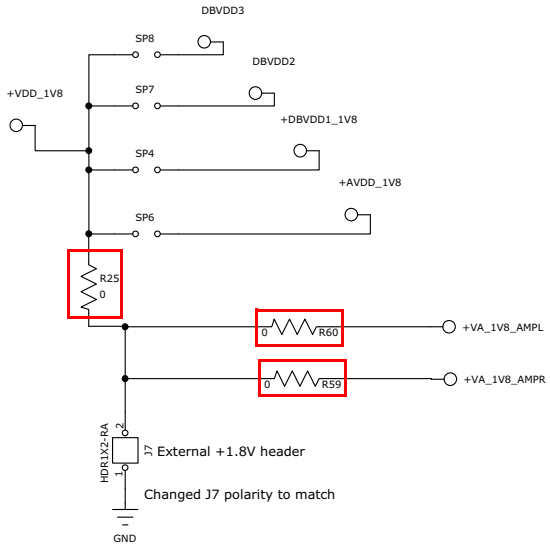



**Figure 2-1. Common 1.8-V Supply**

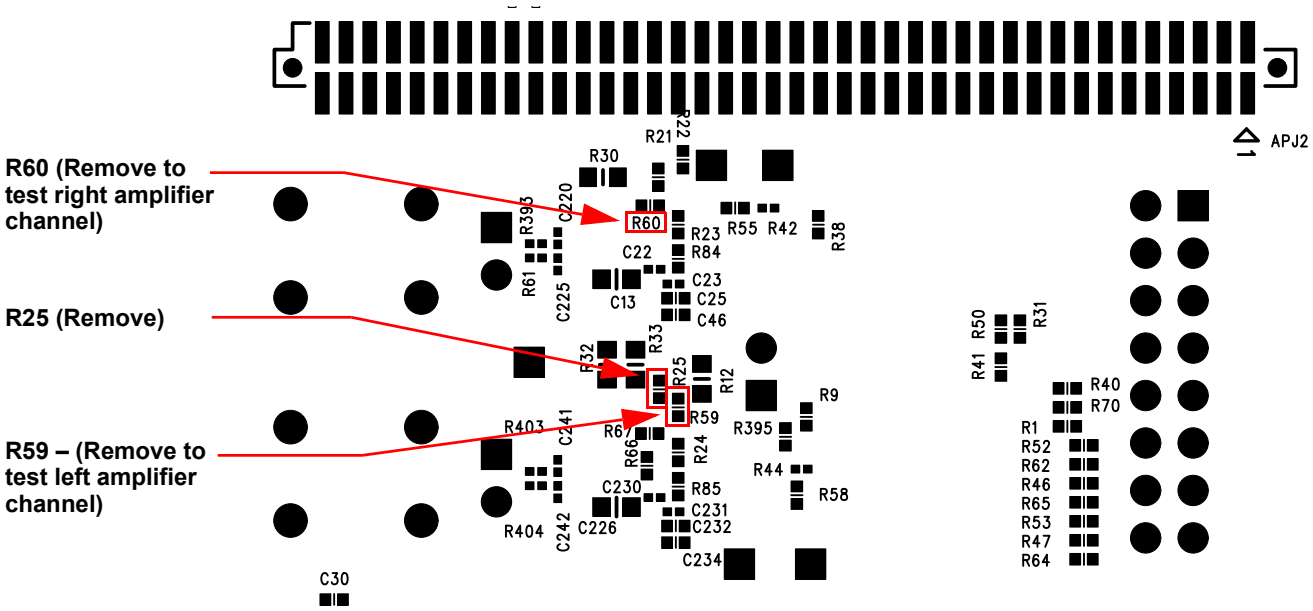



**Figure 2-2. R25, R59 and R60 location (bottom side of the PCB)**

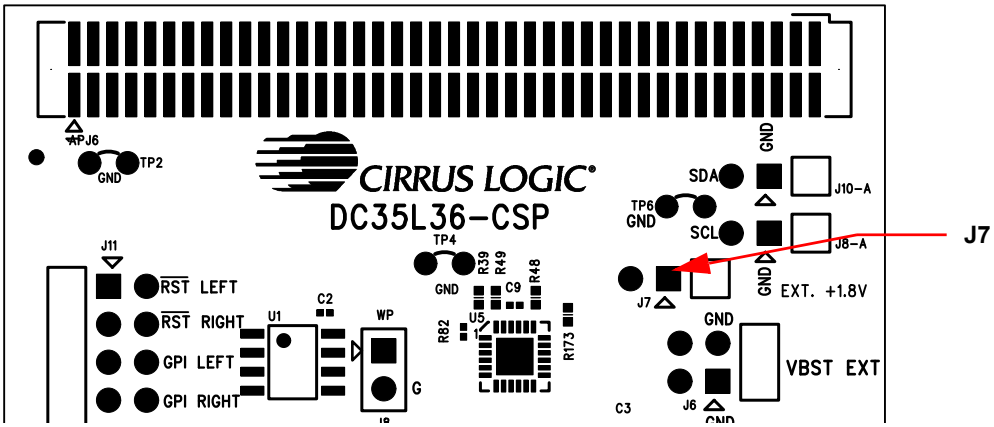



**Figure 2-3. J7 location (external 1.8-V supply)**

### 2.1.2 External power supply for VP (2.5 V – 5.5 V)

Follow these steps to use an external power supply for VP.

1. Remove R11, R16, R17, R18 on the bottom side of the PCB (Fig. 2-5).
2. Connect external 2.5-V – 5.5-V power supply to J10 to supply VP for the Left amplifier (Fig. 2-6).
3. If needed, connect external 2.5-V – 5.5-V power supply to J5 to supply VP for the Right amplifier (Fig. 2-6). The external power supply must provide at least 5.0 A for a stereo setup and at least 2.5 A for mono setup.

**Note:** VP power should be applied before VA is applied

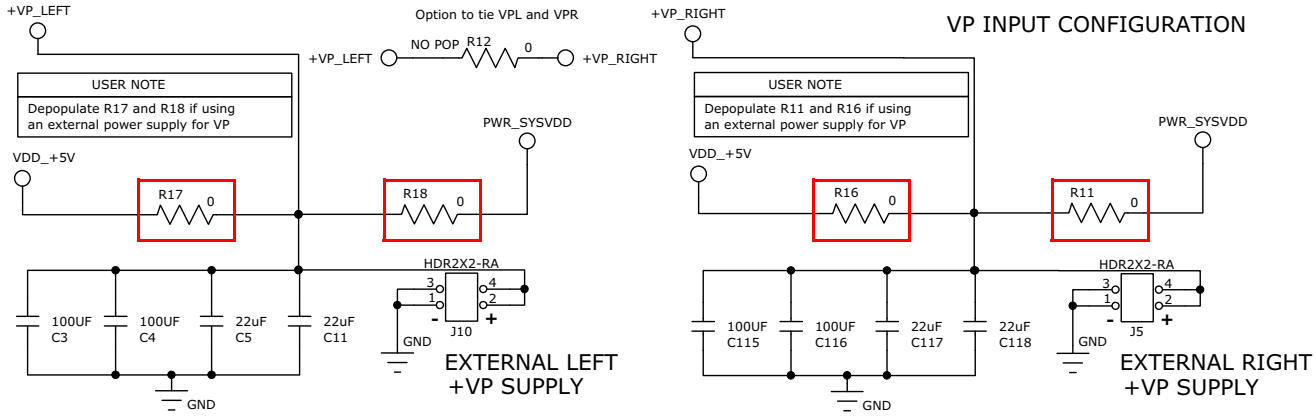



**Figure 2-4. Modifications – R11, R16, R17, R18**

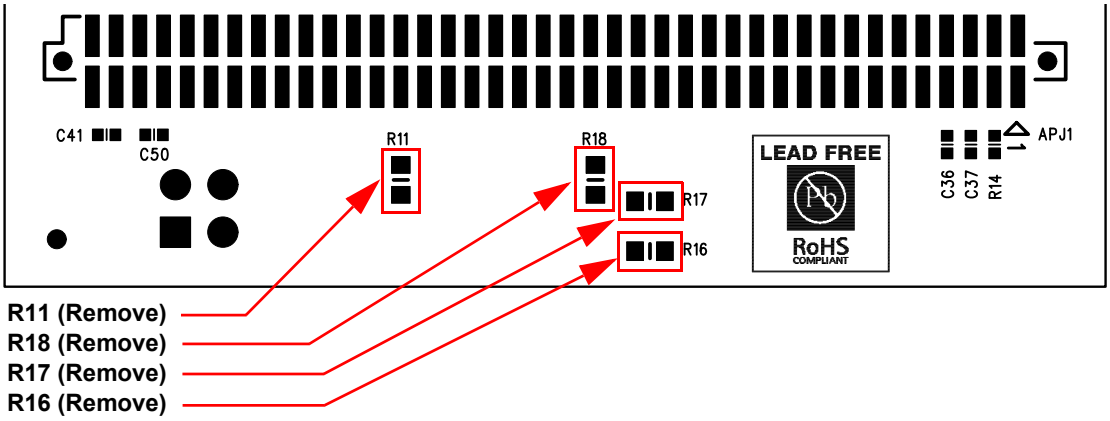



**Figure 2-5. Location – R11, R16, R17, and R18 (bottom side of the PCB)**

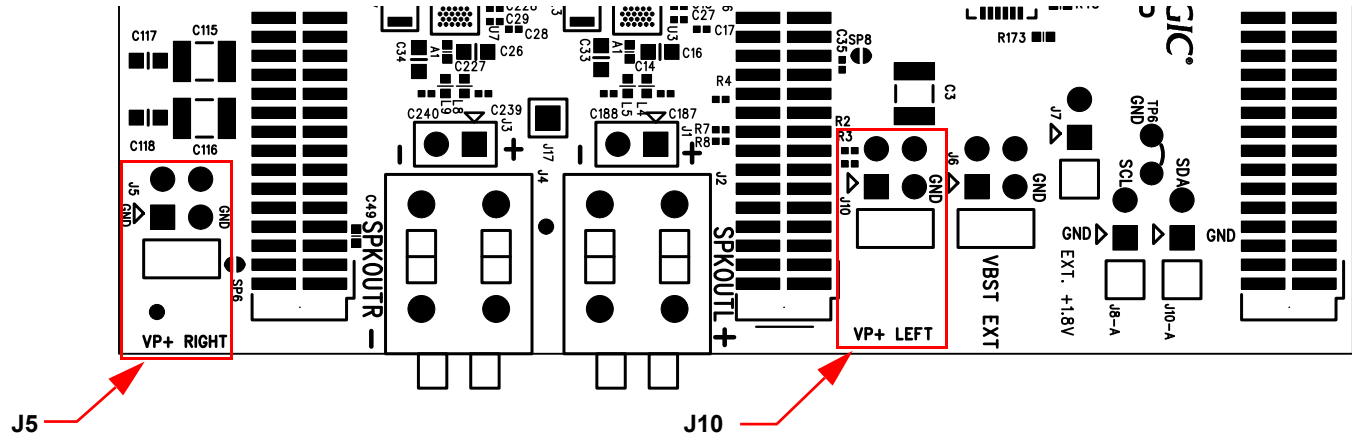



**Figure 2-6. Location – J5, J10 (VP+ Right and VP+ Left)**

## 2.2 Connecting External Digital Audio Sources

The following sections describe the board modifications that are required to connect PCM or PDM serial digital audio sources to the DC35L36 daughter card. Table 2-3 provides a summary of the modifications.

**Table 2-3. Board Modifications - Connecting Serial Audio**

| | R19 | R20 | R57 | R63 | R40 | R52 |
|---|---|---|---|---|---|---|
| **Default** | Not Populated | Installed | Not Populated | Installed | Installed | Not Populated |
| **PCM** | No modifications needed. Use Default resistor configuration. | | | | | |
| **PDM**[1] | Short | Remove | Short | Remove | Remove | Short |

1.See Table 1-1, and the PCB silk screen for J9 pin identification.

### 2.2.1 Applying PCM Signal

Follow these steps to apply a PCM signal to header J9.

1. Connect serial audio interface PCM signal source to connector J9 (Fig. 2-7). Please refer to Table 1-1, schematic or J9 silkscreen on the PCB for pinout.
2. Use an appropriate WISCE script to configure signal path from J9 to amplifiers on the daughter card.

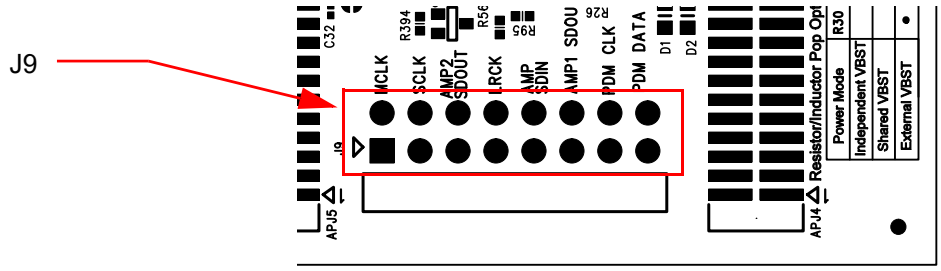



**Figure 2-7. PCM serial audio connection to J9**

### 2.2.2 Applying PDM Signal

Follow these steps to apply a PDM signal to header J9.

1. On the top side of the PCB:
   - Remove R20, R63 (Fig. 2-9)
   - Short R19, R57 (Fig. 2-9)

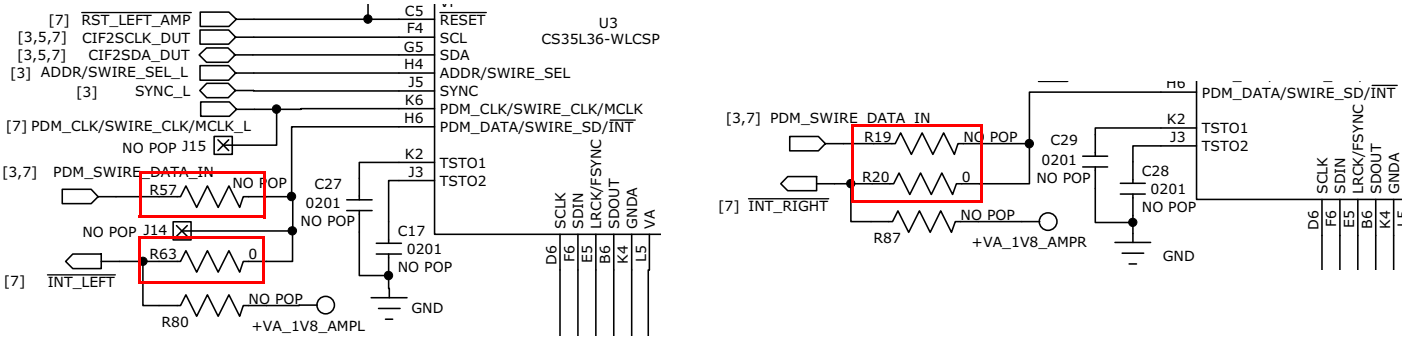



**Figure 2-8. Modifications – R19, R20, R57, R63**

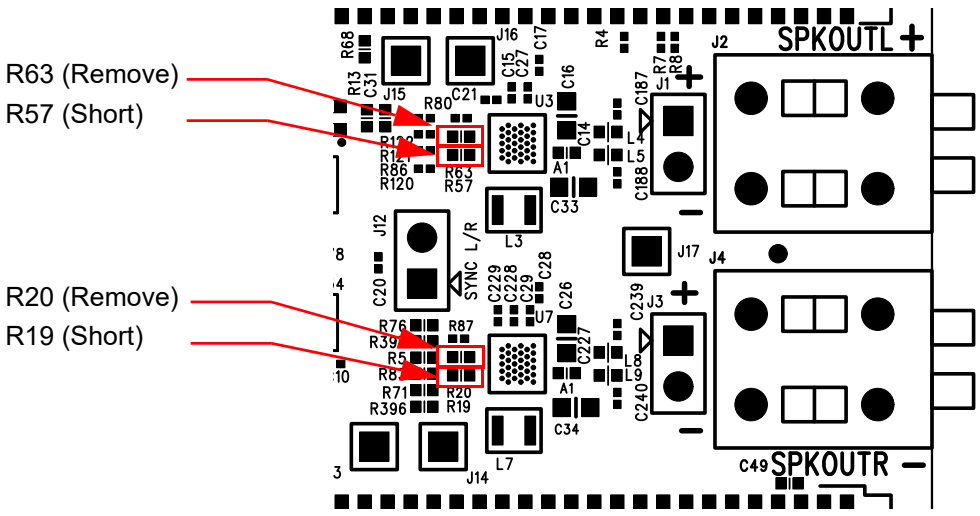



**Figure 2-9. Location – R19, R20, R57, R63**

2. On the bottom side of the PCB:
   - Remove R40 on the bottom side of the PCB (Fig. 2-11)
   - Short R52 on the bottom side of the PCB (Fig. 2-11)

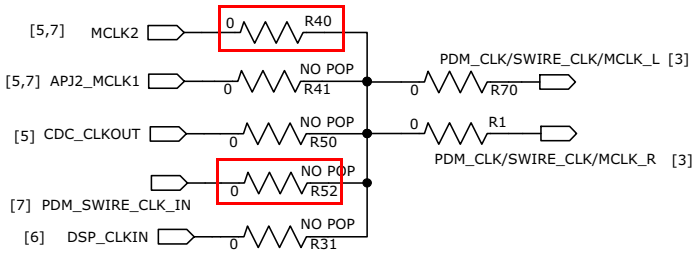



**Figure 2-10. Modifications – R40, R52**

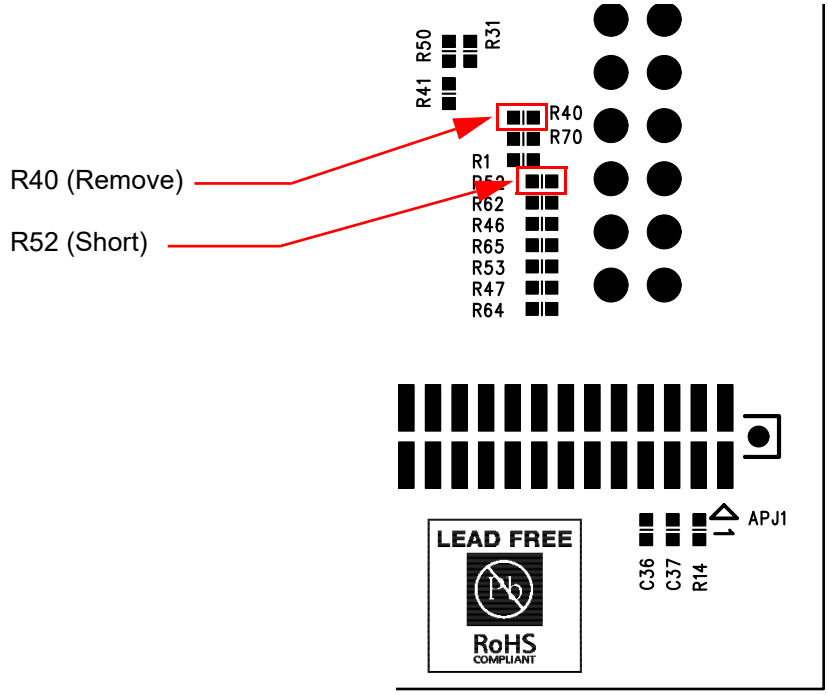



**Figure 2-11. Location – R40, R52 (bottom side of the PCB)**

3. Connect PDM signal source to connector J9 (Fig. 2-7). Please refer to Table 1-1, schematic or the J9 silkscreen on the PCB for pinout.
4. Use an appropriate WISCE script to configure and activate signal path from J9 to amplifiers on the daughter card.

# 3 Software Control Using WISCE

The Cirrus Logic WISCE application is a graphical interface that allows users to easily create projects and configure software modifiable options on the DC35L36, such as the register settings of the CS35L36 and TCA9539 I/O Expander.

All screen shots shown in this section were taken with a Lochnagar 2 board and CS35L36 Device Pack installed on the PC.

## 3.1 Start-Up Setup

To set up WISCE for use with the DC35L36, follow these steps:

1. Dock the DC35L36 Board onto Lochnagar and then apply +5 V (assuming the daughter card is powered by Lochnagar).
2. Run WISCE. Upon initialization the system detects the Aardvark I2C Host Adapter and displays all devices connected to the I2C bus as shown in Fig. 3-1. The device shown with I2C slave address 0xE8 corresponds to TCA9539 I/O expander.

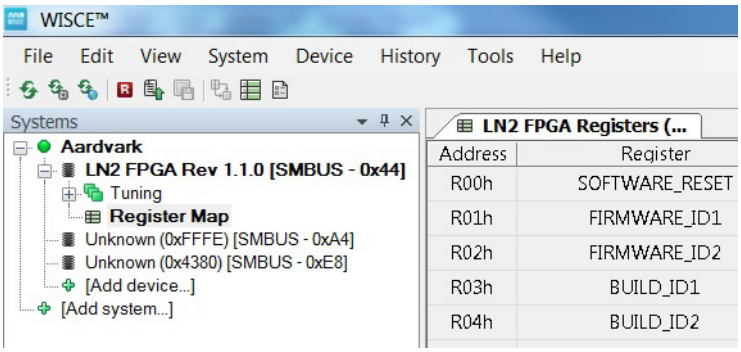



**Figure 3-1. Devices Found by WISCE**

3. To link a device with its corresponding register map, double click on the device address and select the name of the device from the drop-down menu, as shown in Fig. 3-2.

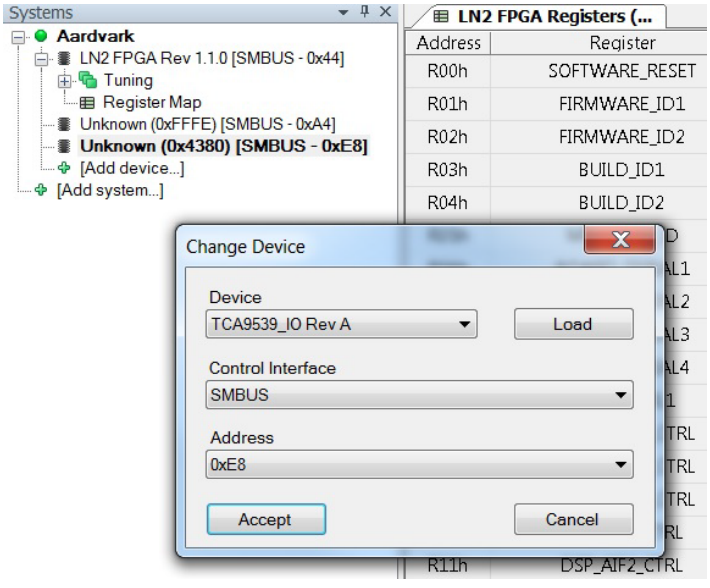



**Figure 3-2. Linking a Device with Its Register Map**

4. To add CS35L36 devices click on the “Add device” tab, select CS35L36 Rev B0 from the pull-down menu, and click the “Accept” button (Fig. 3-3).The first added CS35L36 device is assigned I2C address 0x80 by default (left amplifier on the daughter card). The second added CS35L36 is assigned address 0x82 (right amplifier on the daughter card).

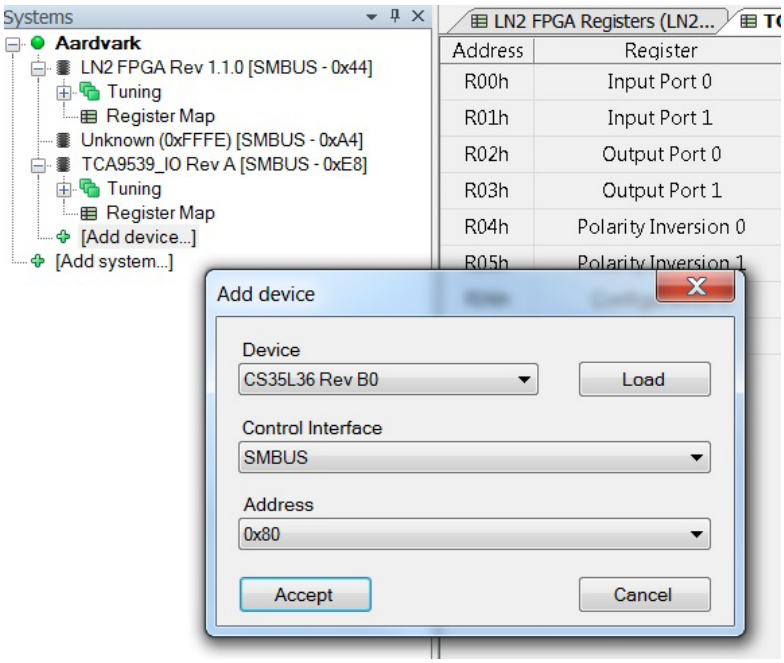



**Figure 3-3. Adding CS35L36 Devices**

5. After the devices are added, the initial WISCE screen for CS35L36 appears as part of the user panel, as shown in Fig. 3-4.

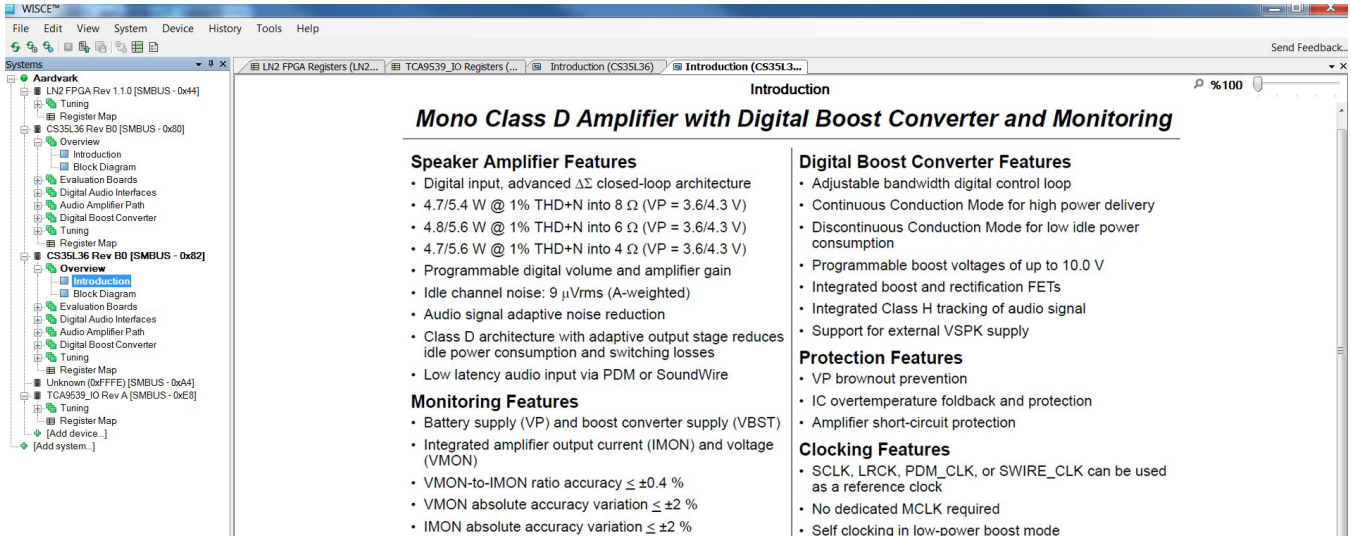



**Figure 3-4. CS35L36 WISCE Initial Screen**

The CS35L36 settings can be changed in the panels “Digital Audio Interfaces”, “Audio Amplifier Path”, “Digital boost Converter”, or directly in the “Register Map” panel.

Changes to the device settings can be saved. Select “File>Save Settings>Save changed registers…” Then select “File>Load …” to run the saved configuration file.

# 4 Revision History

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| Revision | Changes |
|---|---|
| DC1<br>NOV ‘17 | Initial release. |
| DC2<br>JAN ‘21 | Removed Confidential Only document restriction. Updated legal end matter. |

## Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.