AN0486 - CS35L38A Schematic and Layout Guidelines

1 Introduction

This document describes the Schematic and Layout guidelines for the CS35L38A Amplifier. This information augments but does not take precedence over the specifications provided in the CS35L38A data sheet.

2 Schematic Reference

The schematic below corresponds to a basic configuration for the amplifier with connection to 2-terminal speaker load.

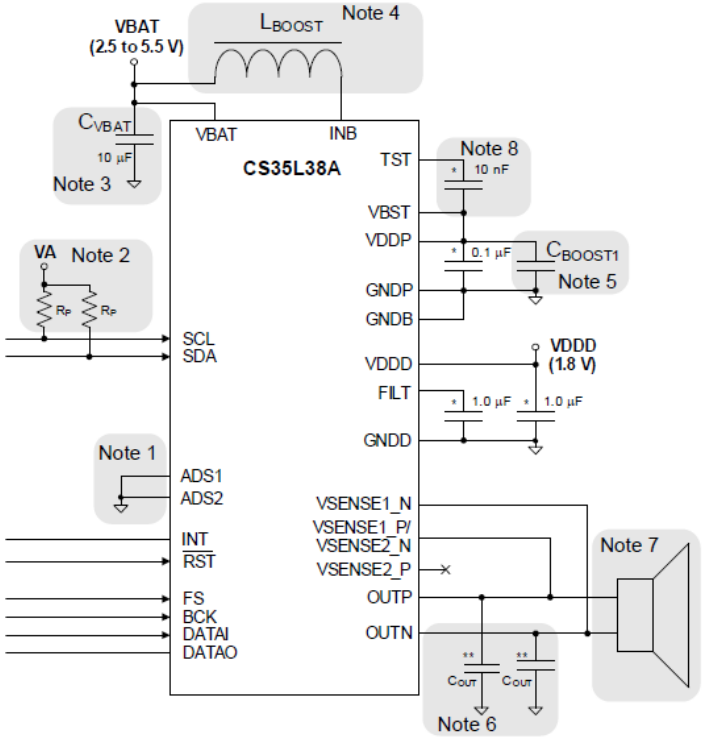

Figure 1 - Schematic Diagram

2.1 Component Selection

Note 1. This shows one example of how to configure the 7-bit I²C address. The I²C address is set as 0x50 in this case.

Note 2. Minimum RP value is determined from the maximum VDDD level, the minimum sink current strength of their respective output, and the maximum low-level output voltage (VOL). Maximum RP values may be determined by how fast their associated signals must transition, taking into account load capacitance. These resistors may be optional, if there are pull-up resistors on I²C bus elsewhere in the system.

Note 3. Place the 10-uF bulk capacitor close to the LBOOST inductor.

Note 4. Boost converter LBOOST inductor values of 2.2 to 1.0 uH are supported for typical use operation. However, the selected LBOOST inductor must not derate to a value of less than 0.7 uH during normal use to maintain proper loop stability.

Note 5. The boost converter CBOOST capacitors are recommended to have a maximum voltage rating of at least 16 V and must not derate to a combined capacitance value of less than 3.6 uF when 12.0 VDC is applied across the capacitors. Note that ceramic capacitors can derate considerably when a DC voltage is applied to them. The total derated CBOOST capacitance at 12.0 VDC must not exceed 58 uF.

Note 6. The COUT capacitors are optional EMI suppressors that are used depending on the application requirements. It is recommended that the value of these components not exceed 2 nF, as switching losses increase linearly with increases to these capacitances.

Note 7. When using a simulated speaker load of 8 Ohm + 33 uH, a Coilcraft DO5040H-333MLB inductor is used.

Note 8. Presence of capacitor on pin impact no functionality during normal operation. It may be omitted and is completely optional

3 Layout Suggestions

The following sections contain suggested procedures regarding layout and routing of specific nets and signals.

3.1 VBAT Routing

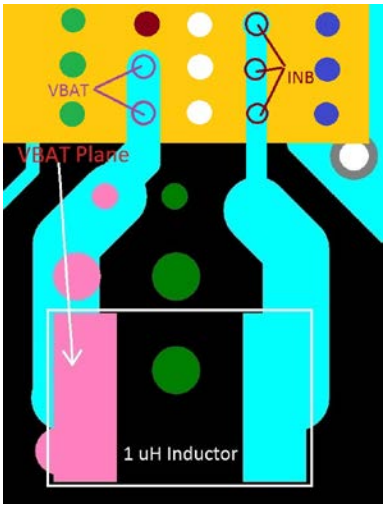

Figure 2 - VBAT Routing

1. Use Power plane for VBAT delivery
2. Connect VBAT to inductor with multiple vias
3. VBAT pins (C1, C2) drop down directly to VBAT plane.
4. Use wide (~25mil) and as short as possible trace connecting the inductor to INB node (E1, E2, E3)

3.2 VBAT Decoupling

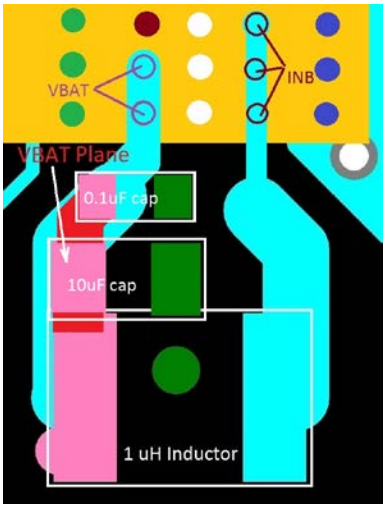

Figure 3 - VBAT Decoupling

1. Place 0.1uF capacitor as close to the VBAT pins (C1, C2) as possible.
2. Place 10uF CVBAT capacitor as close to the inductor connection to the VBAT supply as possible. Depending on available board space, it can be placed on either side of the board.

3.3 VBST Routing

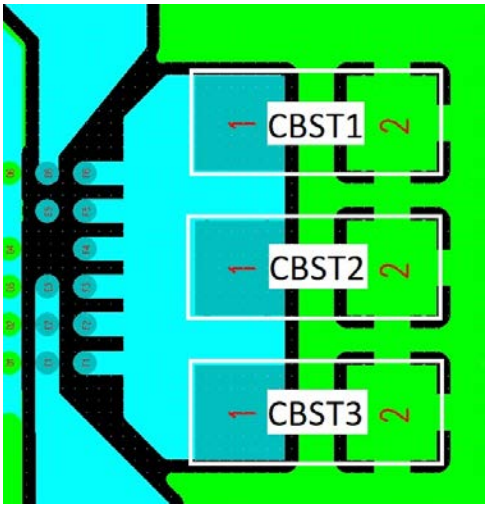

Figure 4 - VBST Routing

1. Place 0. 1uF CBST bypass capacitor as close to VBST pins (F1, F2, F3) as possible. It may be placed at the bottom side of the PCB.
2. Place larger CBST bypass capacitors close to VBST pads.
3. Tie all VBST/VDDP pins together (F1 … F6) by 8 - 10 mil wide traces that come out to a copper flood for the CBST capacitors.

3.4 Speaker Routing

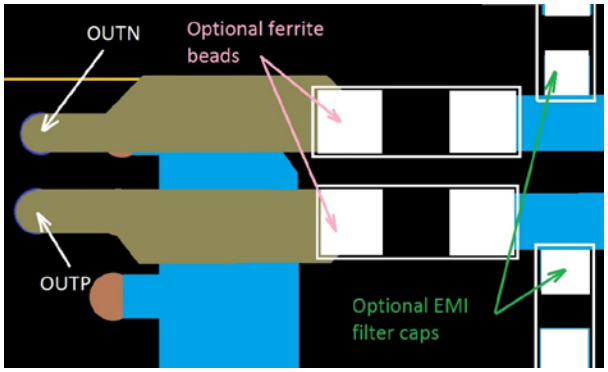

Figure 5 - Speaker Routing

1. OUTP and OUTN traces should be as symmetrical as possible.
2. Bring out signals on inner layer and come up to top layer.
3. Maintain 30~40 mil trace width as traces go out to the SPKR pads.
4. Maintain distance from VBST/VDDP before bringing traces up to top layer.
5. Have GND shield around output traces to avoid noise coupling.

3.5 VSENSE Routing

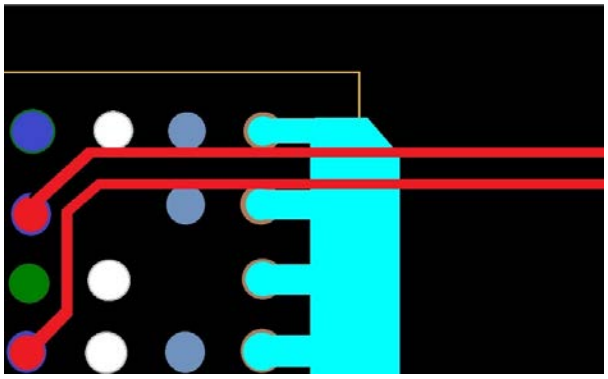

Figure 6 - VSENSE Routing

1. Run traces differentially between VSENSE1_N and VSENSE1_P/VSENSE2_N pads and output side of the EMI filter (speaker side).
2. Provide GND shielding around VSENSE1_N and VSENSE1_P/VSENSE2_N traces to minimize noise coupling from the Class-D outputs.
3. May need to add filter on each VSENSE1_N and VSENSE1_P/VSENSE2_N trace if using output EMI filtering.

3.6 Other

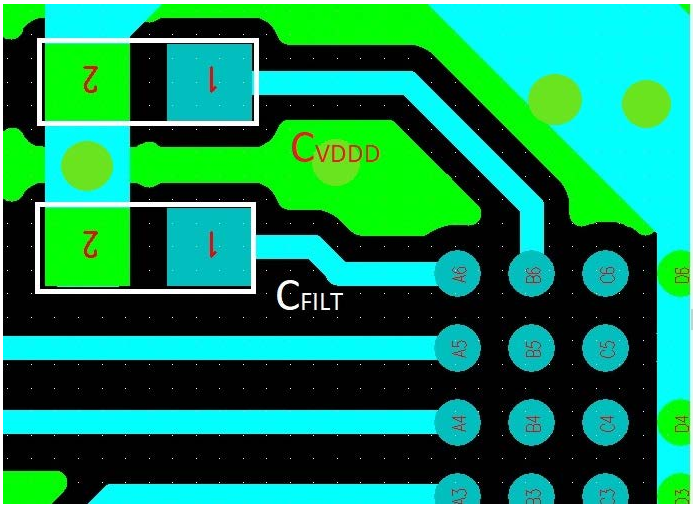

Figure 7 - Other

1. Place FILT decoupling capacitor as close as possible to the pad A6.
2. Place VDDD decoupling capacitor as close as possible to the pad B6.
3. All ground pins need to be connected to the same ground plane.

4 Revision History

Revision	Changes
R1 OCT 2019	• Initial release

Contacting Cirrus Logic Support
For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.