System Interconnect 7

2014.06.30

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The hard processor system (HPS) level 3 (L3) interconnect and level 4 (L4) peripheral buses are implemented with the ARM® CoreLink™ Network Interconnect (NIC-301). The NIC-301 provides a foundation for a high-performance HPS interconnect based on the ARM Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™), Advanced High-Performance Bus (AHB™), and Advanced Peripheral Bus (APB™) protocols. The L3 interconnect implements a multilayer, nonblocking architecture that supports multiple simultaneous transactions between masters and slaves, including the Cortex®-A9 microprocessor unit (MPU) subsystem. The interconnect provides five independent L4 buses to access control and status registers (CSRs) of peripherals, managers, and memory controllers

Related Information

ARM Infocenter (http://infocenter.arm.com)
Additional information is available in the *AMBA Network Interconnect (NIC-301) Technical Reference Manual*, revision r2p3, which you can download from the ARM info center website.

Features of the L3 System Interconnect

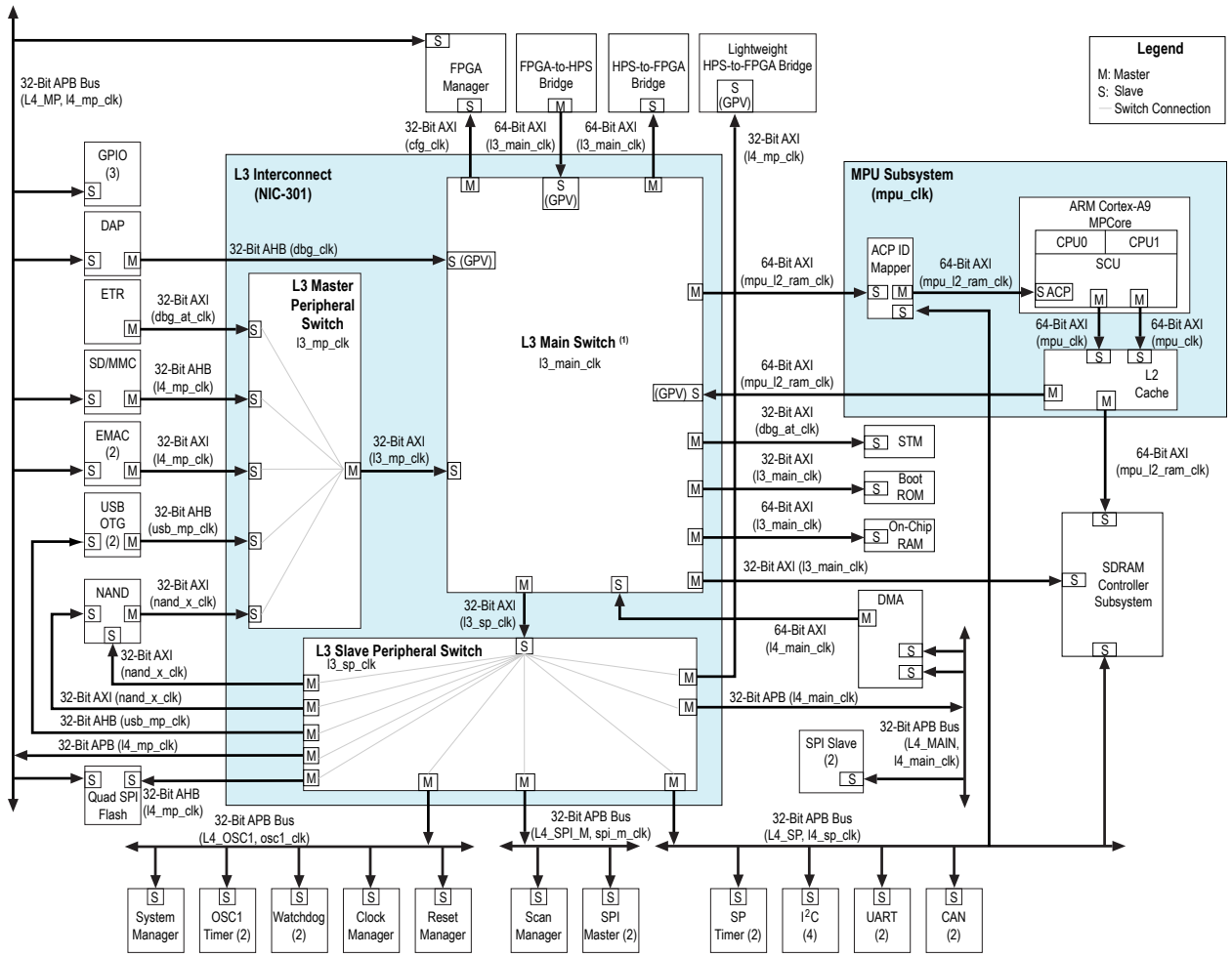
The L3 system interconnect supports high-throughput peripheral devices. The L3 interconnect has the following characteristics:

- Main internal data width of 64 bits
- Programmable master priority with single-cycle arbitration
- Full pipelining to prevent master stalls
- Programmable control for FIFO buffer transaction release
- Security of the following types:
  - Secure
  - Nonsecure
  - Per transaction security
- Five independent L4 buses

Interconnect Block Diagram and System Integration

Interconnect Block Diagram

The following figure shows the L3 interconnect and L4 buses.



Note: Interconnect slaves are available for connection from peripheral masters. Interconnect masters connect to peripheral slaves. This terminology is the reverse of conventional terminology used in Qsys.

Related Information

- **Master to Slave Connectivity Matrix** on page 7-4
- **Main Connectivity Matrix** on page 7-3

System Interconnect Architecture

The L3 interconnect is a partially-connected switch fabric. Not all masters can access all slaves.

Internally, the L3 interconnect is partitioned into the following subswitches:

- L3 interconnect
  - Interconnect used to transfer high-throughput 64-bit data
  - Operates at up to half the MPU main clock frequency
  - Provides masters with low-latency connectivity to AXI bridges, on-chip memories, SDRAM, and FPGA manager
- L3 master peripheral switch
  - Used to connect memory-mastering peripherals to the interconnect
  - 32-bit data width
  - Operates at up to half the interconnect clock frequency
- L3 slave peripheral switch
  - Used to provide access to level 3 and 4 slave interfaces for masters of the master peripheral and interconnects
  - 32-bit data width
  - Five independent L4 buses

The L3 master and slave peripheral switches are fully-connected crossbars. The L3 interconnect is a partially-connected crossbar. The following table shows the connectivity matrix of all the master and slave interfaces of the L3 interconnect.

Main Connectivity Matrix

The L3 master and slave peripheral switches are fully-connected crossbars. The L3 interconnect is a partially-connected crossbar. The following table shows the connectivity matrix of all the master and slave interfaces of the L3 interconnect.

Masters	Slaves							
	L3 Slave Peripheral Switch *(1)*	FPGA Manager	HPS-to-FPGA Bridge	ACP ID Mapper Data	STM	Boot ROM	On-Chip RAM	SDRAM Controller Subsystem L3 Data
L3 Master Peripheral Switch *(1)*			✓	✓			✓	✓
L2 Cache Master 0	✓	✓	✓		✓	✓	✓	
FPGA-to-HPS Bridge	✓			✓	✓		✓	✓
DMA	✓	✓	✓	✓	✓		✓	✓
DAP	✓	✓	✓	✓			✓	✓

(1) For details of the masters and slaves connected to the L3 master peripheral switch and L3 master peripheral switch, refer to "Interconnect Block Diagram".

Related Information

Interconnect Block Diagram on page 7-1

Functional Description of the Interconnect

Master to Slave Connectivity Matrix

The interconnect is a partially-connected crossbar. The following table shows the connectivity matrix of all the master and slave interfaces of the interconnect.

Figure 7-1: Interconnect Connectivity Matrix

Masters	Slaves																
	L4 SP Bus Slaves	L4 MP Bus Slaves	L4 OSC1 Bus Slaves	L4 MAIN Bus Slaves	L4 SPIM Bus Slaves	Lightweight HPS-to-FPGA Bridge	USB OTG 0/1 CSR	NAND CSR	NAND Command and Data	Quad SPI Flash Data	FPGA Manager	HPS-to-FPGA Bridge	ACP ID Mapper Data	STM	Boot ROM	On-Chip RAM	SDRAM Controller Subsystem L3 Data
L2 Cache Master 0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	
FPGA-to-HPS Bridge	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓		✓	✓
DMA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
EMAC 0/1												✓	✓			✓	✓
USB OTG 0/1												✓	✓			✓	✓
NAND												✓	✓			✓	✓
SD/MMC												✓	✓			✓	✓
ETR												✓	✓			✓	✓
DAP	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓

Address Remapping

The interconnect supports address remapping through the `remap` register in the `l3regs` group. Remapping allows software to control which memory device (SDRAM, on-chip RAM, or boot ROM) is accessible at address 0x0 and the accessibility of the HPS-to-FPGA and lightweight HPS-to-FPGA bridges. The `remap` register is one of the NIC-301 Global Programmers View (GPV) registers. The following L3 masters can manipulate `remap`, because it maps into their address space:

- MPU
- FPGA-to-HPS bridge
- DAP

The remapping bits in the `remap` register are not mutually exclusive. The lowest order remap bit has higher priority when multiple slaves are remapped to the same address. Each bit allows different combinations of address maps to be formed. There is only one remapping register available in the GPV, so modifying the `remap` register affects all memory maps of all the masters of the interconnect.

The effects of the remap bits can be categorized in the following groups:

- MPU master interface
  - L2 cache master 0 interface

- Non-MPU master interfaces
  - DMA master interface
  - Master peripheral interfaces
  - Debug Access Port (DAP) master interface
  - FPGA-to-HPS bridge master interface

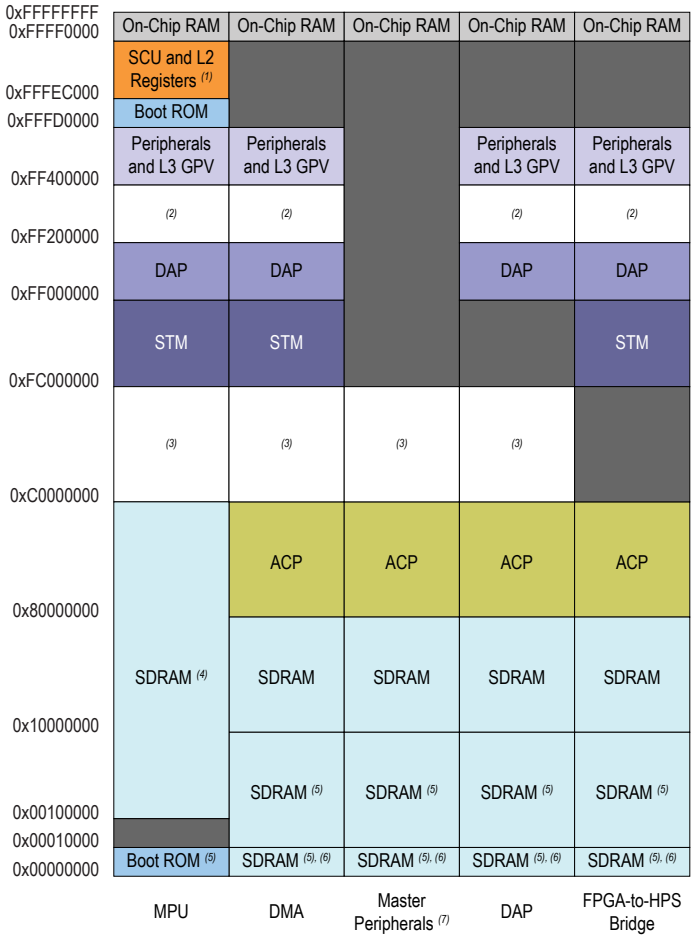
Related Information

- **L3 (NIC-301) GPV Registers Address Map** on page 7-16
  Information about the GPV registers
- **remap** on page 7-23
  Description of the `remap` register
- **Cortex-A9 Microprocessor Unit Subsystem**
  For general information about the MPU subsystem, refer to the Cortex-A9 Microprocessor Unit Subsystem chapter in the *Cyclone V Device Handbook, Volume 3*.
- **Cortex-A9 Microprocessor Unit Subsystem**
  For information about virtual ID mapping in the ACP ID mapper, refer to "HPS Peripheral Master Input IDs" in the Cortex-A9 Microprocessor Unit Subsystem chapter of the *Cyclone V Device Handbook, Volume 3*.

Available Address Maps

Figure 7-2: Address Maps for Interconnect Masters

The following figure shows the default interconnect address maps for all masters. The figure is not to scale.



Notes on Address Maps

(1) Transactions on these addresses pass through the L2 interconnect.

(2) This region can be configured to access slaves on the lightweight HPS-to-FPGA bridge, by using the `remap` register.

(3) This region can be configured to access slaves on the HPS-to-FPGA bridge, by using the `remap` register.

(4) The MPU accesses SDRAM through a dedicated port.

(5) This region can be configured to access the ACP, by using the `remap` register.

(6) This region can be configured to access on-chip RAM, by using the `remap` register.

(7) The following peripherals can master the interconnect:

- Ethernet MACs
- USB-2 OTG controllers
- NAND controllers

- ETR
- SD/MMC controller

For the MPU L3 master, either the boot ROM or on-chip RAM maps to address 0x0 and obscures the lowest 64 KB of SDRAM. The address space from 0x00010000 to 0x00100000 is not accessible because the MPU L2 filter registers only have a granularity of 1 MB. After booting completes, the MPU can change address filtering to use the lowest 1 MB of SDRAM.

For non-MPU masters, either the on-chip RAM or the SDRAM maps to address 0x0. When mapped to address 0x0, the on-chip RAM obscures the lowest 64 KB of SDRAM for non-MPU masters.

Related Information

remap on page 7-23
Description of the `remap` register

Memory Map Remap Bits

Bit Name	Bit Offset	Description
`mpuzero`	0	When set to 0, the boot ROM maps to address 0x0 for the MPU L3 master. When set to 1, the on-chip RAM maps to address 0x0 for the MPU L3 master. This bit has no effect on non-MPU masters. Note that regardless of this setting, the boot ROM also always maps to address 0xffff0000 and the on-chip RAM also always maps to address 0xfffd0000 for the MPU L3 master.
`nonmpuzero`	1	When set to 0, the SDRAM maps to address 0x0 for the non-MPU L3 masters. When set to 1, the on-chip RAM maps to address 0x0 for the non-MPU masters. This bit has no effect on the MPU L3 master. Note that regardless of this setting, the on-chip RAM also always maps to address 0xfffd0000 for the non-MPU L3 masters.
Reserved	2	Must always be set to 0.
`hps2fpga`	3	When set to 1, the HPS-to-FPGA bridge slave port is visible to the L3 masters. When set to 0, accesses to the associated address range return an AXI decode error to the master.
`lwhp2fpga`	4	When set to 1, the lightweight HPS-to-FPGA bridge slave port is visible to the L3 masters. When set to 0, accesses to the associated address range return an AXI decode error to the master.
Reserved	31:5	Must always be set to 0.

Note: L2 filter registers in the MPU subsystem, not the interconnect, allow the SDRAM to be remapped to address `0x0` for the MPU.

Master Caching and Buffering Overrides

Some of the peripheral masters connected to the interconnect do not have the ability to drive the caching and buffering signals of their interfaces. The system manager provides registers so that you can enable

cacheable and bufferable transactions for these masters. The system manager drives the caching and buffering signals of the following masters:

Master Peripheral	System Manager Register Group	Register
EMAC0 and EMAC1	emacgrp	l3master
USB OTG 0 and USB OTG 1	usbgrp	l3master
NAND flash	nandgrp	l3master
SD/MMC	sdmmcgrp	l3master

At reset time, the system manager drives the cache and buffering signals for these masters low. In other words, the masters listed do not support cacheable or bufferable accesses until you enable them after reset. There is no synchronization between the system manager and the interconnect, so avoid changing these settings when any of the masters are active.

Related Information

System Manager
For more information about enabling or disabling these features, refer to the *System Manager* chapter in the *Cyclone V Device Handbook, Volume 3*.

Security

Slave Security

The interconnect enforces security through the slave settings. The slave settings are controlled by the address region control registers accessible through the GPV registers. Each L3 and L4 slave has its own security check and programmable security settings. After reset, every slave of the interconnect is set to a secure state (referred to as boot secure). The only accesses allowed to secure slaves are by secure masters.

The GPV can only be accessed by secure masters. The security state of the interconnect is not accessible through the GPV as the security registers are write-only. Any nonsecure accesses to the GPV receive a DECERR response, and no register access is provided. Updates to the security settings through the GPV do not take effect until all transactions to the affected slave have completed.

Master Security

Masters of the interconnect are either secure, nonsecure, or the security is set on a per transaction basis. The DAP is capable of performing only secure accesses. The L2 cache master 0, FPGA-to-HPS-bridge, and DMA perform secure and nonsecure accesses on a per transaction basis. All other interconnect masters perform nonsecure accesses.

Accesses to secure slaves by unsecure masters result in a response of DECERR and the transaction does not reach the slave.

Related Information

Interconnect Master Properties on page 7-10

Arbitration

At the entry point to the interconnect, all transactions are allocated a local quality of service (QoS). QoS specifies the transaction's arbitration priority. The interconnect allows transactions with a higher QoS to

use a greater share of interconnect bandwidth. The transaction arbitration throughout the interconnect uses this QoS value. The QoS controls for each master connected to the interconnect are separated into read and write QoS priority values.

At any arbitration node, a fixed priority exists for transactions with different QoS values. The highest QoS value has the highest priority. If there are coincident transactions at an arbitration node with the same QoS value that require arbitration, then the interconnect uses a least recently used (LRU) algorithm.

You can programmatically configure the QoS value for each master through the appropriate `write_qos` register.

Related Information

L3 (NIC-301) GPV Registers Address Map on page 7-16
Information about the GPV `write_qos` registers

Cyclic Dependency Avoidance Schemes

The AXI protocol permits re-ordering of transactions. As a result, when routing concurrent multiple transactions from a single point of divergence to multiple slaves, the interconnect might need to enforce rules to prevent deadlock.

Each master of the interconnect is configured with one of three possible cyclic dependency avoidance schemes (CDAS). The same CDAS scheme is configured for both read and write transactions, but they operate independently.

Single Slave on page 7-9

Single Slave Per ID on page 7-9

Single Active Slave on page 7-10

Related Information

Interconnect Master Properties on page 7-10
Contains descriptions of the CDAS implementation for the masters.

Single Slave

Single slave (SS) ensures the following conditions at a slave interface of a switch:

- All outstanding read transactions are to a single end destination.
- All outstanding write transactions are to a single end destination.

If a master issues another transaction to a different destination than the current destination for that transaction type (read or write), the network stalls the transactions until all the outstanding transactions of that type have completed.

Single Slave Per ID

Single slave per ID (SSPID) ensures the following conditions at a slave interface of a switch:

- All outstanding read transactions with the same ID go the same destination.
- All outstanding write transactions with the same ID go the same destination.

When a master issues a transaction, the following situations can occur:

- If the transaction has an ID that does not match any outstanding transactions, it passes the CDAS.

- If the transaction has an ID that matches the ID of an outstanding transaction, and the destinations also match, it passes the CDAS.
- If the transaction has an ID that matches the ID of an outstanding transaction, and the destinations do not match, the transaction fails the CDAS check and stalls.

Single Active Slave

Single active slave (SAS) is the same as the SSPID scheme, with an added check for write transactions. SAS ensures that a master cannot issue a new write address until all of the data from the previous write transaction has been sent.

Interconnect Master Properties

The system interconnect connects to various slave interfaces through the L3 interconnect and L3 slave peripheral switch.

Table 7-1: Interconnect Master Interfaces

TrustZone security:

- Secure: All transactions are marked TrustZone secure
- Nonsecure: All transactions are marked TrustZone non-secure
- Per transaction: Transactions can be marked TrustZone secure or TrustZone non-secure, depending on the state of the interconnect master.

Issuance is based on the number of read, write, and total transactions.

The FIFO buffer depth for AXI is based on the AW, AR, R, W, and B channels. For AHB and APB, the depth is based on W, A, and D channels.

Master	Interface Width	Clock	Switch	TrustZone Security	GPV Access	CDAS	Issuance	FIFO Buffer Depth	Type
L2 cache M0	64	`mpu_l2_ram_clk`	L3 interconnect	Per Transaction	Yes	SSPID	7, 12, 19	2, 2, 2, 2, 2	AXI
FPGA-to-HPS bridge	64	`l3_main_clk`	L3 interconnect	Per Transaction	Yes	SAS	16, 16, 32	2, 2, 6, 6, 2	AXI
DMA	64	`l4_main_clk`	L3 interconnect	Per Transaction	No	SSPID	8, 8, 8	2, 2, 2, 2, 2	AXI
EMAC 0/1	32	`l4_main_clk`	L3 master peripheral switch	Secure	No	SSPID	16, 16, 32	2, 2, 2, 2, 2	AXI
USB OTG 0/1	32	`usb_mp_clk`	L3 master peripheral switch	Nonsecure	No	SSPID	2, 2, 4	2, 2, 2	AHB

Master	Interface Width	Clock	Switch	TrustZone Security	GPV Access	CDAS	Issuance	FIFO Buffer Depth	Type
NAND	32	nand_x_clk	L3 master peripheral switch	Nonsecure	No	SSPID	1, 8, 9	2, 2, 2, 2, 2	AXI
SD/MMC	32	l4_mp_clk	L3 master peripheral switch	Nonsecure	No	SSPID	2, 2, 4	2, 2, 2	AHB
ETR	32	dbg_at_clk	L3 master peripheral switch	Per Transaction	No	SSPID	32, 1, 32	2, 2, 2, 2, 2	AXI
DAP	32	dbg_clk	L3 interconnect	Secure	Yes	SS	1, 1, 1	2, 2, 2	AHB

Interconnect Slave Properties

The interconnect connects to various slave interfaces through the L3 interconnect, L3 slave peripheral switch, and the five L4 peripheral buses. After reset, all slave interfaces are set to the secure state.

Table 7-2: Interconnect Slave Interfaces

Acceptance is based on the number of read, write, and total transactions. The FIFO buffer depth for AXI is based on the AW, AR, R, W, and B channels. For AHB and APB, the depth is based on the W, A, and D channels.

Slave	Interface Width	Clock	Mastered By	Acceptance(2)	Buffer Depth (3)	Type
SDRAM subsystem CSR	32	l4_sp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB
SP timer 0/1	32	l4_sp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB
I^2C 0/1/2/3	32	l4_sp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB
UART 0/1	32	l4_sp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB
CAN 0/1	32	l4_sp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB
GPIO 0/1/2	32	l4_mp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB
ACP ID mapper CSR	32	l4_mp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB
FPGA manager CSR	32	l4_mp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB

(3) The FIFO buffer depth for AXI is based on the AW, AR, R, W, and B channels. For AHB and APB, the depth is based on W, A, and D channels.
(2) Acceptance is based on the number of read, write, and total transactions.

Slave	Interface Width	Clock	Mastered By	Acceptance[2]	Buffer Depth [3]	Type
DAP CSR	32	l4_mp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB
Quad SPI flash CSR	32	l4_mp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB
SD/MMC CSR	32	l4_mp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB
EMAC 0/1 CSR	32	l4_mp_clk	L4 SP bus master	1, 1, 1	2, 2, 2	APB
System manager	32	osc1_clk	L4 OSC1 bus master	1, 1, 1	2, 2, 2	APB
OSC1 timer 0/1	32	osc1_clk	L4 OSC1 bus master	1, 1, 1	2, 2, 2	APB
Watchdog 0/1	32	osc1_clk	L4 OSC1 bus master	1, 1, 1	2, 2, 2	APB
Clock manager	32	osc1_clk	L4 OSC1 bus master	1, 1, 1	2, 2, 2	APB
Reset manager	32	osc1_clk	L4 OSC1 bus master	1, 1, 1	2, 2, 2	APB
DMA secure CSR	32	l4_main_clk	L4 main bus master	1, 1, 1	2, 2, 2	APB
DMA nonsecure CSR	32	l4_main_clk	L4 main bus master	1, 1, 1	2, 2, 2	APB
SPI slave 0/1	32	l4_main_clk	L4 main bus master	1, 1, 1	2, 2, 2	APB
Scan manager	32	spi_m_clk	L4 main bus master	1, 1, 1	2, 2, 2	APB
SPI master 0/1	32	spi_m_clk	L4 main bus master	1, 1, 1	2, 2, 2	APB
Lightweight HPS-to-FPGA bridge	32	l4_main_clk	L3 slave peripheral switch	16, 16, 32	2, 2, 2, 2, 2	AXI
USB OTG 0/1	32	usb_mp_clk	L3 slave peripheral switch	1, 1, 1	2, 2, 2	AHB
NAND CSR	32	nand_x_clk	L3 slave peripheral switch	1, 1, 1	2, 2, 2	AXI
NAND command and data	32	nand_x_clk	L3 slave peripheral switch	1, 1, 1	2, 2, 2	AXI
Quad SPI flash data	32	l4_mp_clk	L3 slave peripheral switch	1, 1, 1	2, 2, 2	AHB
FPGA manager data	32	cfg_clk	L3 interconnect	1, 2, 3	2, 2, 2, 32, 2	AXI
HPS-to-FPGA bridge	64	l3_main_clk	L3 interconnect	16, 16, 32	2, 2, 6, 6, 2	AXI

(3) The FIFO buffer depth for AXI is based on the AW, AR, R, W, and B channels. For AHB and APB, the depth is based on W, A, and D channels.
(2) Acceptance is based on the number of read, write, and total transactions.

Slave	Interface Width	Clock	Mastered By	Acceptance[2]	Buffer Depth [3]	Type
ACP ID mapper data	64	mpu_l2_ram_clk	L3 interconnect	13, 5, 18	2, 2, 2, 2, 2	AXI
STM	32	dbg_at_clk	L3 interconnect	1, 2, 2	2, 2, 2, 2, 2	AXI
On-chip boot ROM	32	l3_main_clk	L3 interconnect	1, 1, 2	0, 0, 0, 0, 0	AXI
On-chip RAM	64	l3_main_clk	L3 interconnect	2, 2, 2	0, 0, 0, 8, 0	AXI
SDRAM subsystem L3 data	32	l3_main_clk	L3 interconnect	16, 16, 16	2, 2, 2, 2, 2	AXI

Upsizing Data Width Function

The upsizing function combines narrow transactions into wider transactions to increase the overall system bandwidth. Upsizing only packs data for read or write transactions that are cacheable. If the interconnect splits input-exclusive transactions into more than one output bus transaction, it removes the exclusive information from the multiple transactions it creates.

The upsizing function can expand the data width by the following ratios:

- 1:2
- 1:4

If multiple responses from created transactions are combined into one response, then the following order of priority applies:

- DECERR is the highest priority
- SLVERR is the next highest priority
- OKAY is the lowest priority.

Related Information

ARM Infocenter (http://infocenter.arm.com)

Additional information is available in the *AMBA Network Interconnect (NIC-301) Technical Reference Manual*, revision r2p3, which you can download from the ARM Infocenter website.

Incrementing Bursts

The interconnect converts all input INCR bursts that complete within a single output data width to an INCR1 burst of the minimum SIZE possible, and packs all INCR bursts into INCR bursts of the optimal size possible for maximum data throughout.

[3] The FIFO buffer depth for AXI is based on the AW, AR, R, W, and B channels. For AHB and APB, the depth is based on W, A, and D channels.

[2] Acceptance is based on the number of read, write, and total transactions.

Wrapping Bursts

All WRAP bursts are either passed through unconverted as WRAP bursts, or converted to one or two INCR bursts of the output bus. The interconnect converts input WRAP bursts that have a total payload less than the output data width to a single INCR burst.

Fixed Bursts

All FIXED bursts pass through unconverted.

Bypass Merge

Bypass merge is accessible through the GPV registers and is only accessible to secure masters. If the programmable bit bypass_merge is enabled, the interconnect does not alter any transactions that could pass through legally without alteration.

Downsizing Data Width Function

The downsizing function reduces the data width of a transaction to match the optimal data width at the destination. Downsizing does not merge multiple-transaction data narrower than the destination bus if the transactions are marked as noncacheable.

The downsizing function reduces the data width by the following ratios:

- 2:1
- 4:1

Incrementing Bursts

The interconnect converts INCR bursts that fall within the maximum payload size of the output data bus to a single INCR burst. It converts INCR bursts that are greater than the maximum payload size of the output data bus to multiple INCR bursts.

INCR bursts with a size that matches the output data width pass through unconverted.

The interconnect packs INCR bursts with a SIZE smaller than the output data width to match the output width whenever possible, using the upsizing function.

Related Information

Upsizing Data Width Function on page 7-13

For more information about AXI terms such as DECERR, WRAP, and INCR, refer to the *AMBA AXI Protocol Specification v1.0*, which you can download from the ARM website.

Wrapping Bursts

The interconnect always converts WRAP bursts to WRAP bursts of twice the length, up to the output data width maximum size of WRAP16, and treats the WRAP burst as two INCR bursts that can each be converted into one or more INCR bursts.

Fixed Bursts

The interconnect converts FIXED bursts to one or more INCR1 or INCRn bursts depending on the downsize ratio.

Bypass Merge

Bypass merge is accessible through the GPV registers and is only accessible to secure masters. If the programmable bit `bypass_merge` in the `fn_mod2` register is enabled, the interconnect does not perform any packing of beats to match the optimal size for maximum throughput, up to the output data width size.

If an exclusive transaction is split into multiple transactions at the output of the downsizing function, the exclusive flag is removed and the master never receives an `EXOKAY` response. Response priority is the same as for the upsizing function.

Related Information

- **fn_mod2** on page 7-78
- **Upsizing Data Width Function** on page 7-13
  For more information about AXI terms such as `DECERR`, `WRAP`, and `INCR`, refer to the *AMBA AXI Protocol Specification v1.0*, which you can download from the ARM website.

Lock Support

Lock is not supported by the interconnect. For atomic accesses, masters can perform exclusive accesses when sharing data located in the HPS SDRAM.

Related Information

SDRAM Controller Subsystem
For more information about exclusive access support, refer to the *SDRAM Controller Subsystem* chapter in the *Cyclone V Device Handbook, Volume 3*.

FIFO Buffers and Clocks

The interconnect contains FIFO buffers in the majority of the interfaces exposed to the HPS master and slaves, as well as between the subswitches. These FIFO buffers also provide clock domain crossing for masters and slaves that operate at a different clock frequency than the switch they connect to.

Data Release Mechanism

For interconnect ports with data FIFO buffers whose depth is greater than zero, you can set a write tidemark function, `wr_tidemark`. This tidemark level stalls the release of the transaction until one of the following situations occurs:

- The interconnect receives the `WLAST` beat of a burst.
- The write data FIFO buffer becomes full.
- The number of occupied slots in the write data FIFO buffer exceeds the write tidemark.

Related Information

- **Interconnect Master Properties** on page 7-10
  Indicates which master interfaces have data FIFO buffers with a nonzero depth
- **Interconnect Slave Properties** on page 7-11
  Indicates which slave interfaces have data FIFO buffers with a nonzero depth

Resets

The interconnect has one reset signal. The reset manager drives this signal to the interconnect on a cold or warm reset. On reset, the boot ROM is mapped to address 0x0.

Related Information

Reset Manager
For more information, refer to the *Reset Manager* chapter in the *Cyclone V Device Handbook, Volume 3*.

Interconnect Address Map and Register Definitions

This section lists the interconnect register address map and describes the registers.

Note: Interconnect slaves are available for connection from peripheral masters. Interconnect masters connect to peripheral slaves. This terminology is the reverse of conventional terminology used in Qsys.

Related Information

- **Introduction to the Hard Processor System**
  Lists the base addresses of all modules.
- **Cyclone V SoC HPS Address Map and Register Definitions**
  Web-based address map and register definitions

L3 (NIC-301) GPV Registers Address Map

Registers to control L3 interconnect settings

Base Address: `0xFF800000`

L3 (NIC-301) GPV Registers

Register	Offset	Width	Access	Reset Value	Description
remap on page 7-23	0x0	32	WO	0x0	Remap

Security Register Group

Register	Offset	Width	Access	Reset Value	Description
l4main on page 7-26	0x8	32	WO	0x0	L4 main peripherals security
l4sp on page 7-27	0xC	32	WO	0x0	L4 SP Peripherals Security
l4mp on page 7-30	0x10	32	WO	0x0	L4 MP Peripherals Security
l4osc1 on page 7-33	0x14	32	WO	0x0	L4 OSC1 Peripherals Security
l4spim on page 7-35	0x18	32	WO	0x0	L4 SPIM Peripherals Security
stm on page 7-36	0x1C	32	WO	0x0	STM Peripheral Security
lwhps2fpgaregs on page 7-37	0x20	32	WO	0x0	LWHPS2FPGA AXI Bridge Registers Peripheral Security

Register	Offset	Width	Access	Reset Value	Description
usb1 on page 7-38	0x28	32	WO	0x0	USB1 Registers Peripheral Security
nanddata on page 7-38	0x2C	32	WO	0x0	NAND Flash Controller Data Peripheral Security
usb0 on page 7-39	0x80	32	WO	0x0	USB0 Registers Peripheral Security
nandregs on page 7-40	0x84	32	WO	0x0	NAND Flash Controller Registers Peripheral Security
qspidata on page 7-40	0x88	32	WO	0x0	QSPI Flash Controller Data Peripheral Security
fpgamgrdata on page 7-41	0x8C	32	WO	0x0	FPGA Manager Data Peripheral Security
hps2fpgaregs on page 7-42	0x90	32	WO	0x0	HPS2FPGA AXI Bridge Registers Peripheral Security
acp on page 7-42	0x94	32	WO	0x0	MPU ACP Peripheral Security
rom on page 7-43	0x98	32	WO	0x0	ROM Peripheral Security
ocram on page 7-44	0x9C	32	WO	0x0	On-chip RAM Peripheral Security
sdrdata on page 7-44	0xA0	32	WO	0x0	SDRAM Data Peripheral Security

ID Register Group

Register	Offset	Width	Access	Reset Value	Description
periph_id_4 on page 7-46	0x1FD0	32	RO	0x4	Peripheral ID4 Register
periph_id_0 on page 7-46	0x1FE0	32	RO	0x1	Peripheral ID0 Register
periph_id_1 on page 7-47	0x1FE4	32	RO	0xB3	Peripheral ID1 Register
periph_id_2 on page 7-47	0x1FE8	32	RO	0x6B	Peripheral ID2 Register
periph_id_3 on page 7-47	0x1FEC	32	RO	0x0	Peripheral ID3 Register
comp_id_0 on page 7-48	0x1FF0	32	RO	0xD	Component ID0 Register
comp_id_1 on page 7-48	0x1FF4	32	RO	0xF0	Component ID1 Register
comp_id_2 on page 7-49	0x1FF8	32	RO	0x5	Component ID2 Register
comp_id_3 on page 7-49	0x1FFC	32	RO	0xB1	Component ID3 Register

L4 MAIN

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-50	0x2008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register

L4 SP

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-51	0x3008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register

L4 MP

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-52	0x4008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register

L4 OSC1

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-53	0x5008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register

L4 SPIM

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-54	0x6008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register

STM

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-55	0x7008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
fn_mod on page 7-56	0x7108	32	RW	0x0	Issuing Functionality Modification Register

LWHPS2FPGA

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-57	0x8008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
fn_mod on page 7-57	0x8108	32	RW	0x0	Issuing Functionality Modification Register

USB1

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-58	0xA008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register

Register	Offset	Width	Access	Reset Value	Description
ahb_cntl on page 7-59	0xA044	32	RW	0x0	AHB Control Register

NANDDATA

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-60	0xB008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
fn_mod on page 7-61	0xB108	32	RW	0x0	Issuing Functionality Modification Register

USB0

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-62	0x20008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
ahb_cntl on page 7-62	0x20044	32	RW	0x0	AHB Control Register

NANDREGS

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-64	0x21008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
fn_mod on page 7-64	0x21108	32	RW	0x0	Issuing Functionality Modification Register

QSPIDATA

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-65	0x22008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
ahb_cntl on page 7-66	0x22044	32	RW	0x0	AHB Control Register

FPGAMGRDATA

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-67	0x23008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
wr_tidemark on page 7-68	0x23040	32	RW	0x4	Write Tidemark
fn_mod on page 7-69	0x23108	32	RW	0x0	Issuing Functionality Modification Register

HPS2FPGA

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-70	0x24008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
wr_tidemark on page 7-70	0x24040	32	RW	0x4	Write Tidemark
fn_mod on page 7-71	0x24108	32	RW	0x0	Issuing Functionality Modification Register

ACP

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-72	0x25008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
fn_mod on page 7-72	0x25108	32	RW	0x0	Issuing Functionality Modification Register

Boot ROM

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-73	0x26008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
fn_mod on page 7-74	0x26108	32	RW	0x0	Issuing Functionality Modification Register

On-chip RAM

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 7-75	0x27008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
wr_tidemark on page 7-76	0x27040	32	RW	0x4	Write Tidemark
fn_mod on page 7-76	0x27108	32	RW	0x0	Issuing Functionality Modification Register

DAP

Register	Offset	Width	Access	Reset Value	Description
fn_mod2 on page 7-78	0x42024	32	RW	0x0	Functionality Modification 2 Register
fn_mod_ahb on page 7-78	0x42028	32	RW	0x0	Functionality Modification AHB Register
read_qos on page 7-79	0x42100	32	RW	0x0	Read Channel QoS Value
write_qos on page 7-80	0x42104	32	RW	0x0	Write Channel QoS Value

Register	Offset	Width	Access	Reset Value	Description
fn_mod on page 7-80	0x42108	32	RW	0x0	Issuing Functionality Modification Register

MPU

Register	Offset	Width	Access	Reset Value	Description
read_qos on page 7-81	0x43100	32	RW	0x0	Read Channel QoS Value
write_qos on page 7-82	0x43104	32	RW	0x0	Write Channel QoS Value
fn_mod on page 7-82	0x43108	32	RW	0x0	Issuing Functionality Modification Register

SDMMC

Register	Offset	Width	Access	Reset Value	Description
fn_mod_ahb on page 7-83	0x44028	32	RW	0x0	Functionality Modification AHB Register
read_qos on page 7-84	0x44100	32	RW	0x0	Read Channel QoS Value
write_qos on page 7-85	0x44104	32	RW	0x0	Write Channel QoS Value
fn_mod on page 7-85	0x44108	32	RW	0x0	Issuing Functionality Modification Register

DMA

Register	Offset	Width	Access	Reset Value	Description
read_qos on page 7-86	0x45100	32	RW	0x0	Read Channel QoS Value
write_qos on page 7-87	0x45104	32	RW	0x0	Write Channel QoS Value
fn_mod on page 7-87	0x45108	32	RW	0x0	Issuing Functionality Modification Register

FPGA2HPS

Register	Offset	Width	Access	Reset Value	Description
wr_tidemark on page 7-88	0x46040	32	RW	0x4	Write Tidemark
read_qos on page 7-89	0x46100	32	RW	0x0	Read Channel QoS Value
write_qos on page 7-89	0x46104	32	RW	0x0	Write Channel QoS Value
fn_mod on page 7-90	0x46108	32	RW	0x0	Issuing Functionality Modification Register

ETR

Register	Offset	Width	Access	Reset Value	Description
read_qos on page 7-91	0x47100	32	RW	0x0	Read Channel QoS Value
write_qos on page 7-91	0x47104	32	RW	0x0	Write Channel QoS Value
fn_mod on page 7-92	0x47108	32	RW	0x0	Issuing Functionality Modification Register

EMAC0

Register	Offset	Width	Access	Reset Value	Description
read_qos on page 7-93	0x48100	32	RW	0x0	Read Channel QoS Value
write_qos on page 7-93	0x48104	32	RW	0x0	Write Channel QoS Value
fn_mod on page 7-94	0x48108	32	RW	0x0	Issuing Functionality Modification Register

EMAC1

Register	Offset	Width	Access	Reset Value	Description
read_qos on page 7-95	0x49100	32	RW	0x0	Read Channel QoS Value
write_qos on page 7-95	0x49104	32	RW	0x0	Write Channel QoS Value
fn_mod on page 7-96	0x49108	32	RW	0x0	Issuing Functionality Modification Register

USB0

Register	Offset	Width	Access	Reset Value	Description
fn_mod_ahb on page 7-97	0x4A028	32	RW	0x0	Functionality Modification AHB Register
read_qos on page 7-98	0x4A100	32	RW	0x0	Read Channel QoS Value
write_qos on page 7-99	0x4A104	32	RW	0x0	Write Channel QoS Value
fn_mod on page 7-99	0x4A108	32	RW	0x0	Issuing Functionality Modification Register

NAND

Register	Offset	Width	Access	Reset Value	Description
read_qos on page 7-100	0x4B100	32	RW	0x0	Read Channel QoS Value
write_qos on page 7-100	0x4B104	32	RW	0x0	Write Channel QoS Value
fn_mod on page 7-101	0x4B108	32	RW	0x0	Issuing Functionality Modification Register

USB1

Register	Offset	Width	Access	Reset Value	Description
fn_mod_ahb on page 7-102	0x4C028	32	RW	0x0	Functionality Modification AHB Register
read_qos on page 7-103	0x4C100	32	RW	0x0	Read Channel QoS Value
write_qos on page 7-104	0x4C104	32	RW	0x0	Write Channel QoS Value
fn_mod on page 7-104	0x4C108	32	RW	0x0	Issuing Functionality Modification Register

remap

The L3 interconnect has separate address maps for the various L3 Masters. Generally, the addresses are the same for most masters. However, the sparse interconnect of the L3 switch causes some masters to have holes in their memory maps. The remap bits are not mutually exclusive. Each bit can be set independently and in combinations. Priority for the bits is determined by the bit offset: lower offset bits take precedence over higher offset bits.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800000

Offset: 0x0

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											lwhps2fpga WO 0x0	hps2fpga WO 0x0	Reserved	nonmpuzero WO 0x0	mpuzero WO 0x0

remap Fields

Bit	Name	Description	Access	Reset
4	lwhps2fpga	Controls whether the Lightweight HPS2FPGA AXI Bridge is visible to L3 masters or not. **Value** — **Description** 0x0 — The LWHPS2FPGA AXI Bridge is not visible to L3 masters. Accesses to the associated address range return an AXI decode error to the master. 0x1 — The LWHPS2FPGA AXI Bridge is visible to L3 masters.	WO	0x0
3	hps2fpga	Controls whether the HPS2FPGA AXI Bridge is visible to L3 masters or not. **Value** — **Description** 0x0 — The HPS2FPGA AXI Bridge is not visible to L3 masters. Accesses to the associated address range return an AXI decode error to the master. 0x1 — The HPS2FPGA AXI Bridge is visible to L3 masters.	WO	0x0
1	nonmpuzero	Controls the mapping of address 0x0 for L3 masters other than the MPU. Determines whether address 0x0 for these masters is mapped to the SDRAM or on-chip RAM. Only affects the following masters: DMA controllers (standalone and those built in to peripherals) , FPGA-to-HPS Bridge, and DAP. **Value** — **Description** 0x0 — Maps the SDRAM to address 0x0 for the non-MPU L3 masters. 0x1 — Maps the On-chip RAM to address 0x0 for the non-MPU L3 masters. Note that the On-chip RAM is also always mapped to address 0xffff_0000 for the non-MPU L3 masters independent of this field's value.	WO	0x0

Bit	Name	Description	Access	Reset
0	mpuzero	Controls whether address 0x0 for the MPU L3 master is mapped to the Boot ROM or On-chip RAM. This field only has an effect on the MPU L3 master. **Value** — **Description** 0x0 — Maps the Boot ROM to address 0x0 for the MPU L3 master. Note that the Boot ROM is also always mapped to address 0xfffd_0000 for the MPU L3 master independent of this field's value. 0x1 — Maps the On-chip RAM to address 0x0 for the MPU L3 master. Note that the On-chip RAM is also always mapped to address 0xffff_0000 for the MPU L3 master independent of this field's value.	WO	0x0

Security Register Group Register Descriptions

Registers that control slave security.

Offset: 0x8

l4main on page 7-26
Controls security settings for L4 main peripherals

l4sp on page 7-27
Controls security settings for L4 SP peripherals.

l4mp on page 7-30
Controls security settings for L4 MP peripherals.

l4osc1 on page 7-33
Controls security settings for L4 OSC1 peripherals.

l4spim on page 7-35
Controls security settings for L4 SPIM peripherals.

stm on page 7-36
Controls security settings for STM peripheral.

lwhps2fpgaregs on page 7-37
Controls security settings for LWHPS2FPGA AXI Bridge Registers peripheral.

usb1 on page 7-38
Controls security settings for USB1 Registers peripheral.

nanddata on page 7-38
Controls security settings for NAND Flash Controller Data peripheral.

usb0 on page 7-39
Controls security settings for USB0 Registers peripheral.

nandregs on page 7-40
Controls security settings for NAND Flash Controller Registers peripheral.

qspidata on page 7-40
Controls security settings for QSPI Flash Controller Data peripheral.

fpgamgrdata on page 7-41
Controls security settings for FPGA Manager Data peripheral.

hps2fpgaregs on page 7-42
Controls security settings for HPS2FPGA AXI Bridge Registers peripheral.

acp on page 7-42
Controls security settings for MPU ACP peripheral.

rom on page 7-43
Controls security settings for ROM peripheral.

ocram on page 7-44
Controls security settings for On-chip RAM peripheral.

sdrdata on page 7-44
Controls security settings for SDRAM Data peripheral.

l4main

Controls security settings for L4 main peripherals

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800008

Offset: 0x8

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												dmanonsecure WO 0x0	dmasecure WO 0x0	spis1 WO 0x0	spis0 WO 0x0

l4main Fields

Bit	Name	Description	Access	Reset
3	dmanonsecure	Controls whether secure or non-secure masters can access the DMA Non-secure slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
2	dmasecure	Controls whether secure or non-secure masters can access the DMA Secure slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
1	spis1	Controls whether secure or non-secure masters can access the SPI Slave 1 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
0	spis0	Controls whether secure or non-secure masters can access the SPI Slave 0 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

l4sp

Controls security settings for L4 SP peripherals.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF80000C

Offset: 0xC

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					sptimer1 WO 0x0	can1 WO 0x0	can0 WO 0x0	uart1 WO 0x0	uart0 WO 0x0	i2c3 WO 0x0	i2c2 WO 0x0	i2c1 WO 0x0	i2c0 WO 0x0	sptimer0 WO 0x0	sdrregs WO 0x0

l4sp Fields

Bit	Name	Description	Access	Reset
10	sptimer1	Controls whether secure or non-secure masters can access the SP Timer 1 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
9	can1	Controls whether secure or non-secure masters can access the CAN 1 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
8	can0	Controls whether secure or non-secure masters can access the CAN 0 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

Bit	Name	Description	Access	Reset
7	uart1	Controls whether secure or non-secure masters can access the UART 1 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
6	uart0	Controls whether secure or non-secure masters can access the UART 0 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
5	i2c3	Controls whether secure or non-secure masters can access the I2C3 (EMAC 1) slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
4	i2c2	Controls whether secure or non-secure masters can access the I2C2 (EMAC 0) slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
3	i2c1	Controls whether secure or non-secure masters can access the I2C1 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

Bit	Name	Description	Access	Reset
2	i2c0	Controls whether secure or non-secure masters can access the I2C0 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
1	sptimer0	Controls whether secure or non-secure masters can access the SP Timer 0 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
0	sdrregs	Controls whether secure or non-secure masters can access the SDRAM Registers slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

l4mp

Controls security settings for L4 MP peripherals.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800010

Offset: 0x10

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						gpio2 WO 0x0	gpio1 WO 0x0	gpio0 WO 0x0	acpidmap WO 0x0	emac1 WO 0x0	emac0 WO 0x0	sdmmc WO 0x0	qspiregs WO 0x0	dap WO 0x0	fpgamgrregs WO 0x0

l4mp Fields

Bit	Name	Description	Access	Reset
9	gpio2	Controls whether secure or non-secure masters can access the GPIO 2 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
8	gpio1	Controls whether secure or non-secure masters can access the GPIO 1 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
7	gpio0	Controls whether secure or non-secure masters can access the GPIO 0 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

Bit	Name	Description	Access	Reset
6	acpidmap	Controls whether secure or non-secure masters can access the ACP ID Mapper slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
5	emac1	Controls whether secure or non-secure masters can access the EMAC 1 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
4	emac0	Controls whether secure or non-secure masters can access the EMAC 0 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
3	sdmmc	Controls whether secure or non-secure masters can access the SDMMC slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
2	qspiregs	Controls whether secure or non-secure masters can access the QSPI Registers slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

Bit	Name	Description	Access	Reset
1	dap	Controls whether secure or non-secure masters can access the DAP slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
0	fpgamgrregs	Controls whether secure or non-secure masters can access the FPGA Manager Register slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

l4osc1

Controls security settings for L4 OSC1 peripherals.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800014

Offset: 0x14

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									osc1timer1 WO 0x0	osc1timer0 WO 0x0	sysmgr WO 0x0	rstmgr WO 0x0	clkmgr WO 0x0	l4wd1 WO 0x0	l4wd0 WO 0x0

l4osc1 Fields

Bit	Name	Description	Access	Reset
6	osc1timer1	Controls whether secure or non-secure masters can access the OSC1 Timer 1 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
5	osc1timer0	Controls whether secure or non-secure masters can access the OSC1 Timer 0 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
4	sysmgr	Controls whether secure or non-secure masters can access the System Manager slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
3	rstmgr	Controls whether secure or non-secure masters can access the Reset Manager slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

Bit	Name	Description	Access	Reset
2	clkmgr	Controls whether secure or non-secure masters can access the Clock Manager slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
1	l4wd1	Controls whether secure or non-secure masters can access the L4 Watchdog Timer 0 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
0	l4wd0	Controls whether secure or non-secure masters can access the L4 Watchdog Timer 0 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

l4spim

Controls security settings for L4 SPIM peripherals.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800018

Offset: 0x18

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													scanmgr WO 0x0	spim1 WO 0x0	spim0 WO 0x0

l4spim Fields

Bit	Name	Description	Access	Reset
2	scanmgr	Controls whether secure or non-secure masters can access the Scan Manager slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
1	spim1	Controls whether secure or non-secure masters can access the SPI Master 1 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0
0	spim0	Controls whether secure or non-secure masters can access the SPI Master 0 slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

stm

Controls security settings for STM peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF80001C

Offset: 0x1C

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

stm Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the STM slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

lwhps2fpgaregs

Controls security settings for LWHPS2FPGA AXI Bridge Registers peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800020

Offset: 0x20

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

lwhps2fpgaregs Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the LWHPS2FPGA AXI Bridge Registers slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

usb1

Controls security settings for USB1 Registers peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800028

Offset: 0x28

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

usb1 Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the USB1 Registers slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

nanddata

Controls security settings for NAND Flash Controller Data peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF80002C

Offset: 0x2C

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

nanddata Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the NAND Flash Controller Data slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

usb0

Controls security settings for USB0 Registers peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800080

Offset: 0x80

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

usb0 Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the USB0 Registers slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

nandregs

Controls security settings for NAND Flash Controller Registers peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800084

Offset: 0x84

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

nandregs Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the NAND Flash Controller Registers slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

qspidata

Controls security settings for QSPI Flash Controller Data peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800088

Offset: 0x88

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

qspidata Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the QSPI Flash Controller Data slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

fpgamgrdata

Controls security settings for FPGA Manager Data peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF80008C

Offset: 0x8C

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

fpgamgrdata Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the FPGA Manager Data slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

hps2fpgaregs

Controls security settings for HPS2FPGA AXI Bridge Registers peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800090

Offset: 0x90

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

hps2fpgaregs Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the HPS2FPGA AXI Bridge Registers slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

acp

Controls security settings for MPU ACP peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800094

Offset: 0x94

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

acp Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the MPU ACP slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

rom

Controls security settings for ROM peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF800098

Offset: 0x98

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

rom Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the ROM slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

ocram

Controls security settings for On-chip RAM peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF80009C

Offset: 0x9C

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

ocram Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the On-chip RAM slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

sdrdata

Controls security settings for SDRAM Data peripheral.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF8000A0

Offset: 0xA0

Access: WO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															s WO 0x0

sdrdata Fields

Bit	Name	Description	Access	Reset
0	s	Controls whether secure or non-secure masters can access the SDRAM Data slave. **Value** — **Description** 0x0 — The slave can only be accessed by a secure master. 0x1 — The slave can only be accessed by a secure or non-secure masters.	WO	0x0

ID Register Group Register Descriptions

Contains registers that identify the ARM NIC-301 IP Core.

Offset: 0x1000

comp_id_3 on page 7-49
Component ID3

periph_id_4

JEP106 continuation code

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF801FD0

Offset: 0x1FD0

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								periph_id_4 RO 0x4							

periph_id_4 Fields

Bit	Name	Description	Access	Reset
7:0	periph_id_4	JEP106 continuation code	RO	0x4

periph_id_0

Peripheral ID0

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF801FE0

Offset: 0x1FE0

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								pn7to0 RO 0x1							

periph_id_0 Fields

Bit	Name	Description	Access	Reset
7:0	pn7to0	Part Number [7:0]	RO	0x1

periph_id_1

Peripheral ID1

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF801FE4

Offset: 0x1FE4

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								jep3to0_pn11to8 RO 0xB3							

periph_id_1 Fields

Bit	Name	Description	Access	Reset
7:0	jep3to0_pn11to8	JEP106[3:0], Part Number [11:8]	RO	0xB3

periph_id_2

Peripheral ID2

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF801FE8

Offset: 0x1FE8

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								rev_jepcode_jep6to4 RO 0x6B							

periph_id_2 Fields

Bit	Name	Description	Access	Reset
7:0	rev_jepcode_jep6to4	Revision, JEP106 code flag, JEP106[6:4]	RO	0x6B

periph_id_3

Peripheral ID3

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF801FEC

Offset: 0x1FEC

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								rev_and RO 0x0				cust_mod_num RO 0x0			

periph_id_3 Fields

Bit	Name	Description	Access	Reset
7:4	rev_and	Revision	RO	0x0
3:0	cust_mod_num	Customer Model Number	RO	0x0

comp_id_0

Component ID0

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF801FF0

Offset: 0x1FF0

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0xD							

comp_id_0 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0xD

comp_id_1

Component ID1

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF801FF4

Offset: 0x1FF4

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								genipcompcls_preamble RO 0xF0							

comp_id_1 Fields

Bit	Name	Description	Access	Reset
7:0	genipcompcls_preamble	Generic IP component class, Preamble	RO	0xF0

comp_id_2

Component ID2

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF801FF8

Offset: 0x1FF8

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0x5							

comp_id_2 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0x5

comp_id_3

Component ID3

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF801FFC

Offset: 0x1FFC

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0xB1							

comp_id_3 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0xB1

Master Register Group Register Descriptions

Registers associated with master interfaces in the L3 Interconnect. Note that a master in the L3 Interconnect connects to a slave in a module.

Offset: 0x2000

L4 MAIN Register Descriptions

Registers associated with the L4 MAIN master. This master is used to access the APB slaves on the L4 MAIN bus.

Offset: 0x0

fn_mod_bm_iss on page 7-50
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF802008

Offset: 0x2008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	Value: Description 0x0: Multiple outstanding write transactions 0x1: Only a single outstanding write transaction	RW	0x0
0	rd	Value: Description 0x0: Multiple outstanding read transactions 0x1: Only a single outstanding read transaction	RW	0x0

L4 SP Register Descriptions

Registers associated with the L4 SP master. This master is used to access the APB slaves on the L4 SP bus.

Offset: 0x1000

fn_mod_bm_iss on page 7-51
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF803008

Offset: 0x3008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	Value: 0x0 — Multiple outstanding write transactions Value: 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	Value: 0x0 — Multiple outstanding read transactions Value: 0x1 — Only a single outstanding read transaction	RW	0x0

L4 MP Register Descriptions

Registers associated with the L4 MP master. This master is used to access the APB slaves on the L4 MP bus.

Offset: 0x2000

fn_mod_bm_iss on page 7-52
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF804008

Offset: 0x4008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	Value: Description 0x0: Multiple outstanding write transactions 0x1: Only a single outstanding write transaction	RW	0x0
0	rd	Value: Description 0x0: Multiple outstanding read transactions 0x1: Only a single outstanding read transaction	RW	0x0

L4 OSC1 Register Descriptions

Registers associated with the L4 OSC1 master. This master is used to access the APB slaves on the L4 OSC1 bus.

Offset: 0x3000

fn_mod_bm_iss on page 7-53
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF805008

Offset: 0x5008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	Value: 0x0 — Multiple outstanding write transactions Value: 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	Value: 0x0 — Multiple outstanding read transactions Value: 0x1 — Only a single outstanding read transaction	RW	0x0

L4 SPIM Register Descriptions

Registers associated with the L4 SPIM master. This master is used to access the APB slaves on the L4 SPIM bus.

Offset: 0x4000

fn_mod_bm_iss on page 7-54
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF806008

Offset: 0x6008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	Value: Description 0x0: Multiple outstanding write transactions 0x1: Only a single outstanding write transaction	RW	0x0
0	rd	Value: Description 0x0: Multiple outstanding read transactions 0x1: Only a single outstanding read transaction	RW	0x0

STM Register Descriptions

Registers associated with the STM master. This master is used to access the STM AXI slave.

Offset: 0x5000

fn_mod_bm_iss on page 7-55
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

fn_mod on page 7-56
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF807008

Offset: 0x7008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	Value: 0x0 — Multiple outstanding write transactions Value: 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	Value: 0x0 — Multiple outstanding read transactions Value: 0x1 — Only a single outstanding read transaction	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF807108

Offset: 0x7108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	Value: 0x0 — Multiple outstanding write transactions Value: 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	Value: 0x0 — Multiple outstanding read transactions Value: 0x1 — Only a single outstanding read transaction	RW	0x0

LWHPS2FPGA Register Descriptions

Registers associated with the LWHPS2FPGA AXI Bridge master. This master is used to access the LWHPS2FPGA AXI Bridge slave. This slave is used to access the registers for all 3 AXI bridges and to access slaves in the FPGA connected to the LWHPS2FPGA AXI Bridge.

Offset: `0x6000`

fn_mod_bm_iss on page 7-57
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

fn_mod on page 7-57
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF808008

Offset: `0x8008`

Access: `RW`

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 — Multiple outstanding read transactions 0x1 — Only a single outstanding read transaction	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF808108

Offset: 0x8108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	Value: Description 0x0: Multiple outstanding write transactions 0x1: Only a single outstanding write transaction	RW	0x0
0	rd	Value: Description 0x0: Multiple outstanding read transactions 0x1: Only a single outstanding read transaction	RW	0x0

USB1 Register Descriptions

Registers associated with the USB1 master. This master is used to access the registers in USB1.

Offset: 0x8000

fn_mod_bm_iss on page 7-58
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

ahb_cntl on page 7-59
Sets the block issuing capability to one outstanding transaction.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF80A008

Offset: 0xA008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

ahb_cntl

Sets the block issuing capability to one outstanding transaction.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF80A044

Offset: 0xA044

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														force_incr RW 0x0	decerr_en RW 0x0

ahb_cntl Fields

Bit	Name	Description	Access	Reset
1	force_incr	**Value** / **Description** 0x0 Multiple outstanding write transactions 0x1 If a beat is received that has no write data strobes set, that write data beat is replaced with an IDLE beat. Also, causes all transactions that are to be output to the AHB domain to be an undefined length INCR.	RW	0x0
0	decerr_en	**Value** / **Description** 0x0 No DECERR response. 0x1 If the AHB protocol conversion function receives an unaligned address or a write data beat without all the byte strobes set, creates a DECERR response.	RW	0x0

NANDDATA Register Descriptions

Registers associated with the NANDDATA master. This master is used to access data in the NAND flash controller.

Offset: 0x9000

fn_mod_bm_iss on page 7-60
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

fn_mod on page 7-61
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF80B008

Offset: 0xB008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	Value: 0x0 — Multiple outstanding write transactions Value: 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	Value: 0x0 — Multiple outstanding read transactions Value: 0x1 — Only a single outstanding read transaction	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF80B108

Offset: 0xB108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	Value: 0x0 — Multiple outstanding write transactions Value: 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	Value: 0x0 — Multiple outstanding read transactions Value: 0x1 — Only a single outstanding read transaction	RW	0x0

USB0 Register Descriptions

Registers associated with the USB0 master. This master is used to access the registers in USB0.

Offset: `0x1e000`

fn_mod_bm_iss on page 7-62
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

ahb_cntl on page 7-62
Sets the block issuing capability to one outstanding transaction.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF820008

Offset: `0x20008`

Access: `RW`

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	Value: Description 0x0: Multiple outstanding write transactions 0x1: Only a single outstanding write transaction	RW	0x0
0	rd	Value: Description 0x0: Multiple outstanding read transactions 0x1: Only a single outstanding read transaction	RW	0x0

ahb_cntl

Sets the block issuing capability to one outstanding transaction.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF820044

Offset: 0x20044

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														force_incr RW 0x0	decerr_en RW 0x0

ahb_cntl Fields

Bit	Name	Description	Access	Reset
1	force_incr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — If a beat is received that has no write data strobes set, that write data beat is replaced with an IDLE beat. Also, causes all transactions that are to be output to the AHB domain to be an undefined length INCR.	RW	0x0
0	decerr_en	**Value** / **Description** 0x0 — No DECERR response. 0x1 — If the AHB protocol conversion function receives an unaligned address or a write data beat without all the byte strobes set, creates a DECERR response.	RW	0x0

NANDREGS Register Descriptions

Registers associated with the NANDREGS master. This master is used to access the registers in the NAND flash controller.

Offset: 0x1f000

fn_mod_bm_iss on page 7-64
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

fn_mod on page 7-64
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF821008

Offset: 0x21008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF821108

Offset: 0x21108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

QSPIDATA Register Descriptions

Registers associated with the QSPIDATA master. This master is used to access data in the QSPI flash controller.

Offset: 0x20000

fn_mod_bm_iss on page 7-65
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

ahb_cntl on page 7-66
Sets the block issuing capability to one outstanding transaction.

fn_mod_bm_iss
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF822008

Offset: 0x22008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

ahb_cntl

Sets the block issuing capability to one outstanding transaction.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF822044

Offset: 0x22044

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														force_incr RW 0x0	decerr_en RW 0x0

ahb_cntl Fields

Bit	Name	Description	Access	Reset
1	force_incr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — If a beat is received that has no write data strobes set, that write data beat is replaced with an IDLE beat. Also, causes all transactions that are to be output to the AHB domain to be an undefined length INCR.	RW	0x0
0	decerr_en	**Value** / **Description** 0x0 — No DECERR response. 0x1 — If the AHB protocol conversion function receives an unaligned address or a write data beat without all the byte strobes set, creates a DECERR response.	RW	0x0

FPGAMGRDATA Register Descriptions

Registers associated with the FPGAMGRDATA master. This master is used to send FPGA configuration image data to the FPGA Manager.

Offset: 0x21000

fn_mod_bm_iss on page 7-67
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

wr_tidemark on page 7-68
Controls the release of the transaction in the write data FIFO.

fn_mod on page 7-69
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF823008

Offset: 0x23008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

wr_tidemark

Controls the release of the transaction in the write data FIFO.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF823040

Offset: 0x23040

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												level RW 0x4			

wr_tidemark Fields

Bit	Name	Description	Access	Reset
3:0	level	Stalls the transaction in the write data FIFO until the number of occupied slots in the write data FIFO exceeds the level. Note that the transaction is released before this level is achieved if the network receives the WLAST beat or the write FIFO becomes full.	RW	0x4

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF823108

Offset: 0x23108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	Value: Description 0x0: Multiple outstanding write transactions 0x1: Only a single outstanding write transaction	RW	0x0
0	rd	Value: Description 0x0: Multiple outstanding read transactions 0x1: Only a single outstanding read transaction	RW	0x0

HPS2FPGA Register Descriptions

Registers associated with the HPS2FPGA AXI Bridge master. This master is used to access the HPS2FPGA AXI Bridge slave. This slave is used to access slaves in the FPGA connected to the HPS2FPGA AXI Bridge.

Offset: 0x22000

fn_mod_bm_iss on page 7-70
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

wr_tidemark on page 7-70
Controls the release of the transaction in the write data FIFO.

fn_mod on page 7-71
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF824008

Offset: 0x24008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	Value: 0x0 — Multiple outstanding write transactions Value: 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	Value: 0x0 — Multiple outstanding read transactions Value: 0x1 — Only a single outstanding read transaction	RW	0x0

wr_tidemark

Controls the release of the transaction in the write data FIFO.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF824040

Offset: 0x24040

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												level RW 0x4			

wr_tidemark Fields

Bit	Name	Description	Access	Reset
3:0	level	Stalls the transaction in the write data FIFO until the number of occupied slots in the write data FIFO exceeds the level. Note that the transaction is released before this level is achieved if the network receives the WLAST beat or the write FIFO becomes full.	RW	0x4

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF824108

Offset: 0x24108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 — Multiple outstanding read transactions 0x1 — Only a single outstanding read transaction	RW	0x0

ACP Register Descriptions

Registers associated with the ACP master. This master is used to access the MPU ACP slave via the ACP ID Mapper.

Offset: 0x23000

fn_mod_bm_iss on page 7-72
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

fn_mod on page 7-72
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF825008

Offset: 0x25008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 — Multiple outstanding read transactions 0x1 — Only a single outstanding read transaction	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF825108

Offset: 0x25108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

Boot ROM Register Descriptions

Registers associated with the Boot ROM master. This master is used to access the contents of the Boot ROM.

Offset: 0x24000

fn_mod_bm_iss on page 7-73
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

fn_mod on page 7-74
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF826008

Offset: 0x26008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF826108

Offset: 0x26108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	Value: 0x0 — Multiple outstanding write transactions; 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	Value: 0x0 — Multiple outstanding read transactions; 0x1 — Only a single outstanding read transaction	RW	0x0

On-chip RAM Register Descriptions

Registers associated with the On-chip RAM master. This master is used to access the contents of the On-chip RAM.

Offset: 0x25000

fn_mod_bm_iss on page 7-75
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

wr_tidemark on page 7-76
Controls the release of the transaction in the write data FIFO.

fn_mod on page 7-76
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF827008

Offset: 0x27008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	Value: 0x0 — Multiple outstanding write transactions Value: 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	Value: 0x0 — Multiple outstanding read transactions Value: 0x1 — Only a single outstanding read transaction	RW	0x0

wr_tidemark

Controls the release of the transaction in the write data FIFO.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF827040

Offset: 0x27040

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												level RW 0x4			

wr_tidemark Fields

Bit	Name	Description	Access	Reset
3:0	level	Stalls the transaction in the write data FIFO until the number of occupied slots in the write data FIFO exceeds the level. Note that the transaction is released before this level is achieved if the network receives the WLAST beat or the write FIFO becomes full.	RW	0x4

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF827108

Offset: 0x27108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	Value: Description 0x0: Multiple outstanding write transactions 0x1: Only a single outstanding write transaction	RW	0x0
0	rd	Value: Description 0x0: Multiple outstanding read transactions 0x1: Only a single outstanding read transaction	RW	0x0

Slave Register Group Register Descriptions

Registers associated with slave interfaces.

Offset: 0x42000

DAP Register Descriptions

Registers associated with the DAP slave interface. This slave is used by the DAP to access slaves attached to the L3/L4 Interconnect.

Offset: 0x0

fn_mod2 on page 7-78
Controls bypass merge of upsizing/downsizing.

fn_mod_ahb on page 7-78
Controls how AHB-lite burst transactions are converted to AXI tranactions.

read_qos on page 7-79
QoS (Quality of Service) value for the read channel.

write_qos on page 7-80
QoS (Quality of Service) value for the write channel.

fn_mod on page 7-80
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod2

Controls bypass merge of upsizing/downsizing.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF842024

Offset: 0x42024

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															bypass_merge RW 0x0

fn_mod2 Fields

Bit	Name	Description	Access	Reset
0	bypass_merge	Controls bypass merge of upsizing/downsizing. Value: Description 0x0: The network can alter transactions. 0x1: The network does not alter any transactions that could pass through the upsizer legally without alteration.	RW	0x0

fn_mod_ahb

Controls how AHB-lite burst transactions are converted to AXI tranactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF842028

Offset: 0x42028

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr_incr_override RW 0x0	rd_incr_override RW 0x0

fn_mod_ahb Fields

Bit	Name	Description	Access	Reset
1	wr_incr_override	Controls how AHB-lite write burst transactions are converted to AXI tranactions. **Value** — **Description** 0x0 — The L3 Interconnect converts AHB-lite write bursts to AXI transactions in accordance with the default behavior as specified in the ARM NIC-301 documentation. 0x1 — The L3 Interconnect converts AHB-lite write bursts to AXI single transactions.	RW	0x0
0	rd_incr_override	Controls how AHB-lite read burst transactions are converted to AXI tranactions. **Value** — **Description** 0x0 — The L3 Interconnect converts AHB-lite read bursts to AXI transactions in accordance with the default behavior as specified in the ARM NIC-301 documentation. 0x1 — The L3 Interconnect converts AHB-lite read bursts to AXI single transactions.	RW	0x0

read_qos

QoS (Quality of Service) value for the read channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF842100

Offset: 0x42100

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

read_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the read channel. A higher value has a higher priority.	RW	0x0

write_qos

QoS (Quality of Service) value for the write channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF842104

Offset: 0x42104

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

write_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the write channel. A higher value has a higher priority.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF842108

Offset: 0x42108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

MPU Register Descriptions

Registers associated with the MPU slave interface. This slave is used by the MPU to access slaves attached to the L3/L4 Interconnect.

Offset: 0x1000

read_qos on page 7-81
QoS (Quality of Service) value for the read channel.

write_qos on page 7-82
QoS (Quality of Service) value for the write channel.

fn_mod on page 7-82
Sets the block issuing capability to multiple or single outstanding transactions.

read_qos
QoS (Quality of Service) value for the read channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF843100

Offset: 0x43100

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

read_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the read channel. A higher value has a higher priority.	RW	0x0

write_qos

QoS (Quality of Service) value for the write channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF843104

Offset: 0x43104

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

write_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the write channel. A higher value has a higher priority.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF843108

Offset: 0x43108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	Value: Description 0x0: Multiple outstanding write transactions 0x1: Only a single outstanding write transaction	RW	0x0
0	rd	Value: Description 0x0: Multiple outstanding read transactions 0x1: Only a single outstanding read transaction	RW	0x0

SDMMC Register Descriptions

Registers associated with the SDMMC slave interface. This slave is used by the DMA controller built into the SDMMC to access slaves attached to the L3/L4 Interconnect.

Offset: 0x2000

fn_mod_ahb on page 7-83
Controls how AHB-lite burst transactions are converted to AXI tranactions.

read_qos on page 7-84
QoS (Quality of Service) value for the read channel.

write_qos on page 7-85
QoS (Quality of Service) value for the write channel.

fn_mod on page 7-85
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_ahb

Controls how AHB-lite burst transactions are converted to AXI tranactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF844028

Offset: 0x44028

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr_incr_override RW 0x0	rd_incr_override RW 0x0

fn_mod_ahb Fields

Bit	Name	Description	Access	Reset
1	wr_incr_override	Controls how AHB-lite write burst transactions are converted to AXI tranactions. **Value** **Description** 0x0 The L3 Interconnect converts AHB-lite write bursts to AXI transactions in accordance with the default behavior as specified in the ARM NIC-301 documentation. 0x1 The L3 Interconnect converts AHB-lite write bursts to AXI single transactions.	RW	0x0
0	rd_incr_override	Controls how AHB-lite read burst transactions are converted to AXI tranactions. **Value** **Description** 0x0 The L3 Interconnect converts AHB-lite read bursts to AXI transactions in accordance with the default behavior as specified in the ARM NIC-301 documentation. 0x1 The L3 Interconnect converts AHB-lite read bursts to AXI single transactions.	RW	0x0

read_qos

QoS (Quality of Service) value for the read channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF844100

Offset: 0x44100

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

read_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the read channel. A higher value has a higher priority.	RW	0x0

write_qos

QoS (Quality of Service) value for the write channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF844104

Offset: 0x44104

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

write_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the write channel. A higher value has a higher priority.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF844108

Offset: 0x44108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

DMA Register Descriptions

Registers associated with the DMA Controller slave interface. This slave is used by the DMA Controller to access slaves attached to the L3/L4 Interconnect.

Offset: 0x3000

read_qos on page 7-86
QoS (Quality of Service) value for the read channel.

write_qos on page 7-87
QoS (Quality of Service) value for the write channel.

fn_mod on page 7-87
Sets the block issuing capability to multiple or single outstanding transactions.

read_qos
QoS (Quality of Service) value for the read channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF845100

Offset: 0x45100

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

read_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the read channel. A higher value has a higher priority.	RW	0x0

write_qos

QoS (Quality of Service) value for the write channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF845104

Offset: 0x45104

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

write_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the write channel. A higher value has a higher priority.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF845108

Offset: 0x45108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

FPGA2HPS Register Descriptions

Registers associated with the FPGA2HPS AXI Bridge slave interface. This slave is used by the FPGA2HPS AXI Bridge to access slaves attached to the L3/L4 Interconnect.

Offset: 0x4000

wr_tidemark on page 7-88
Controls the release of the transaction in the write data FIFO.

read_qos on page 7-89
QoS (Quality of Service) value for the read channel.

write_qos on page 7-89
QoS (Quality of Service) value for the write channel.

fn_mod on page 7-90
Sets the block issuing capability to multiple or single outstanding transactions.

wr_tidemark

Controls the release of the transaction in the write data FIFO.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF846040

Offset: 0x46040

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												level RW 0x4			

wr_tidemark Fields

Bit	Name	Description	Access	Reset
3:0	level	Stalls the transaction in the write data FIFO until the number of occupied slots in the write data FIFO exceeds the level. Note that the transaction is released before this level is achieved if the network receives the WLAST beat or the write FIFO becomes full.	RW	0x4

read_qos

QoS (Quality of Service) value for the read channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF846100

Offset: 0x46100

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

read_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the read channel. A higher value has a higher priority.	RW	0x0

write_qos

QoS (Quality of Service) value for the write channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF846104

Offset: 0x46104

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

write_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the write channel. A higher value has a higher priority.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF846108

Offset: 0x46108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 — Multiple outstanding read transactions 0x1 — Only a single outstanding read transaction	RW	0x0

ETR Register Descriptions

Registers associated with the ETR (TMC) slave interface. This slave is used by the ETR to access slaves attached to the L3/L4 Interconnect.

Offset: `0x5000`

read_qos on page 7-91
QoS (Quality of Service) value for the read channel.

write_qos on page 7-91
QoS (Quality of Service) value for the write channel.

fn_mod on page 7-92
Sets the block issuing capability to multiple or single outstanding transactions.

read_qos

QoS (Quality of Service) value for the read channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF847100

Offset: `0x47100`

Access: `RW`

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

read_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the read channel. A higher value has a higher priority.	RW	0x0

write_qos

QoS (Quality of Service) value for the write channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF847104

Offset: `0x47104`

Access: `RW`

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

write_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the write channel. A higher value has a higher priority.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF847108

Offset: 0x47108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 — Multiple outstanding read transactions 0x1 — Only a single outstanding read transaction	RW	0x0

EMAC0 Register Descriptions

Registers associated with the EMAC0 slave interface. This slave is used by the DMA controller built into the EMAC0 to access slaves attached to the L3/L4 Interconnect.

Offset: `0x6000`

read_qos on page 7-93
QoS (Quality of Service) value for the read channel.

write_qos on page 7-93
QoS (Quality of Service) value for the write channel.

fn_mod on page 7-94
Sets the block issuing capability to multiple or single outstanding transactions.

read_qos

QoS (Quality of Service) value for the read channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF848100

Offset: `0x48100`

Access: `RW`

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

read_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the read channel. A higher value has a higher priority.	RW	0x0

write_qos

QoS (Quality of Service) value for the write channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF848104

Offset: `0x48104`

Access: `RW`

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

write_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the write channel. A higher value has a higher priority.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF848108

Offset: 0x48108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 — Multiple outstanding read transactions 0x1 — Only a single outstanding read transaction	RW	0x0

EMAC1 Register Descriptions

Registers associated with the EMAC1 slave interface. This slave is used by the DMA controller built into the EMAC1 to access slaves attached to the L3/L4 Interconnect.

Offset: `0x7000`

read_qos on page 7-95
QoS (Quality of Service) value for the read channel.

write_qos on page 7-95
QoS (Quality of Service) value for the write channel.

fn_mod on page 7-96
Sets the block issuing capability to multiple or single outstanding transactions.

read_qos

QoS (Quality of Service) value for the read channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF849100

Offset: `0x49100`

Access: `RW`

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

read_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the read channel. A higher value has a higher priority.	RW	0x0

write_qos

QoS (Quality of Service) value for the write channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF849104

Offset: `0x49104`

Access: `RW`

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

write_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the write channel. A higher value has a higher priority.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF849108

Offset: 0x49108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — Only a single outstanding write transaction	RW	0x0
0	rd	**Value** / **Description** 0x0 — Multiple outstanding read transactions 0x1 — Only a single outstanding read transaction	RW	0x0

USB0 Register Descriptions

Registers associated with the USB0 slave interface. This slave is used by the DMA controller built into the USB0 to access slaves attached to the L3/L4 Interconnect.

Offset: `0x8000`

fn_mod_ahb on page 7-97
Controls how AHB-lite burst transactions are converted to AXI tranactions.

read_qos on page 7-98
QoS (Quality of Service) value for the read channel.

write_qos on page 7-99
QoS (Quality of Service) value for the write channel.

fn_mod on page 7-99
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_ahb

Controls how AHB-lite burst transactions are converted to AXI tranactions.

Module Instance	Base Address	Register Address
`l3regs`	`0xFF800000`	`0xFF84A028`

Offset: `0x4A028`

Access: `RW`

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														`wr_incr_override` RW 0x0	`rd_incr_override` RW 0x0

fn_mod_ahb Fields

Bit	Name	Description	Access	Reset
1	wr_incr_override	Controls how AHB-lite write burst transactions are converted to AXI tranactions. **Value** — **Description** 0x0 — The L3 Interconnect converts AHB-lite write bursts to AXI transactions in accordance with the default behavior as specified in the ARM NIC-301 documentation. 0x1 — The L3 Interconnect converts AHB-lite write bursts to AXI single transactions.	RW	0x0
0	rd_incr_override	Controls how AHB-lite read burst transactions are converted to AXI tranactions. **Value** — **Description** 0x0 — The L3 Interconnect converts AHB-lite read bursts to AXI transactions in accordance with the default behavior as specified in the ARM NIC-301 documentation. 0x1 — The L3 Interconnect converts AHB-lite read bursts to AXI single transactions.	RW	0x0

read_qos

QoS (Quality of Service) value for the read channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF84A100

Offset: 0x4A100

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

read_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the read channel. A higher value has a higher priority.	RW	0x0

write_qos

QoS (Quality of Service) value for the write channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF84A104

Offset: 0x4A104

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

write_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the write channel. A higher value has a higher priority.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF84A108

Offset: 0x4A108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — Only a single outstanding write transaction	RW	0x0

Bit	Name	Description	Access	Reset
0	rd	Value: 0x0 — Multiple outstanding read transactions Value: 0x1 — Only a single outstanding read transaction	RW	0x0

NAND Register Descriptions

Registers associated with the NAND slave interface. This slave is used by the DMA controller built into the NAND flash controller to access slaves attached to the L3/L4 Interconnect.

Offset: 0x9000

read_qos on page 7-100
QoS (Quality of Service) value for the read channel.

write_qos on page 7-100
QoS (Quality of Service) value for the write channel.

fn_mod on page 7-101
Sets the block issuing capability to multiple or single outstanding transactions.

read_qos

QoS (Quality of Service) value for the read channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF84B100

Offset: 0x4B100

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

read_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the read channel. A higher value has a higher priority.	RW	0x0

write_qos

QoS (Quality of Service) value for the write channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF84B104

Offset: 0x4B104

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

write_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the write channel. A higher value has a higher priority.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF84B108

Offset: 0x4B108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — Only a single outstanding write transaction	RW	0x0

Bit	Name	Description	Access	Reset
0	rd	Value: 0x0 — Multiple outstanding read transactions Value: 0x1 — Only a single outstanding read transaction	RW	0x0

USB1 Register Descriptions

Registers associated with the USB1 slave interface. This slave is used by the DMA controller built into the USB1 to access slaves attached to the L3/L4 Interconnect.

Offset: 0xa000

fn_mod_ahb on page 7-102
Controls how AHB-lite burst transactions are converted to AXI tranactions.

read_qos on page 7-103
QoS (Quality of Service) value for the read channel.

write_qos on page 7-104
QoS (Quality of Service) value for the write channel.

fn_mod on page 7-104
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_ahb

Controls how AHB-lite burst transactions are converted to AXI tranactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF84C028

Offset: 0x4C028

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr_incr_override RW 0x0	rd_incr_override RW 0x0

fn_mod_ahb Fields

Bit	Name	Description	Access	Reset
1	wr_incr_override	Controls how AHB-lite write burst transactions are converted to AXI tranactions. **Value** **Description** 0x0 The L3 Interconnect converts AHB-lite write bursts to AXI transactions in accordance with the default behavior as specified in the ARM NIC-301 documentation. 0x1 The L3 Interconnect converts AHB-lite write bursts to AXI single transactions.	RW	0x0
0	rd_incr_override	Controls how AHB-lite read burst transactions are converted to AXI tranactions. **Value** **Description** 0x0 The L3 Interconnect converts AHB-lite read bursts to AXI transactions in accordance with the default behavior as specified in the ARM NIC-301 documentation. 0x1 The L3 Interconnect converts AHB-lite read bursts to AXI single transactions.	RW	0x0

read_qos

QoS (Quality of Service) value for the read channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF84C100

Offset: 0x4C100

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

read_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the read channel. A higher value has a higher priority.	RW	0x0

write_qos

QoS (Quality of Service) value for the write channel.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF84C104

Offset: 0x4C104

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												pri RW 0x0			

write_qos Fields

Bit	Name	Description	Access	Reset
3:0	pri	QoS (Quality of Service) value for the write channel. A higher value has a higher priority.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
l3regs	0xFF800000	0xFF84C108

Offset: 0x4C108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** / **Description** 0x0 — Multiple outstanding write transactions 0x1 — Only a single outstanding write transaction	RW	0x0

Bit	Name	Description	Access	Reset
0	rd	**Value** / **Description** 0x0 — Multiple outstanding read transactions 0x1 — Only a single outstanding read transaction	RW	0x0

Document Revision History

Table 7-3: Document Revision History

Date	Version	Changes

June 2014	2014.06.30	• Corrected master interconnect security properties for:
		  • Ethernet MAC
		  • ETR
		• Added address map and register descriptions

February 2014	2014.02.28	Maintenance release
December 2013	2013.12.30	Maintenance release
November 2012	1.2	Minor updates.
June 2012	1.1	• Added interconnect connectivity matrix. • Rearranged functional description sections. • Simplified address remapping section. • Added address map and register definitions section.
January 2012	1.0	Initial release.