Introduction to Cyclone V Hard Processor System

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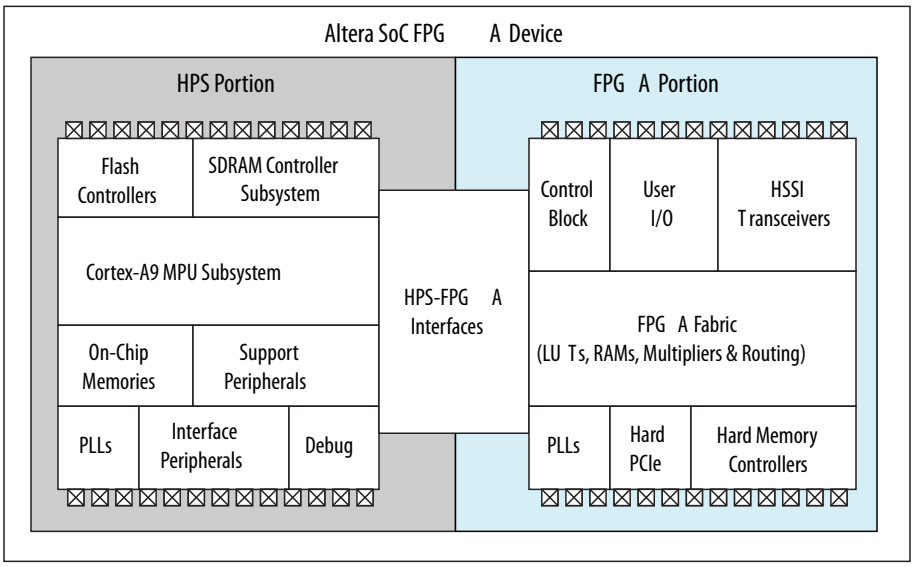
The Cyclone V device is a single-die system on a chip (SoC) that consists of two distinct parts—a hard processor system (HPS) portion and an FPGA portion.

The following figure shows a high-level block diagram of the Altera SoC device.

Figure 1-1: Altera SoC FPGA Device Block Diagram



The HPS contains a microprocessor unit (MPU) subsystem with single or dual ARM® Cortex®-A9 MPCore processors, flash memory controllers, SDRAM L3 Interconnect, on-chip memories, support peripherals, interface peripherals, debug capabilities, and phase-locked loop (PLLs). The dual-processor HPS supports symmetric (SMP) and asymmetric (AMP) multiprocessing.

The FPGA portion of the device contains the FPGA fabric, a control block (CB), phase-locked loops (PLLs), and depending on the device variant, high-speed serial interface (HSSI) transceivers, hard PCI Express® (PCIe®) controllers, and hard memory controllers.

The HPS and FPGA portions of the device are distinctly different. The HPS can boot from multiple sources, including the FPGA fabric and external flash. In contrast, the FPGA must be configured through either the HPS or an externally supported device.

The HPS and FPGA portions of the device each have their own pins. Pins are not freely shared between the HPS and the FPGA fabric. The HPS I/O pins are configured by software executing in the HPS. Software executing on the HPS accesses control registers in the system manager to assign HPS I/O pins to the available HPS modules. The FPGA I/O pins are configured by an FPGA configuration image through the HPS or any external source supported by the device.

The MPU subsystem can boot from flash devices connected to the HPS pins. Or, when the FPGA portion is configured by an external source, the MPU subsystem can boot from memory available to the FPGA portion of the device.

The HPS and FPGA portions of the device have separate external power supplies and independently power on. You can power on the HPS without powering on the FPGA portion of the device. However, to power on the FPGA portion, the HPS must already be on or powered on at the same time as the FPGA portion. You can also turn off the FPGA portion of the device while leaving the HPS power on.

Related Information

- **Cyclone V Device Overview**
  For information about the FPGA portion of the device, refer to *Cyclone V Device Handbook*.
- **Booting and Configuration**
  For more information, refer to the *Booting and Configuration* appendix in the *Cyclone V Device Handbook, Volume 3*.

Features of the HPS

The following list contains the main modules of the HPS:

- MPU subsystem featuring dual ARM Cortex-A9 MPCore processors
- General-purpose Direct Memory Access (DMA) controller
- Two Ethernet media access controllers (EMACs)
- Two USB 2.0 On-The-Go (OTG) controllers
- NAND flash controller
- Quad SPI flash controller
- Secure Digital (SD) / MultiMediaCard (MMC) controller
- Two serial peripheral interface (SPI) master controllers
- Two SPI slave controllers
- Four inter-integrated circuit (I^2C) controllers
- 64 KB on-chip RAM
- 64 KB on-chip boot ROM
- Two UARTs
- Four timers
- Two watchdog timers
- Three general-purpose I/O (GPIO) interfaces
- Two controller area network (CAN) controllers

- ARM CoreSight™ debug components
  - Debug Access Port (DAP)
  - Trace Port Interface Unit (TPIU)
  - System Trace Macrocell (STM)
  - Program Trace Macrocell (PTM)
  - Embedded Trace Router (ETR)
  - Embedded Cross Trigger (ECT)
- System Manager
- Clock Manager
- Reset Manager
- Scan manager
- FPGA manager

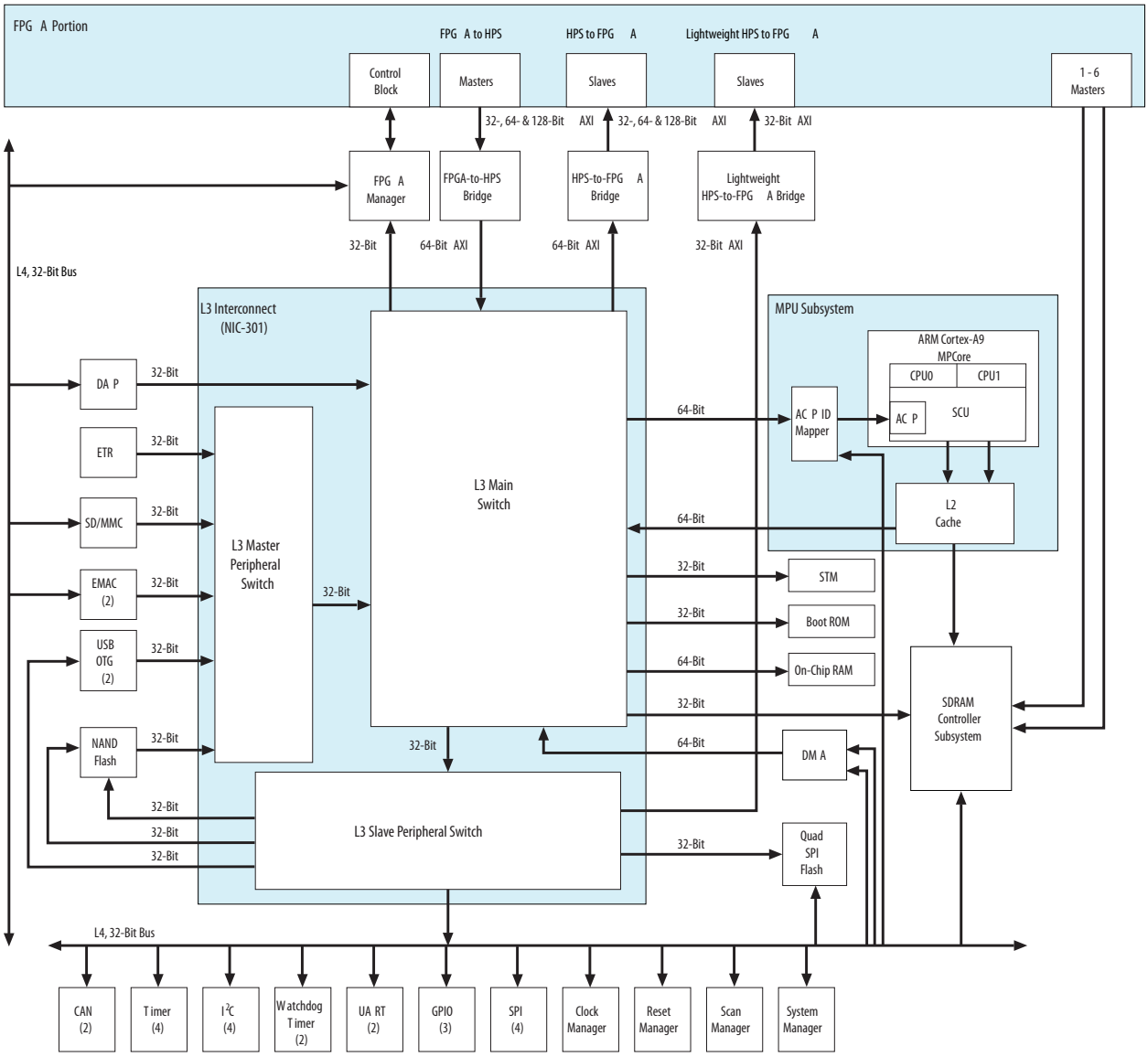
HPS Block Diagram and System Integration

The following figure shows a block diagram of the HPS, excluding the debug system module.

Note: The HPS incorporates third-party intellectual property (IP) from several vendors.

HPS Block Diagram

Figure 1-2: HPS Block Diagram



MPU Subsystem

The MPU subsystem provides the following functionality:

- ARM Cortex-A9 MPCore
  - One or two ARM Cortex-A9 processors in a cluster
  - NEON™ Single Instruction, Multiple Data (SIMD) coprocessor and Vector Floating-Point v3 (VFPv3) per processor
  - Snoop Control Unit (SCU) to ensure coherency within the cluster
  - Accelerator coherency port (ACP) that accepts coherency memory access requests
  - Interrupt controller
  - One general-purpose timer and one watchdog timer per processor
  - Debug and trace features
  - 32 KB instruction and 32 KB data level 1 (L1) caches per processor
  - Memory management unit (MMU) per processor
- ARM L2-310 level 2 (L2) cache
  - Shared 512 KB L2 cache
- ACP ID mapper
- Maps the 12-bit ID from the level 3 (L3) interconnect to the 3-bit ID supported by the ACP

As shown in the "HPS Block Diagram", the L2 cache has one 64-bit master port that is connected to the L3 interconnect, one 64-bit master port connected to the SDRAM L3 Interconnect, and three ports that connect the FPGA to the SDRAM L3 Interconnect. A programmable address filter in the L2 cache controls which portions of the 32-bit physical address space use each master.

Related Information

- **HPS Block Diagram** on page 1-4
- **Cortex-A9 MPU Subsystem**
  For more information, refer to the *Cortex-A9 MPU Subsystem* chapter in the *Cyclone V Device Handbook, Volume 3*.

Interconnect

The interconnect consists of the L3 interconnect and level 4 (L4) buses. The L3 interconnect is an ARM NIC-301 module composed of the following switches:

- L3 main switch
  - Connects the master, slaves, and other subswitches
  - Provides 64-bit switching capabilities
- L3 master peripheral switch
  - Connects master ports of peripherals with integrated DMA controllers to the L3 main switch
- L3 slave peripheral switch
  - Connects slave ports of peripherals to the L3 main switch

The L4 buses are each connected to a master in the L3 slave peripheral switch.

- Each L4 bus is 32 bits wide and is connected to multiple slaves.
- Each L4 bus operates on a separate clock source.

Related Information

Interconnect
For more information, refer to the *Interconnect* chapter in the *Cyclone V Device Handbook, Volume 3*.

Memory Controllers

SDRAM Controller Subsystem

The SDRAM controller subsystem is mastered by HPS masters and FPGA fabric masters.

The SDRAM controller subsystem implements the following high-level features:

- Support for double data rate 2 (DDR2), DDR3, and low-power double data rate 2 (LPDDR2) devices
- Software-configurable priority scheduling on individual SDRAM bursts
- Error correction code (ECC) support, including calculation, single-bit error correction and write-back, and error counters
- Fully-programmable timing parameter support for all JEDEC-specified timing parameters
- All ports support memory protection and mutual accesses
- Support for ARM Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) quality of service (QoS) for the fabric interfaces

The SDRAM controller subsystem is composed of the SDRAM controller and the DDR PHY.

Related Information

SDRAM Controller Subsystem
For more information, refer to the *SDRAM Controller Subsystem* chapter in the *Cyclone V Device Handbook, Volume 3*.

SDRAM Controller

The SDRAM controller contains a multiport front end (MPFE) that accepts requests from HPS masters and from soft logic in the FPGA fabric via the FPGA-to-HPS SDRAM interface.

The SDRAM controller offers the following features:

- Up to 4 GB address range
- 8-, 16-, and 32-bit data widths
- Optional ECC support
- Low-voltage 1.35V DDR3L and 1.2V DDR3U support
- Full memory device power management support
- Two chip selects

The SDRAM controller provides the following features to maximize memory performance:

- Command reordering (look-ahead bank management)
- Data reordering (out of order transactions)
- Deficit round-robin arbitration with aging for bandwidth management
- High-priority bypass for latency sensitive traffic

Related Information

SDRAM Controller Subsystem
For more information, refer to the *SDRAM Controller Subsystem* chapter in the *Cyclone V Device Handbook, Volume 3*.

DDR PHY

The DDR PHY interfaces the single port memory controller to the HPS memory I/O.

Related Information

SDRAM Controller Subsystem

For more information, refer to the *SDRAM Controller Subsystem* chapter in the *Cyclone V Device Handbook, Volume 3*.

NAND Flash Controller

The NAND flash controller is based on the Cadence® Design IP® NAND Flash Memory Controller and offers the following functionality and features:

- Supports one x8 NAND flash device
- Supports Open NAND Flash Interface (ONFI) 1.0
- Supports NAND flash memories from Hynix, Samsung, Toshiba, Micron, and ST Micro
- Supports programmable 512 byte (4-, 8-, or 16-bit correction) or 1024 byte (24-bit correction) error correction code (ECC) sector size
- Supports pipeline read-ahead and write commands for enhanced read/write throughput
- Supports devices with 32, 64, 128, 256, 384, or 512 pages per block
- Supports multiplane devices
- Supports page sizes of 512 bytes, 2 kilobytes (KB), 4 KB, or 8 KB
- Supports single-level cell (SLC) and multi-level cell (MLC) devices with programmable correction capabilities
- Provides internal direct memory access (DMA)
- Provides programmable access timing

Related Information

NAND Flash Controller

For more information, refer to the *NAND Flash Controller* chapter in the *Cyclone V Device Handbook, Volume 3*.

Quad SPI Flash Controller

The Quad SPI flash controller is based on Cadence Quad SPI Flash Controller and offers the following features:

- Supports SPIx1, SPIx2, or SPIx4 (Quad SPI) serial NOR flash devices
- Supports direct access and indirect access modes.
- Supports single, dual, and quad I/O instructions
- Programmable data frame size of 8, 16, or 32 bits
- Support up to four chip selects

Related Information

Quad SPI Flash Controller

For more information, refer to the *Quad SPI Flash Controller* chapter in the *Cyclone V Device Handbook, Volume 3*.

SD/MMC Controller

The SD/MMC controller is based on Synopsys® DesignWare® Mobile Storage Host controller and offers the following features:

- Integrated descriptor-based DMA
- Supports CE-ATA digital protocol commands
- Supports single card
- Single data rate (SDR) mode only
- Programmable card width: 1-, 4-, and 8-bit
- Programmable card types: SD, SDIO, or MMC version 4.3 and 4.4 devices
- Up to 64 KB programmable block size

Note: For an inclusive list of the programmable card types versions supported, refer to the *SD/MMC Controller* chapter.

Related Information

SD/MMC Controller

For more information, refer to the *SD/MMC Controller Controller* chapter in the *Cyclone V Device Handbook, Volume 3*.

Support Peripherals

Clock Manager

The clock manager offers the following features:

- Manages clocks for HPS
- Supports dynamic clock tuning

Related Information

Clock Manager

For more information, refer to the *Clock Manager* chapter in the *Cyclone V Device Handbook, Volume 3*.

Reset Manager

The reset manager manages resets for HPS.

Related Information

Reset Manager

For more information, refer to the *Reset Manager* chapter in the *Cyclone V Device Handbook, Volume 3*.

System Manager

The system manager offers the following features:

- ECC monitoring and control
- Pin multiplexing
- Low-level control of peripheral features not accessible through the control and status registers (CSRs)
- Freeze controller that places I/O elements into a safe state for configuration

Related Information

System Manager

For more information, refer to the *System Manager* chapter in the *Cyclone V Device Handbook, Volume 3*.

Scan Manager

The scan manager drives serial scan-chains to FPGA JTAG and HPS I/O bank configuration.

Related Information

Scan Manager
For more information, refer to the *Scan Manager* chapter in the *Cyclone V Device Handbook, Volume 3*.

Timers

The four timers are based on the Synopsys DesignWare APB Timer peripheral and offer the following features:

- 32-bit timer resolution
- Free-running timer mode
- Programmable time-out period up to approximately 86 seconds (assuming a 50 MHz input clock frequency)
- Interrupt generation

Related Information

Timer
For more information, refer to the *Timer* chapter in the *Cyclone V Device Handbook, Volume 3*.

Watchdog Timers

The two watchdog timers are based on the Synopsys DesignWare APB Watchdog Timer peripheral and offer the following features:

- 32-bit timer resolution
- Interrupt request
- Reset request
- Programmable time-out period up to approximately 86 seconds (assuming a 50 MHz input clock frequency)

Related Information

Watchdog Timer
For more information, refer to the *Watchdog Timer* chapter in the *Cyclone V Device Handbook, Volume 3*.

DMA Controller

The DMA controller provides high-bandwidth data transfers for modules without integrated DMA controllers. The DMA controller is based on the ARM Corelink™ DMA Controller (DMA-330) and offers the following features:

- Micro-coded to support flexible transfer types
- Supports up to eight channels
- Supports flow control with 31 peripheral handshake interfaces

Related Information

DMA Controller
For more information, refer to the *DMA Controller* chapter in the *Cyclone V Device Handbook, Volume 3*.

FPGA Manager

The FPGA manager offers the following features:

- Manages configuration of the FPGA portion of the device
- 32-bit fast passive parallel configuration interface to the FPGA CSS block
- Partial reconfiguration
- Compressed FPGA configuration images
- Advanced Encryption Standard (AES) encrypted FPGA configuration images
- Monitors configuration-related signals in FPGA
- Provides 32 general-purpose inputs and 32 general-purpose outputs to the FPGA fabric

Related Information

FPGA Manager
For more information, refer to the *FPGA Manager* chapter in the *Cyclone V Device Handbook, Volume 3*.

Interface Peripherals

EMACs

The two EMACs are based on the Synopsys DesignWare 3504-0 Universal 10/100/1000 Ethernet MAC and offer the following features:

- Supports 10, 100, and 1000 Mbps standard
- Supports RGMII external PHY interface
- Provides full GMII interface when using FPGA interface
- Integrated DMA controller

Related Information

Ethernet Media Access Controller
For more information, refer to the *Ethernet Media Access Controller* chapter in the *Cyclone V Device Handbook, Volume 3*.

USB Controllers

The two USB 2.0 On-The-Go (OTG) controllers are based on the Synopsys DesignWare Cores USB 2.0 Hi-Speed On-The-Go controller and offer the following features:

- Complies with both Revision 1.3 and Revision 2.0 of the "On the Go and Embedded Host Supplement to the USB Revision 2.0 Specification
- Supports software-configurable modes of operation between OTG 1.3 and OTG 2.0
- Supports all USB 2.0 speeds:
  - High speed (HS, 480-Mbps)
  - Full speed (FS, 12-Mbps)
  - Low speed (LS, 1.5-Mbps)

  Note: In host mode, all speeds are supported. However, in device mode, only high speed and full speed are supported.

Ont the integration side, the USB OTG controller supports the following features:

- Different clocks for system and PHY interfaces
- Dedicated TX FIFO buffer for each device IN endpoint in direct memory access (DMA) mode
- Packet-based, dynamic FIFO memory allocation for endpoints for small FIFO buffers and flexible, efficient use of RAM that can be dynamically sized by software
- Ability to change an endpoint's FIFO memory size during transfers
- Clock gating support during USB suspend and session-off modes
  - PHY clock gating support
  - System clock gating support
- Data FIFO RAM clock gating support
- Local buffering with error correction code (ECC) support

  Note: The USB OTG controller does not support the following protocols:

  - Enhanced Host Controller Interface (EHCI)
  - Open Host Controller Interface (OHCI)
  - Universal Host Controller Interface (UHCI)
- Supports USB 2.0 ULPI PHYs (SDR mode only)
- Supports up to 16 bidirectional endpoints, including control endpoint 0

  Note: Only seven periodic device IN endpoints are supported.
- Supports up to 16 host channels

  Note: In host mode, when the number of device endpoints is greater than the number of host channels, software can reprogram the channels to support up to 127 devices, each having 32 endpoints (IN + OUT), for a maximum of 4,064 endpoints
- Supports generic root hub
- Supports automatic ping capability

Related Information

USB 2.0 OTG Controller

For more information, refer to the *USB 2.0 OTG Controller* chapter in the *Cyclone V Device Handbook, Volume 3*.

I²C Controllers

The four I²C controllers are based on Synopsys DesignWare APB I²C controller and offer the following features:

- Two controllers support I²C management interfaces for the EMAC controllers which are for Ethernet control
- Support both 100 KBps and 400 KBps modes
- Support both 7-bit and 10-bit addressing modes
- Support master and slave operating mode
- Direct access for host processor
- DMA controller may be used for large transfers

Related Information

I²C Controller

For more information, refer to the *I²C Controller* chapter in the *Cyclone V Device Handbook, Volume 3*.

UARTs

The two UART modules are based on Synopsys DesignWare APB Universal Asynchronous Receiver/ Transmitter peripheral and offer the following features:

- 16550 compatible UART
- Supports the auto flow control as specified in 16750 specification
- Supports IrDA 1.0 SIR mode
- Programmable baud rate up to 115.2 Kbps
- Direct access for host processor
- DMA controller may be used for large transfers

Related Information

UART Controller

For more information, refer to the *UART Controller* chapter in the *Cyclone V Device Handbook, Volume 3*.

CAN Controllers

The two CAN controllers are based on the Bosch® D_CAN controller and offer the following features:

- Compliant with CAN protocol specification 2.0 part A & B
- Programmable communication rate up to 1 Mbps
- Holds up to 128 messages
- Supports 11-bit standard and 29-bit extended identifiers
- Programmable interrupt scheme
- Direct access for host processor
- DMA controller may be used for large transfers
- Available on certain device variants only

Related Information

Can Controller

For more information, refer to the *Can Controller* chapter in the *Cyclone V Device Handbook, Volume 3*.

SPI Master Controllers

The two SPI master controllers are based on Synopsys DesignWare Synchronous Serial Interface (SSI) controller and offer the following features:

- Programmable data frame size from 4 to 16 bits
- Supports full- and half-duplex
- Supports up to four chip selects
- Direct access for host processor
- DMA controller may be used for large transfers

Related Information

SPI Controller

For more information, refer to the *SPI Controller* chapter in the *Cyclone V Device Handbook, Volume 3*.

SPI Slave Controllers

The two SPI slave controllers are based on Synopsys DesignWare Synchronous Serial Interface (SSI) controller and offer the following features:

- Programmable data frame size from 4 to 16 bits
- Supports full- and half-duplex
- Direct access for host processor
- DMA controller may be used for large transfers

Related Information

SPI Controller
For more information, refer to the *SPI Controller* chapter in the *Cyclone V Device Handbook, Volume 3*.

GPIO Interfaces

The HPS provides three GPIO interfaces that are based on Synopsys DesignWare APB General Purpose Programming I/O peripheral and offer the following features:

- Supports digital de-bounce
- Configurable interrupt mode
- Supports up to 71 I/O pins and 14 input-only pins, based on device variant
- Supports up to 67 I/O pins and 14 input-only pins

Related Information

General Purpose I/O Interface
For more information, refer to the *General Purpose I/O Interface* chapter in the *Cyclone V Device Handbook, Volume 3*.

On-Chip Memory

On-Chip RAM

The on-chip RAM offers the following features:

- 64 KB size
- 64-bit slave interface
- High performance for all burst lengths

Related Information

On-Chip Memory
For more information, refer to the *On-Chip Memory* chapter in the *Cyclone V Device Handbook, Volume 3*.

Boot ROM

The boot ROM offers the following features:

- 64 KB size
- Contains the code required to support HPS boot from cold or warm reset
- Used exclusively for booting the HPS

Related Information

On-Chip Memory

For more information, refer to the *On-Chip Memory* chapter in the *Cyclone V Device Handbook, Volume 3*.

Endian Support

The HPS is natively a little-endian system. All HPS slaves are little-endian.

The processors masters are software configurable to interpret data as little-endian or big-endian, byte-invariant (BE8). All other masters, including the USB interface, are little-endian.

The FPGA-to-HPS, HPS-to-FPGA, FPGA-to-SDRAM, and lightweight HPS-to-FPGA interfaces are little-endian.

If a processor is set to BE8 mode, software must convert endianness for accesses to peripherals and DMA linked lists in memory.

The ARM Cortex-A9 MPU supports a single instruction to change the endianness of the processor and provides the REV and REV16 instructions to swap the endianness of bytes or half-words respectively. The MMU page tables are software configurable to be organized as little-endian or BE8.

The ARM DMA controller is software configurable to perform byte lane swapping during a transfer.

HPS-FPGA Interfaces

The HPS-FPGA interfaces provide a variety of communication channels between the HPS and the FPGA fabric. The HPS is highly integrated with the FPGA fabric, resulting in thousands of connecting signals. The HPS-FPGA interfaces include:

- FPGA-to-HPS bridge—a high-performance bus with a configurable data width of 32, 64, and 128 bits, allowing the FPGA fabric to master transactions to the slaves in the HPS. This interface allows the FPGA fabric to have full visibility into the HPS address space. This interface also provides access to the coherent memory interface.
- HPS-to-FPGA bridge—a high-performance interface with a configurable data width of 32, 64, and 128 bits, allowing the HPS to master transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA bridge—an interface with a 32-bit fixed data width, allowing the HPS to master transactions to slaves in the FPGA fabric.
- FPGA clocks and resets—provide flexible clocks to and from the HPS.
- HPS-to-FPGA JTAG—allows the HPS to master the FPGA JTAG chain.
- TPIU trace—sends trace data created in the HPS to the FPGA fabric.
- FPGA System Trace Macrocell (STM) events—an interface that allows the FPGA fabric to send hardware events stored in the HPS trace using STM.
- FPGA cross-trigger—an interface that allows triggers to and from the CoreSight trigger system.
- DMA peripheral interface—multiple peripheral-request channels.
- FPGA manager interface—signals that communicate with FPGA fabric for boot and configuration.
- Interrupts—allow soft IP to supply interrupts directly to the MPU interrupt controller.
- MPU standby and events—signals that notify the FPGA fabric that the MPU is in standby mode and signals that wake up Cortex-A9 processors from a wait for event (WFE) state.
- HPS debug interface - an interface that allows HPS debug control domain (debug APB) to extend into FPGA

Related Information

HPS-FPGA Bridges

For more information, refer to the *HPS-FPGA Bridges* chapter in the *Cyclone V Device Handbook, Volume 3*.

HPS Address Map

The address map specifies the addresses of slaves, such as memory and peripherals, as viewed by the MPU and other masters. The HPS has multiple address spaces, defined in the following section.

HPS Address Spaces

The following table shows the HPS address spaces and their sizes.

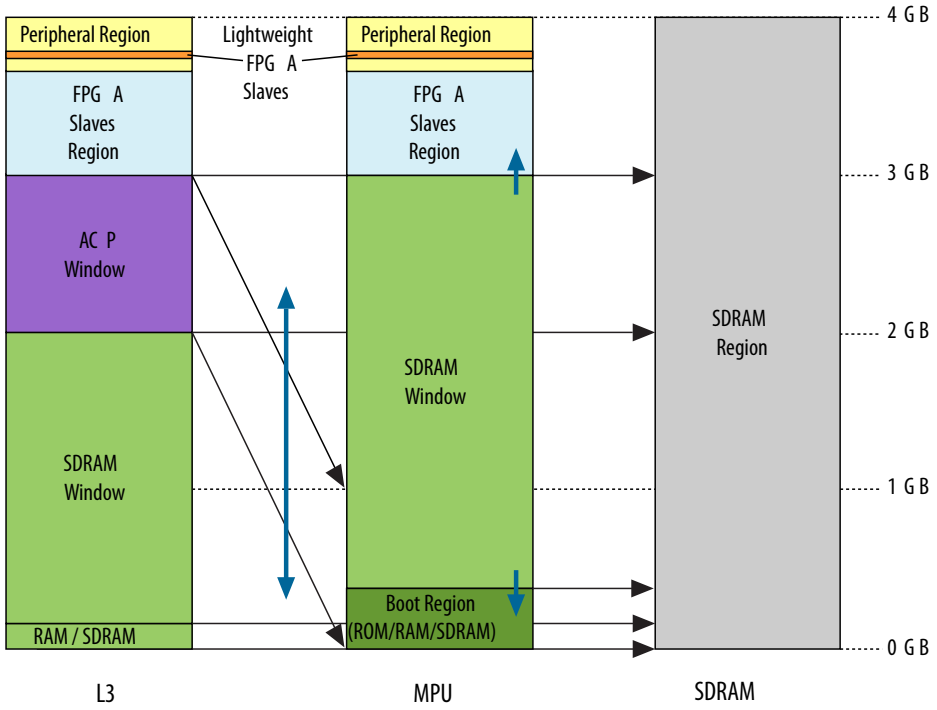
Table 1-1: HPS Address Spaces

Name	Description	Size
MPU	MPU subsystem	4 GB
L3	L3 interconnect	4 GB
SDRAM	SDRAM controller subsystem	4 GB

Address spaces are divided into one or more nonoverlapping regions. For example, the MPU address space has the peripheral, FPGA slaves, SDRAM window, and boot regions.

The following figure shows the relationships between the HPS address spaces. The figure is not to scale.

Figure 1-3: HPS Address Space Relationships



The window regions provide access to other address spaces. The thin black arrows indicate which address space is accessed by a window region (arrows point to accessed address space). For example, accesses to the ACP window in the L3 address space map to a 1 GB region of the MPU address space.

The SDRAM window in the MPU address space can grow and shrink at the top and bottom (short, blue vertical arrows) at the expense of the FPGA slaves and boot regions. For specific details, refer to “MPU Address Space”.

The ACP window can be mapped to any 1 GB region in the MPU address space (blue vertical bidirectional arrow), on gigabyte-aligned boundaries.

The following table shows the base address and size of each region that is common to the L3 and MPU address spaces.

Table 1-2: Common Address Space Regions

Identifier	Region Name	Base Address	Size
FPGASLAVES	FPGA slaves	0xC0000000	960 MB
PERIPH	Peripheral	0xFC000000	64 MB
LWFPGASLAVES (1)	Lightweight FPGA slaves	0xFF200000	2 MB

(1) This space is part of the "PERIPH" space.

Related Information

MPU Address Space on page 1-17

SDRAM Address Space

The SDRAM address space is up to 4 GB. The entire address space can be accessed through the FPGA-to-HPS SDRAM interface from the FPGA fabric. The total amount of SDRAM addressable from the other address spaces can be configured at runtime.

Related Information

- MPU Address Space on page 1-17
- L3 Address Space on page 1-17
- Interconnect on page 1-5
  For details of how to configure the SDRAM address space.

MPU Address Space

The MPU address space is 4 GB and applies to addresses generated inside the MPU. The MPU address space contains the following regions:

- The SDRAM window region provides access to a large, configurable portion of the 4 GB SDRAM address space.
- The MPU L2 cache controller contains a master connected to the L3 interconnect and a master connected to the SDRAM.
- The address filtering start and end registers in the L2 cache controller define the SDRAM window boundaries.
  - The boundaries are megabyte-aligned.
  - Addresses within the boundaries route to the SDRAM master.
  - Addresses outside the boundaries route to the L3 interconnect master.

Related Information

- HPS Address Spaces on page 1-15
  For more information, refer to the "HPS Address Space Relationships" table.
- Interconnect
  For information about the L3 `remap` control register bits, refer to the *Interconnect* chapter in the *Cyclone V Device Handbook, Volume 3*.
- Cortex-A9 Microprocessor Unit Subsystem
  For information about L2 address filtering, refer to the Cortex-A9 Microprocessor Unit Subsystem chapter in the *Cyclone V Device Handbook, Volume 3*.

L3 Address Space

The L3 address space is 4 GB and applies to all L3 masters except the MPU. The L3 address space has more configuration options than the other address spaces.

Related Information

- Interconnect
  For information about the L3 `remap` control register bits, refer to the *Interconnect* chapter in the *Cyclone V Device Handbook, Volume 3*.

- **Cortex-A9 Microprocessor Unit Subsystem**
  For more information about the ACP ID mapper, refer to the Cortex-A9 Microprocessor Unit Subsystem chapter in the *Cyclone V Device Handbook, Volume 3*.

HPS Peripheral Region Address Map

Table 1-5 lists the slave identifier, slave title, base address, and size of each slave in the peripheral region. The Slave Identifier column lists the names used in the HPS register map.

Table 1-5: Peripheral Region Address Map

Slave Identifier	Slave Title	Base Address	Size
STM	STM	0xFC000000	48 MB
DAP	DAP	0xFF000000	2 MB
LWFPGASLAVES	FPGA slaves accessed with lightweight FPGA-to-HPS bridge	0xFF200000	2 MB
LWHPS2FPGAREGS	Lightweight FPGA-to-HPS bridge GPV	0xFF400000	1 MB
HPS2FPGAREGS	HPS-to-FPGA bridge GPV	0xFF500000	1 MB
FPGA2HPSREGS	FPGA-to-HPS bridge GPV	0xFF600000	1 MB
EMAC0	EMAC0	0xFF700000	8 KB
EMAC1	EMAC1	0xFF702000	8 KB
SDMMC	SD/MMC	0xFF704000	4 KB
QSPIREGS	Quad SPI flash controller registers	0xFF705000	4 KB
FPGAMGRREGS	FPGA manager registers	0xFF706000	4 KB
ACPIDMAP	ACP ID mapper registers	0xFF707000	4 KB
GPIO0	GPIO0	0xFF708000	4 KB
GPIO1	GPIO1	0xFF709000	4 KB
GPIO2	GPIO2	0xFF70A000	4 KB
L3REGS	L3 interconnect GPV	0xFF800000	1 MB
NANDDATA	NAND controller data	0xFF900000	1 MB

Slave Identifier	Slave Title	Base Address	Size
QSPIDATA	Quad SPI flash data	0xFFA00000	1 MB
USB0	USB0 OTG controller registers	0xFFB00000	256 KB
USB1	USB1 OTG controller registers	0xFFB40000	256 KB
NANDREGS	NAND controller registers	0xFFB80000	64 KB
FPGAMGRDATA	FPGA manager configuration data	0xFFB90000	4 KB
CAN0	CAN0 controller registers	0xFFC00000	4 KB
CAN1	CAN1 controller registers	0xFFC01000	4 KB
UART0	UART0	0xFFC02000	4 KB
UART1	UART1	0xFFC03000	4 KB
I2C0	I2C0	0xFFC04000	4 KB
I2C1	I2C1	0xFFC05000	4 KB
I2C2	I2C2	0xFFC06000	4 KB
I2C3	I2C3	0xFFC07000	4 KB
SPTIMER0	SP Timer0	0xFFC08000	4 KB
SPTIMER1	SP Timer1	0xFFC09000	4 KB
SDRREGS	SDRAM controller subsystem registers	0xFFC20000	128 KB
OSC1TIMER0	OSC1 Timer0	0xFFD00000	4 KB
OSC1TIMER1	OSC1 Timer1	0xFFD01000	4 KB
L4WD0	Watchdog0	0xFFD02000	4 KB
L4WD1	Watchdog1	0xFFD03000	4 KB
CLKMGR	Clock manager	0xFFD04000	4 KB
RSTMGR	Reset manager	0xFFD05000	4 KB

Slave Identifier	Slave Title	Base Address	Size
SYSMGR	System manager	0xFFD08000	16 KB
DMANONSECURE	DMA nonsecure registers	0xFFE00000	4 KB
DMASECURE	DMA secure registers	0xFFE01000	4 KB
SPIS0	SPI slave0	0xFFE02000	4 KB
SPIS1	SPI slave1	0xFFE03000	4 KB
SPIM0	SPI master0	0xFFF00000	4 KB
SPIM1	SPI master1	0xFFF01000	4 KB
SCANMGR	Scan manager registers	0xFFF02000	4 KB
ROM	Boot ROM	0xFFFD0000	64 KB
MPUSCU	MPU SCU registers	0xFFFEC000	8 KB
MPUL2	MPU L2 cache controller registers	0xFFFEF000	4 KB
OCRAM	On-chip RAM	0xFFFF0000	64 KB

Related Information

Cyclone V SoC HPS Address Map and Register Definitions

Document Revision History

Table 1-6: Document Revision History

Date	Version	Changes
June 2014	2014.06.30	Maintenance release
February 2014	2014.02.28	Maintenance release
December 2013	2013.12.30	Maintenance release
November 2012	1.3	Minor updates.
June 2012	1.2	Updated address spaces section.
May 2012	1.1	Added peripheral region address map.

Date	Version	Changes
January 2012	1.0	Initial release.