HPS-FPGA Bridges 8

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This chapter describes the bridges in the hard processor system (HPS) used to communicate data between the FPGA fabric and HPS logic. The bridges use the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) protocol, and are based on the AMBA Network Interconnect (NIC-301).

The HPS contains the following HPS-FPGA bridges:

- FPGA-to-HPS Bridge
- HPS-to-FPGA Bridge
- Lightweight HPS-to-FPGA Bridge

Related Information

- **FPGA-to-HPS Bridge** on page 8-4
- **HPS-to-FPGA Bridge Clocks and Resets** on page 8-48
- **Lightweight HPS-to-FPGA Bridge Clocks and Resets** on page 8-48
- **http://infocenter.arm.com/**
  Additional information is available in the AMBA AXI Protocol Specification v1.0 and the AMBA Network Interconnect (NIC-301) Technical Reference Manual, which you can download from the ARM Infocenter website.

Features of the HPS-FPGA Bridges

The HPS-FPGA bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic and vice versa. For example, you can instantiate additional memories or peripherals in the FPGA fabric, and master interfaces belonging to components in the HPS logic can access them. You can also instantiate components such as a Nios® II processor in the FPGA fabric and their master interfaces can access memories or peripherals in the HPS logic.

Table 8-1: HPS-FPGA Bridge Features

Feature	FPGA-to-HPS Bridge	HPS-to-FPGA Bridge	Lightweight HPS-to-FPGA Bridge
Supports the AMBA AXI3 interface protocol	Y	Y	Y

Feature	FPGA-to-HPS Bridge	HPS-to-FPGA Bridge	Lightweight HPS-to-FPGA Bridge
Implements clock crossing and manages the transfer of data across the clock domains in the HPS logic and the FPGA fabric	Y	Y	Y
Performs data width conversion between the HPS logic and the FPGA fabric	Y	Y	Y
Allows configuration of FPGA interface widths at instantiation time	Y	Y	N

Each bridge consists of a master-slave pair with one interface exposed to the FPGA fabric and the other exposed to the HPS logic. The FPGA-to-HPS bridge exposes an AXI slave interface that you can connect to AXI master or Avalon-MM interfaces in the FPGA fabric. The HPS-to-FPGA and lightweight HPS-to-FPGA bridges expose an AXI master interface that you can connect to AXI or Avalon-MM slave interfaces in the FPGA fabric.

Related Information

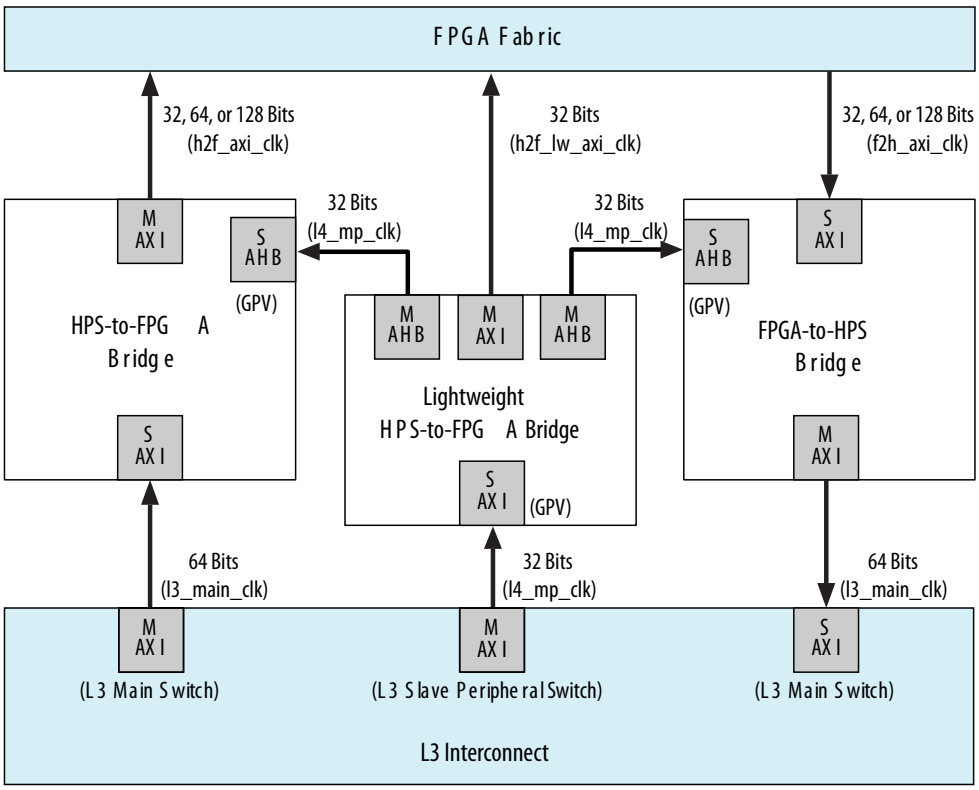
Instantiating the HPS Component

For information about configuring the AXI bridges, refer to the *Instantiating the HPS Component* chapter of the *Cyclone V Device Handbook, Volume 3*.

HPS-FPGA Bridges Block Diagram and System Integration

Figure 8-1: HPS-FPGA Bridge Connectivity

The following figure shows the HPS-FPGA bridges in the context of the FPGA fabric and the L3 interconnect to the HPS. Each master (M) and slave (S) interface is shown with its data width(s). The clock domain for each interconnect is shown in parentheses.



The HPS-to-FPGA bridge is mastered by the level 3 (L3) main switch and the lightweight HPS-to-FPGA bridge is mastered by the L3 slave peripheral switch.

The FPGA-to-HPS bridge masters the L3 main switch, allowing any master implemented in the FPGA fabric to access most slaves in the HPS. For example, the FPGA-to-HPS bridge can access the accelerator coherency port (ACP) of the Cortex-A9 MPU subsystem to perform cache-coherent accesses to the SDRAM subsystem.

All three bridges contain global programmers view (GPV) registers. The GPV registers control the behavior of the bridge. Access to the GPV registers of all three bridges is provided through the lightweight HPS-to-FPGA bridge.

Related Information

- **Clocks and Resets** on page 8-47
- **Interconnect**
  For detailed information about connectivity, such as which masters have access to each bridge, refer to the *Interconnect* chapter of the *Cyclone V Device Handbook, Volume 3*.

Functional Description of the HPS-FPGA Bridges

The Global Programmers View

The HPS-to-FPGA bridge includes a set of registers called the GPV. The GPV provides settings to control the bridge properties and behavior. Access to the GPV registers of all three bridges is provided through the lightweight HPS-to-FPGA bridge.

The GPV registers can only be accessed by secure masters in the HPS or the FPGA fabric.

FPGA-to-HPS Bridge

The FPGA-to-HPS bridge provides access to the peripherals and memory in the HPS. This access is available to any master implemented in the FPGA fabric. You can configure the bridge slave, which is exposed to the FPGA fabric, to support 32-, 64-, or 128-bit data. The master interface of the bridge, connected to the L3 interconnect, has a data width of 64 bits.

Table 8-2: FPGA-to-HPS Bridge Properties

The following table lists the properties of the FPGA-to-HPS bridge, including the configurable slave interface exposed to the FPGA fabric.

Bridge Property	FPGA Slave Interface	L3 Master Interface
Data width[1]	32, 64, or 128 bits	64 bits
Clock domain	`f2h_axi_clk`	`l3_main_clk`
Byte address width	32 bits	32 bits
ID width	8 bits	8 bits
Read acceptance	16 transactions	16 transactions
Write acceptance	16 transactions	16 transactions
Total acceptance	32 transactions	32 transactions

The FPGA-to-HPS bridge address map contains a GPV. The GPV registers provide settings that adjust the bridge slave properties when the FPGA slave interface is configured to be 32 or 128 bits wide. The slave issuing capability can be adjusted, through the `fn_mod` register, to allow one or multiple transactions to be outstanding in the HPS. The slave bypass merge feature can also be enabled, through the `bypass_merge` bit in the `fn_mod2` register. This feature ensures that the upsizing and downsizing logic does not alter any transactions when the FPGA slave interface is configured to be 32 or 128 bits wide.

Note: It is critical to provide the correct `l4_mp_clk` clock to support access to the GPV, as described in "GPV Clocks".

[1] The bridge slave data width is user-configurable at the time you instantiate the HPS component in your system.

Related Information

- **The Global Programmers View** on page 8-4
- **GPV Clocks** on page 8-48

FPGA-to-HPS Access to ACP

When the error correction code (ECC) option is enabled in the level 2 (L2) cache controller, all accesses from the FPGA-to-HPS bridge to the ACP must be 64 bits wide and aligned on 8-byte boundaries after up- or downsizing takes place.

Table 8-3: FPGA Master and FPGA-to-HPS Bridge Configurations

The following table lists some possible master and FPGA-to-HPS bridge slave configurations that support accesses to the L2 cache with ECC enabled.

Soft Logic Master Width	Soft Logic Master Alignment	Soft Logic Master Burst Size (Width)	Soft Logic Master Burst Length	FPGA-to-HPS Bridge Slave Width
32 bits	8 bytes	4 bytes	2, 4, 6, 8, 10, 12, 14, or 16 beats	32 bits
64 bits	8 bytes	8 bytes	1 to 16 beats	32 bits
128 bits	8 or 16 bytes	8 or 16 bytes	1 to 16 beats	32 bits
32 bits	8 bytes	4 bytes	2, 4, 6, 8, 10, 12, 14, or 16 beats	64 bits
64 bits	8 bytes	8 bytes	1 to 16 beats	64 bits
128 bits	8 or 16 bytes	8 or 16 bytes	1 to 16 beats	64 bits
32 bits	8 bytes	4 bytes	2, 4, 6, 8, 10, 12, 14, or 16 beats	128 bits
64 bits	8 bytes	8 bytes	1 to 16 beats	128 bits
128 bits	8 or 16 bytes	8 or 16 bytes	1 to 16 beats	128 bits

Related Information

Cortex-A9 Microprocessor Unit Subsystem

For more information about the ECC option of the L2 cache or about interconnect master IDs, refer to the *Cortex-A9 Microprocessor Unit Subsystem* chapter of the *Cyclone V Device Handbook, Volume 3*.

FPGA-to-HPS Bridge Slave Signals

The FPGA-to-HPS bridge slave address channels support user-sideband signals, routed to the ACP in the MPU subsystem. All the signals have a fixed width except the data and write strobes for the read and write data channels. The variable width signals depend on the data width setting of the bridge.

The following tables list all the signals exposed by the FPGA-to-HPS slave interface to the FPGA fabric.

Table 8-4: FPGA-to-HPS Bridge Slave Write Address Channel Signals

Signal	Width	Direction	Description
AWID	8 bits	Input	Write address ID
AWADDR	32 bits	Input	Write address
AWLEN	4 bits	Input	Burst length
AWSIZE	3 bits	Input	Burst size
AWBURST	2 bits	Input	Burst type
AWLOCK	2 bits	Input	Lock type—Valid values are 00 (normal access) and 01 (exclusive access)
AWCACHE	4 bits	Input	Cache policy type
AWPROT	3 bits	Input	Protection type
AWVALID	1 bit	Input	Write address channel valid
AWREADY	1 bit	Output	Write address channel ready
AWUSER	5 bits	Input	User sideband signals

Table 8-5: FPGA-to-HPS Bridge Slave Write Data Channel Signals

Signal	Width	Direction	Description
WID	8 bits	Input	Write ID
WDATA	32, 64, or 128 bits	Input	Write data
WSTRB	4, 8, or 16 bits	Input	Write data strobes
WLAST	1 bit	Input	Write last data identifier
WVALID	1 bit	Input	Write data channel valid
WREADY	1 bit	Output	Write data channel ready

Table 8-6: FPGA-to-HPS Bridge Slave Write Response Channel Signals

Signal	Width	Direction	Description
BID	8 bits	Output	Write response ID

Signal	Width	Direction	Description
BRESP	2 bits	Output	Write response
BVALID	1 bit	Output	Write response channel valid
BREADY	1 bit	Input	Write response channel ready

Table 8-7: FPGA-to-HPS Bridge Slave Read Address Channel Signals

Signal	Width	Direction	Description
ARID	8 bits	Input	Read address ID
ARADDR	32 bits	Input	Read address
ARLEN	4 bits	Input	Burst length
ARSIZE	3 bits	Input	Burst size
ARBURST	2 bits	Input	Burst type
ARLOCK	2 bits	Input	Lock type—Valid values are 00 (normal access) and 01 (exclusive access)
ARCACHE	4 bits	Input	Cache policy type
ARPROT	3 bits	Input	Protection type
ARVALID	1 bit	Input	Read address channel valid
ARREADY	1 bit	Output	Read address channel ready
ARUSER	5 bits	Input	Read user sideband signals

Table 8-8: FPGA-to-HPS Bridge Slave Read Data Channel Signals

Signal	Width	Direction	Description
RID	8 bits	Output	Read ID
RDATA	32, 64, or 128 bits	Output	Read data
RRESP	2 bits	Output	Read response
RLAST	1 bit	Output	Read last data identifier
RVALID	1 bit	Output	Read data channel valid

Signal	Width	Direction	Description
RREADY	1 bit	Input	Read data channel ready

FPGA2HPS AXI Bridge Module Address Map

Registers in the FPGA2HPS AXI Bridge Module.

Base Address: `0xFF600000`

ID Register Group

Register	Offset	Width	Access	Reset Value	Description
periph_id_4 on page 8-9	0x1FD0	32	RO	0x4	Peripheral ID4 Register
periph_id_0 on page 8-10	0x1FE0	32	RO	0x1	Peripheral ID0 Register
periph_id_1 on page 8-10	0x1FE4	32	RO	0xB3	Peripheral ID1 Register
periph_id_2 on page 8-10	0x1FE8	32	RO	0x6B	Peripheral ID2 Register
periph_id_3 on page 8-11	0x1FEC	32	RO	0x0	Peripheral ID3 Register
comp_id_0 on page 8-11	0x1FF0	32	RO	0xD	Component ID0 Register
comp_id_1 on page 8-12	0x1FF4	32	RO	0xF0	Component ID1 Register
comp_id_2 on page 8-12	0x1FF8	32	RO	0x5	Component ID2 Register
comp_id_3 on page 8-13	0x1FFC	32	RO	0xB1	Component ID3 Register

32-bit Slave

Register	Offset	Width	Access	Reset Value	Description
fn_mod2 on page 8-14	0x42024	32	RW	0x0	Functionality Modification 2 Register
fn_mod on page 8-14	0x42108	32	RW	0x0	Issuing Functionality Modification Register

128-bit Slave

Register	Offset	Width	Access	Reset Value	Description
fn_mod2 on page 8-15	0x44024	32	RW	0x0	Functionality Modification 2 Register
fn_mod on page 8-16	0x44108	32	RW	0x0	Issuing Functionality Modification Register

ID Register Group Register Descriptions

Contains registers that identify the ARM NIC-301 IP Core.

Offset: `0x1000`

periph_id_4

JEP106 continuation code

Module Instance	Base Address	Register Address
`fpga2hpsregs`	`0xFF600000`	`0xFF601FD0`

Offset: `0x1FD0`

Access: `RO`

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								periph_id_4 RO 0x4							

periph_id_4 Fields

Bit	Name	Description	Access	Reset
7:0	`periph_id_4`	JEP106 continuation code	RO	`0x4`

periph_id_0

Peripheral ID0

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF601FE0

Offset: 0x1FE0

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								pn7to0 RO 0x1							

periph_id_0 Fields

Bit	Name	Description	Access	Reset
7:0	pn7to0	Part Number [7:0]	RO	0x1

periph_id_1

Peripheral ID1

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF601FE4

Offset: 0x1FE4

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								jep3to0_pn11to8 RO 0xB3							

periph_id_1 Fields

Bit	Name	Description	Access	Reset
7:0	jep3to0_pn11to8	JEP106[3:0], Part Number [11:8]	RO	0xB3

periph_id_2

Peripheral ID2

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF601FE8

Offset: 0x1FE8

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								rev_jepcode_jep6to4 RO 0x6B							

periph_id_2 Fields

Bit	Name	Description	Access	Reset
7:0	rev_jepcode_jep6to4	Revision, JEP106 code flag, JEP106[6:4]	RO	0x6B

periph_id_3
Peripheral ID3

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF601FEC

Offset: 0x1FEC

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								rev_and RO 0x0				cust_mod_num RO 0x0			

periph_id_3 Fields

Bit	Name	Description	Access	Reset
7:4	rev_and	Revision	RO	0x0
3:0	cust_mod_num	Customer Model Number	RO	0x0

comp_id_0
Component ID0

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF601FF0

Offset: 0x1FF0

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0xD							

comp_id_0 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0xD

comp_id_1
Component ID1

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF601FF4

Offset: 0x1FF4

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								genipcompcls_preamble RO 0xF0							

comp_id_1 Fields

Bit	Name	Description	Access	Reset
7:0	genipcompcls_preamble	Generic IP component class, Preamble	RO	0xF0

comp_id_2
Component ID2

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF601FF8

Offset: 0x1FF8

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0x5							

comp_id_2 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0x5

comp_id_3
Component ID3

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF601FFC

Offset: 0x1FFC

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0xB1							

comp_id_3 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0xB1

Slave Register Group Register Descriptions

Registers associated with slave interfaces.

Offset: 0x42000

32-bit Slave Register Descriptions

Registers associated with the 32-bit AXI slave interface. These registers are only active when the FPGA2HPS AXI Bridge is configured with a 32-bit FPGA AXI slave interface.

Offset: 0x0

fn_mod2 on page 8-14
Controls bypass merge of upsizing/downsizing.

fn_mod on page 8-14
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod2
Controls bypass merge of upsizing/downsizing.

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF642024

Offset: 0x42024

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															bypass_merge RW 0x0

fn_mod2 Fields

Bit	Name	Description	Access	Reset
0	bypass_merge	Controls bypass merge of upsizing/downsizing. **Value** **Description** 0x0 The network can alter transactions. 0x1 The network does not alter any transactions that could pass through the upsizer legally without alteration.	RW	0x0

fn_mod
Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF642108

Offset: 0x42108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

128-bit Slave Register Descriptions

Registers associated with the 128-bit AXI slave interface. These registers are only active when the FPGA2HPS AXI Bridge is configured with a 128-bit FPGA AXI slave interface.

Offset: 0x2000

fn_mod2 on page 8-15
Controls bypass merge of upsizing/downsizing.

fn_mod on page 8-16
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod2

Controls bypass merge of upsizing/downsizing.

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF644024

Offset: 0x44024

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															bypass_merge RW 0x0

fn_mod2 Fields

Bit	Name	Description	Access	Reset
0	bypass_merge	Controls bypass merge of upsizing/downsizing. **Value** **Description** 0x0 The network can alter transactions. 0x1 The network does not alter any transactions that could pass through the upsizer legally without alteration.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
fpga2hpsregs	0xFF600000	0xFF644108

Offset: 0x44108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

HPS-to-FPGA Bridge

The HPS-to-FPGA bridge provides a configurable-width, high-performance master interface to the FPGA fabric. The bridge provides most masters in the HPS with access to logic, peripherals, and memory implemented in the FPGA. The effective size of the address space is 0x3FFF0000, or 1 gigabyte (GB) minus 64 megabytes (MB). The address space size is less than 1 GB because 64 MB is occupied by peripherals, lightweight HPS-to-FPGA bridge, on-chip RAM, and boot ROM in the HPS. You can configure the bridge master exposed to the FPGA fabric for 32-, 64-, or 128-bit data. The amount of address space exposed to the MPU subsystem can also be reduced through the L2 cache address filtering mechanism.

The slave interface of the bridge in the HPS logic has a data width of 64 bits. The bridge provides width adaptation and clock crossing logic that allows the logic in the FPGA to operate in any clock domain, asynchronous from the HPS.

Note: The HPS-to-FPGA bridge is accessed if the MPU boots from the FPGA. Before the MPU boots from the FPGA, the FPGA portion of the SoC device must be configured, and the HPS-to-FPGA bridge must be remapped into addressable space.

Table 8-9: HPS-to-FPGA Bridge Properties

The following table lists the properties of the HPS-to-FPGA bridge, including the configurable master interface exposed to the FPGA fabric.

Bridge Property	L3 Slave Interface	FPGA Master Interface
Data width (2)	64 bits	32, 64, or 128 bits
Clock domain	l3_main_clk	h2f_axi_clk
Byte address width	32 bits	30 bits
ID width	12 bits	12 bits

(2) The bridge master data width is user-configurable at the time you instantiate the HPS component in your system.

Bridge Property	L3 Slave Interface	FPGA Master Interface
Read acceptance	16 transactions	16 transactions
Write acceptance	16 transactions	16 transactions
Total acceptance	32 transactions	32 transactions

The HPS-to-FPGA bridge's GPV, described in "The Global Programmers View", provides settings to adjust the bridge master properties. The master issuing capability can be adjusted, through the `fn_mod` register, to allow one or multiple transactions to be outstanding in the FPGA fabric. The master bypass merge feature can also be enabled, through the `bypass_merge` bit in the `fn_mod2` register. This feature ensures that the upsizing and downsizing logic does not alter any transactions when the FPGA master interface is configured to be 32 or 128 bits wide.

Note: It is critical to provide the correct `l4_mp_clk` clock to support access to the GPV, as described in "GPV Clocks".

Related Information

- **The Global Programmers View** on page 8-4
- **GPV Clocks** on page 8-48
- **Interconnect**
  For detailed information about connectivity, such as which masters have access to each bridge, refer to the *Interconnect* chapter of the *Cyclone V Device Handbook, Volume 3*.
- **Cortex-A9 Microprocessor Unit Subsystem**
  For details about L2 cache address filtering, refer to the *Cortex-A9 Microprocessor Unit Subsystem* chapter of the *Cyclone V Device Handbook, Volume 3*.
- **Instantiating the HPS Component**
  For information about configuring the AXI bridges, refer to the *Instantiating the HPS Component* chapter of the *Cyclone V Device Handbook, Volume 3*.

HPS-to-FPGA Bridge Master Signals

All the HPS-to-FPGA bridge master signals have a fixed width except the data and write strobes for the read and write data channels. The variable-width signals depend on the data width setting of the bridge interface exposed to the FPGA logic.

The following tables list all the signals exposed by the HPS-to-FPGA master interface to the FPGA fabric.

Table 8-10: HPS-to-FPGA Bridge Master Write Address Channel Signals

Signal	Width	Direction	Description
`AWID`	12 bits	Output	Write address ID
`AWADDR`	30 bits	Output	Write address
`AWLEN`	4 bits	Output	Burst length
`AWSIZE`	3 bits	Output	Burst size

Signal	Width	Direction	Description
AWBURST	2 bits	Output	Burst type
AWLOCK	2 bits	Output	Lock type—Valid values are 00 (normal access) and 01 (exclusive access)
AWCACHE	4 bits	Output	Cache policy type
AWPROT	3 bits	Output	Protection type
AWVALID	1 bit	Output	Write address channel valid
AWREADY	1 bit	Input	Write address channel ready

Table 8-11: HPS-to-FPGA Bridge Master Write Data Channel Signals

Signal	Width	Direction	Description
WID	12 bits	Output	Write ID
WDATA	32, 64, or 128 bits	Output	Write data
WSTRB	4, 8, or 16 bits	Output	Write data strobes
WLAST	1 bit	Output	Write last data identifier
WVALID	1 bit	Output	Write data channel valid
WREADY	1 bit	Input	Write data channel ready

Table 8-12: HPS-to-FPGA Bridge Master Write Response Channel Signals

Signal	Width	Direction	Description
BID	12 bits	Input	Write response ID
BRESP	2 bits	Input	Write response
BVALID	1 bit	Input	Write response channel valid
BREADY	1 bit	Output	Write response channel ready

Table 8-13: HPS-to-FPGA Bridge Master Read Address Channel Signals

Signal	Width	Direction	Description
ARID	12 bits	Output	Read address ID

Signal	Width	Direction	Description
ARADDR	30 bits	Output	Read address
ARLEN	4 bits	Output	Burst length
ARSIZE	3 bits	Output	Burst size
ARBURST	2 bits	Output	Burst type
ARLOCK	2 bits	Output	Lock type—Valid values are 00 (normal access) and 01 (exclusive access)
ARCACHE	4 bits	Output	Cache policy type
ARPROT	3 bits	Output	Protection type
ARVALID	1 bit	Output	Read address channel valid
ARREADY	1 bit	Input	Read address channel ready

Table 8-14: HPS-to-FPGA Bridge Master Read Data Channel Signals

Signal	Width	Direction	Description
RID	12 bits	Input	Read ID
RDATA	32, 64, or 128 bits	Input	Read data
RRESP	2 bits	Input	Read response
RLAST	1 bit	Input	Read last data identifier
RVALID	1 bit	Input	Read data channel valid
RREADY	1 bit	Output	Read data channel ready

HPS2FPGA AXI Bridge Module Address Map

Registers in the HPS2FPGA AXI Bridge Module.

Base Address: `0xFF500000`

ID Register Group

Register	Offset	Width	Access	Reset Value	Description
periph_id_4 on page 8-22	0x1FD0	32	RO	0x4	Peripheral ID4 Register

Register	Offset	Width	Access	Reset Value	Description
periph_id_0 on page 8-22	0x1FE0	32	RO	0x1	Peripheral ID0 Register
periph_id_1 on page 8-23	0x1FE4	32	RO	0xB3	Peripheral ID1 Register
periph_id_2 on page 8-23	0x1FE8	32	RO	0x6B	Peripheral ID2 Register
periph_id_3 on page 8-24	0x1FEC	32	RO	0x0	Peripheral ID3 Register
comp_id_0 on page 8-24	0x1FF0	32	RO	0xD	Component ID0 Register
comp_id_1 on page 8-25	0x1FF4	32	RO	0xF0	Component ID1 Register
comp_id_2 on page 8-25	0x1FF8	32	RO	0x5	Component ID2 Register
comp_id_3 on page 8-26	0x1FFC	32	RO	0xB1	Component ID3 Register

32-bit Master

Register	Offset	Width	Access	Reset Value	Description
fn_mod2 on page 8-27	0x2024	32	RW	0x0	Functionality Modification 2 Register
fn_mod on page 8-27	0x2108	32	RW	0x0	Issuing Functionality Modification Register

128-bit Master

Register	Offset	Width	Access	Reset Value	Description
fn_mod2 on page 8-28	0x4024	32	RW	0x0	Functionality Modification 2 Register
fn_mod on page 8-29	0x4108	32	RW	0x0	Issuing Functionality Modification Register

ID Register Group Register Descriptions

Contains registers that identify the ARM NIC-301 IP Core.

Offset: 0x1000

periph_id_4 on page 8-22
JEP106 continuation code

periph_id_0 on page 8-22
Peripheral ID0

periph_id_1 on page 8-23
Peripheral ID1

periph_id_2 on page 8-23
Peripheral ID2

periph_id_3 on page 8-24
Peripheral ID3

comp_id_0 on page 8-24
Component ID0

comp_id_1 on page 8-25
Component ID1

comp_id_2 on page 8-25
Component ID2

comp_id_3 on page 8-26
Component ID3

periph_id_4

JEP106 continuation code

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF501FD0

Offset: 0x1FD0

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								periph_id_4 RO 0x4							

periph_id_4 Fields

Bit	Name	Description	Access	Reset
7:0	periph_id_4	JEP106 continuation code	RO	0x4

periph_id_0

Peripheral ID0

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF501FE0

Offset: 0x1FE0

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								pn7to0 RO 0x1							

periph_id_0 Fields

Bit	Name	Description	Access	Reset
7:0	pn7to0	Part Number [7:0]	RO	0x1

periph_id_1
Peripheral ID1

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF501FE4

Offset: 0x1FE4

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								jep3to0_pn11to8 RO 0xB3							

periph_id_1 Fields

Bit	Name	Description	Access	Reset
7:0	jep3to0_pn11to8	JEP106[3:0], Part Number [11:8]	RO	0xB3

periph_id_2
Peripheral ID2

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF501FE8

Offset: 0x1FE8

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								rev_jepcode_jep6to4 RO 0x6B							

periph_id_2 Fields

Bit	Name	Description	Access	Reset
7:0	rev_jepcode_jep6to4	Revision, JEP106 code flag, JEP106[6:4]	RO	0x6B

periph_id_3
Peripheral ID3

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF501FEC

Offset: 0x1FEC

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								rev_and RO 0x0				cust_mod_num RO 0x0			

periph_id_3 Fields

Bit	Name	Description	Access	Reset
7:4	rev_and	Revision	RO	0x0
3:0	cust_mod_num	Customer Model Number	RO	0x0

comp_id_0
Component ID0

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF501FF0

Offset: 0x1FF0

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0xD							

comp_id_0 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0xD

comp_id_1
Component ID1

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF501FF4

Offset: 0x1FF4

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								genipcompcls_preamble RO 0xF0							

comp_id_1 Fields

Bit	Name	Description	Access	Reset
7:0	genipcompcls_preamble	Generic IP component class, Preamble	RO	0xF0

comp_id_2
Component ID2

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF501FF8

Offset: 0x1FF8

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0x5							

comp_id_2 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0x5

comp_id_3
Component ID3

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF501FFC

Offset: 0x1FFC

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0xB1							

comp_id_3 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0xB1

Master Register Group Register Descriptions

Registers associated with master interfaces.

Offset: 0x2000

32-bit Master Register Descriptions

Registers associated with the 32-bit AXI master interface. These registers are only active when the HPS2FPGA AXI Bridge is configured with a 32-bit FPGA AXI master interface.

Offset: 0x0

fn_mod2 on page 8-27
Controls bypass merge of upsizing/downsizing.

fn_mod on page 8-27
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod2
Controls bypass merge of upsizing/downsizing.

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF502024

Offset: 0x2024

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															bypass_merge RW 0x0

fn_mod2 Fields

Bit	Name	Description	Access	Reset
0	bypass_merge	Controls bypass merge of upsizing/downsizing. **Value** **Description** 0x0 The network can alter transactions. 0x1 The network does not alter any transactions that could pass through the upsizer legally without alteration.	RW	0x0

fn_mod
Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF502108

Offset: 0x2108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

128-bit Master Register Descriptions

Registers associated with the 128-bit AXI master interface. These registers are only active when the HPS2FPGA AXI Bridge is configured with a 128-bit FPGA AXI master interface.

Offset: 0x2000

fn_mod2 on page 8-28
Controls bypass merge of upsizing/downsizing.

fn_mod on page 8-29
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod2

Controls bypass merge of upsizing/downsizing.

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF504024

Offset: 0x4024

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															bypass_merge RW 0x0

fn_mod2 Fields

Bit	Name	Description	Access	Reset
0	bypass_merge	Controls bypass merge of upsizing/downsizing. **Value** **Description** 0x0 The network can alter transactions. 0x1 The network does not alter any transactions that could pass through the upsizer legally without alteration.	RW	0x0

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
hps2fpgaregs	0xFF500000	0xFF504108

Offset: 0x4108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

Lightweight HPS-to-FPGA Bridge

The lightweight HPS-to-FPGA bridge provides a lower-performance interface to the FPGA fabric. This interface is useful for accessing the control and status registers of soft peripherals. The bridge provides a 2 MB address space and access to logic, peripherals, and memory implemented in the FPGA fabric. The MPU subsystem, direct memory access (DMA) controller, and debug access port (DAP) can use the lightweight HPS-to-FPGA bridge to access the FPGA fabric or GPV. Master interfaces in the FPGA fabric can also use the lightweight HPS-to-FPGA bridge to access the GPV registers in all three bridges.

The bridge master exposed to the FPGA fabric has a fixed data width of 32 bits. The slave interface of the bridge in the HPS logic has a fixed data width of 32 bits.

Use the lightweight HPS-to-FPGA bridge as a secondary, lower-performance master interface to the FPGA fabric. With a fixed width and a smaller address space, the lightweight bridge is useful for low-bandwidth traffic, such as memory-mapped register accesses to FPGA peripherals. This approach diverts traffic from the high-performance HPS-to-FPGA bridge, and can improve both CSR access latency and overall system performance.

Table 8-15: Lightweight HPS-to-FPGA Bridge Properties

This table lists the properties of the lightweight HPS-to-FPGA bridge, including the master interface exposed to the FPGA fabric.

Bridge Property	L3 Slave Interface	FPGA Master Interface
Data width	32 bits	32 bits
Clock domain	l4_mp_clk	h2f_lw_axi_clk
Byte address width	32 bits	21 bits
ID width	12 bits	12 bits
Read acceptance	16 transactions	16 transactions
Write acceptance	16 transactions	16 transactions

Bridge Property	L3 Slave Interface	FPGA Master Interface
Total acceptance	32 transactions	32 transactions

The lightweight HPS-to-FPGA bridge has three master interfaces. The master interface connected to the FPGA fabric provides a lightweight interface from the HPS to custom logic in the FPGA fabric. The two other master interfaces, connected to the HPS-to-FPGA and FPGA-to-HPS bridges, allow you to access the GPV registers for each bridge.

The lightweight HPS-to-FPGA bridge also has a set of registers GPV to control the behavior of its four interfaces (one slave and three masters).

The GPV allows you to set the bridge's issuing capabilities to support single or multiple transactions. The GPV also lets you set a write tidemark through the `wr_tidemark` register, to control how much data is buffered in the bridge before data is written to slaves in the FPGA fabric.

Note: It is critical to provide correct clock settings for the lightweight HPS-to-FPGA bridge, even if your design does not use this bridge. The `l4_mp_clk` clock is required for GPV access on the HPS-to-FPGA and FPGA-to-HPS bridges.

Related Information

- **HPS-FPGA Bridges Block Diagram and System Integration** on page 8-3
  Figure showing the lightweight HPS-to-FPGA bridge's three master interfaces
- **The Global Programmers View** on page 8-4
  Includes a description of the lightweight HPS-to-FPGA bridge GPV
- **Interconnect**
  For detailed information about connectivity, such as which masters have access to each bridge, refer to the *Interconnect* chapter of the *Cyclone V Device Handbook, Volume 3*.
- **Interconnect**
  For detailed information about the `wr_tidemark` register, refer to the *Interconnect* chapter of the *Cyclone V Device Handbook, Volume 3*.
- **Instantiating the HPS Component**
  For information about configuring the AXI bridges, refer to the *Instantiating the HPS Component* chapter of the *Cyclone V Device Handbook, Volume 3*.

Lightweight HPS-to-FPGA Bridge Master Signals

All the lightweight HPS-to-FPGA bridge master signals have a fixed width.

The following tables list all the signals exposed by the lightweight HPS-to-FPGA master interface to the FPGA fabric.

Table 8-16: Lightweight HPS-to-FPGA Bridge Master Write Address Channel Signals

Signal	Width	Direction	Description
`AWID`	12 bits	Output	Write address ID
`AWADDR`	21 bits	Output	Write address
`AWLEN`	4 bits	Output	Burst length

Signal	Width	Direction	Description
AWSIZE	3 bits	Output	Burst size
AWBURST	2 bits	Output	Burst type
AWLOCK	2 bits	Output	Lock type—Valid values are 00 (normal access) and 01 (exclusive access)
AWCACHE	4 bits	Output	Cache policy type
AWPROT	3 bits	Output	Protection type
AWVALID	1 bit	Output	Write address channel valid
AWREADY	1 bit	Input	Write address channel ready

Table 8-17: Lightweight HPS-to-FPGA Bridge Master Write Data Channel Signals

Signal	Width	Direction	Description
WID	12 bits	Output	Write ID
WDATA	32 bits	Output	Write data
WSTRB	4 bits	Output	Write data strobes
WLAST	1 bit	Output	Write last data identifier
WVALID	1 bit	Output	Write data channel valid
WREADY	1 bit	Input	Write data channel ready

Table 8-18: Lightweight HPS-to-FPGA Bridge Master Write Response Channel Signals

Signal	Width	Direction	Description
BID	12 bits	Input	Write response ID
BRESP	2 bits	Input	Write response
BVALID	1 bit	Input	Write response channel valid
BREADY	1 bit	Output	Write response channel ready

Table 8-19: Lightweight HPS-to-FPGA Bridge Master Read Address Channel Signals

Signal	Width	Direction	Description
ARID	12 bits	Output	Read address ID
ARADDR	21 bits	Output	Read address
ARLEN	4 bits	Output	Burst length
ARSIZE	3 bits	Output	Burst size
ARBURST	2 bits	Output	Burst type
ARLOCK	2 bits	Output	Lock type—Valid values are 00 (normal access) and 01 (exclusive access)
ARCACHE	4 bits	Output	Cache policy type
ARPROT	3 bits	Output	Protection type
ARVALID	1 bit	Output	Read address channel valid
ARREADY	1 bit	Input	Read address channel ready

Table 8-20: Lightweight HPS-to-FPGA Bridge Master Read Data Channel Signals

Signal	Width	Direction	Description
RID	12 bits	Input	Read ID
RDATA	32 bits	Input	Read data
RRESP	2 bits	Input	Read response
RLAST	1 bit	Input	Read last data identifier
RVALID	1 bit	Input	Read data channel valid
RREADY	1 bit	Output	Read data channel ready

LWHPS2FPGA AXI Bridge Module Address Map

Registers in the LWHPS2FPGA AXI Bridge Module.

Base Address: `0xFF400000`

ID Register Group

Register	Offset	Width	Access	Reset Value	Description
periph_id_4 on page 8-35	0x1FD0	32	RO	0x4	Peripheral ID4 Register
periph_id_0 on page 8-36	0x1FE0	32	RO	0x1	Peripheral ID0 Register
periph_id_1 on page 8-36	0x1FE4	32	RO	0xB3	Peripheral ID1 Register
periph_id_2 on page 8-37	0x1FE8	32	RO	0x6B	Peripheral ID2 Register
periph_id_3 on page 8-37	0x1FEC	32	RO	0x0	Peripheral ID3 Register
comp_id_0 on page 8-38	0x1FF0	32	RO	0xD	Component ID0 Register
comp_id_1 on page 8-38	0x1FF4	32	RO	0xF0	Component ID1 Register
comp_id_2 on page 8-39	0x1FF8	32	RO	0x5	Component ID2 Register
comp_id_3 on page 8-39	0x1FFC	32	RO	0xB1	Component ID3 Register

FPGA2HPS AXI Bridge Registers

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 8-40	0x2008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
ahb_cntl on page 8-41	0x2044	32	RW	0x0	AHB Control Register

HPS2FPGA AXI Bridge Registers

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 8-42	0x3008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
ahb_cntl on page 8-43	0x3044	32	RW	0x0	AHB Control Register

32-bit Master

Register	Offset	Width	Access	Reset Value	Description
fn_mod_bm_iss on page 8-44	0x5008	32	RW	0x0	Bus Matrix Issuing Functionality Modification Register
wr_tidemark on page 8-45	0x5040	32	RW	0x4	Write Tidemark

Register	Offset	Width	Access	Reset Value	Description
fn_mod on page 8-45	0x5108	32	RW	0x0	Issuing Functionality Modification Register

L3 Slave Register Group

Register	Offset	Width	Access	Reset Value	Description
fn_mod on page 8-46	0x45108	32	RW	0x0	Issuing Functionality Modification Register

ID Register Group Register Descriptions

Contains registers that identify the ARM NIC-301 IP Core.

Offset: 0x1000

periph_id_4

JEP106 continuation code

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF401FD0

Offset: 0x1FD0

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								periph_id_4 RO 0x4							

periph_id_4 Fields

Bit	Name	Description	Access	Reset
7:0	periph_id_4	JEP106 continuation code	RO	0x4

periph_id_0
Peripheral ID0

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF401FE0

Offset: 0x1FE0

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								pn7to0 RO 0x1							

periph_id_0 Fields

Bit	Name	Description	Access	Reset
7:0	pn7to0	Part Number [7:0]	RO	0x1

periph_id_1
Peripheral ID1

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF401FE4

Offset: 0x1FE4

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								jep3to0_pn11to8 RO 0xB3							

periph_id_1 Fields

Bit	Name	Description	Access	Reset
7:0	jep3to0_pn11to8	JEP106[3:0], Part Number [11:8]	RO	0xB3

periph_id_2
Peripheral ID2

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF401FE8

Offset: 0x1FE8

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								rev_jepcode_jep6to4 RO 0x6B							

periph_id_2 Fields

Bit	Name	Description	Access	Reset
7:0	rev_jepcode_jep6to4	Revision, JEP106 code flag, JEP106[6:4]	RO	0x6B

periph_id_3
Peripheral ID3

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF401FEC

Offset: 0x1FEC

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								rev_and RO 0x0				cust_mod_num RO 0x0			

periph_id_3 Fields

Bit	Name	Description	Access	Reset
7:4	rev_and	Revision	RO	0x0
3:0	cust_mod_num	Customer Model Number	RO	0x0

comp_id_0
Component ID0

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF401FF0

Offset: 0x1FF0

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0xD							

comp_id_0 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0xD

comp_id_1
Component ID1

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF401FF4

Offset: 0x1FF4

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								genipcompcls_preamble RO 0xF0							

comp_id_1 Fields

Bit	Name	Description	Access	Reset
7:0	genipcompcls_preamble	Generic IP component class, Preamble	RO	0xF0

comp_id_2
Component ID2

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF401FF8

Offset: 0x1FF8

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0x5							

comp_id_2 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0x5

comp_id_3
Component ID3

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF401FFC

Offset: 0x1FFC

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								preamble RO 0xB1							

comp_id_3 Fields

Bit	Name	Description	Access	Reset
7:0	preamble	Preamble	RO	0xB1

Master Register Group Register Descriptions

Registers associated with master interfaces.

Offset: 0x2000

FPGA2HPS AXI Bridge Registers Register Descriptions

Registers associated with the FPGA2HPS master interface. This master interface provides access to the registers in the FPGA2HPS AXI Bridge.

Offset: 0x0

fn_mod_bm_iss on page 8-40
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

ahb_cntl on page 8-41
Sets the block issuing capability to one outstanding transaction.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF402008

Offset: 0x2008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

ahb_cntl

Sets the block issuing capability to one outstanding transaction.

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF402044

Offset: 0x2044

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														force_incr RW 0x0	decerr_en RW 0x0

ahb_cntl Fields

Bit	Name	Description	Access	Reset
1	force_incr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 If a beat is received that has no write data strobes set, that write data beat is replaced with an IDLE beat. Also, causes all transactions that are to be output to the AHB domain to be an undefined length INCR.	RW	0x0

Bit	Name	Description	Access	Reset
0	decerr_en	**Value** **Description** 0x0 No DECERR response. 0x1 If the AHB protocol conversion function receives an unaligned address or a write data beat without all the byte strobes set, creates a DECERR response.	RW	0x0

HPS2FPGA AXI Bridge Registers Register Descriptions

Registers associated with the HPS2FPGA master interface. This master interface provides access to the registers in the HPS2FPGA AXI Bridge.

Offset: 0x1000

fn_mod_bm_iss on page 8-42
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

ahb_cntl on page 8-43
Sets the block issuing capability to one outstanding transaction.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF403008

Offset: 0x3008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0

Bit	Name	Description	Access	Reset
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

ahb_cntl

Sets the block issuing capability to one outstanding transaction.

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF403044

Offset: 0x3044

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														force_incr RW 0x0	decerr_en RW 0x0

ahb_cntl Fields

Bit	Name	Description	Access	Reset
1	force_incr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 If a beat is received that has no write data strobes set, that write data beat is replaced with an IDLE beat. Also, causes all transactions that are to be output to the AHB domain to be an undefined length INCR.	RW	0x0

Bit	Name	Description	Access	Reset
0	decerr_en	Value: Description 0x0: No DECERR response. 0x1: If the AHB protocol conversion function receives an unaligned address or a write data beat without all the byte strobes set, creates a DECERR response.	RW	0x0

32-bit Master Register Descriptions

Registers associated with the 32-bit AXI master interface. This master provides access to slaves in the FPGA.

Offset: 0x3000

fn_mod_bm_iss on page 8-44
Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

wr_tidemark on page 8-45
Controls the release of the transaction in the write data FIFO.

fn_mod on page 8-45
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod_bm_iss

Sets the issuing capability of the preceding switch arbitration scheme to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF405008

Offset: 0x5008

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod_bm_iss Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

wr_tidemark

Controls the release of the transaction in the write data FIFO.

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF405040

Offset: 0x5040

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												level RW 0x4			

wr_tidemark Fields

Bit	Name	Description	Access	Reset
3:0	level	Stalls the transaction in the write data FIFO until the number of occupied slots in the write data FIFO exceeds the level. Note that the transaction is released before this level is achieved if the network receives the WLAST beat or the write FIFO becomes full.	RW	0x4

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF405108

Offset: 0x5108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

Slave Register Group Register Descriptions

Registers associated with slave interfaces.

Offset: 0x42000

L3 Slave Register Group Register Descriptions

Registers associated with the 32-bit AXI slave interface. This slave connects to the L3 Interconnect.

Offset: 0x3000

fn_mod on page 8-46
Sets the block issuing capability to multiple or single outstanding transactions.

fn_mod

Sets the block issuing capability to multiple or single outstanding transactions.

Module Instance	Base Address	Register Address
lwhps2fpgaregs	0xFF400000	0xFF445108

Offset: 0x45108

Access: RW

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														wr RW 0x0	rd RW 0x0

fn_mod Fields

Bit	Name	Description	Access	Reset
1	wr	**Value** **Description** 0x0 Multiple outstanding write transactions 0x1 Only a single outstanding write transaction	RW	0x0
0	rd	**Value** **Description** 0x0 Multiple outstanding read transactions 0x1 Only a single outstanding read transaction	RW	0x0

FPGA Slaves Accessed Via Lightweight HPS2FPGA AXI Bridge (lwfpgaslaves) Address Map

This address space is allocated for FPGA-configured slaves driven by the lightweight HPS-to-FPGA bridge master. Address assignment within this space is user-defined. For more information about Lightweight HPS-to-FPGA bridges, refer to the *HPS-FPGA Bridges* chapter of the *Hard Processor System Technical Reference Manual*.

Table 8-21: lwfpgaslaves Address Range

Module Instance	Start Address	End Address
LWFPGASLAVES	0xFF200000	0xFF3FFFFF

Clocks and Resets

FPGA-to-HPS Bridge Clocks and Resets

The master interface of the bridge in the HPS logic operates in the `l3_main_clk` clock domain. The slave interface exposed to the FPGA fabric operates in the `f2h_axi_clk` clock domain provided by the user logic. The bridge provides clock crossing logic that allows the logic in the FPGA to operate in any clock domain, asynchronous from the HPS.

The FPGA-to-HPS bridge has one reset signal, `fpga2hps_bridge_rst_n`. The reset manager drives this signal to FPGA-to-HPS bridge on a cold or warm reset.

Related Information

- **Clock Manager**
  For information about the l3_main_clk and l4_mp_clk clocks, refer to the *Clock Manager* chapter of the *Cyclone V Device Handbook, Volume 3*.
- **http://www.altera.com/literature/hb/cyclone-v/cv_54003.pdf**
- **HPS Component Interfaces**
  For information about the f2h_axi_clk clock, refer to the *HPS Component Interfaces* chapter of the *Cyclone V Device Handbook, Volume 3*.

HPS-to-FPGA Bridge Clocks and Resets

The master interface into the FPGA fabric operates in the `h2f_axi_clk` clock domain. The `h2f_axi_clk` clock is provided by user logic. The slave interface of the bridge in the HPS logic operates in the `l3_main_clk` clock domain. The bridge provides clock crossing logic that allows the logic in the FPGA to operate in any clock domain, asynchronous from the HPS.

The HPS-to-FPGA bridge has one reset signal, `hps2fpga_bridge_rst_n`. The reset manager drives this signal to HPS-to-FPGA bridge on a cold or warm reset.

Related Information

- **Clock Manager**
  For information about the l3_main_clk and l4_mp_clk clocks, refer to the *Clock Manager* chapter of the *Cyclone V Device Handbook, Volume 3*.
- **http://www.altera.com/literature/hb/cyclone-v/cv_54003.pdf**
- **HPS Component Interfaces**
  For information about the f2h_axi_clk clock, refer to the *HPS Component Interfaces* chapter of the *Cyclone V Device Handbook, Volume 3*.

Lightweight HPS-to-FPGA Bridge Clocks and Resets

The master interface into the FPGA fabric operates in the `h2f_lw_axi_clk` clock domain provided by custom logic in the FPGA fabric. The slave interface of the bridge in the HPS logic operates in the `l4_mp_clk` clock domain. The bridge provides clock crossing logic that allows the logic in the FPGA to operate in any clock domain, asynchronous from the HPS.

The lightweight HPS-to-FPGA bridge has one reset signal, `lwhps2fpga_bridge_rst_n`. The reset manager drives this signal to the lightweight HPS-to-FPGA bridge on a cold or warm reset.

Related Information

- **Clock Manager**
  For information about the l3_main_clk and l4_mp_clk clocks, refer to the *Clock Manager* chapter of the *Cyclone V Device Handbook, Volume 3*.
- **http://www.altera.com/literature/hb/cyclone-v/cv_54003.pdf**
- **HPS Component Interfaces**
  For information about the f2h_axi_clk clock, refer to the *HPS Component Interfaces* chapter of the *Cyclone V Device Handbook, Volume 3*.

GPV Clocks

The FPGA-to-HPS and HPS-to-FPGA bridges have GPV slave interfaces, mastered by the lightweight HPS-to-FPGA bridge. These interfaces operate in the `l4_mp_clk` clock domain. Even if you do not use the lightweight HPS-to-FPGA bridge in your FPGA design, you must ensure that a valid `l4_mp_clk` clock is

being generated, so that the GPV registers in the HPS-to-FPGA and FPGA-to-HPS bridges can be programmed. The GPV logic in all three bridges is in the `l4_mp_clk` domain.

Related Information

The Global Programmers View on page 8-4

Data Width Sizing

The HPS-to-FPGA and FPGA-to-HPS bridges allow 32-, 64-, and 128-bit interfaces to be exposed to the FPGA fabric. For 32-bit and 128-bit interfaces, the bridge performs data width conversion to the fixed 64-bit interface within the HPS. This conversion is called *upsizing* in the case of data being converted from a 64-bit interface to a 128-bit interface. It is called *downsizing* in the case of data being converted from a 64-bit interface to a 32-bit interface. If an exclusive access is split into multiple transactions, the transactions lose their exclusive access information.

During the upsizing or downsizing process, transactions can also be resized using a data merging technique. For example, in the case of a 32-bit to 64-bit upsizing, if the size of each beat entering the bridge's 32-bit interface is only two bytes, the bridge can merge up to four beats to form a single 64-bit beat. Similarly, in the case of a 128-bit to 64-bit downsizing, if the size of each beat entering the bridge's 128-bit interface is only four bytes, the bridge can merge two beats to form a single 64-bit beat.

The bridges do not perform transaction merging for accesses marked as noncacheable.

Note: You can set the `bypass_merge` bit in the GPV to prevent the bridge from merging data and responses. If the bridge merges multiple responses into a single response, that response is the one with the highest priority. The response types have the following priorities:

1. DECERR
2. SLVERR
3. OKAY

HPS-FPGA Bridges Address Map and Register Definitions

The address map and register definitions for the HPS-FPGA bridges consist of the following regions:

- FPGA-to-HPS Bridge Module
- HPS-to-FPGA Bridge Module
- Lightweight HPS-to-FPGA Bridge Module
- FPGA Slaves Accessed via Lightweight HPS-to-FPGA AXI Bridge

Related Information

- **FPGA2HPS AXI Bridge Module Address Map** on page 8-8
- **HPS2FPGA AXI Bridge Module Address Map** on page 8-20
- **LWHPS2FPGA AXI Bridge Module Address Map** on page 8-33
- **FPGA Slaves Accessed Via Lightweight HPS2FPGA AXI Bridge (lwfpgaslaves) Address Map** on page 8-47

This address space is allocated for FPGA-configured slaves driven by the lightweight HPS-to-FPGA bridge master. Address assignment within this space is user-defined. For more information about Lightweight HPS-to-FPGA bridges, refer to the *HPS-FPGA Bridges* chapter of the *Hard Processor System Technical Reference Manual*.

- **Introduction to the Hard Processor System**
  Lists the base addresses of all modules
- **Cyclone V SoC HPS Address Map and Register Definitions**
  Web-based address map and register definitions

Document Revision History

Table 8-22: Document Revision History

Date	Version	Changes
June 2014	2014.06.30	Added address maps and register definitions
February 2014	2014.02.28	Maintenance release
December 2013	2013.12.30	Maintenance release
November 2012	1.1	Described GPV
January 2012	1.0	Initial release