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ECE 4203

PROJECT 2: SPICE Simulations for Logical Effort

Steps:

LTSpice Simulation Tutorial

1) This is not required, but highly recommended. Go through the simulation tutorial described in https://youtu.be/IpArMJVgYS0. This project also draws heavily from **Chapter 8.4 of Weste and Harris**.

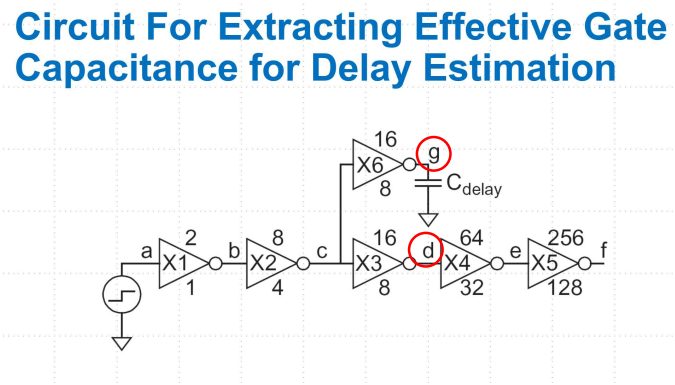
Logical Effort

2) Find the effective gate capacitance (per µm transistor width) for the process by using procedure in "Weste and Harris", section 8.4.3. For this simulation use inverters as shown in the schematic below.

Hints:

a) For this simulation, make sure to set the transistor parameters related to output diffusion area to zero (i.e. set AD, AS, PD, PS to zero for both NMOS and PMOS). If you don't do this, you won't be able to isolate just the gate capacitance.

b) Once you've equalized the delays to nodes "d" and "g", remember to divide by gate width of your load to get fF/µm of transistor width (note that is the not capacitance per unit area, so you'll have to normalize for gate length.

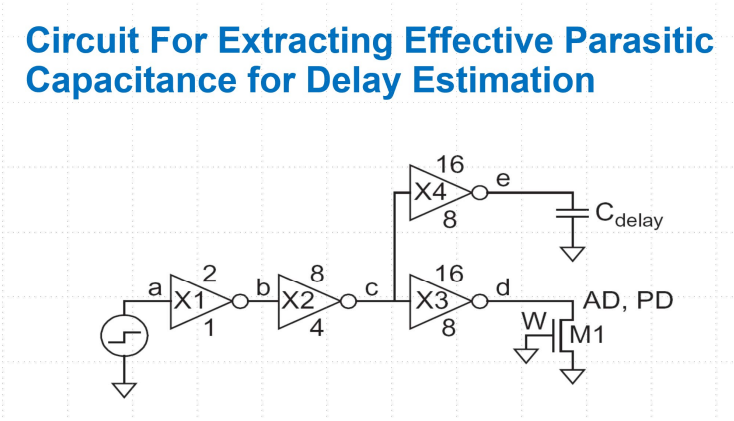


3) Find the effective parasitic capacitance of the transistor drains (per µm transistor width) for the process. You'll have to do a separate simulation for PMOS. For PMOS the schematic use a PMOS with it's Gate and Source connected to VDD. Use inverters for this simulation.

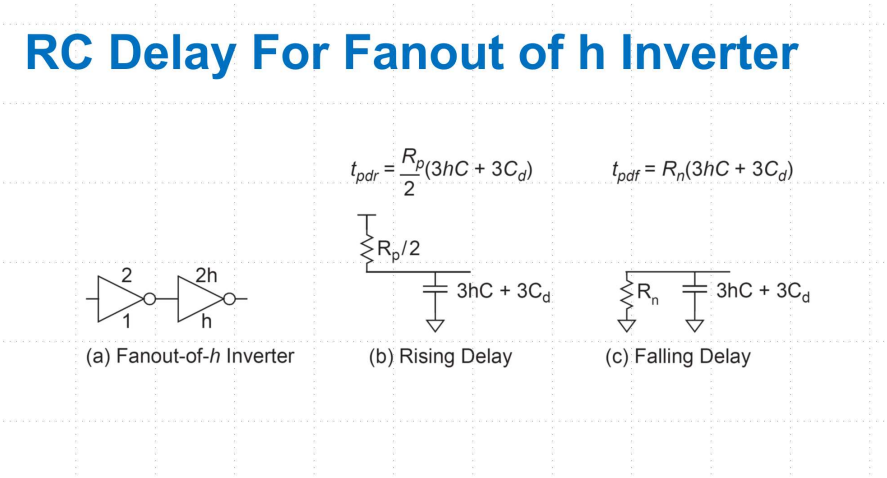
Hints:

a) For this simulation, make sure to set the transistor parameters related to output diffusion area to the appropriate value (i.e. calculate AD, AS, PD, PS to zero for both NMOS and PMOS). If you don't, you won't get the appropriate diffusion capacitance. Watch you units carefully here – you can easily end up with orders of magnitude higher capacitance).

b) Once you've equalized the delays to nodes "d" and "g", remember to divide by gate width of your load to get fF/µm of transistor width.



4) Calculate the Effective resistance of the process:



The dependence on parasitics can be removed by calculating the difference between delays at different fanouts. For example, the difference between delays for $h = 3$ and $h = 4$ are

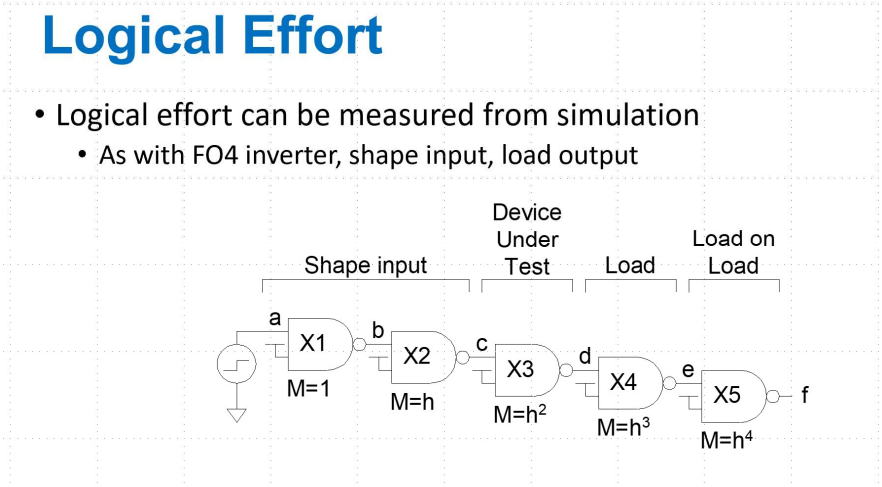
$$\Delta t_{pdr} = \frac{R_p}{2}(3\times 4\times C + 3C_d) - \frac{R_p}{2}(3\times 3\times C + 3C_d) = \tfrac{3}{2}R_pC \qquad (8.7)$$

$$\Delta t_{pdf} = R_n(3\times 4\times C + 3C_d) - R_n(3\times 3\times C + 3C_d) = 3R_nC$$

As C is known from the effective gate capacitance extraction, R_n and R_p are readily calculated. These represent the effective resistance of single nMOS and pMOS transistors for delay estimation.

Excerpt from "Weste and Harris", section 8.4.5

5) Logical effort simulation
   a. **Simulate** the logical effort **of the circuit assigned to you in Project 1**.
   b. Use the methodology in Section 8.5.3 of Weste and Harris (figure replicated below for your reference).
   c. Plot the logical effort for your circuit for h=1, 2, 3, and 4

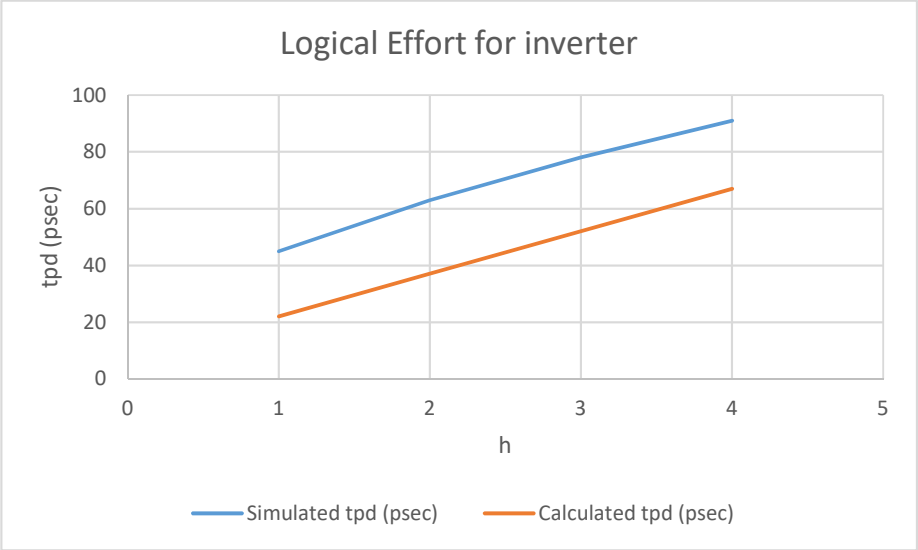


6) Logical effort calculation
   a. **Calculate** the logical effort **of the circuit assigned to you in Project 1**.
   b. Plot the logical effort for your circuit for h=1, 2, 3, and 4 using the values for gate capacitance, parasitic capacitance, and equivalent resistance that you found in problems steps 2, 3, and 5.

Results:

1) **Write down your simulated values for R_N, R_P, C_{gn}, C_{gp}, C_{dn}, C_{dp} from 2,3 and 4 above.**
2) **Use Microsoft Excel to merge the two plots created in 5c and 6b**
3) **Turn in a printout with both. Make sure to include your name.**

The graph below is an example of what this should look like (the example is for a minimum sized inverter).



Plot example for project results