



Name : CJ kiran  
Reg Noe : 24MVD0166  
School : SENSE

## ASIC DESIGN LAB

**Prof. Dr. Nithish Kumar V**

### TASK-02

**Question :**

**ALU Logical Synthesis & Physical Synthesis.**

## Logical Synthesis

```
Activities alu.tcl (v-ALU_8) - gnuif (m synopsys.vit.ac.in) Feb 6 14:40
Open - alu.tcl alu.tcl alu.tcl Save
set svf "alu_top.svf"
set search_path "/home/synopsys/installs/LIBRARIES/SAED14nm_EDK_00_2024/SAED14nm_EDK_STD_RVT/liberty/nldm/base -/ ";
set TARGET_LIBRARY_FILES saed14rvt_base.t06p65v25c.db;

set app_var search_path "$search_path"
set_app_var target_library TARGET_LIBRARY_FILES
set_app_var link_library - target_library

## Point to the new 14nm SAED libs
#set DESIGN_REF_PATH "/home/synopsys/installs/LIBRARIES/SAED14nm_EDK_00_2024/SAED14nm_EDK_STD_RVT/liberty/nldm/base"

#set SEARCH_PATH ". / \\"
#$(DESIGN_REF_PATH)\

#set TARGET_LIBRARY_FILES "\\"
#$(DESIGN_REF_PATH)/stdcell_rvt/t06p6v125c.db \
#$(DESIGN_REF_PATH)/stdcell_hvt/db_nldm/saed14hvt_t06p6v125c.db \
#$(DESIGN_REF_PATH)/stdcell_lvt/db_nldm/saed14lvt_t06p6v125c.db"

#set LINK_LIBRARY_FILES "\\"
#$(DESIGN_REF_PATH)/stdcell_rvt/db_nldm/saed14rvt_t06p6v125c.db \
#$(DESIGN_REF_PATH)/stdcell_rvt/db_nldm/saed14rvt_t06p6v125c.db \
#$(DESIGN_REF_PATH)/stdcell_lvt/db_nldm/saed14lvt_t06p6v125c.db \
#$(DESIGN_REF_PATH)/stdcell_rvt/db_nldm/saed14rvt_t06p6v125c.db \
g*

#####
# Logical Library Settings
#####
set app_var search_path "$search_path"
set_app_var target_library "TARGET_LIBRARY_FILES"
set_app_var link_library "$LINK_LIBRARY_FILES"

read_verilog alu_top.v,arith_block.v,comparator_block.v,logic_block.v,mux_v,fa_v,ha_v,reg_block.v,shifter_block.v
# write all verilog file name

current design alu

#set operating_conditions t06p6v125c
#set operating_conditions -min f06p6bv125c -max ss0p6v125c

link

## Generating intermediate technology independent (GTECH) design #####
#write_file -format verilog -output ./alu_gtech.v

check design quality
check_design

source ./alu.sdc

Tcl Tab Width: 8 Ln: 1, Col: 19
```

**ALU\_TCL**

```
Activities alu.tcl (-ALU_3) - gedit [on synopsys.vta.ac.in] Feb 6 14:40
Open alu.tcl alu.sdc alu.tclv
Save

set svf "alu_top.svf"

set search_path "~/root/synopsys/installs/LIBRARIES/SAEDI4nm_EDK_08_2024/SAEDI4nm_EDK STD RV7/liberty/nldm/base ./" ;
set TARGET_LIBRARY_FILES saedi4rvrt_base_tt08bv125c.db;

set app_var search_path "$search_path"
set app_var target_library $TARGET_LIBRARY_FILES
set app_var link_library "$target_library"

## Point to the new 14nm SAED libs
#set DESIGN_REF_PATH "~/root/synopsys/installs/LIBRARIES/SAEDI4nm_EDK_08_2024/SAEDI4nm_EDK STD RV7/liberty/nldm/base"

#set SEARCH_PATH "*" ; \
#$(DESIGN_REF_PATH)*

#set TARGET_LIBRARY_FILES "*" \
#$(DESIGN_REF_PATH)/saedi4rvrt_tt08bv125c.db \
#$(DESIGN_REF_PATH)/stdcell_rvt/db/nldm/saedi4rvrt_tt08bv125c.db \
#$(DESIGN_REF_PATH)/stdcell_lv1/db/nldm/saedi4rvrt_tt08bv125c.db \

#set LINK_LIBRARY_FILES "*" \
#$(DESIGN_REF_PATH)/stdcell_rvt/db/nldm/saedi4rvrt_tt08bv125c.db \
#$(DESIGN_REF_PATH)/stdcell_rvt/db/nldm/saedi4rvrt_tt08bv125c.db \
#$(DESIGN_REF_PATH)/stdcell_rvt/db/nldm/saedi4rvrt_tt08bv125c.db \
#

#####
# Logical Library Settings
#####
#set app_var search_path "$SEARCH_PATH"
#set app_var target_library "$TARGET_LIBRARY_FILES"
#set app_var link_library "$LINK_LIBRARY_FILES"

read verilog alu_top.v,arith_block.v,comparator_block.v,logic_block.v,mux.v,fa.v,ha.v,reg_block.v,shifter_block.v
write all verilog file name

current_design alu_top

#set operating_conditions tt08bv125c
#set operating_conditions -min ffp08bv125c -max ssdp6v125c

link

## Generating intermediate technology independent (GTECH) design #####
#write file -format verilog -output ./alu_gtech.v

# check design quality
check_design

source ./alu.sdc

Verilog Tab Width: 8 Ln 1, Col 1
```

## ALU\_TCL

```
Documents ▾ Open ▾ mylogic_netlist.v ~ALU_8 Save ▢ ▢ ▢
tcl x alu.tcl x constraint.sdc x alu.sdc x mylogic_netlist.v
straint.sdc x // Created by: Synopsys DC Ultra(TM) in wire load mode
.sdc x // Version : V-2023.12-SP4
// Date : Wed Feb 5 10:59:43 2025
logic_netlist.v
module alu ( f, z, c, v, agtb, altb, aeqb, a, b, s, clk, rst );
output [7:0] f;
input [7:0] a;
input [7:0] b;
input [3:0] s;
input clk, rst;
output z, c, v, agtb, altb, aeqb;
wire s_r_3, n156, n158, n159, n160, n161, n162, n163, n164, n165, n166,
n167, n168, n169, n170, n171, n172, n173, n174, n175, n176, n177,
n178, n179, n180, n181, n182, n183, n184, n185, n186, n187, n188,
n189, n190, n191, n192, n193, n194, n195, n196, n197, n198, n199,
n200, n201, n202, n203, n204, n205, n206, n207, n208, n209, n210,
n211, n212, n213, n214, n215, n216, n217, n218, n219, n220, n221,
n222, n223, n224, n225, n226, n227, n228, n229, n230, n231, n232,
n233, n234, n235, n236, n237, n238, n239, n240, n241, n242, n243,
n244, n245, n246, n247, n248, n249, n250, n251, n252, n253;
wire [7:0] a_r;
wire [7:0] b_r;
tri clk;
tri rst;
reg_block rb ( .p1(clk), .p2(rst) );
SAEDRVT14 FDPBQ V2LP_0P5 a_r_reg_7 ( .D(a[7]), .CK(clk), .RD(n156), .Q(
a_r[7]) );
SAEDRVT14 FDPBQ V2LP_0P5 a_r_reg_5 ( .D(a[5]), .CK(clk), .RD(n156), .Q(
a_r[5]) );
SAEDRVT14 FDPBQ V2LP_0P5 a_r_reg_6 ( .D(a[6]), .CK(clk), .RD(n156), .Q(
a_r[6]) );
SAEDRVT14 FDPBQ V2LP_0P5 a_r_reg_2 ( .D(a[2]), .CK(clk), .RD(n156), .Q(
a_r[2]) );
SAEDRVT14 FDPBQ V2LP_0P5 a_r_reg_3 ( .D(a[3]), .CK(clk), .RD(n156), .Q(
a_r[3]) );
SAEDRVT14 FDPBQ V2LP_0P5 b_r_reg_7 ( .D(b[7]), .CK(clk), .RD(n156), .Q(
b_r[7]) );
SAEDRVT14 FDPBQ V2LP_0P5 a_r_reg_4 ( .D(a[4]), .CK(clk), .RD(n156), .Q(
a_r[4]) );
SAEDRVT14 FDPBQ V2LP_0P5 b_r_reg_6 ( .D(b[6]), .CK(clk), .RD(n156), .Q(
b_r[6]) );
SAEDRVT14 FDPBQ V2LP_0P5 a_r_reg_0 ( .D(a[0]), .CK(clk), .RD(n156), .Q(
a_r[0]) );
SAEDRVT14 FDPBQ V2LP_0P5 b_r_reg_5 ( .D(b[5]), .CK(clk), .RD(n156), .Q(
b_r[5]) );
SAEDRVT14 FDPBQ V2LP_0P5 b_r_reg_2 ( .D(b[2]), .CK(clk), .RD(n156), .Q(
b_r[2]) );
SAEDRVT14 FDPBQ V2LP_0P5 a_r_reg_1 ( .D(a[1]), .CK(clk), .RD(n156), .Q(
a_r[1]) );
SAEDRVT14 FDPBQ V2LP_0P5 b_r_reg_3 ( .D(b[3]), .CK(clk), .RD(n156), .Q(
a_r[1]) );
Verilog ▾ Tab Width: 8 ▾ Ln 1, Col 1 ▾
```

## mylogic\_netlist.v

```
Activities ▢ alu.tcl (~ALU_8) - gedit (on synopsys.vit.ac.in) ▾ Feb 6 14:40 ▢
Open ▾ alu.sdc ~ALU_8 Save ▢ ▢ ▢
alu.tcl x alu.sdc x alu.tcl.v
# Created by write_sdc on Thu Feb 6 14:37:00 2025
#####
#####
set sdc version 2.1
#####
set units -time ns -resistance kOhm -capacitance pF -voltage V -current uA
set wire_load_model top
set wire_load_model -name 8000 -library saed14rvt_base_tt0p65v25c
set_max_transition 0.5 [current_design]
set_max_fanout 20 [current_design]
set_max_capacitance 100 [current_design]
create_clock [get_ports clk] -name clock -period 10 -waveform {0 5}
set_clock_latency 1 [get_clocks clock]
set_clock_latency -source 1 [get_clocks clock]
set_clock_uncertainty 0.15 [get_clocks clock]
set_clock_transition -max -rise 0.12 [get_clocks clock]
set_clock_transition -max -fall 0.12 [get_clocks clock]
set_clock_transition -min -rise 0.12 [get_clocks clock]
set_clock_transition -min -fall 0.12 [get_clocks clock]
group_path -name CLOCK -to [get_clocks clock]
group_path -name INPUTS -through [list [get_ports {a[7]}] [get_ports {a[6]}] [get_ports {a[5]}] \
[get_ports {a[4]}] [get_ports {a[3]}] [get_ports {a[2]}] [get_ports {a[1]}] \
[get_ports {a[0]}] [get_ports {b[7]}] [get_ports {b[6]}] [get_ports {b[5]}] \
[get_ports {b[4]}] [get_ports {b[3]}] [get_ports {b[2]}] [get_ports {b[1]}] \
[get_ports {b[0]}] [get_ports {s[3]}] [get_ports {s[2]}] [get_ports {s[1]}] \
[get_ports {s[0]}] [get_ports clk] [get_ports rst]]
group_path -name OUTPUTS -to [list [get_ports {f[7]}] [get_ports {f[6]}] [get_ports {f[5]}] [get_ports \
{f[4]}] [get_ports {f[3]}] [get_ports {f[2]}] [get_ports {f[1]}] [get_ports \
{f[0]}] [get_ports z] [get_ports c] [get_ports v] [get_ports agtb] [get_ports \
altb] [get_ports aeqb]]
set_input_delay -clock clock -max 1 [get_ports clk]
set_input_delay -clock clock -min 0.5 [get_ports clk]
set_input_delay -clock clock -max 1 [get_ports {a[7]}]
set_input_delay -clock clock -min 0.5 [get_ports {a[7]}]
set_input_delay -clock clock -max 1 [get_ports {a[6]}]
set_input_delay -clock clock -min 0.5 [get_ports {a[6]}]
set_input_delay -clock clock -max 1 [get_ports {a[5]}]
set_input_delay -clock clock -min 0.5 [get_ports {a[5]}]
set_input_delay -clock clock -max 1 [get_ports {a[4]}]
set_input_delay -clock clock -min 0.5 [get_ports {a[4]}]
set_input_delay -clock clock -max 1 [get_ports {a[3]}]
set_input_delay -clock clock -min 0.5 [get_ports {a[3]}]
set_input_delay -clock clock -max 1 [get_ports {a[2]}]
set_input_delay -clock clock -min 0.5 [get_ports {a[2]}]
set_input_delay -clock clock -max 1 [get_ports {a[1]}]
set_input_delay -clock clock -min 0.5 [get_ports {a[1]}]
set_input_delay -clock clock -max 1 [get_ports {a[0]}]
set_input_delay -clock clock -min 0.5 [get_ports {a[0]}]
set_input_delay -clock clock -max 1 [get_ports {b[7]}]
set_input_delay -clock clock -min 0.5 [get_ports {b[7]}]
```

## ALU\_SDC

```
#set sdc version 2.1
reset_design

set PERIOD 10.0
set INPUT_DELAY 1.0
set OUTPUT_DELAY 1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_TO_DELAY 0.5

## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports clk]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]

#set_min_pulse_width 5 [get_clocks clock]

## GROUPING
group_path -name CLOCK\
-to clock\
-weight 1

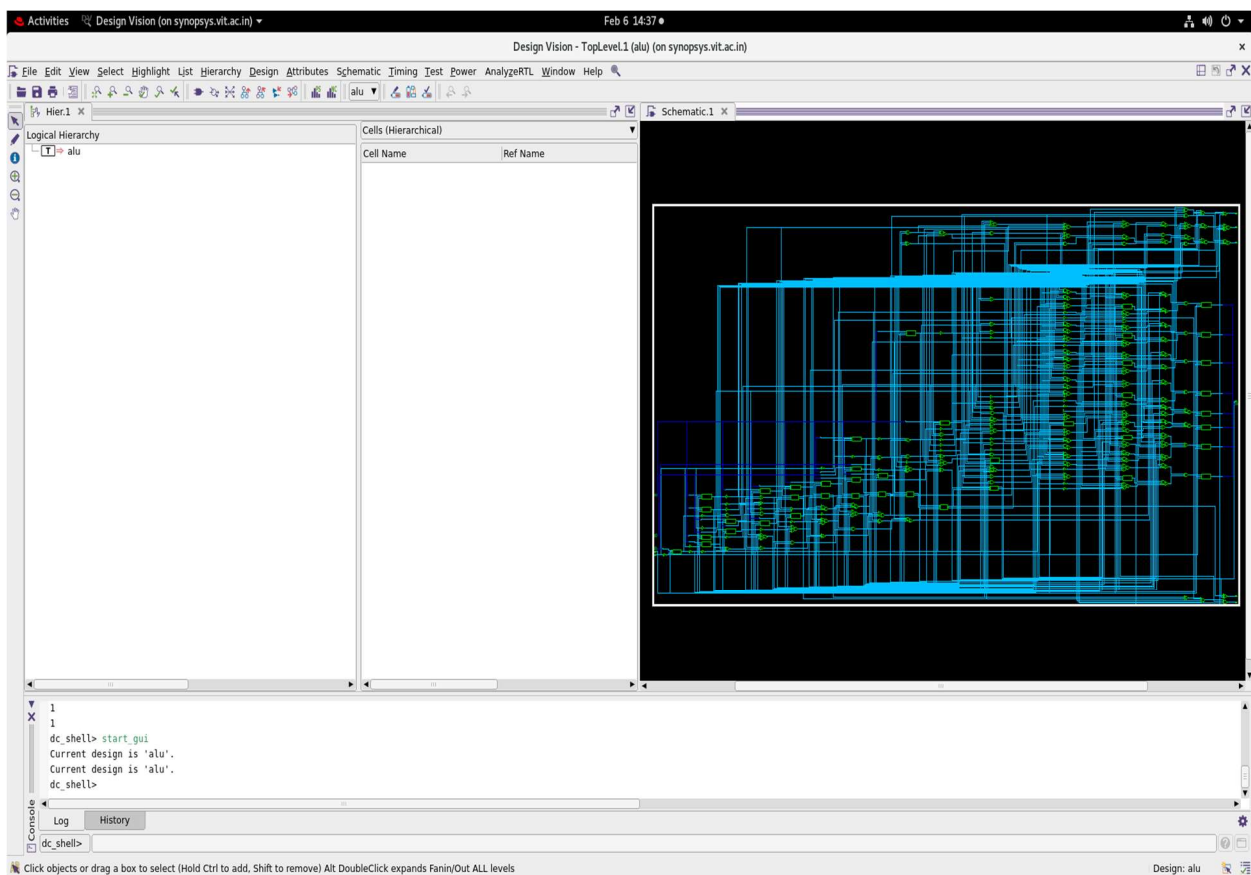
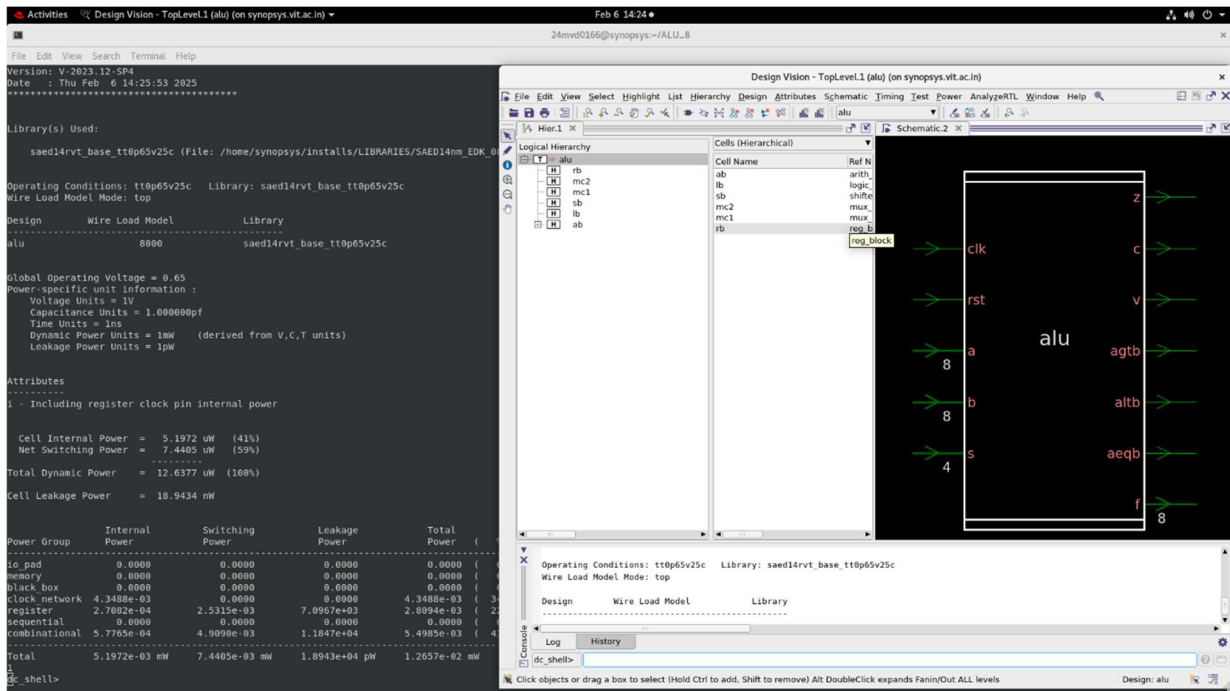
group_path -name INPUTS\
-through [all_inputs]\
-weight 1

group_path -name OUTPUTS\
-to [all_outputs]\
-weight 1

## IN/OUT
#set INPUTPORTS [remove_from_collection [all_inputs] [get_ports clk]]
set INPUTPORTS [all_inputs]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_input_delay -clock "clock" -min $MIN_TO_DELAY $INPUTPORTS
```

## Constraint.sdc



```
Activities Terminal Feb 6 14:23 24mvd0166@synopsys:~/ALU_8
File Edit View Search Terminal Help
Version: V-2023.12-SP4
Date : Thu Feb 6 14:25:53 2025
*****
Library(s) Used:
  saed14rvt_base_tt0p65v25c (File: /home/synopsys/installs/LIBRARIES/SAED14nm_EDK_00_2024/SAED14nm_EDK_STD_RVT/Liberty/nldm/base/saed14rvt_base_tt0p65v25c.db)

Operating Conditions: tt0p65v25c Library: saed14rvt_base_tt0p65v25c
Wire Load Model Mode: top

Design Wire Load Model Library
alu 8000 saed14rvt_base_tt0p65v25c

Global Operating Voltage = 0.65
Power-specific unit information :
  Voltage Units = 1V
  Capacitance Units = 1.000000pf
  Time Units = 1ns
  Dynamic Power Units = 1mW (derived from V,C,T units)
  Leakage Power Units = 1pW

Attributes
i - Including register clock pin internal power

Cell Internal Power = 5.1972 uW (41%)
Net Switching Power = 7.4405 uW (59%)
-----
Total Dynamic Power = 12.6377 uW (100%)
Cell Leakage Power = 10.9434 nW

Power Group Internal Power Switching Power Leakage Power Total Power ( % ) Attrs
-----
io_pad 0.0000 0.0000 0.0000 0.0000 ( 0.00%)
memory 0.0000 0.0000 0.0000 0.0000 ( 0.00%)
black_box 0.0000 0.0000 0.0000 0.0000 ( 0.00%)
clock_network 4.3480e-03 0.0000 0.0000 4.3480e-03 ( 34.30%) 1
register 2.7082e-04 2.5315e-03 7.0967e+03 2.8094e-03 ( 22.20%)
sequential 0.0000 0.0000 0.0000 0.0000 ( 0.00%)
combinational 5.7765e-04 4.9090e-03 1.1847e+04 5.4985e-03 ( 43.44%)
-----
Total 5.1972e-03 mW 7.4405e-03 mW 1.8943e+04 pW 1.2657e-02 mW
1
dc_shell>
```

Activities Design Vision - TopLevel1 (alu) (on synopsys.vit.ac.in) Feb 6 14:24 24mvd0166@synopsys:~/ALU\_8

File Edit View Search Terminal Help

Version: V-2023.12-SP4  
Date : Thu Feb 6 14:25:53 2025  
\*\*\*\*\*

Library(s) Used:  
saed14rvt\_base\_tt0p65v25c (File: /home/synopsys/installs/LIBRARIES/SAED14nm\_EDK\_00\_2024/SAED14nm\_EDK\_STD\_RVT/Liberty/nldm/base/saed14rvt\_base\_tt0p65v25c.db)

Operating Conditions: tt0p65v25c Library: saed14rvt\_base\_tt0p65v25c  
Wire Load Model Mode: top

Design Wire Load Model Library  
alu 8000 saed14rvt\_base\_tt0p65v25c

Global Operating Voltage = 0.65  
Power-specific unit information :  
Voltage Units = 1V  
Capacitance Units = 1.000000pf  
Time Units = 1ns  
Dynamic Power Units = 1mW (derived from V,C,T units)  
Leakage Power Units = 1pW

Attributes  
i - Including register clock pin internal power

Cell Internal Power = 5.1972 uW (41%)  
Net Switching Power = 7.4405 uW (59%)  
-----  
Total Dynamic Power = 12.6377 uW (100%)  
Cell Leakage Power = 10.9434 nW

Power Group Internal Power Switching Power Leakage Power Total Power ( % ) Attrs  
-----  
io\_pad 0.0000 0.0000 0.0000 0.0000 ( 0.00%)  
memory 0.0000 0.0000 0.0000 0.0000 ( 0.00%)  
black\_box 0.0000 0.0000 0.0000 0.0000 ( 0.00%)  
clock\_network 4.3480e-03 0.0000 0.0000 4.3480e-03 ( 34.30%) 1  
register 2.7082e-04 2.5315e-03 7.0967e+03 2.8094e-03 ( 22.20%)  
sequential 0.0000 0.0000 0.0000 0.0000 ( 0.00%)  
combinational 5.7765e-04 4.9090e-03 1.1847e+04 5.4985e-03 ( 43.44%)  
-----  
Total 5.1972e-03 mW 7.4405e-03 mW 1.8943e+04 pW 1.2657e-02 mW  
1  
dc\_shell>

Design Vision - TopLevel1 (alu) (on synopsys.vit.ac.in)

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzerRTL Window Help

Hier1 X

Logical Hierarchy

Cells (Hierarchical)

Cell Name Ref N

ab

arith

lb

logic

sb

shifter

mc2

mux

mc1

reg\_b

rb

Cell

Cell touch

Cell touch

is\_hierarchical

is\_hierarchical

is\_mapped

is\_mapped

is\_sequential

is\_sequential

1/1 (F1=cycle;?query;Ctrl+F1=focus)

Operating Conditions: tt0p65v25c Library: saed14rvt\_base\_tt0p65v25c  
Wire Load Model Mode: top

Design Wire Load Model Library

Log History

dc\_shell>

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt:DoubleClick expands FanOut ALL levels

No Selection

## Power analysis report

```
Activities Terminal Feb 6 14:38
24mvd0166@synopsys:~/ALU_8

File Edit View Search Terminal Help

[ISCL] 02/06/2025 14:40:45 PID:448576 Client:synopsys.vit.ac.in checkin Power-Optimization
1
change_names -rule verilog -hier
1
write -hierarchy -format verilog -output ./mylogic_netlist.no.v
writing verilog file '/home/userdata/24mvd0166/ALU_8/mylogic_netlist.no.v'.
1
write_sdc ./aluno.sdc
1
dc_shell> start gui
[ISCL] 02/06/2025 14:41:11 PID:448576 Client:synopsys.vit.ac.in Server:27020@14.139.1.126 Authorization succeeded Design-Vision 2023.09
Checkout succeeded: Design-Vision/DF58F18DE113F909A898
License File: 27020@14.139.1.126
License Server: 27020@14.139.1.126
[ISCL] 02/06/2025 14:41:11 Checking status for feature Design-Vision
[ISCL] 02/06/2025 14:41:11 PID:448576 Client:synopsys.vit.ac.in Server:27020@14.139.1.126 Checkout succeeded Design-Vision 2023.09
dc_shell> current design is 'alu'.
dc_shell> current design is 'alu'.
dc_shell> report area

*****
Report : area
Design : alu
Version: V-2023.12-SP4
Date : Thu Feb 6 14:42:20 2025
*****
Library(s) Used:

saed14rvt_base_tt0p65v25c (File: /home/synopsys/installs/LIBRARIES/SAED14nm_EDK_08_2024/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_tt0p65v25c.db)

Number of ports: 36
Number of nets: 239
Number of cells: 210
Number of combinational cells: 176
Number of sequential cells: 34
Number of macros/black boxes: 0
Number of buf/inv: 37
Number of references: 37

Combinational area: 52.569599
Buf/Inv area: 6.882000
Noncombinational area: 36.230401
Macro/Black Box area: 0.000000
Net Interconnect area: 123.771134

Total cell area: 88.800001
Total area: 212.571134
1
dc_shell>
```

```
Activities Terminal Feb 6 14:39
24mvd0166@synopsys:~/ALU_8

File Edit View Search Terminal Help

-----
data required time 11.83
data arrival time -4.74
-----
slack (NET) 7.09

-----
Startpoint: s[0] (input port clocked by clock)
Endpoint: rb_out_reg_2
(rising edge-triggered flip-flop clocked by clock)
Path Group: INPUTS
Path Type: max

Des/Clust/Port Wire Load Model Library
-----
alu 8000 saed14rvt_base_tt0p65v25c

Point Incr Path
-----
clock clock (rise edge) 0.00 0.00
clock network delay (ideal) 2.00 2.00
input external delay 1.00 3.00 r
s[0] (in) 0.00 3.00 r
U224/X (SAEDRVT14_INV_0P5) 0.14 3.14 f
U225/X (SAEDRVT14_NR2_1) 0.20 3.34 r
U228/X (SAEDRVT14_ND2_CDC_1) 0.38 3.72 f
U171/X (SAEDRVT14_NR2_1P5) 0.52 4.24 r
U231/X (SAEDRVT14_INV_0P5) 0.36 4.60 f
U314/X (SAEDRVT14_OAT22_0P5) 0.16 4.76 r
U315/X (SAEDRVT14_A0221_0P5) 0.11 4.87 r
U316/X (SAEDRVT14_A0121_0P5) 0.06 4.93 f
U317/X (SAEDRVT14_OAT21_0P5) 0.10 5.03 r
rb_out_reg_2_0 (SAEDRVT14_FDPBQ_V2_0P5) 0.00 5.03 r
data arrival time 5.03

clock clock (rise edge) 10.00 10.00
clock network delay (ideal) 2.00 12.00
clock uncertainty -0.15 11.85
rb_out_reg_2_0/CK (SAEDRVT14_FDPBQ_V2_0P5) 0.00 11.85 r
library setup time -0.03 11.82
data required time 11.82
data arrival time 11.82
-----
slack (NET) 6.79

-----
Startpoint: s_r_reg_3 (rising edge-triggered flip-flop clocked by clock)
Endpoint: z (output port clocked by clock)
Path Group: OUTPUTS
Path Type: max

Des/Clust/Port Wire Load Model Library
-----
```

```
Activities Terminal Feb 6 14:39 24mvd0166@synopsys:~/ALU_8
File Edit View Search Terminal Help
fb_out reg 2 /CK (SAEDRV14_FDPBQ_V2_0P5) 0.00 11.85 r
library setup time -0.03 11.82
data required time 11.82
-----
data required time 11.82
data arrival time -5.03
-----
slack (MET) 6.79

Startpoint: s_r_reg_3 (rising edge-triggered flip-flop clocked by clock)
Endpoint: z (output port clocked by clock)
Path Group: OUTPUTS
Path Type: max

Des/Clust/Port Wire Load Model Library
-----
alu 8000 saed14rvt_base_tt0p65v25c

Point Incr Path
-----
clock clock (rise edge) 0.00 0.00
clock network delay (ideal) 2.00 2.00
s_r_reg_3 /CK (SAEDRV14_FDPBQ_V2LP_1) 0.00 2.00 r
s_r_reg_3 /Q (SAEDRV14_FDPBQ_V2LP_1) 0.15 2.15 r
U168/X (SAEDRV14_DEL_R2V1_1) 0.34 2.49 r
U177/X (SAEDRV14_INV_2) 0.48 2.96 f
U258/X (SAEDRV14_OA122_1) 0.27 3.24 r
U259/X (SAEDRV14_ND2_CDC_1) 0.20 3.44 f
U260/X (SAEDRV14_NP2_NM_1) 0.19 3.63 r
U261/X (SAEDRV14_ND2_CDC_1) 0.20 3.83 f
U262/X (SAEDRV14_NP2_NM_1) 0.14 3.97 r
U263/X (SAEDRV14_A0121_0P5) 0.15 4.12 f
lntadd0_0 U2/CO (SAEDRV14_ADDF_V1_1) 0.13 4.25 f
U318/S (SAEDRV14_ADDF_V1_1) 0.10 4.35 r
U305/X (SAEDRV14_INV_0P5) 0.08 4.43 f
U336/X (SAEDRV14_AN4_1) 0.07 4.50 f
z (out) 0.00 4.50 f
data arrival time 4.50

clock clock (rise edge) 10.00 10.00
clock network delay (ideal) 2.00 12.00
clock uncertainty -0.15 11.85
output external delay -1.00 10.85
data required time 10.85
-----
data required time 10.85
data arrival time -4.50
-----
slack (MET) 6.35

1
dc shell>
```

## Area & timing report