



VIT[®]

Vellore Institute of Technology
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Winter Semester 2024-2025
MVLD505L –ASIC Lab task- 3

Slot : L23+L24

Submitted to School of Electronics
Engineering

Submitted to
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Submitted by

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Lab Task 3: Performing Layout-Based STA Using PrimeTime (PT_Shell)

Objective

The goal of this lab task is to perform **Static Timing Analysis (STA)** after layout using **Synopsys PrimeTime (PT_Shell)**. This involves analyzing timing violations, checking setup/hold constraints, and ensuring that the design meets its timing requirements post-layout.

Invoking Pt_shell

```
Activities Terminal Mar 13 14:54
24mvd0166@synopsys:~/ALU_8
File Edit View Search Terminal Help
clock_r_REG08 S3/D -0.08 (VIOLATED)
clock_r_REG12 S3/D -0.08 (VIOLATED)
clock_r_REG15 S3/D -0.08 (VIOLATED)
clock_r_REG18 S3/D -0.08 (VIOLATED)
clock_r_REG21 S3/D -0.08 (VIOLATED)
clock_r_REG1 S2/D -0.05 (VIOLATED)
clock_r_REG7 S2/D -0.05 (VIOLATED)
clock_r_REG11 S2/D -0.05 (VIOLATED)
clock_r_REG14 S2/D -0.05 (VIOLATED)
clock_r_REG17 S2/D -0.05 (VIOLATED)
clock_r_REG20 S2/D -0.05 (VIOLATED)

min_capacitance
Pin Required Actual Slack
Capacitance Capacitance
-----
clock_r_REG10 S1/Q 0.00 0.00 0.00 (VIOLATED: increase significant digits)
clock_r_REG13 S1/Q 0.00 0.00 0.00 (VIOLATED: increase significant digits)
clock_r_REG16 S1/Q 0.00 0.00 0.00 (VIOLATED: increase significant digits)
clock_r_REG19 S1/Q 0.00 0.00 0.00 (VIOLATED: increase significant digits)

*****
Report : bottleneck
-cost type path_count
-max cells 20
-worst_paths 100
Design : alu
Version: V-2023.12-SP4
Date : Thu Mar 13 14:55:43 2025
*****
Bottleneck Cost = Number of violating paths through cell

Cell Reference Bottleneck
----- Cost -----
No changes to write
*****
Report : write_sdf ./prime.sdf
Design : alu
Version: V-2023.12-SP4
Date : Thu Mar 13 14:55:43 2025
*****
Information: SDC supports a subset of the constraints supported by PrimeTime. Some constraints cannot be preserved by the write_sdc command. (WSCR-002)
Information: Defining new variable 'TARGET_LIBRARY_FILES'. (CMD-041)
pt_shell>
```

```
Mar 13 14:57
24mvd0166@synopsys-~/ALU_8

File Edit View Search Terminal Help

Information: Starting updating timing at [ Thu Mar 13 14:58:03 2025 ]...
Information: Finished updating timing at [ Thu Mar 13 14:58:03 2025 ]...
Information: Analyzing timing improvement...
Information: Tuning changes...
Information: Starting updating timing at [ Thu Mar 13 14:58:03 2025 ]...
Information: Finished updating timing at [ Thu Mar 13 14:58:03 2025 ]...
Information: 16 buffers have been inserted.

Information: Starting timing fix iteration 3 at [ Thu Mar 13 14:58:03 2025 ]...
Information: 16 violating endpoints located... (PTECO-022)
Information: 16 endpoints are being considered for fixing... (PTECO-027)
Information: Fixing violations...
Information: Starting updating timing at [ Thu Mar 13 14:58:03 2025 ]...
Information: Finished updating timing at [ Thu Mar 13 14:58:03 2025 ]...
Information: Analyzing timing improvement...
Information: Tuning changes...
Information: Starting updating timing at [ Thu Mar 13 14:58:03 2025 ]...
Information: Finished updating timing at [ Thu Mar 13 14:58:03 2025 ]...
Information: 26 buffers have been inserted.

Information: Starting timing fix iteration 4 at [ Thu Mar 13 14:58:03 2025 ]...
Information: Quality of results may not improve in following iterations...
Information: No more fixes are available.
Information: The timing violation fixing process is complete.

Inserted buffers:
Count Lib cell Area Total_area
-----
57 SAEDRV14 BUF_20 1.29 73.39
57 TOTAL 73.39

Final ECO Summary:
Number of insert buffer commands 57
Total number of commands 57
Area increased by buffer insertion 73.39
Total area increased 73.39

Fixing Summary:
Total violating endpoints found 16
Total violating endpoints fixed 0
Total violating endpoints remaining 16
Total percentage of violations fixed 0.0%

Information: Elapsed time [ 1 seconds ]
Information: Completed at [ Thu Mar 13 14:58:03 2025 ]

1
pt_shell> pt_shell>
```

Design Import: Import the design's netlist and Standard Delay Format (SDF) file into PrimeTime.

PT.tcl

```
Mar 13 15:01
24mvd0166@synopsys-~/ALU_8

File Edit View Search Terminal Help

Design : alu
Version: V-2023.12-SP4
Date : Thu Mar 13 15:00:08 2025

Startpoint: s[0] (Input port clocked)
Endpoint: clock_r_REG3_S2
(rising edge-triggered)
Path Group: INPUTS
Path Type: max

Point
-----
clock clock (rise edge)
clock network delay (ideal)
input external delay
s[0] (in)
U171/X (SAEDRV14 INV_S_0P75)
U187/X (SAEDRV14 ND2_1)
U188/X (SAEDRV14 ND2 CDC 1)
U189/X (SAEDRV14 INV_0P5)
U170/X (SAEDRV14 ND2_0P5)
U233/X (SAEDRV14 OA31_1)
U PTECO_HOLD BUF39/X (SAEDRV14 BUF_20)
U PTECO_HOLD BUF70/X (SAEDRV14 BUF_20)
U PTECO_HOLD BUF16/X (SAEDRV14 BUF_20)
U241/X (SAEDRV14 OA121_0P5)
U PTECO_HOLD BUF61/X (SAEDRV14 BUF_20)
U PTECO_HOLD BUF32/X (SAEDRV14 BUF_20)
U PTECO_HOLD BUF1/X (SAEDRV14 BUF_20)
U PTECO_HOLD BUF49/X (SAEDRV14 BUF_20)
clock_r_REG3_S2/D (SAEDRV14 FDPBQ_0P5)
data arrival time

clock clock (rise edge) 2.00 12.00
clock network delay (ideal) 0.00 12.00
clock reconvergence pessimism 0.00 12.00
clock uncertainty -0.15 11.85
clock_r_REG3_S2/CK (SAEDRV14 FDPBQ_V2LP_0P5) 0.02 11.85 r
library setup time 11.87
data required time 11.87
data required time 11.87
data arrival time -3.91
slack (MET) 7.96

1
pt_shell>
```

```
pt.tcl
-ALU_8

#set svf "alu.svf"
set search_path "/home/synopsys/installs/LIBRARIES/SAED14nm_EDK_08_2024/SAED14nm_EDK_STD_RVT/liberty/nldm/base ./ ";
set TARGET_LIBRARY_FILES saedi4rvt_base.ttp69v25c.db;
set TARGET_LIBRARY_FILES saedi4rvt_base_ff6p80v25c.db;
set_app_var search_path "search_path"
set_app_var target_library $TARGET_LIBRARY_FILES
set_app_var link_library "target_library"

read_verilog physical_netlist.v
current_design alu
link
source ./alu.sdc
check_timing
read_parasitics_parasitics.reduced
read_sdf alu.sdf
report_timing -delay_type min
report_analysis_coverage
report_constraint
report_constraint -all_violators
report_bottleneck
#report_path

write_changes -output prime_changes.tcl
write_verilog -output prime_netlist.v
write_sdf ./prime.sdf

Tcl Tab Width: 8 Ln 1, Col 1 INS
```


Reporting: Generate detailed timing reports, highlighting critical paths and violations.

Report_analysis_coverage

```

1
pt_shell> pt_shell> report_analysis_coverage
*****
Report : analysis_coverage
Design : alu
Version : V-2023.12-SP4
Date   : Thu Mar 13 14:58:22 2025
*****

Type of Check      Total      Met      Violated      Untested
-----
setup              34      34 (100%)    0 ( 0%)    0 ( 0%)
hold               34      18 ( 53%)   16 ( 47%)    0 ( 0%)
recovery           34      34 (100%)    0 ( 0%)    0 ( 0%)
removal            34      34 (100%)    0 ( 0%)    0 ( 0%)
min_pulse_width    272     136 ( 50%)    0 ( 0%)   136 ( 50%)
out_setup          14       8 ( 57%)    0 ( 0%)    6 ( 43%)
out_hold           14       8 ( 57%)    0 ( 0%)    6 ( 43%)
-----
All Checks         436     272 ( 62%)   16 (  4%)   148 ( 34%)
-----

1
pt_shell>
```

```

1
pt_shell> pt_shell> start_gui
pt_shell>

```

PrimeTime - MainWindow.3 (on synopsys.vit.ac.in)

PrimeTime - MainWindow.3 - alu (on synopsys.vit.ac.in)

Information: Finished updating ti
Information: Analyzing timing imp
Information: Tuning changes...
Information: Starting updating ti
Information: Finished updating ti
Information: 9 buffers have been
Information: Starting timing fix
Information: 2 violating endpoints
Information: 2 endpoints are bein
Information: Fixing violations...
Information: Starting updating ti
Information: Finished updating ti
Information: Analyzing timing imp
Information: Tuning changes...
Information: Starting updating ti
Information: Finished updating ti
Information: 2 buffers have been
Information: Starting timing fix
Information: No timing violations
Information: No more fixes are av
Information: The timing violation

Inserted buffers:

Count	Lib cell	Area	Total area
45	SAEDRV14_BUF_20	1.29	73.39
45	TOTAL		73.39

Final ECO Summary:

Number of insert buffer commands: 57
Total number of commands: 57
Area increased by buffer insertion: 16
Total area increased: 73.39

Fixing Summary:

Total violating endpoints found	Total violating endpoints fixed	Total violating endpoints remaining	Total percentage of violations fixed
16	0	16	0.0%

Information: Elapsed time [0 seconds]
Information: Completed at [Thu Mar 13 14:59:38 2025]

14 endpoint groups

Scenario	Mode	Corner	Path Group	Analysis	Endpoints	NVE	WNS	TNS
default	default	default	**async_default**	setup	***	0	0.000	0.000
default	default	default	**async_default**	hold	***	0	0.000	0.000
default	default	default	**clock_gating_default**	setup	***	0	0.000	0.000
default	default	default	**clock_gating_default**	hold	***	0	0.000	0.000
default	default	default	**default**	setup	***	0	0.000	0.000
default	default	default	**default**	hold	***	0	0.000	0.000
default	default	default	CLOCK	setup	***	0	0.000	0.000
default	default	default	CLOCK	hold	***	0	0.000	0.000
default	default	default	INPUTS	setup	***	0	0.000	0.000
default	default	default	INPUTS	hold	***	0	0.000	0.000
default	default	default	OUTPUTS	setup	***	0	0.000	0.000
default	default	default	OUTPUTS	hold	***	0	0.000	0.000
default	default	default	clock	setup	***	0	0.000	0.000
default	default	default	clock	hold	***	0	0.000	0.000

14 endpoint groups

Console x Script Editor x

Ready

No Selection

Power User Unit: 1uW

```
Activities Terminal Mar 13 14:59
24mvd0166@synopsys:~/ALU.8
File Edit View Search Terminal Help
Design : alu
Version: V-2023.12-SP4
Date : Thu Mar 13 15:00:08 2025
*****

Startpoint: s[0] (input port clocked by clock)
Endpoint: clock_r_REG3_S2
(rising edge-triggered flip-flop clocked by clock)
Path Group: INPUTS
Path Type: max

Point-----Incr-----Path-----
clock clock (rise edge) 0.00 0.00
clock network delay (ideal) 2.00 2.00
input external delay 1.00 3.00 f
s[0] (in) 0.00 3.00 f
U171/X (SAEDRVT14 INV_S_0P75) 0.19 H 3.19 r
U187/X (SAEDRVT14 NR2_1) 0.12 H 3.31 f
U188/X (SAEDRVT14 ND2_CDC_1) 0.20 H 3.51 r
U189/X (SAEDRVT14 INV_0P5) 0.10 H 3.61 f
U170/X (SAEDRVT14 ND2_0P5) 0.13 H 3.75 r
U233/X (SAEDRVT14_0A31_1) 0.06 H 3.80 r
U_PTECO_HOLD_BUF39/X (SAEDRVT14_BUF_20) 0.01 3.82 r
U_PTECO_HOLD_BUF79/X (SAEDRVT14_BUF_20) 0.01 H 3.83 r
U_PTECO_HOLD_BUF16/X (SAEDRVT14_BUF_20) 0.01 + 3.83 r
U241/X (SAEDRVT14_0A121_0P5) 0.03 H 3.87 f
U_PTECO_HOLD_BUF61/X (SAEDRVT14_BUF_20) 0.02 H 3.88 f
U_PTECO_HOLD_BUF32/X (SAEDRVT14_BUF_20) 0.01 + 3.89 f
U_PTECO_HOLD_BUF1/X (SAEDRVT14_BUF_20) 0.01 H 3.90 f
U_PTECO_HOLD_BUF49/X (SAEDRVT14_BUF_20) 0.01 H 3.91 f
clock_r_REG3_S2/D (SAEDRVT14_FDPRBQ_V2LP_0P5) 0.00 + 3.91 f
data arrival time 3.91

clock clock (rise edge) 10.00 10.00
clock network delay (ideal) 2.00 12.00
clock reconvergence pessimism 0.00 12.00
clock uncertainty -0.15 11.85
clock_r_REG3_S2/CK (SAEDRVT14_FDPRBQ_V2LP_0P5) 0.02 11.87
library setup time 11.87
data required time 11.87
-----
data required time 11.87
data arrival time -3.91
-----
slack (MET) 7.96

pt_shell>
```

Conclusion

The STA analysis using PT_Shell provides a **detailed insight into the timing health of the design** post-layout. The results guide further optimizations and help ensure that the design is **functionally correct and meets timing constraints**