VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Winter Semester 2024-2025

MVLD505L –ASIC Lab task- 3

Slot : L23+L24

Submitted to School of Electronics Engineering

Submitted to

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Submitted by

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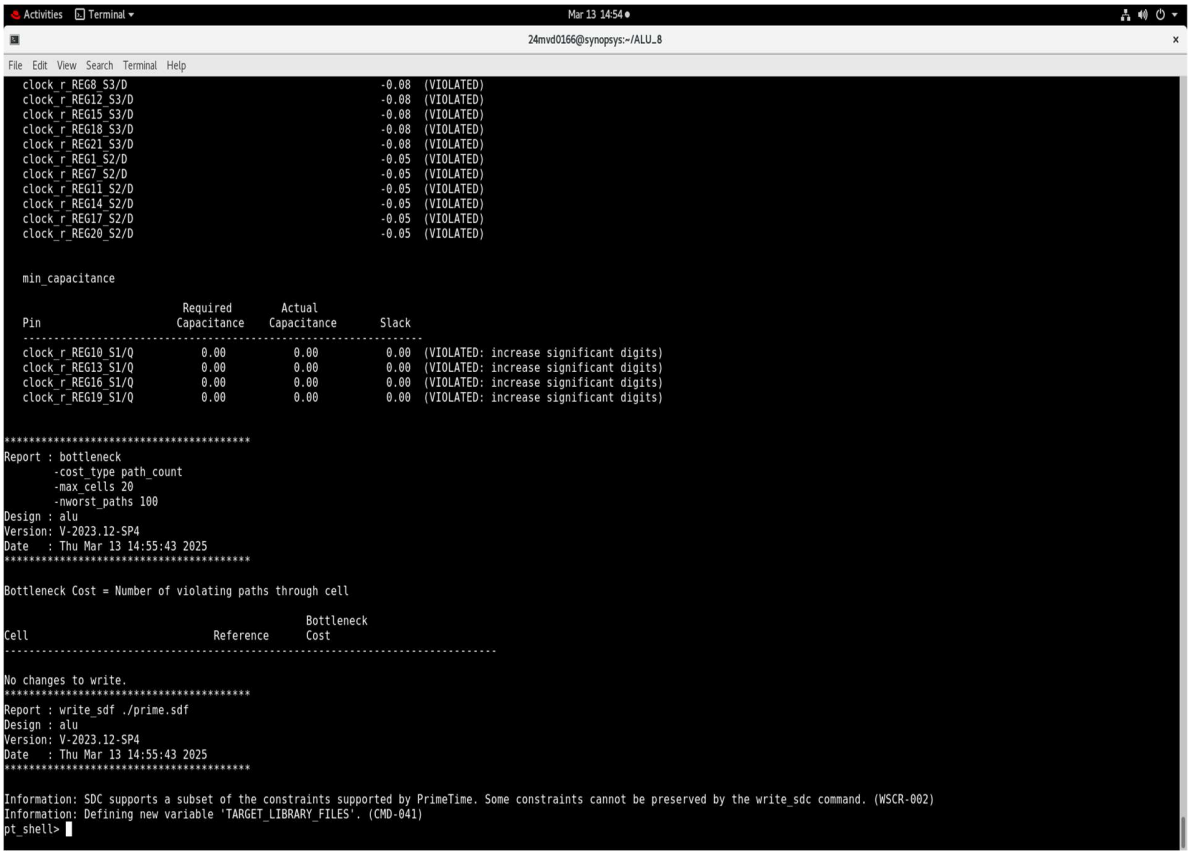
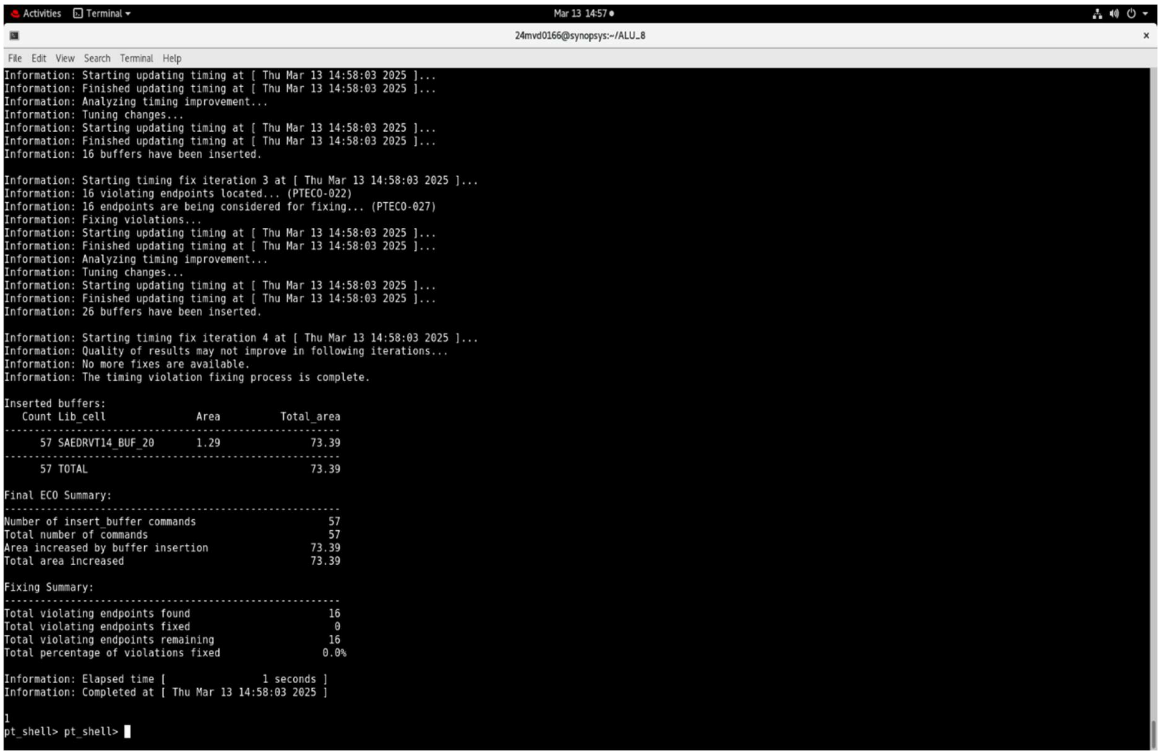
Lab Task 3: Performing Layout-Based STA Using PrimeTime (PT_Shell)

Objective

The goal of this lab task is to perform **Static Timing Analysis (STA)** after layout using **Synopsys PrimeTime (PT_Shell)**. This involves analyzing timing violations, checking setup/hold constraints, and ensuring that the design meets its timing requirements post-layout.

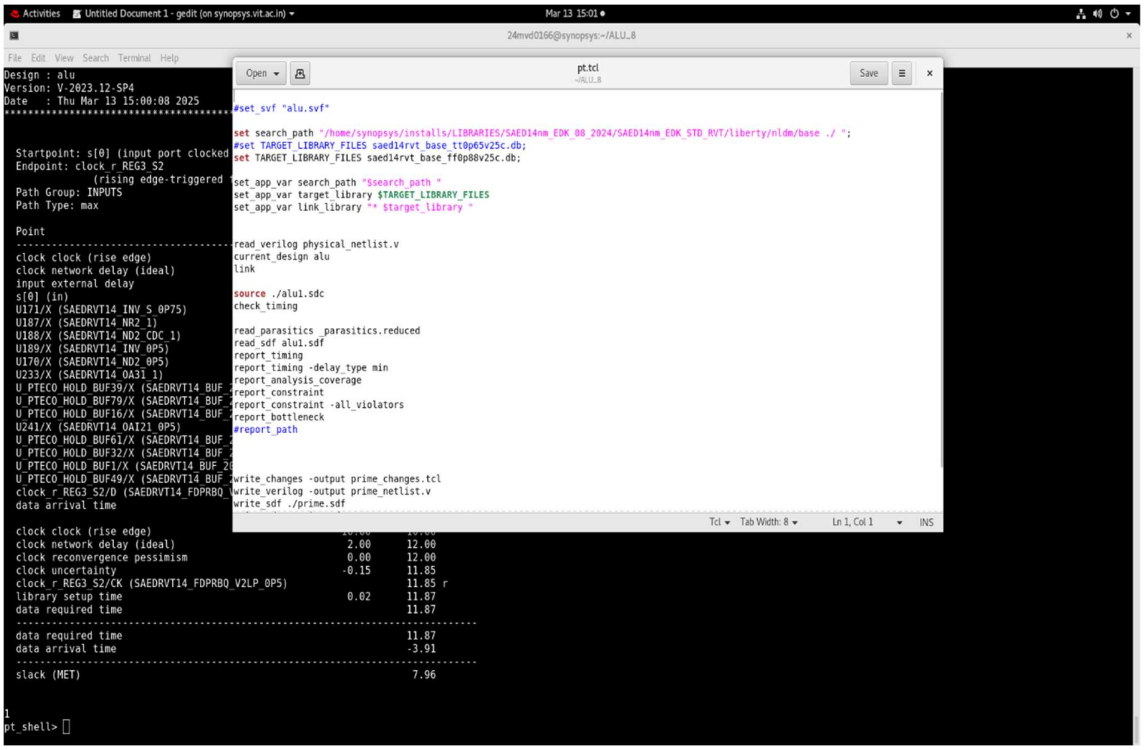
Invoking Pt_shell

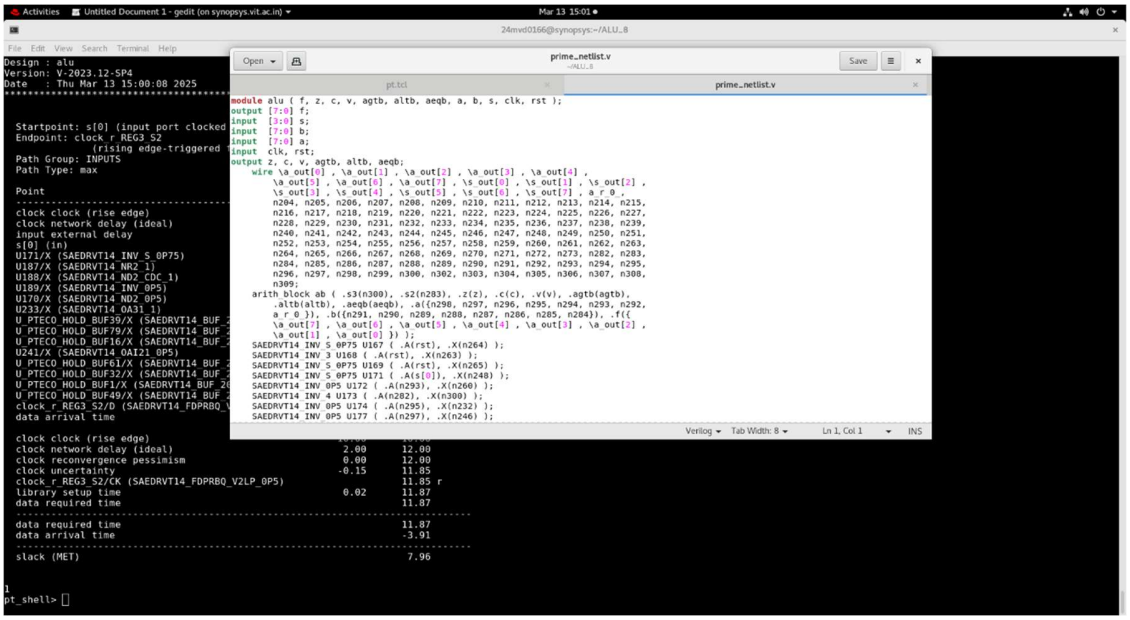




Design Import: Import the design's netlist and Standard Delay Format (SDF) file into PrimeTime.

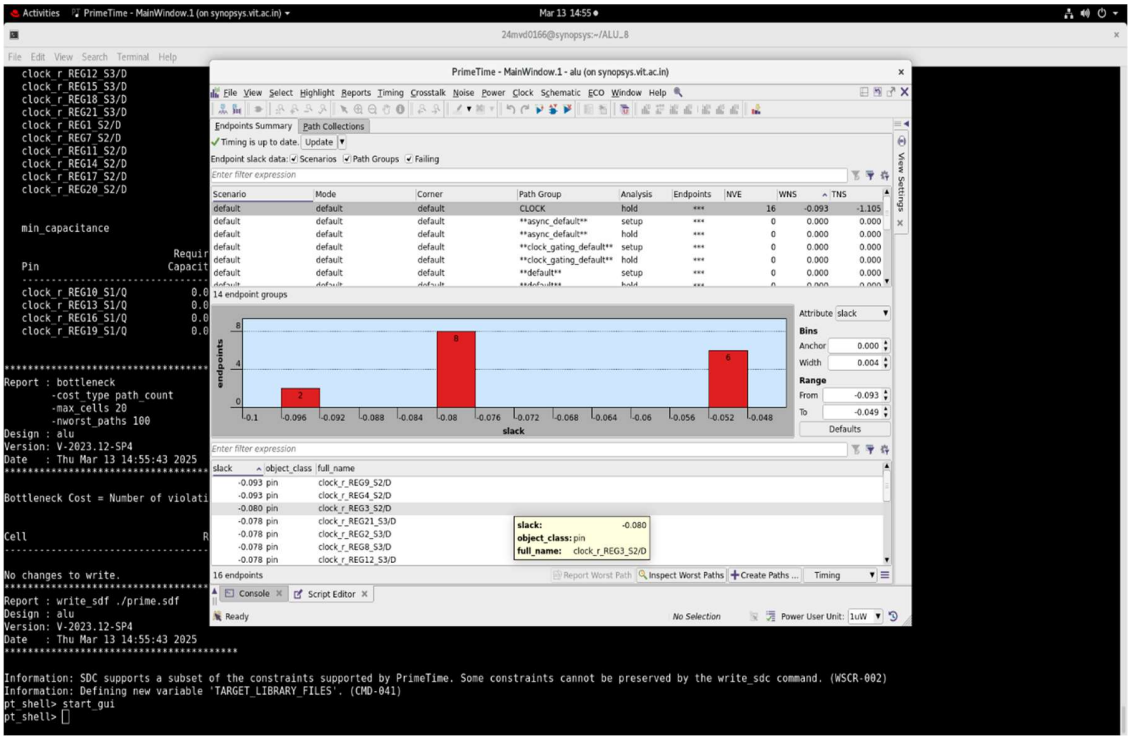
PT.tcl





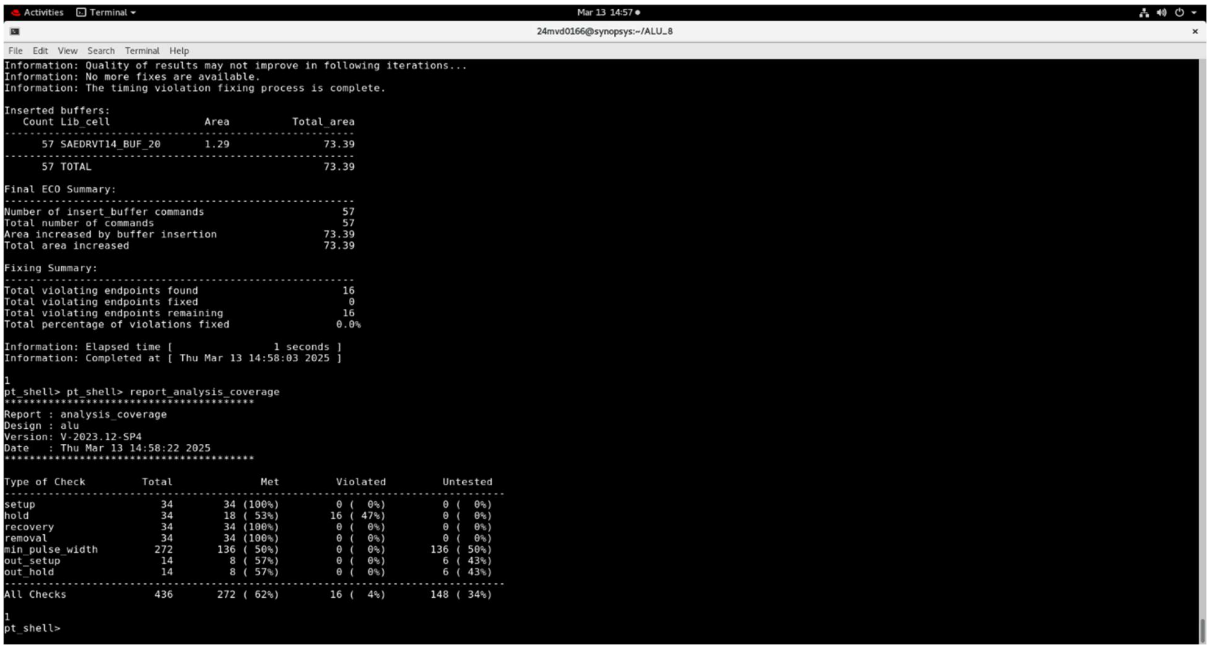
Prime_netlist.v

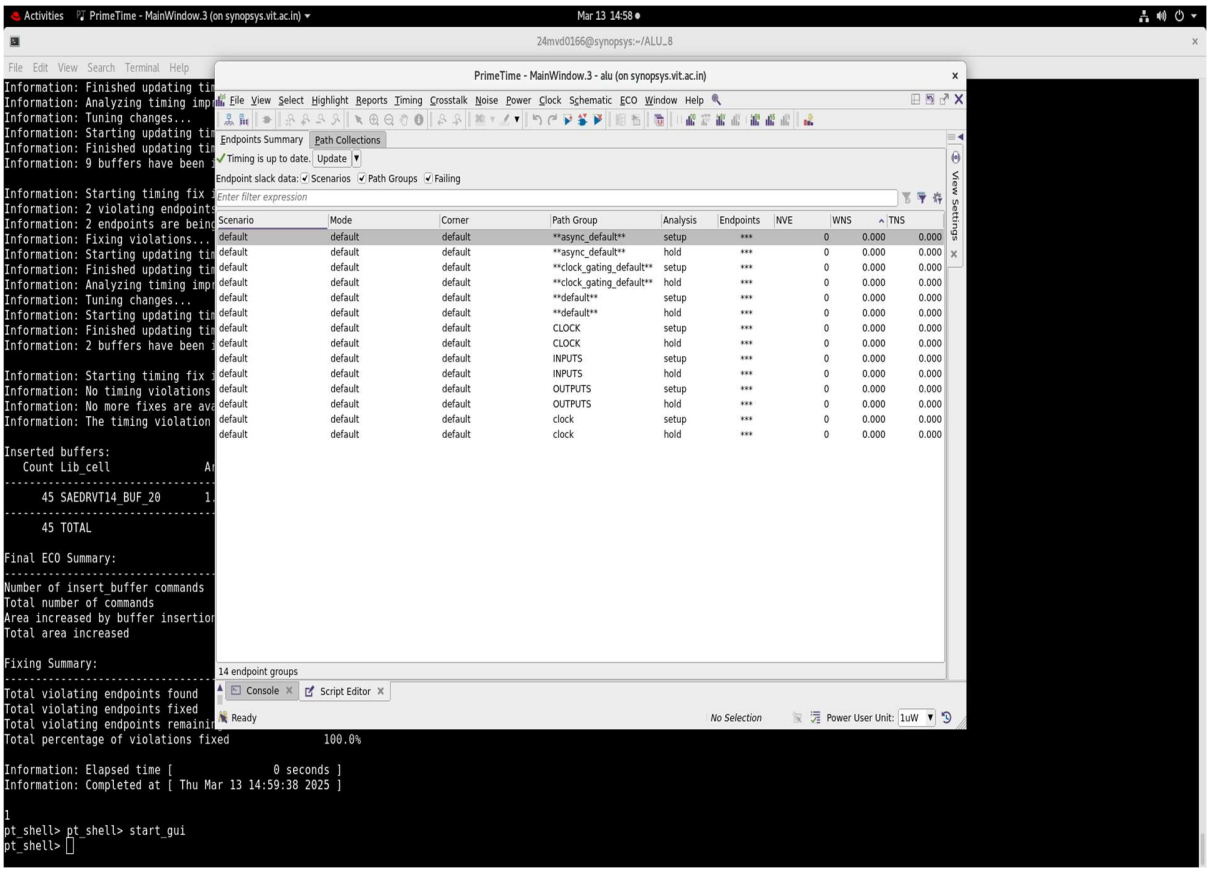
PrimeTime MainWindow:

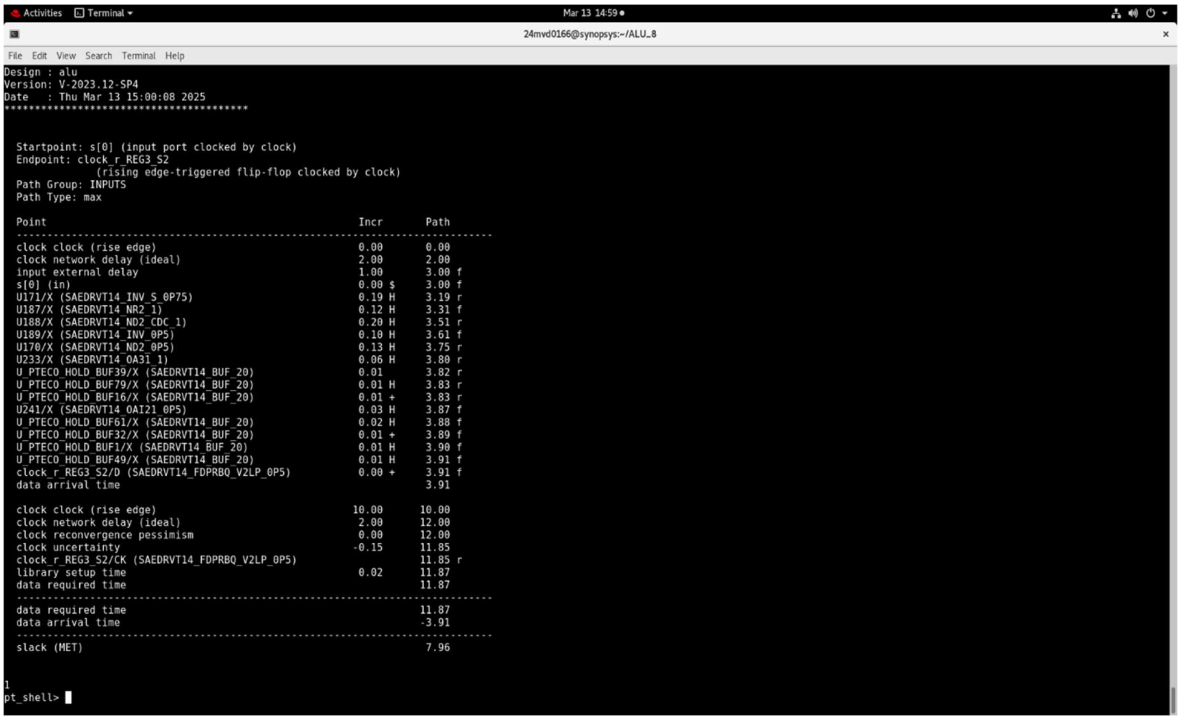


Reporting: Generate detailed timing reports, highlighting critical paths and violations.

Report_analysis_coverage







Conclusion

The STA analysis using PT_Shell provides **a detailed insight into the timing health of the design** post-layout. The results guide further optimizations and help ensure that the design is **functionally correct and meets timing constraints**