

I2C ASIC Project – RTL to GDSII Flow

This project implements an 8-bit Arithmetic Logic Unit (ALU) using the **ASIC RTL to GDSII flow**, covering all stages: RTL design, simulation, synthesis, formal verification, STA, physical design, and GDSII generation.

Tools Used

Step	Tool
RTL Design	Verilog (custom code)
Simulation	Synopsys VCS
Synthesis	Synopsys Design Compiler
Formal Verification	Synopsys Formality
STA	Synopsys PrimeTime
Physical Design	Synopsys IC Compiler II
Physical Verification	Synopsys IC Validator
GDSII Export	IC Compiler II or Calibre

Project Directory Structure

8bit-ALU-ASIC-RTL-to-GDSII/

```
|-- rtl/      # Verilog source files
|-- sim/      # Simulation files (VCS)
|-- syn/      # Synthesis with DC Shell
|-- formal/   # Formal verification (Formality)
|-- pt/        # STA with PrimeTime
|-- pd/        # Physical design with ICC2
|-- gds/       # GDSII and final signoff
-- README.md   # Project summary
```

I2C ASIC Project – RTL to GDSII Flow

RTL to GDSII Flow

1. RTL Design

- Write Verilog modules for the 8-bit ALU.
 - Operations include: ADD, SUB, AND, OR, XOR, etc.
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2. Functional Simulation (VCS)

- Testbench: alu_top_tb.v
- Script: `vcs -full64 -debug_all ..//rtl/*.* v alu_top_tb.v -o simv
./simv +vcs+vcdpluson`

3. Synthesis (DC Shell)

- Use dc_script.tcl and alu_top.sdc

```
dc_shell -f dc_script.tcl
```

Outputs:

- alu_top_synth.v
 - alu_top.sdf
 - alu_top_area.rep, alu_top_timing.rep, alu_top_power.rep
 - - alu_top_area.rep, alu_top_timing.rep, alu_top_power.rep
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4. Formal Verification (Formality)

- Compare RTL and Netlist:

```
verify
```

```
report_verification -verbose
```

5. Static Timing Analysis (PrimeTime)

```
read_verilog alu_top_synth.v
```

```
read_sdf alu_top.sdf
```

```
read_sdc alu_top.sdc
```

I2C ASIC Project – RTL to GDSII Flow

6. Physical Design (IC Compiler II)

```
read_verilog alu_top_synth.v  
read_def floorplan.def  
place_opt  
clock_opt  
route_opt  
write_gds alu_top.gdsOutputs: alu_top.gds, layout reports
```

7. Physical Verification (ICV / Calibre)

```
icv -drc alu_top.drc.runset  
icv -lvs alu_top.lvs.runset
```

Final Deliverables

File	Description
alu_top_synth.v	Synthesized gate-level netlist
alu_top.sdf	Timing delays for STA and simulation
alu_top_area.rep	Area utilization report
alu_top_power.rep	Power report (dyn + leakage)
alu_top.gds	Final layout GDSII
dump.vcd	Simulation waveform
simulation.log	Functional simulation log

References

- Synopsys Tool Suite Documentation
- "CMOS VLSI Design" – Weste & Harris
- "Algorithms for VLSI Design Automation" – Naveed Sherwani