

Архитектура процессора TMS320F28335

Кафедра **ЭО**Петрухин О.М.

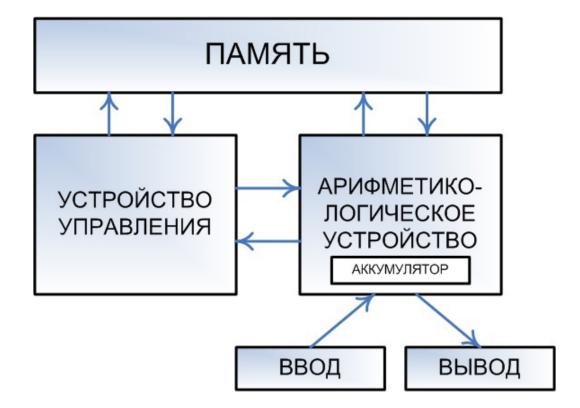


CPU vs DSP





Архитектура фон-Неймана

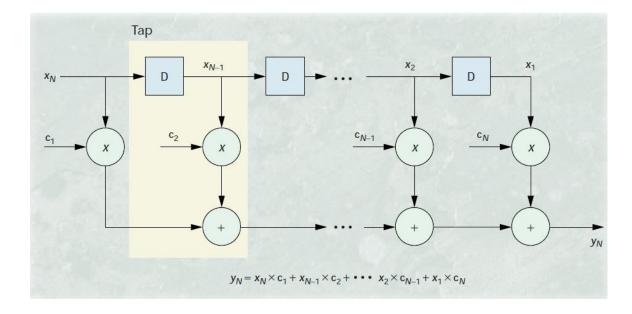


Гарвардская архитектура





MAC onepaquu



16x16 Multiply Operations						
DMAC	ACC:P,loc32,*XAR7/++	16-bit dual multiply and accumulate				
MAC	P,loc16,0:pma	Multiply and accumulate				
MAC	P,loc16,*XAR7/++	Multiply and Accumulate				
MPY	P,T,loc16	16 X 16 multiply				
MPY	P,loc16,#16bit	16 X 16-bit multiply				
MPY	ACC,T,loc16	16 X 16-bit multiply				
MPY	ACC,loc16,#16bit	16 X 16-bit multiply				
MPYA	P,loc16,#16bit	16 X 16-bit multiply and add previous product				
MPYA	P,T,loc16	16 X 16-bit multiply and add previous product				
MPYB	P,T,#8bit	Multiply signed value by unsigned 8-bit constant				
MPYS	P,T,loc16	16 X 16-bit multiply and subtract				
MPYB	ACC,T,#8bit	Multiply by 8-bit constant				
MPYU	ACC,T,loc16	16 X 16-bit unsigned multiply				
MPYU	P,T,loc16	Unsigned 16 X 16 multiply				
MPYXU	P,T,loc16	Multiply signed value by unsigned value				
MPYXU	ACC,T,loc16	Multiply signed value by unsigned value				
SQRA	loc16	Square value and add P to accumulator				
SQRS	loc16	Square value and subtract from accumulator				
XMAC	P,loc16,*(pma)	C2xLP source-compatible multiply and accumulate				
XMACD	P,loc16,*(pma)	C2xLP source-compatible multiply and accumulate with data move				
32x32 Multipl	y Operations					
IMACL	P,loc32,*XAR7/++	Signed 32 X 32-bit multiply and accumulate (lower half)				
IMPYAL	P,XT,loc32	Signed 32-bit multiply (lower half) and add previous P				
IMPYL	P,XT,loc32	Signed 32 X 32-bit multiply (lower half)				
IMPYL	ACC,XT,loc32	Signed 32 X 32-bit multiply (lower half)				
IMPYSL	P,XT,loc32	Signed 32-bit multiply (lower half) and subtract P				
IMPYXUL	P,XT,loc32	Signed 32 X unsigned 32-bit multiply (lower half)				
QMACL	P,loc32,*XAR7/++	Signed 32 X 32-bit multiply and accumulate (upper half)				
QMPYAL	P,XT,loc32	Signed 32-bit multiply (upper half) and add previous P				
QMPYL	ACC,XT,loc32	Signed 32 X 32-bit multiply (upper half)				

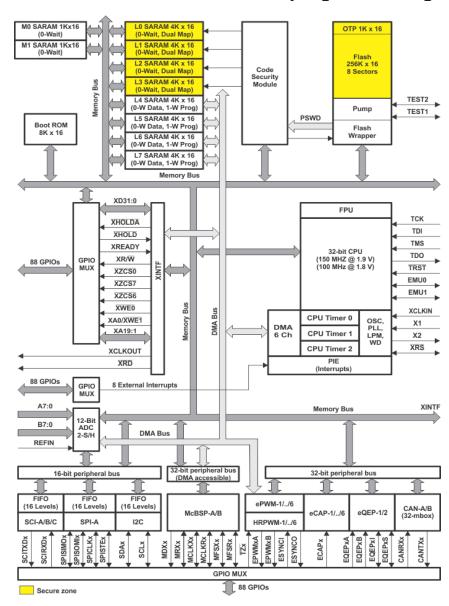


	CPU (Intel)	DSP (TI)	
Частота	2.5 ГГц	500 МГц	
Число ядер	28	1	
Пиковая производительность	560 GIPS	1.8 GIPS	
Энергопотребление	205 Вт	1 Вт	
Out-of-order	Да	Нет	
Цена	\$13K (+ система охлаждения)	\$35 (оптовая цена)	
Target applications	Любые	- Большое число циклов- Высокий параллелизм по данным- Регулярный паттерн доступа в память	
Производительность / Вт / ядро	0.097 GIPS/Вт/ядро	1.7 GIPS/Вт/ядро (в 17 раз лучше Intel)	
Производительность / Вт / ядро / \$	0.0075 MIPS/Вт/ядро/\$	0.051 GIPS/Вт/ядро/\$ (в 7000 раз лучше Intel)	

(Источник: https://habr.com/ru/company/samsung/blog/564282/)



Внутренняя архитектура DSP TMS320F28335



Периферийные устройства управления:

- ePWM
- eCAP
- eQEP
- ADC

Периферийные устройства связи:

- SPI
- SC
- I2C
- CAN
- XINTF

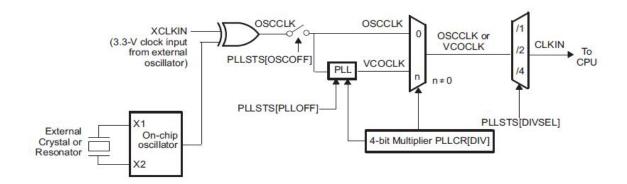
Table 3-6. Boot Mode Selection

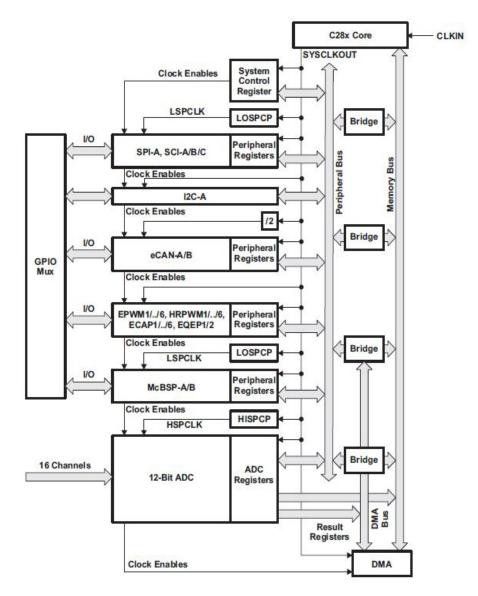
MODE	GPIO87/XA15	GPIO86/XA14	GPIO85/XA13	GPIO84/XA12	MODE ⁽¹⁾
F	1	1	1	1	Jump to Flash
E	1	1	1	0	SCI-A boot
D	1	1	0	1	SPI-A boot
С	1	1	0	0	I2C-A boot
В	1	0	1	1	eCAN-A boot
Α	1	0	1	0	McBSP-A boot
9	1	0	0	1	Jump to XINTF x16
8	1	0	0	0	Jump to XINTF x32
7	0	1	1	1	Jump to OTP
6	0	1	1	0	Parallel GPIO I/O boot
5	0	1	0	1	Parallel XINTF boot
4	0	1	0	0	Jump to SARAM
3	0	0	1	1	Branch to check boot mode
2	0	0	1	0	Branch to Flash, skip ADC calibration
1	0	0	0	1	Branch to SARAM, skip ADC calibration
0	0	0	0	0	Branch to SCI, skip ADC calibration

⁽¹⁾ All four GPIO pins have an internal pullup



Тактирование DSP TMS320F28335







Спасибо за внимание!