

**Design and Construction of an  
Advanced STATCOM for Reactive Power  
Control and Harmonic Cancellation**

by

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**2012**

*A thesis submitted in partial fulfilment of the requirements for  
the degree of Bachelor of Engineering in Electrical Engineering  
at The University of Newcastle, Australia.*





## **Abstract**

This project involved the development of a power electronics-based device for the purpose of power conditioning on the electrical grid. The device, called an ‘Advanced STATCOM’, combines the benefits of a static compensator (STATCOM) and an active harmonic filter (AHF). It is capable of simultaneously providing harmonic cancellation and reactive power control for power factor correction. The physical basis for the device is the voltage source converter (VSC), so an initial study was used to provide fundamental knowledge of switching hardware design. This study illustrated the advantages and limitations of various switching topologies and methods. ‘Instantaneous power theory’ and its application to power system analysis were then reviewed, as these concepts forms the basis of control techniques employed in state of the art FACTS devices. The Advanced STATCOM’s sophisticated control scheme involves two control loops, which generate and synthesise the currents required to improve power quality. The outer loop controller uses a novel adaptation of p-q Theory to achieve its control objectives of reactive power control and harmonic filtering. The inner current control loop was designed with deadbeat predictive algorithms operating a symmetrical space vector pulse width modulation scheme. The outer and inner loop controllers work together to provide very high performance in both steady and transient states. The Saber simulation platform was used to validate design considerations and prove the STATCOM’s functionality by assessing it in a simulated power system. The same system was physically constructed to replicate a configurable “distribution system” hardware test bed. To assist in control and monitoring of this test bed, a computer application was also developed which interfaces with the Texas Instruments DSP-based controller. Using this complete power system test bed, experimental results were obtained to provide a practical demonstration of the device’s functionality. Significant improvements in both power factor and total harmonic distortion were obtained, with a high correlation between measured and simulated results. Tests conducted demonstrated that the power factor was increased to unity in all scenarios assessed. Additionally, the STATCOM’s active harmonic filtering reduced current distortions by 70%. These results clearly illustrate the substantial power quality improvements provided by the developed STATCOM as indicated by theoretical studies.



# Acknowledgements

This project has been made possible by a number of people and it is my pleasure to convey my appreciation to them in this humble acknowledgement.

Foremost, I would like to express my sincere gratitude to my academic supervisor, Terry Summers. Without Terry's invaluable expertise, encouragement and patience, this project would not have been possible. His guidance throughout the year has allowed me to spend my time efficiently and produce the best work I am capable of. I could not have imagined a better supervisor and mentor for this project.

In addition to my supervisor, I would like to thank the other academics and lab staff who have provided much assistance and encouragement since the start of my degree. This project is formed on the base of knowledge learned over a number of years, which could not have been achieved without the quality of teaching and support provided by staff at the University of Newcastle.

My thanks also goes to Ausgrid for the cadetship which has provided me invaluable experience throughout my degree. The experience gained through my various work placements has given me an insight into the operation and maintenance of transmission and distribution networks, which provided part of the inspiration to undertake this project.

I would also like to thank my fellow students for the stimulating discussions, brainstorming sessions, encouragement and company during the numerous sleepless nights working towards deadlines over the course of this degree.

Last but certainly not least, I would like to thank my family and friends for their love and support throughout my life, and in particular, this very challenging year.



# Contributions

My key contributions to this project are listed below:

- Performed a review of power converter topologies, current control techniques and instantaneous power theory,
- Designed a novel Advanced STATCOM controller based on instantaneous power theory,
- Designed a three-phase deadbeat predictive current controller with space vector pulse-centred PWM voltage synthesis,
- Designed a novel single-phase phase-locked loop that improves on the performance of the Karimi-Ghatermani phase-locked loop,
- Simulated the Advanced STATCOM (with complete digital control using DLLs) in a test power system to demonstrate the substantial performance benefits,
- Designed and built an experimental power system test bed to provide practical demonstrations of the Advanced STATCOM's functionality,
- Designed and developed a computer application for interfacing with both the Advanced STATCOM and an oscilloscope.

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Mr. Kumaran Nathan

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Dr. Terrence Summers

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# Nomenclature

a, b, c	Phase identifiers
AC	Alternating Current
ADC	Analog-to-Digital converter
AHF	Active Harmonic Filter
CAN	Controller Area Network
CSC	Current Source Converter
DAC	Digital-to-Analog converter
DC	Direct Current
DFT	Discrete Fourier Transform
DLL	Dynamic Link Library
dq0	Direct, quadrature and zero axes
DSP	Digital Signal Processing
FACTS	Fleixble AC Transmission Systems
FFT	Fast Fourier Transform
$f_s$	Switching frequency
GUI	Graphical User Interface
IGBT	Insulated Gate Bipolar Transistor
$i_{load}$	Load currents

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IPFC	Interline Power Flow Controller
$i_{source}$	Source currents
$i_{STATCOM}$	STATCOM output currents
NER	National Electricity Rules
PLL	Phase-Locked Loop
PWM	Pulse-Width Modulation
RMS	Root Mean Square
SCPI	Standard Commands for Programmable Instruments
SNR	Signal-to-Noise Ratio
SSSC	Static Synchronous Series Compensator
STATCOM	Static Compensator
SVC	Static VAr Compensator
SVPWM	Space Vector Pulse-Width Modulation
$t_f$	Fall time
THD	Total Harmonic Distortion
$t_r$	Rise time
$T_s$	Switching period
VAr	Volt-Ampere reactive
VCP	Virtual COM Port
$V_{DC}$	STATCOM DC bus voltage
VISA	Virtual Instrument Systems Architecture
$V_{PCC}$	AC bus voltage at the point of common coupling
VSC	Voltage Source Converter
VSD	Variable Speed Drive
VSI	Voltage Source Inverter

# Chapter 1

## Introduction

*This chapter provides a contextual outline of the modern day issues facing power systems to establish the motivation for this project. It then outlines the aims of the project and briefly explains how the project helps to solve the aforementioned problems. The chapter concludes with an outline of the structure of this thesis.*

### 1.1 Project Motivation

There are a growing number of loads connected to the electrical grid that have very poor power quality characteristics[1]. Power quality can be measured and quantified by the *power factor*, which is the ratio of real power to apparent power flowing into a load[2]. Power factor is dependent on the displacement power factor and the distortion power factor:

- **Displacement power factor** represents a phase shift between the phase voltages and currents at the fundamental frequency (50Hz). A poor displacement power factor is caused by loads that are highly inductive or capacitive (however, highly capacitive loads are far less common). Common examples of highly inductive loads include large motors, solenoids and contactor coils.
- **Distortion power factor** is related to the total harmonic distortion produced by non-linear loads. Common examples of non-linear loads include variable speed drives (VSD), rectifiers, arc furnaces, UPS systems, computing equipment, and fluorescent lighting.

A poor power factor has many significant impacts on the grid and the environment. These effects include voltage distortions, maloperation of sensitive equipment, large neutral currents, excitation of power system resonances, and the possibility of overloading equipment[3].

The effects of these issues can range from equipment damage to large-scale blackouts. To deal with these issues, the network is normally upgraded by replacing existing equipment, or building

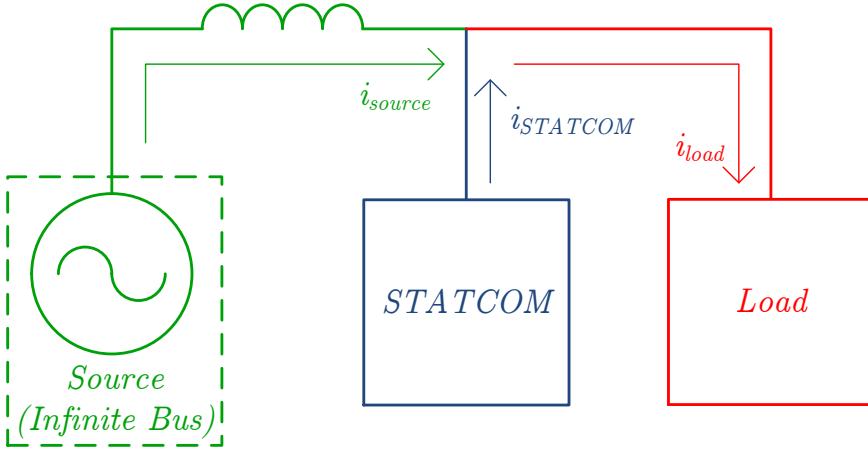


Figure 1.1: Basic power system model

additional infrastructure[4]. The large cost of these projects is ultimately borne by the general public in the form of increased electricity prices.

The increased currents flowing through the impedances of the grid lead to increased real power losses, decreasing the overall efficiency of the grid. This also has the effect of producing additional greenhouse gases as the real power losses must be supplied by electrical generators, most of which use coal as their primary source of fuel[5].

To deal with these issues, Schedule 5.1 of the National Electricity Rules (NER) has been established. This schedule specifies operating standards for frequency, stability, supply voltage, fluctuations, distortion, unbalance and fault clearance times. It is the responsibility of generation, transmission, and distribution companies to abide by these rules.

## 1.2 Project Overview

This project involves the design, simulation and construction of a device that connects to the electrical grid to alleviate the previously discussed issues by increasing the quality of the power that flows through the network. The device works by providing the reactive and harmonic power demands at the load itself, so that only fundamental frequency active power flows through the electrical grid. This results in decreased losses and allows existing infrastructure to be better utilised by increasing the maximum real power transmittable. Figure 1.1 shows a simplified power system model incorporating the Advanced STATCOM.

The device designed and constructed in this project combines the functionality of both the STATCOM and the active harmonic filter into a single unit to achieve power factor correction and harmonic cancellation:

- A **static compensator (STATCOM)** is a power electronics-based device that emulates the functionality of a synchronous compensator, which is a synchronous motor whose shaft is unloaded[6]. The machine's excitation is controlled to vary the reactive power flowing between the machine and the power grid[7]. Thus, the term STATCOM implies control of reactive power at the fundamental frequency only, due to the synchronous nature of the device machine it is based on.
- An **active harmonic filter (AHF)** is a power electronics-based device that can inject or sink harmonic currents from the network to decrease the total harmonic distortion.

Thus, the device is known as an 'Advanced STATCOM', however the term 'STATCOM' may also be used to refer to this device throughout this thesis, so it is important to note the difference between the device in this project and a typical STATCOM which does not inherently provide harmonic minimisation functionality.

The device could be used by high voltage transmission companies, medium/low voltage distribution companies, or industrial companies with poor power quality performance (such as mines and smelters).

### 1.3 Thesis Outline

This thesis is organised into 8 chapters and 3 appendices. Each chapter begins with a very brief summary of the thesis to that point, and an outline of the aims of the chapter. This is included to help with the readability of the thesis and allow any chapter to be read independently of the rest of the thesis.

- **Chapter 1** (this chapter) provides the motivation for the project and an outline of what is achieved.
- **Chapter 2** provides a more detailed background of the theory necessary to understand the context and usefulness of this project. Also provided is a comparison of alternative methods to achieve this project's objectives.
- **Chapter 3** discusses the methods of power processing using PWM converters. This chapter provides an analysis of the voltage source converter, which is the fundamental building block of the Advanced STATCOM and many other power electronics-based devices.
- **Chapter 4** introduces instantaneous power theory, which is the basis for the Advanced STATCOM controller. An understanding of this theory is vital before the Advanced STATCOM control scheme can be introduced.
- **Chapter 5** involves a detailed examination of the Advanced STATCOM controller, including the outer loop reference generation and the inner loop current controller. This chapter also investigates methods for harmonic extraction and discusses a novel PLL algorithm designed in this project.
- **Chapter 6** provides a simulation analysis of the various Advanced STATCOM capabilities in a test power system using the Saber simulation platform.
- **Chapter 7** provides details of the experimental power system test bed design and construction, followed by practical results demonstrating the power quality benefits. This chapter also discusses the computer application designed to interface with the Advanced STATCOM.
- **Chapter 8** summarises the entire project and provides ideas for future work to build on the achievements of this project.
- **Appendix A** provides proofs, derivations and calculations that are relevant to the project, but unnecessary for the main body of the thesis.
- **Appendix B** provides other supplemental information that is superfluous to the main body of the thesis.
- **Appendix ??** contains images of similar devices to the Advanced STATCOM being used in industrial applications.

# Chapter 2

## Background

*This chapter provides a more detailed, technical background of modern issues facing today's power systems to establish the primary motivation for this project. This chapter also provides an overview of alternative methods to help mitigate power quality issues and a justification as to why the particular device designed in this project has been chosen.*

### 2.1 Power Flow

Power systems are built for the purpose of safely, reliably and efficiently transferring electrical power from generators to customers (residential, commercial and industrial). The electrical grid is comprised of many components, including generators, transmission lines, transformers, circuit breakers and busbars. These components all have certain ratings that determine the maximum current, or power, they are able to handle for a duration of time.

Due to economic and environmental factors, the bulk generators (coal-fired power stations) are located away from load centres[5]. This results in a larger impedance between the sources and loads, contrasted with the generators being close to the load centres. The loads connected to the power system may be classified as linear or non-linear loads:

- **Linear loads** produce no harmonics, but may have a power factor less than 1 (meaning they draw both active and reactive power),
- **Non-linear** loads may produce harmonics, generally due to switching involved within the device.

Both reactive and harmonic power provide no real average energy transfer from the source to the load, however, they do result in larger currents[8]. The effect of this is an increase in the real power losses in the power system due to the interaction of the larger currents with the

impedance of the components forming the electrical grid. Additionally, the equipment will be operated closer to ratings (or even pushed beyond their ratings in certain circumstances).

Since reactive and harmonic power provide no real average energy transfer, it is possible to produce these powers close to the load, removing the need for them to flow through the entire electrical grid[9]. This reduces the amount of current flowing through the grid, improving efficiency due to lower losses, and increasing the maximum transmittable real power through existing infrastructure. Reactive power can also be controlled to regulate the voltage of the point of common coupling by injecting reactive power to increase the voltage, or sinking reactive power to decrease the voltage[10].

## 2.2 FACTS Power Electronics Devices

The concept of *Flexible AC Transmission Systems* (FACTS) devices was introduced in 1988 by Dr. Narain G. Hingorani[11]. FACTS devices are power electronics-based and other static devices that are connected to the power network to improve voltage regulation, enhance controllability, increase power transfer, minimise losses, improve supply quality and optimise overall system performance[4]. With the use of FACTS devices, it may be possible to delay expensive capital projects by more effectively utilising existing infrastructure.

FACTS devices can be divided into four categories based on their connection to the grid[12]:

- **Series devices**, which act to vary the impedance of the line to control real power flow. Examples include the series capacitor, series reactor (inductor), and static synchronous series compensator (SSSC),
- **Shunt devices**, which inject or sink current for the primary purpose of controlling reactive power flow. Examples include the shunt capacitor, static VAr compensator (SVC), and the STATCOM. The device designed and built in this project falls into this category,
- **Combined series-series devices**, which can provide real power transfer between compensated lines, as well as reactive series compensation. An example is the interline power flow controller (IPFC) which is a combination of SSSCs sharing a common DC link,
- **Combined series-shunt devices**, which enable both real and reactive power flow control. An example is the unified power flow controller (UPFC) which is a combination of a shunt and series-connected FACTS device sharing a common DC link.

FACTS devices can be also classified as a *variable impedance type*, *voltage source converter-based* (VSC) or *current source converter-based* (CSC)[13]. Section 3.1 in the following chapter will provide a comparison between the VSC and CSC to show that the VSC is a much better option in general than the CSC.

Sections 2.3.3 and 2.4.4 will provide a comparison between variable impedance type FACTS

devices and VSC-based FACTS devices for the purposes of reactive power control and harmonic filtering.

## 2.3 Reactive Power Control

Reactive power is the power that is stored temporarily in magnetic and electric fields, and can do no real work. Reactive power in the form of electric fields occurs in capacitors, and reactive power in the form of magnetic fields occurs in inductors[14].

Reactive power can exist at the fundamental frequency and also at harmonic frequencies, however, in this project reactive power control deals with the fundamental frequency reactive power only. Reactive powers at the harmonic frequencies are dealt with separately in the harmonic filtering section. Reactive power control is used for power factor correction, though it is a simple extension to use reactive power control for voltage regulation[15].

### 2.3.1 Power Factor Correction

*Power factor correction* is achieved when the shunt connected FACTS device provides the reactive power demands of the load so that the source only provides the active power demands.

Figure 2.1 on the next page shows a fundamental frequency voltage waveform (black) and a fundamental frequency current waveform (red), with a phase shift separating them. It is possible to decompose the current waveform into a real component which is in phase with the voltage (green) and an imaginary component which is  $90^\circ$  out of phase with the voltage (blue). Since the imaginary current component transfers no real power to the load, it can be generated by the FACTS device at the load terminals[16]. This results in a decrease in the source current from the red waveform to the green waveform.

The benefit gained from this decrease in current is related to the power factor of the load. For a load which is almost purely real (power factor  $\approx 1$ ), the magnitude of the injected current will be small and hence the decrease in the source current will be small. Conversely, for a load which is almost purely reactive (power factor  $\approx 0$ ), the injected current will be almost the size of the load current, and the decrease in the source current will be large.

### 2.3.2 Voltage Regulation

Reactive power flows and voltage levels throughout the network are very tightly coupled[17]. Thus, *voltage regulation* can be achieved by controlling the FACTS device to be a source or sink of reactive power in order to increase or decrease the voltage at the point of common

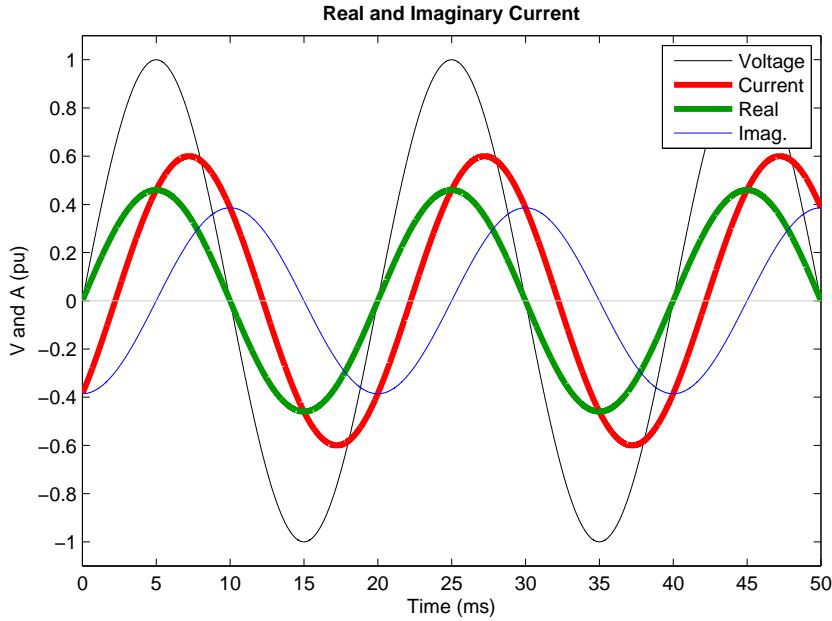


Figure 2.1: Power factor correction

coupling. These FACTS devices may be classed as variable impedance type devices or VSC-based devices[18].

Figure 2.2 on the facing page shows voltage regulation for the case when the load increases. As the load current is increased, the magnitude of the source current increases, and hence the voltage drop across the network impedance increases, lowering the voltage at the load terminals. By injecting reactive currents, the source current is decreased causing the voltage drop to decrease, allowing the voltage at the load terminals to remain close to nominal value.

Conversely, Figure 2.3 on the next page shows voltage regulation for the case when the load decreases. As the load current is decreased, the magnitude of the source current decreases, and hence the voltage drop across the network impedance decreases, increasing the voltage at the load terminals. By sinking reactive currents, the source current is increased causing the voltage drop to increase, allowing the voltage at the load terminals to remain close to nominal value.

### 2.3.3 Methods for Reactive Power Control

The most common variable impedance device for the purpose of reactive power control is the static VAr compensator (SVC)[19]. The main types of SVCs are the thyristor-controlled reactor (TCR) and the thyristor-switched capacitor (TSC)[20]. These SVCs are often used in conjunction with mechanically-switched capacitors and mechanically-switched reactors, as shown in Figure 2.4 on page 10. In a TCR the firing angle of the thyristors can be controlled to vary the effective inductance. Due to capacitor characteristics, the effective capacitance cannot be

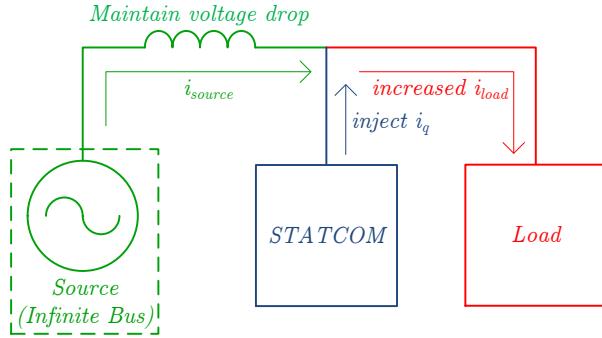


Figure 2.2: Voltage regulation: High load condition

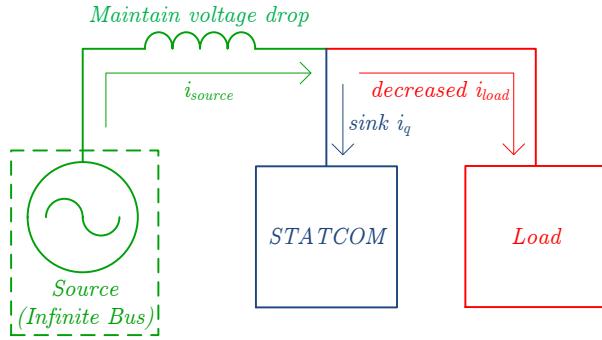


Figure 2.3: Voltage regulation: Low load condition

varied, so in a TSC the capacitor must be switched completely in or out. The mechanically switched capacitors and reactors achieve this switching with the use of circuit breakers instead of thyristors, with a much lower frequency of switching (maximum of a few times per day)[20].

Compared with these variable impedance devices, VSC-based devices offer much more precise and dynamic control over reactive power flows[21]. The most powerful and flexible VSC-based device is the shunt-connected static compensator (STATCOM)[11]. Its functionality is based on the synchronous compensator (or synchronous condenser), which is a synchronous motor with no load connected. The synchronous machine can be over or under-excited to run with leading or lagging power factor as shown in Figures 2.5(a) and (b) respectively. The v-curves shown in Figure 2.6 on the next page show the armature current as a function of the field current and power factor of a synchronous machine. A synchronous compensator is operated on the lowest v-curve, corresponding to operation at 0 pf. The STATCOM provides the same functionality as the synchronous compensator through the use of power electronics, and hence it is called a ‘static synchronous compensator’ though this is generally shortened to ‘static compensator’[19].

The relative advantages and disadvantages of VSC-based devices and variable impedance devices are shown in Table 2.1 on page 11[11].

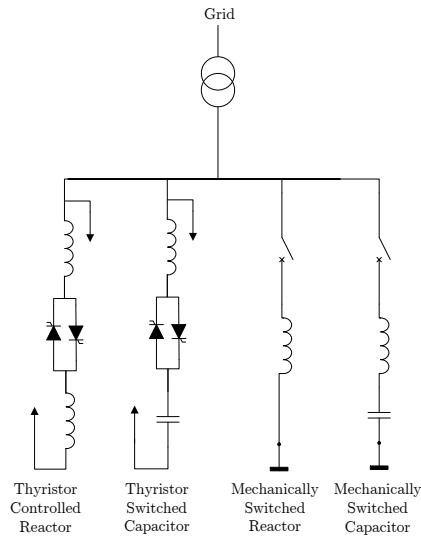


Figure 2.4: Static VAr compensators

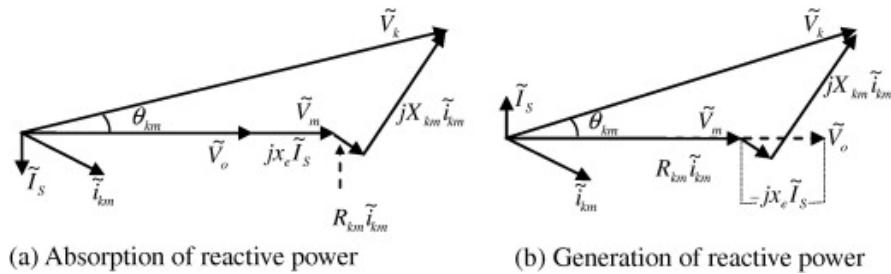


Figure 2.5: Synchronous machine excitation control[22]

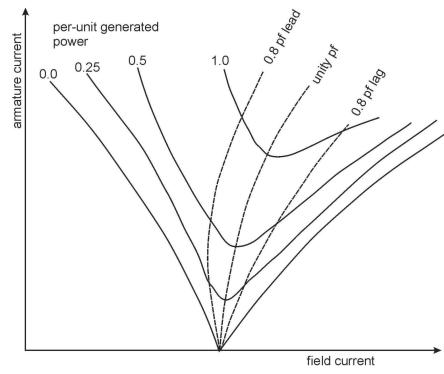


Figure 2.6: Synchronous machine v-curves[23]

VSC-Based Devices	Variable Impedance Devices
<ul style="list-style-type: none"> <li>More compact than variable impedance devices since VSC-based devices can provide the same ratings with a smaller physical size.</li> <li>VSC-based devices can supply the required reactive power even as the bus voltage drops. With variable impedance devices, the reactive power injected or sunk is dependent on voltage at the point of common coupling.</li> <li>VSC-based devices can provide active power if an energy source is provided at the DC bus.</li> <li>VSC-based devices have a faster response than variable impedance devices.</li> </ul>	<ul style="list-style-type: none"> <li>Variable impedance devices are cheaper than VSC-based devices of the same power rating. This is because VSC-based devices require expensive self-commutating power semiconductor devices (however emerging silicon carbide technologies will decrease this cost).</li> </ul>

Table 2.1: Advantages of VSC-based devices and variable impedance devices

## 2.4 Harmonics

The number of non-linear loads connected to the grid has increased significantly in recent years[5]. Non-linear loads may draw non-sinusoidal currents, which are distorted due to the presence of harmonics. Harmonics are sinusoidal components that have frequencies which are integer multiples of the fundamental frequency[4].

Figure 2.7 on the next page provides an example of a distorted current waveform (red) which is made up of a purely sinusoidal component at the fundamental frequency (green) and 5th, 7th and 11th harmonic components (cyan, pink, grey respectively). If a FACTS device can inject the harmonic components, then the source will only need to provide the fundamental frequency current.

This section provides examples of common non-linear loads, outlines a method of measuring the level of harmonics present in a signal, and details the negative effects caused by these harmonics.

### 2.4.1 Examples of Harmonic Loads

Common residential loads with a poor harmonic distortion include fluorescent lighting and computing equipment. The major source of harmonic content on the grid is from large industrial loads, such as arc furnaces, as shown in Figure 2.8, and variable speed drives (which are used in many applications including mining draglines, as shown in Figure 2.9, and steel rolling mills, as shown in Figure 2.10)[5]. Loads with an uncontrolled three-phase rectifier front-end produce

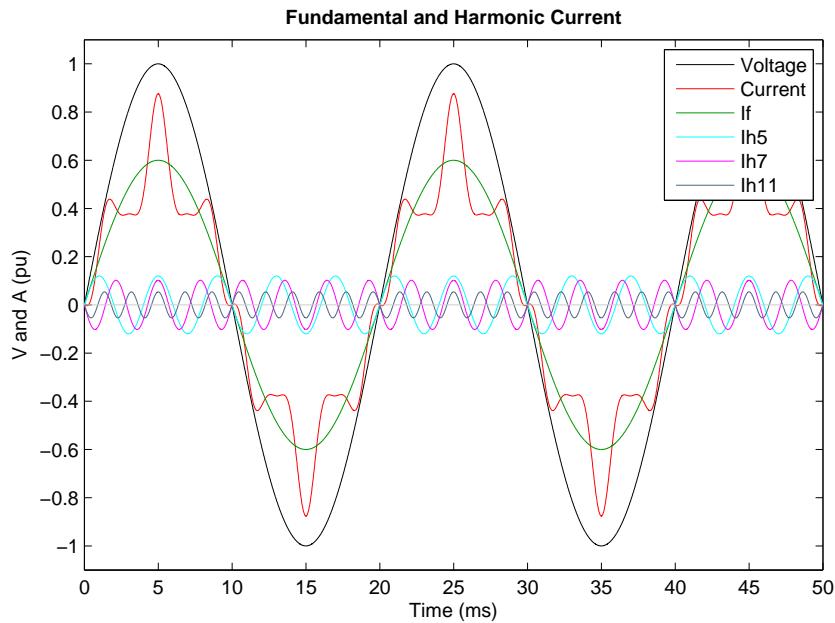


Figure 2.7: Harmonics



Figure 2.8: Arc furnaces[24]



Figure 2.9: Dragline[25]



Figure 2.10: Steel rolling mills[26]

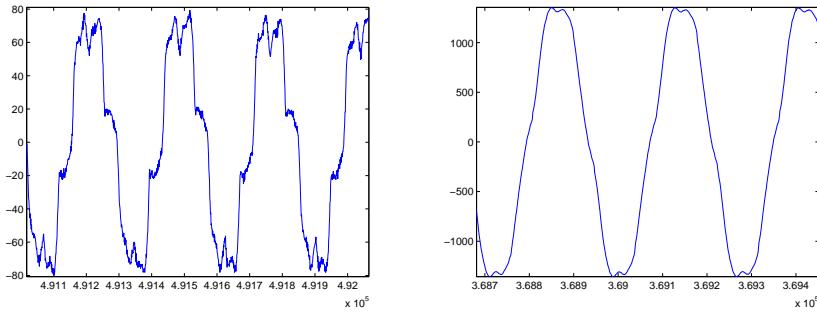


Figure 2.11: Tramming of a machine at a mine: Current and voltage waveforms

significant 5th and 7th harmonics[16].

Figure 2.11 shows a current waveform (phase ‘a’ of a three-phase system) for a large electrical machine tramping at a mine (raw data courtesy of CRCMining). The image on the right shows the voltage distortions created by the current harmonics. Later chapters replicate this type of load to show that a STATCOM can filter the harmonics, leaving clean sinusoidal currents and removing the voltage distortions.

#### 2.4.2 Total Harmonic Distortion

A value known as the *total harmonic distortion* (THD) exists to quantify the harmonic content of the signal. The THD formula for both currents and voltages is:

$$THD = \frac{\sqrt{\sum_{i=1}^{h_{max}} I_h^2}}{I_1} \times 100\%$$

where:

- $h_{max}$  is the highest level harmonic present in the signal,
- $I_h$  is the magnitude of the  $h^{th}$  harmonic component,
- $I_1$  is the magnitude of the fundamental frequency component,

The input currents to a unfiltered, poorly controlled variable-speed drive may have a THD greater than 100%[9].

### 2.4.3 Problems Caused by Harmonics

The current harmonics introduced into the network by non-linear loads have many significant impacts on the grid:

- **Distort supply voltages:** Harmonic currents flowing through the impedance of the network create associated voltage drops at each harmonic frequency. These voltage drops lead to a distorted supply voltage which can be seen by other equipment and customers[9]. Large voltage distortion can cause torque pulsations and increased losses in direct on line motors as the harmonic currents create abnormal flux within the machine[27].
- **Protection and metering maloperation:** False tripping of circuit breakers and incorrect metering are both possible, as relays often monitor RMS current and peak current, both of which are increased in the presence of harmonics[28]. These issues must be mitigated by adjusting protection settings and/or introducing true RMS monitoring.
- **Overrate capacitors:** The impedance of grid-connected capacitors decreases for higher frequencies, so power factor correction capacitors absorb large amounts of harmonic currents. These capacitors must have larger ratings to account for the harmonic currents, or else they may fail[9].
- **Resonance:** Excitation of power system resonances are possible when shunt capacitors are combined with the supply inductance at harmonic frequencies, which can amplify the harmonic distortion and lead to equipment damage[29].
- **Increased losses:** The increased losses in generators, transformers and transmission lines are dissipated mostly as heat, which can lead to a premature breakdown of insulation and an overall decrease in equipment service life[28]. The increased losses decrease the overall grid efficiency and indirectly lead to the production of additional greenhouse gasses as the energy losses are mostly supplied by coal-fired power stations[5]. The increased losses are caused by 3 main factors:
  - **Larger RMS:** The current flowing through the network has a larger RMS due to the presence of harmonic components.
  - **Skin effect:** In transmission lines, high order harmonics tend to be distributed closer to the outer layers of the conductors. This increases the cable's resistance as the effective cross-section is reduced[27].
  - **Eddy currents:** The harmonics also increase losses in transformers and generators due to larger eddy current losses[9].

Odd harmonics: non-multiple of 3		Odd harmonics: multiple of 3		Even harmonics	
Order	Distortion (%)	Order	Distortion (%)	Order	Distortion (%)
5	5	3	4	2	1.6
7	4	9	1.2	4	1
11	3	15	0.3	6	0.5
13	2.5	21	0.2	8	0.4
17	1.6	>21	0.2	10	0.4
19	1.2			12	0.2
23	1.2			>12	0.2
25	1.2				
>25	$0.2 + 0.5 \frac{25}{h}$				

Table 2.2: Harmonic voltage limits for networks up to 35kV (total THD = 6.5%)[30]

To ensure adequate supply quality to all customers, electricity distributors need to abide by the NEM rules which enforce harmonic limits as indicated in AS/NZ Standards 61000.3.6:2001 (Electromagnetic Compatibility). It is important to note that the harmonic limits are on the grid voltage, rather than on a customer's load current. This is because other customers are affected by voltage distortions, and the level of current harmonics which cause these distortions is dependent on many other factors. For example, a harmonic load at the end of a long feeder is likely to cause significant voltage harmonics, however, the same load connected at a substation (approximating an infinite bus) will have a much smaller effect on voltage THD.

The voltage harmonic limits for networks up to 35kV are outlined in Table 2.2. The limits for transmission networks over 35kV are given in Appendix B.

#### 2.4.4 Methods for Harmonic Filtering

The two main methods of minimising harmonics in the network are passive filtering and active filtering[11].

Passive harmonic filters consist of a bank of tuned RLC filter circuits[28, 31]. Passive filters are named as such because they do not need external power, and they have no switching components. Passive harmonic filters are generally high-pass or band-pass filters that will attenuate signals of a particular frequency, or range of frequencies, without affecting others[31]. Some examples of typical passive filter circuits are shown in Figure 2.12 on the following page.

Active filters are generally current-controlled VSC-based devices that inject or sink harmonic currents to minimise the harmonic content of the source current[16]

. Current measurements are made on either the load or the source, and the controller isolates the harmonic components and controls the inverter in such a way that the harmonics are cancelled.

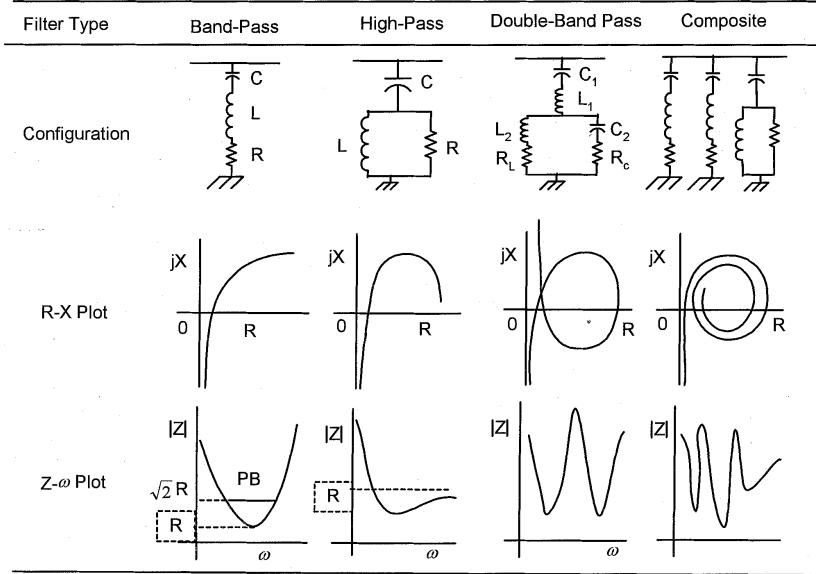


Figure 2.12: Common types of passive harmonic filters[31]

Active Filters	Passive Filters
<ul style="list-style-type: none"> <li>The filtering characteristics of active filters are not affected by the source impedance, unlike passive filters.</li> <li>Active filters do not suffer the same parallel and/or series resonance that a passive filter suffers.</li> <li>Active filters will perform well over a range of loads, where passive filter performance is dependent on the specific load.</li> </ul>	<ul style="list-style-type: none"> <li>Passive filters have a lower initial cost compared with an equivalent active filter.</li> <li>Passive filters are very robust and simple to install.</li> <li>High efficiency.</li> </ul>

Table 2.3: Advantages of active filters and passive filters

The relative advantages and disadvantages of passive filters compared with active filters are shown in Table 2.3[11].

## 2.5 Transformations

This section outlines the Clarke and Park transformations, which are mathematical three-phase to two-phase transformations that can be used in the control of power electronics-based devices[32].

It is not possible to have a transformation that loses one dimension yet still retains all possible data contained within the original three-phase signal. Thus, to ensure no possible information

loss, it would appear that the transformations must output three quantities. The reason a two-phase output is possible however, is that an extra piece of information is known for a three-wire system:  $i_a + i_b + i_c = 0$ . By enforcing this condition, the third output quantity of the transformations will always be 0 and hence the transformations can have two outputs which contain all the information of the original three-phase signal.

This section also introduces the inverse Clarke and Park transformations which allow the three-phase values to be calculated given a set of two-phase inputs.

### 2.5.1 Clarke Transformation

The Clarke transformation is a three-phase ( $abc$ ) to two-phase ( $\alpha\beta$ ) transformation for three-wire systems[32]. The reference axis for the  $\alpha\beta$  components is a stationary frame, so when the input is a balanced three-phase signal, the  $\alpha\beta$  components rotate in time and are offset by  $90^\circ$ . The generalised power variant Clarke transformation is:

$$\begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{-\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}$$

which can simply be written as:

$$I_{\alpha\beta 0} = T_{\alpha\beta 0} I_{abc}$$

The inverse transformation is:

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} & 1 \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix}$$

which can simply be written as:

$$I_{abc} = T_{\alpha\beta 0}^{-1} I_{\alpha\beta 0}$$

For any three-wire system, the sum of the currents must be 0, so  $I_0 = \frac{1}{2}(I_a + I_b + I_c) = 0$  and therefore  $I_0$  can be neglected, leaving:

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{-\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}$$

which can simply be written as:

$$I_{\alpha\beta} = T_{\alpha\beta} I_{abc}$$

With the removal of  $I_0$ , the inverse Clarke transformation is:

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix}$$

which can simply be written as:

$$I_{abc} = T_{\alpha\beta}^{-1} I_{\alpha\beta}$$

### 2.5.2 Park Transformation

The Park transformation (also known as the direct-quadrature-zero transformation) is a three-phase ( $abc$ ) to two-phase ( $dq$ ) transformation for three-wire systems[32]. The reference axis for the  $dq$  components is a rotating frame (which has angle  $\theta$ ), so when the input is a balanced three-phase signal, the output  $dq$  components are constant DC quantities.

$$\begin{bmatrix} I_d \\ I_q \\ I_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}$$

which can simply be written as:

$$I_{dqd} = T_{dqd} I_{abc}$$

The inverse transformation is:

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & -\sin(\theta) & \frac{\sqrt{2}}{2} \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) & \frac{\sqrt{2}}{2} \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} I_d \\ I_q \\ I_o \end{bmatrix}$$

which can simply be written as:

$$I_{abc} = T_{dqd}^{-1} I_{dqd}$$

For any three-wire system, the sum of the currents must be 0, so  $I_0 = \frac{1}{2}(I_a + I_b + I_c) = 0$  and

therefore  $I_0$  can be neglected, leaving:

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}$$

which can simply be written as:

$$I_{dq} = T_{dq} I_{abc}$$

With the removal of  $I_0$ , the inverse Park transformation is:

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix}$$

which can simply be written as:

$$I_{abc} = T_{dq}^{-1} I_{dq}$$

## 2.6 Chapter Summary

This chapter discussed the configuration of the power network, and explained some problems typically associated with it. The concept of FACTS devices was then introduced, as a method of minimising the impact of these issues.

Power factor correction and voltage regulation were then examined as cases of controlling reactive power flows. Common methods for reactive power control were reviewed, with a comparison between variable impedance and VSC-based FACTS devices.

Following this, the causes and problems of harmonics were examined, and methods for mitigating these harmonics were discussed.

Finally, the Clarke and Park transformations were introduced as an understanding of these is vital to the project.



# Chapter 3

## Voltage Source Converter

The previous chapters introduced the background concepts that are necessary to understand this project. This chapter examines the voltage source converter with a discussion of its topology, limitations and an overview of control methods. Later chapters will continue to build on this, as the voltage source converter is the basis of the STATCOM as well as many other power electronics devices.

### 3.1 Power Processing Using a PWM Converter

An appropriately controlled FACTS device will seek to inject or sink reference currents from the network in order to achieve its control objectives. Two alternative device topologies to achieve this are the *voltage source converter* (VSC) and the *current source converter* (CSC)[33, 34]. This section demonstrates the reasons that make the VSC the superior alternative.

Figure 3.1 shows typical VSC and CSC two-level topologies. Both devices have three legs with two power electronic switches per leg. The main difference between the two topologies is the use of a capacitor to provide the voltage source in the VSC, compared with the use of an inductor

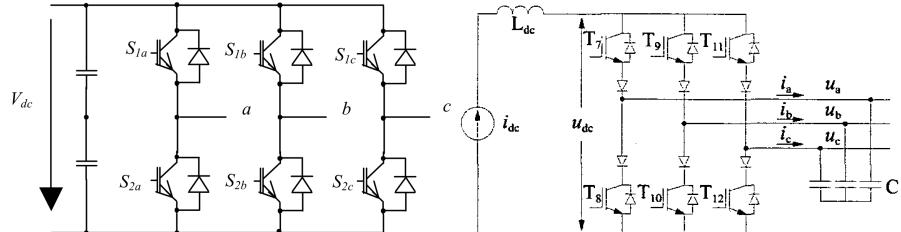


Figure 3.1: VSC and CSC topologies[33]

to provide the current source in the CSC. Also, the output filter of the VSC uses inductors to smooth the currents whereas the output filter of the CSC uses capacitors to smooth the voltages.

CSCs have many disadvantages when compared to VSCs[21]:

- A CSC is more complex than a VSC and filter capacitors add to the cost of the CSC,
- Resonance may be possible between the filter capacitors and AC-side inductance of a CSC,
- A diode generally must be placed in series with the switches of CSC which increase the conduction losses,
- Efficiency of the CSC is lower due to the power loss of an inductor being greater than the power loss of a capacitor.

CSCs do have some advantages, including implicit short circuit protection and lower AC harmonics due to the filtering capacitors used[34], however these do not outweigh the significant disadvantages.

The power electronic switches used in VSCs and CSCs are typically insulated gate bipolar transistors (IGBT), however gate turn-off thyristors (GTO), integrated gate commutated thyristors (IGCT) or MOS turn-off thyristors (MTO) may be used in some applications[14]. Unlike regular thyristors, these devices have both turn-on and turn-off capabilities, allowing self-commutation as opposed to line-commutation[11]. These power electronic switches are operated using a technique known as pulse width modulation (PWM) to vary the average output voltage in the case of the VSC, or output current in the case of the CSC. PWM techniques for current control will be reviewed in Section 3.5.

### 3.2 Two-Level Voltage Source Converter

The voltage source converter (VSC) is the fundamental building block of many power electronic devices including AC motor drives, AC/DC converters and of course, STATCOMs[35]. The most common topology is the two-level VSC, which is a six-pulse converter consisting of three legs which each have two power semiconductor switching devices (with anti-parallel diodes)[36]. The popularity of this topology is due to its simplicity of design and control, and because it can provide adequate performance for a reasonable cost. The STATCOM designed in this project utilises a two-level VSC, however, in some specialist applications a multilevel VSC may be more suitable due to high power or low harmonic requirements[37]. For this reason, Section 3.3 provides a brief outline of the three most common multilevel VSC topologies.

The basic diagram of a two-level VSC can be seen in Figure 3.2 on the next page. Through the switching of the semiconductor devices, the output voltage of each VSC leg may be controlled to be equal to either the positive or negative DC voltage. Since there are six switches, there

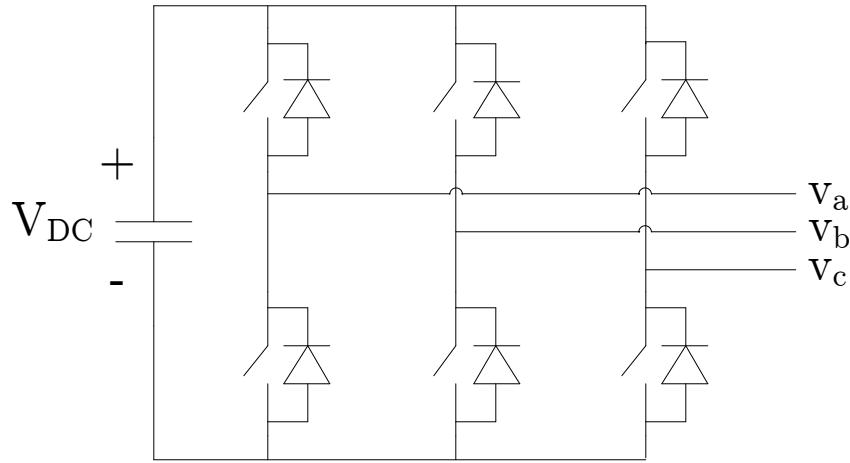


Figure 3.2: Basic topology of a two-level VSC

exist  $2^6 = 64$  possible switching combinations. However, many of these switching combinations are ignored as they result in obvious problems, such as when both switches on any single leg are turned on, causing a short circuit of the DC bus. Eliminating these problematic combinations leaves  $2^3 = 8$  possible legitimate output voltage combinations.

### 3.3 Multilevel Voltage Source Converter

In certain medium and high-power applications, it may be desirable to use multilevel VSCs due to power losses incurred with fast switching, limited withstand voltage of switching devices, and low harmonic specifications[37]. There are many multilevel VSC topologies, each with their own advantages and disadvantages. This section covers three popular topologies on which others are based[37–39]. These topologies are the cascaded H-bridge converter, the diode-clamped converter and the capacitor-clamped converter.

#### 3.3.1 Cascaded H-Bridge

Cascaded H-bridge multilevel converters are based on a series connection of many (typically 3-10) single-phase H-bridge converters[40]. A nine-level cascaded H-bridge converter is shown in Figure 3.3(a). Three-phase cascaded H-bridge multilevel converters can be formed by Y-connecting or  $\Delta$ -connecting single-phase cascaded H-bridge multilevel converters[40].

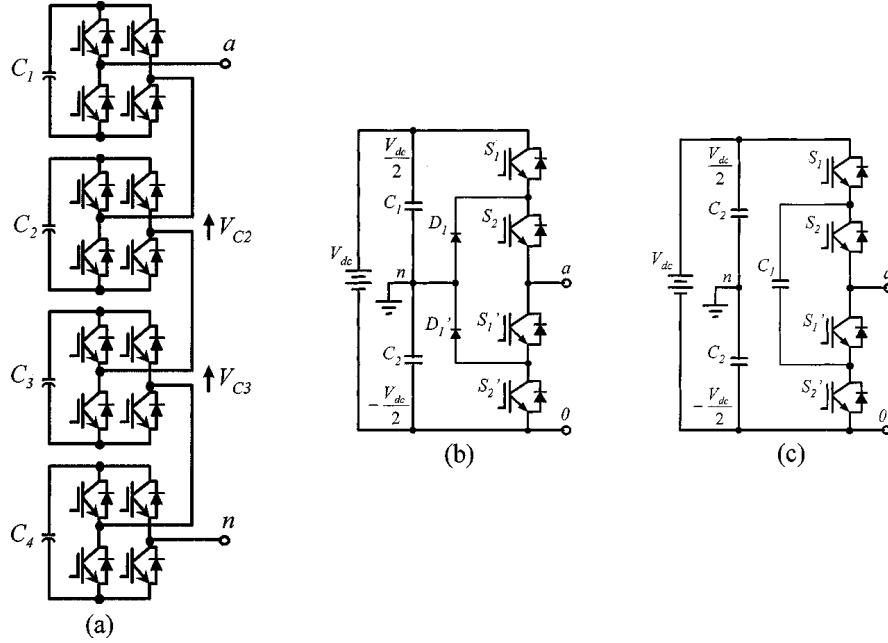


Figure 3.3: Multilevel converter topologies. (a) Cascaded H-bridge. (b) Diode-clamped. (c) Capacitor-clamped.[37]

#### Advantages:

- Utilises standard low-voltage mature technology components,
- Highly modular so faulty components can be easily replaced,
- Smallest number of components per voltage level compared to diode-clamped and capacitor-clamped converters,
- With advanced control strategies, it may be possible to bypass a faulty module and keep operating until it can be replaced[41].

#### Disadvantages:

- Each H-bridge requires an isolated DC voltage which can make real power transfer difficult.

### 3.3.2 Diode-Clamped (Neutral-Point-Clamped)

A three-level diode-clamped converter is shown in Figure 3.3(b). An  $n$ -level diode-clamped converter consists of  $n-1$  capacitors on the DC bus and produces  $n$  levels of the phase voltage[39].

**Advantages:**

- A single DC bus shared between all phases makes real power transfer relatively simple.

**Disadvantages:**

- The number of diodes required increases quadratically with the number of levels, with  $3(n - 1)(n - 2)$  diodes required for an  $n$  level three-phase converter,
- The switching devices have uneven ratings,
- The clamping diodes need to have different voltage ratings for reverse voltage blocking,
- The reverse recovery of the clamping diodes becomes a major problem with PWM schemes[39],
- Balancing capacitor voltages can be an issue as the charging and discharging times for the various capacitors are different[37].

### 3.3.3 Capacitor-Clamped (Flying Capacitors)

A three-level capacitor-clamped converter is shown in Figure 3.3(c). A series connection of capacitors gives different voltage levels between clamping points. The phase legs share a common DC bus, with separate inner-loop balancing capacitors for each of the three phases. It can be shown that an  $n$ -level converter (with  $n - 1$  DC bus capacitors) has  $2n - 1$  line voltage levels[39].

**Advantages:**

- The large amount of capacitors provide extra ride through capabilities during short power outages[38],
- A single DC bus shared between all phases makes real power transfer relatively simple,
- More flexible voltage synthesis compared with a diode-clamped converter.

**Disadvantages:**

- The number of capacitors required increases quadratically with the number of levels, with  $0.5(3n - 4)(n - 1)$  capacitors required for an  $n$  level three-phase converter,
- Complicated control for real power conversion[37].

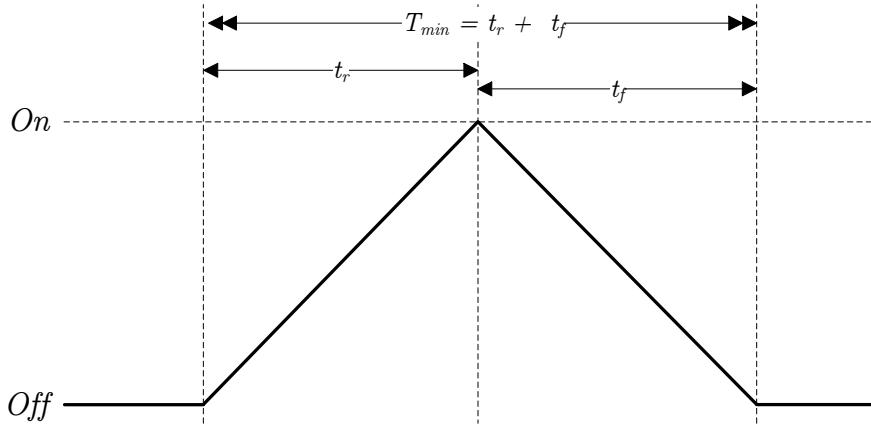


Figure 3.4: Effect of non-zero rise and fall times

## 3.4 Practical Limitations of Voltage Source Converters

### 3.4.1 Non-Zero Rise and Fall Times

A limitation caused by the non-zero rise and fall times is that of limited duty cycles[42]. If rise and fall times were infinitesimally small, it would be possible for a switching device to switch twice almost instantaneously, causing an infinitely small pulse and hence a duty cycle that can approach 0 or 1. However, due to the non-zero rise and fall times, the width of this pulse has a minimum length and hence minimum and maximum duty cycles must be limited. This concept is illustrated in Figure 3.4.

### 3.4.2 Non-Zero Short Circuit Resistance and Non-Infinite Open Circuit Resistance

Along with the non-zero rise and fall times discussed, the non-idealities of the semiconductor switching devices also result in non-zero short circuit resistance and finite open circuit resistance[43]. These non-idealities combine to cause power losses during switching operations, decreasing overall converter efficiency. Most of this power is dissipated as heat which needs to be removed from the switching devices. Thus, a limit must be placed on the number of switching operations per second (switching frequency) so that the heat does not become a damaging problem.

### 3.4.3 Dead Time

The non-zero rise and fall times create the need for *dead time*, which is an amount of time where both switches on a given leg must be off to prevent a dangerous condition known as shoot-through[44]. An example provided in Figure 3.5 on the next page shows the initial output

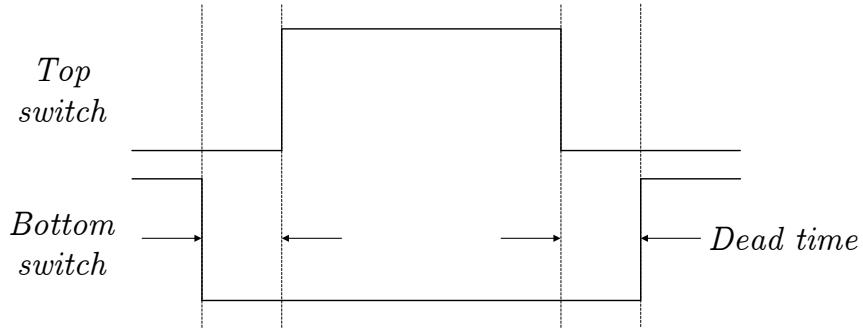


Figure 3.5: Illustration of dead time

of leg A is  $-V_{DC}$ , as the top switch of the leg is open and the bottom switch is closed. If a transition is required so that the output becomes  $+V_{DC}$ , then the top switch must close and the bottom switch must open. With ideal switches, the toggling of these switches could happen simultaneously and instantaneously, however due to the non-idealities of transistor switches, the top switch must be completely off before the bottom switch closes. Without dead time, there may be the possibility of the bottom switch closing before the top switch becomes a complete open circuit, creating a low impedance path across the DC bus which may cause large currents to flow[45].

This dead time is typically in the order of a few microseconds, and the consequence is a lowering of the effective duty cycle since the switches aren't on for as long as desired. The effects of this dead time are greatest when the output voltages are small (around the zero crossing points of the sine wave) since the decrease in effective duty cycle represents a larger percentage of the original desired duty cycle[46].

### 3.5 Current Control of a Voltage Source Converter

With the use of an appropriate output filter, the VSC may be controlled in such a way that it essentially acts as a current source[47]. The performance of the current control may be assessed through the following criteria[42]:

- ideal tracking (no phase or amplitude errors) over the relevant frequency range,
- high dynamic response,
- limited or constant switching frequency to guarantee safe operation of power semiconductor devices,
- low harmonic content,
- high DC link voltage utilisation.

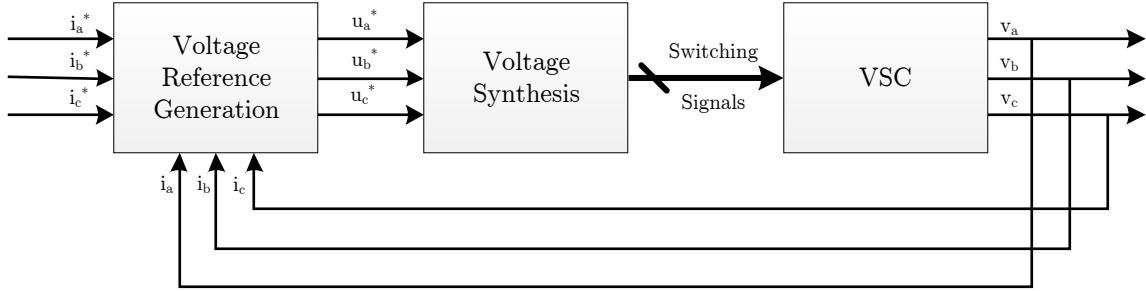


Figure 3.6: General outline for VSC current control

There are several popular methods of current control, each with associated advantages and disadvantages. The choice of which current control method to use will be largely dependent on the application for the VSC. For example, in motor drive applications a coarse level of current control may be sufficient, however, in other applications such as harmonic filtering, a highly accurate current controller is essential[47].

The general current control structure is based on the layout shown in Figure 3.6. The first block generates the voltage references for the VSC based on the desired and measured phase currents. The controllers reviewed in this paper for the first stage are:

- Hysteretic current control,
- PI controller on the abc phase currents,
- PI controller on the dq axis currents,
- Deadbeat predictive controller.

It is worth noting that there exist many other controllers which aren't covered in this paper including PR controllers, state feedback controllers, fuzzy logic controllers and neural network-based controllers[42, 47–50].

Following the voltage reference generation, there is a block that synthesises the VSC output voltages to match the generated reference voltages. The methods for this that are reviewed in this paper are:

- Sinusoidal PWM comparator,
- Space vector PWM.

This section provides an overview of the various current control methods stated above to justify the use of a deadbeat predictive space vector PWM controller for the STATCOM designed in this project. The specific application of this current controller in the project is further discussed in Section 5.6.

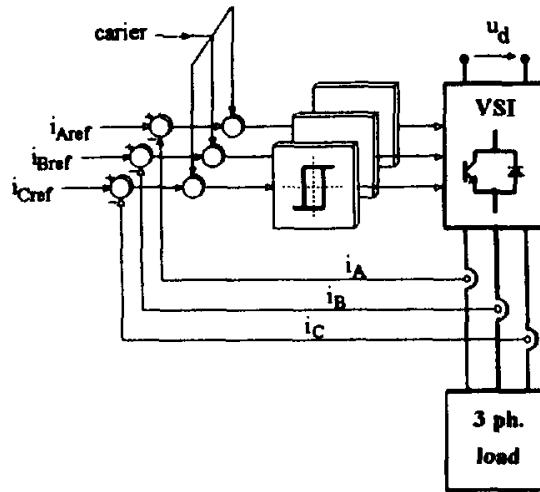


Figure 3.7: Hysteretic current control[42]

### 3.5.1 Hysteretic Current Controller

Hysteretic current control is a very simple method of current control where the reference currents are compared to the measured current, as shown in Figure 3.7. If the measured current for a given phase is less than the reference current, then the voltage for that phase leg is set to the positive DC voltage rail. Conversely, if the measured current is higher than the reference current, then the phase leg is set to the negative DC voltage rail[49].

This can be implemented with a hysteresis band and a variable switching frequency. Alternatively, the switching frequency can be fixed by making the comparisons occur at a constant frequency. The problem with this fixed frequency comparison is that there may be consecutive control periods where no switching occurs, leading to poor harmonic performance[42].

#### Advantages:

- Relatively easy to design,
- Computationally simple for a microcontroller.

#### Disadvantages:

- Large ripple as duty cycles are effectively 0% or 100%,
- Poor harmonic content.

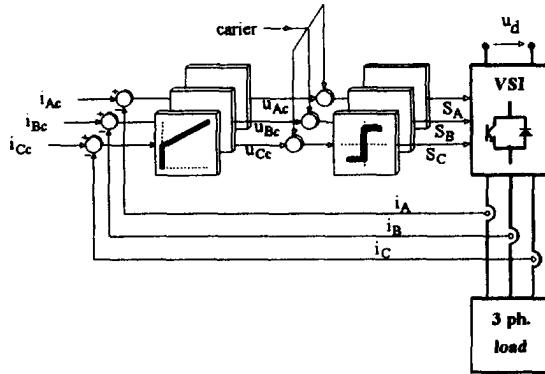


Figure 3.8: PI controllers on phase currents[42]

### 3.5.2 PI Controllers on the abc Phase Currents

The currents generated by the outer control loop form the references for the phase PI controllers, with the measured currents forming the feedback, as shown in Figure 3.8. The control signals generated are the voltages that need to be synthesised by the VSC. The derivative action of PID controllers is usually not used due to the amplification of noise (from measurement, switching or other sources) causing large changes in the generated output[47].

#### Advantages:

- Constant switching frequency,
- Computationally simple, as there are no PLLs or transformations present.

#### Disadvantages:

- Reference currents will be sinusoidal, removing the steady-state error elimination function of the integral part of the PI controller, and introducing phase delays,
- Very difficult to track signals containing harmonics due to the limited bandwidth of the controller.

### 3.5.3 PI Controllers on the dq Axis Currents

The Park transformation ( $abc$  phase currents to  $dq$  axis currents) yields signals that are approximately constant in time, rather than oscillating. This greatly improves the performance and suitability of PI controllers. Thus, a Park transformation carried out on the reference currents and the measured currents allows PI controllers on the  $d$  and  $q$  axes to generate  $dq$  voltages, as

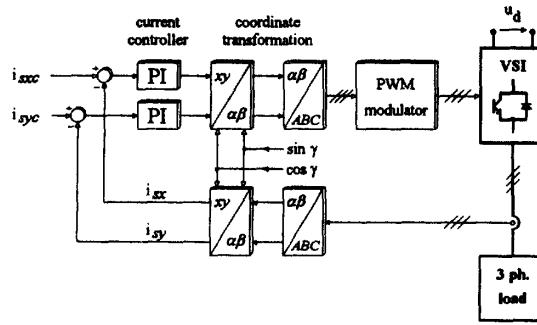


Figure 3.9: PI controllers on dq components[42]

shown in Figure 3.9. Using the inverse Park transformation, the phase voltages which the VSC must synthesise can be calculated.

#### Advantages:

- PI controller performance greatly improved with DC input signal,
- Integral part of PI controller acts to eliminate steady-state error,
- Two PI controllers, instead of three.

#### Disadvantages:

- Some phase delay introduced, limiting the maximum bandwidth and hence performance,
- Requires some method (usually a PLL) to generate a voltage angle,
- Increased complexity and computation requirements to carry out Park and inverse Park transformations,
- Harmonics introduce oscillations into the otherwise constant *dq* signals, greatly impacting performance[51].

#### 3.5.4 Deadbeat Predictive Controller

Deadbeat predictive control, as shown in Figure 3.10 on the next page, is a form of digital control that generates an output based on a model of the system[52]. By measuring the point of common coupling voltage, and knowing the filter model, it is possible to determine the VSC voltage that needs to be applied to bring the output current to the desired value in the minimum number of time steps[17].

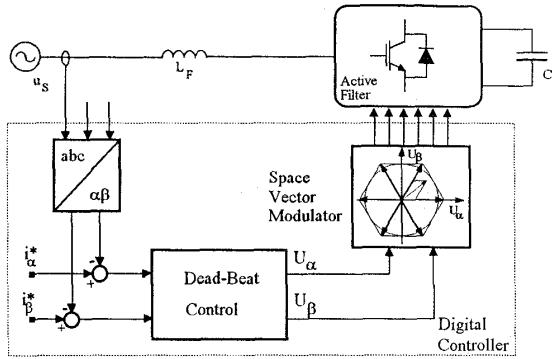


Figure 3.10: Deadbeat predictive controller[53]

**Advantages:**

- Well suited to a digital implementation,
- Optimal current tracking performance,
- Excellent harmonic performance,
- High bandwidth[54].

**Disadvantages:**

- Computationally intensive for a microcontroller,
- Requires an accurate model of the filter,
- Generally requires PLLs to give the accurate future estimations needed[29].

**3.5.5 Sinusoidal PWM Comparator**

A simple strategy for generating PWM waveforms is to compare a reference signal with a high frequency carrier signal, and switch the VSC legs based on the comparison[47]. If a saw-tooth carrier wave is selected, the resulting PWM pulses will be asymmetrical. A triangular carrier wave (as shown in Figure 3.11 on the facing page) will produce symmetrical PWM pulses, which is the preferred option as less harmonics are produced[43].

**Advantages:**

- Easier to implement than SVPWM,
- Over-modulation techniques allow increased utilisation of the DC bus.

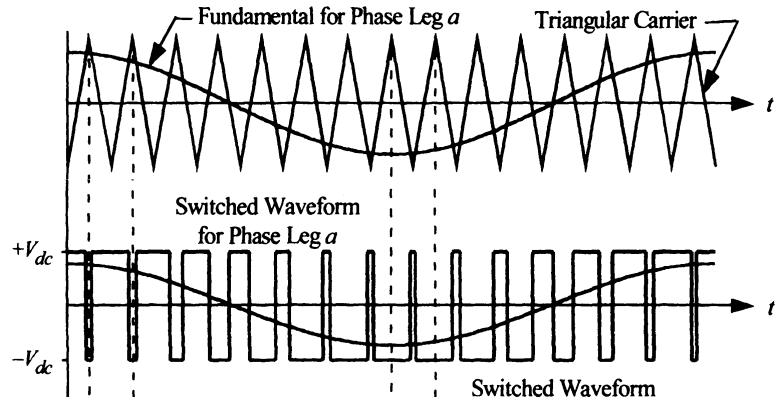


Figure 3.11: Sinusoidal PWM comparator carrier and control waveforms[43]

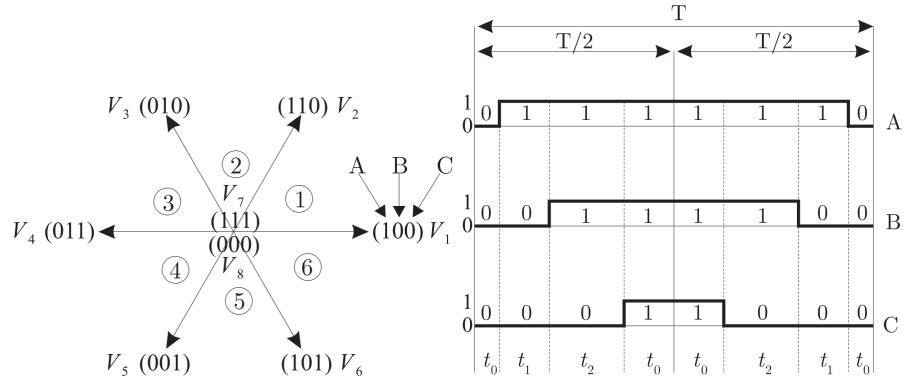


Figure 3.12: Space vector PWM hexagon and sector 1 switching pattern[36]

### Disadvantages:

- Lower modulation index than SVPWM[55],
- More suited to an analogue rather than digital implementation.

### 3.5.6 Space Vector PWM

The 8 switching switching combinations possible for a two-level VSC can be mapped spatially to a hexagon, with 6 vectors mapping to the vertices and the 2 zero vectors mapping to the centre of the hexagon[34]. Vectors within this hexagon can be synthesised using a pulse-centred PWM process with the switching vectors closest to the desired vectors[36]. The space vector hexagon and sector 1 switching times are shown in Figure 3.12. Space vector PWM is the voltage synthesis method used in this project, so a more in-depth analysis is provided in Section 5.6.3.

**Advantages:**

- Efficient utilisation of the DC bus voltage[56],
- Can produce vectors 15% larger than the previous carrier based sinusoidal PWM method[55],
- Highly suited to a digital implementation,
- Only one switching operation at a time.

**Disadvantages:**

- A 3rd harmonic component can be introduced when using the limit hexagon method[43],
- Computationally intensive.

### 3.6 Chapter Summary

This chapter discussed the use of VSC and CSC PWM converters for power processing, and explained the reasons why the VSC is the more popular choice. The two-level VSC was then examined and a basic outline of multilevel converters was provided.

Some practical limitations were introduced due to the non-idealities of the semiconductor switching devices. It was shown that these constraints limit the switching frequency, duty cycle and efficiency of VSCs.

Finally, comparisons of the 4 most common current control methods, and the 2 most common voltage synthesis methods were given. This comparison demonstrated that deadbeat current control combined with space vector pulse-centred PWM gives the best performance in terms of bandwidth, hardware utilisation and harmonic distortion minimisation.

## Chapter 4

# Instantaneous Power Theory

*The previous chapter introduced the VSC and discussed control methods to utilise the VSC as a current source. This chapter introduces ‘instantaneous power theory’, which underpins the entire operation of the Advanced STATCOM’s outer loop controller.*

### 4.1 Background of Instantaneous Power Theory

*Instantaneous power theory* involves a time-domain analysis of voltages and currents to determine instantaneous real and imaginary powers[32]. Since the theory is based on instantaneous voltages and currents, it is highly generalised and applies equally to both steady and transient states. The theory is therefore a very useful basis for designing controllers of high performance power conditioning devices.

A difference should be noted between real and imaginary components, compared with active and reactive components. The real and imaginary components are instantaneous values (calculated purely as a function of present inputs), whereas traditional definitions for active and reactive values refer to averages (calculated as a function of past and present inputs)[14]. Thus, real power may be considered to be instantaneous active power, and imaginary power may be considered to be instantaneous reactive power.

### 4.2 p-q Theory

The ‘p-q Theory’ is based on the power invariant Clarke transformation, which is a modification of the power variant transformation discussed in Section 2.5.1. The three-wire ( $v_0, i_0 = 0$ ) power invariant Clarke and inverse Clarke transformations are given in Equations 4.1 and 4.2

respectively:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (4.1)$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad (4.2)$$

The above equations are used for both current and voltage transformations.

A three-phase instantaneous active power,  $p_{3\phi}$ , is calculated from the instantaneous voltages and currents:

$$\begin{aligned} p_{3\phi}(t) &= v_a(t)i_a(t) + v_b(t)i_b(t) + v_c(t)i_c(t) \\ p_{3\phi} &= v_a i_a + v_b i_b + v_c i_c \end{aligned} \quad (4.3)$$

By using the power invariant Clarke transformation in Equation 4.1, it is possible to formulate Equation 4.3 in terms of  $\alpha\beta$  components:

$$\begin{aligned} p_{3\phi} &= v_a i_a + v_b i_b + v_c i_c \\ &= \sqrt{\frac{2}{3}}^2 \left( v_\alpha i_\alpha + \left( \frac{-1}{2}v_\alpha + \frac{\sqrt{3}}{2}v_\beta \right) \left( \frac{-1}{2}i_\alpha + \frac{\sqrt{3}}{2}i_\beta \right) + \left( \frac{-1}{2}v_\alpha - \frac{\sqrt{3}}{2}v_\beta \right) \left( \frac{-1}{2}i_\alpha - \frac{\sqrt{3}}{2}i_\beta \right) \right) \\ &= \frac{2}{3} \left( v_\alpha i_\alpha + \frac{1}{4}v_\alpha i_\alpha - \frac{\sqrt{3}}{4}v_\alpha i_\beta - \frac{\sqrt{3}}{4}v_\alpha i_\beta + \frac{3}{4}v_\beta i_\beta + \frac{1}{4}v_\alpha i_\alpha + \frac{\sqrt{3}}{4}v_\alpha i_\beta + \frac{\sqrt{3}}{4}v_\alpha i_\beta + \frac{3}{4}v_\beta i_\beta \right) \\ &= \frac{2}{3} \left( v_\alpha i_\alpha + \frac{1}{2}v_\alpha i_\alpha - \frac{\sqrt{3}}{2}v_\alpha i_\beta + \frac{3}{2}v_\beta i_\beta + \frac{\sqrt{3}}{2}v_\alpha i_\beta \right) \\ &= \frac{2}{3} \left( \frac{3}{2}v_\alpha i_\alpha + \frac{3}{2}v_\beta i_\beta \right) \\ p_{3\phi} &= v_\alpha i_\alpha + v_\beta i_\beta \end{aligned} \quad (4.4)$$

Further, the theory defines three instantaneous powers:

- the instantaneous real power,  $p$
- the instantaneous imaginary power,  $q$
- the instantaneous zero-sequence power,  $p_0$ .

Since a three-wire system is used in this project, there are no zero sequence components so  $p_0$  can be neglected. The instantaneous real power has been calculated in Equation 4.4, so only

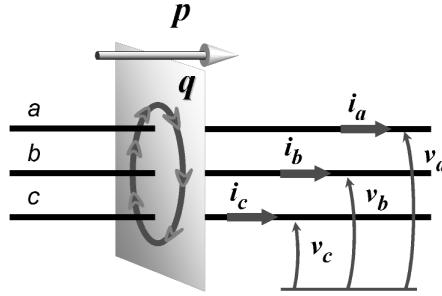


Figure 4.1: Physical meanings of the instantaneous real and imaginary powers[32]

the instantaneous imaginary power is not yet determined. This can be found by computing the instantaneous power using voltage and current vectors:

$$\begin{aligned} s &= vi^* \\ &= (v_\alpha + jv_\beta)(i_\alpha - ji_\beta) \\ s &= \underbrace{(v_\alpha i_\alpha + v_\beta i_\beta)}_p + j \underbrace{(v_\beta i_\alpha - v_\alpha i_\beta)}_q \end{aligned}$$

This can be expressed in matrix form as:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (4.5)$$

Comparing Equation 4.4 with Equation 4.5, it can be seen that  $p_{3\phi} = p$ , as expected.

Both real and imaginary powers are further decomposed into average and oscillating components, represented by  $\bar{p}, \bar{q}$  and  $\tilde{p}, \tilde{q}$  respectively:

$$\begin{array}{rcl} & \text{Average} & \text{Oscillating} \\ \text{Real Power: } p & = & \bar{p} + \tilde{p} \\ \text{Imaginary Power: } q & = & \bar{q} + \tilde{q} \end{array}$$

### 4.2.1 Physical Meanings of the Instantaneous Powers

The definition of real power is the instantaneous total energy flow per unit time (between subsystems). Conversely, imaginary power is defined to be proportional to the quantity of energy that is being exchanged between the phases of the system[57], as illustrated in Figure 4.1.

- **Average real power ( $\bar{p}$ ):** Represents the energy flowing per unit time in one direction only, from one subsystem to another,

- **Oscillating real power ( $\tilde{p}$ ):** Represents the energy flowing back and forth between the subsystems,
- **Average imaginary power ( $\bar{q}$ ):** Represents the energy being exchanged between the phases of the system in one direction only,
- **Oscillating imaginary power ( $\tilde{q}$ ):** Represents the energy flowing back and forth between the phases of the system[7].

It should be noted that the oscillating real and imaginary power are related to harmonics in the load current.

### 4.3 Using p-q Theory for Power Conditioning

It is possible to compensate non-ideal currents based on the components of real and imaginary power. Compensating the imaginary power requires no energy storage, as it is purely an exchange of power between phases[14]. Compensating on  $\tilde{p}$ , however, requires storage that can absorb and supply energy with a zero average value[16].

Compensating  $q$  provides power factor correction alone, as the fundamental reactive power is being supplied by the STATCOM instead of the source. Compensating  $\tilde{q}$  and  $\tilde{p}$  provides harmonic cancellation as all oscillating components are removed from the source current. Combining these two cases to compensate  $q$ ,  $\tilde{q}$  and  $\tilde{p}$  is the optimal case as it results in a purely sinusoidal source current that produces constant real power and zero imaginary power. The load therefore looks like an ideal, linear, purely resistive load. The source current has the minimum RMS value that transfers the same energy as the original load current that produces the average real power  $\bar{p}$ [58].

Once the selected powers to be compensated have been calculated, it is necessary to determine the reference currents based on these powers. Equation 4.5 provided the calculations to determine real and imaginary powers from the load currents, and rearranging this gives an equation to calculate the  $\alpha\beta$  currents for a given pair of real and imaginary powers:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \quad (4.6)$$

The  $\alpha\beta$  currents can then be used directly as a reference to a deadbeat current control scheme, or an inverse Clarke transformation can be carried out to obtain the phase currents for alternative current control schemes that operate on  $abc$  components.

## 4.4 Voltage Measurements in a Three-Wire System

In a three-wire system it is reasonable to question what the reference is for the phase voltages in Equation 4.3. It is shown here that this reference point can be set arbitrarily and the instantaneous active power calculated remains the same:

$$\begin{aligned}
 p_{3\phi} &= v_{ax}i_a + v_{bx}i_b + v_{cx}i_c \\
 &= (v_a - v_x)i_a + (v_b - v_x)i_b + (v_c - v_x)i_c \\
 &= v_a i_a - v_x i_a + v_b i_b - v_x i_b + v_c i_c - v_x i_c \\
 &= v_a i_a + v_b i_b + v_c i_c - v_x (i_a + i_b + i_c) \\
 &= v_a i_a + v_b i_b + v_c i_c - v_x \times 0 \\
 p_{3\phi} &= v_a i_a + v_b i_b + v_c i_c
 \end{aligned}$$

Thus for a three-wire system, the final result is independent of  $v_x$  and so the reference point for the voltages is irrelevant as long as all voltages are measured with respect to the same point.

Rather than arbitrarily picking a reference point for the voltage measurements, better engineering practice is to take phase-to-phase voltage measurements ( $v_{ab}$ ,  $v_{bc}$ ,  $v_{ca}$ ) and use these to obtain phase-to-neutral voltage measurements ( $v_{an}$ ,  $v_{bn}$ ,  $v_{cn}$ ). Since the STATCOM is designed for a three-wire system, there are no zero sequence components and thus  $v_{an} + v_{bn} + v_{cn} = 0$ .

Determining the relationship between phase-to-phase and phase-to-neutral measurements:

$$\begin{aligned}
 v_{ab} - v_{ca} &= (v_{an} - v_{bn}) - (v_{cn} - v_{an}) \\
 &= 2v_{an} - (v_{bn} + v_{cn}) \\
 &= 2v_{an} - (-v_{an}) \\
 v_{ab} - v_{ca} &= 3v_{an}
 \end{aligned} \tag{4.7}$$

By rearranging Equation 4.7 and performing the same calculations for other phases, the following results can be obtained:

$$\begin{aligned}
 v_{an} &= \frac{v_{ab} - v_{ca}}{3} \\
 v_{bn} &= \frac{v_{bc} - v_{ab}}{3} \\
 v_{cn} &= \frac{v_{ca} - v_{bc}}{3}
 \end{aligned}$$

The above results hold true even when the voltages are unbalanced as a result of the presence of negative sequence components.

## 4.5 Chapter Summary

This chapter introduced p-q Theory as a method of analysing power systems with the aim of improving power quality. Distinctions were made between real and imaginary powers, compared with active and reactive powers, to highlight the instantaneous nature of the theory.

Using Clarke transformations, mathematical equivalences were established between three-phase values and  $\alpha\beta$  values to calculate real and imaginary powers. The physical meanings of these powers were then explained, to distinguish between energy exchanged between phases, and energy exchanged between subsystems.

It was then shown how power factor correction and harmonic cancellation could be achieved by forming reference currents based on the average imaginary power, and the oscillating real and imaginary powers.

## Chapter 5

# Controller Design of the Advanced STATCOM

*The previous chapters introduced the VSC as a fundamental building block for many power electronics devices, and p-q Theory as the basis for the Advanced STATCOM controller. This chapter details the development of the control scheme for the VSC to form the Advanced STATCOM.*

### 5.1 Fundamentals of the Advanced STATCOM

The scenario that forms the basis of this project is illustrated in Figure 5.1 on the next page.

The STATCOM provides both active harmonic filtering and reactive power control for the purpose of power factor correction. To provide this functionality, the inputs to the control must include:

- **Point of common coupling voltages** for current control and power factor correction purposes,
- **Load currents** for power factor correction (reactive current) and harmonic filtering (harmonic currents),
- **STATCOM output currents** for current control,
- **DC bus voltage** for DC bus voltage regulation.

The final outputs from the STATCOM controller are the six control signals to drive the power electronic switching devices in the VSC to produce a square voltage at each phase terminal of

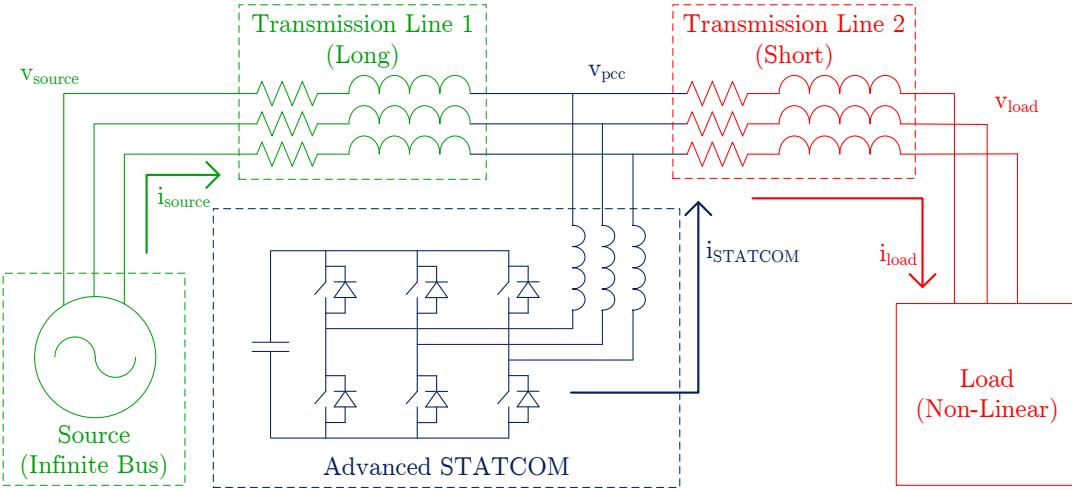


Figure 5.1: STATCOM test power system

the VSC. Inductive filters need to be connected between the VSC legs and the point of common coupling in order to smooth the currents that flow into or out of the STATCOM.

Figure 5.2 on the facing page provides a high level block diagram to give an overview of the Advanced STATCOM controller. It can be seen that the overall controller can be divided into the outer loop controller and the inner loop controller:

- **Outer loop controller:** Generates the reference currents to achieve the overall STATCOM objectives of power factor correction and harmonic cancellation. A block diagram of the outer loop controller is shown in Figure 5.3 on the next page,
- **Inner loop controller:** The current controller aims to generate the switching signals to force the STATCOM output currents to track the reference currents provided by the outer loop controller. A block diagram of the inner loop controller is shown in Figure 5.6 on page 50.

The remainder of this chapter examines each of the key blocks within the outer and inner loop controllers:

- Voltage regulation of the DC bus,
- Extraction of fundamental and harmonic frequency components using PLLs,
- Power factor correction,
- Harmonic filtering,
- Current controller (including output filter design, deadbeat algorithms and SVPWM).

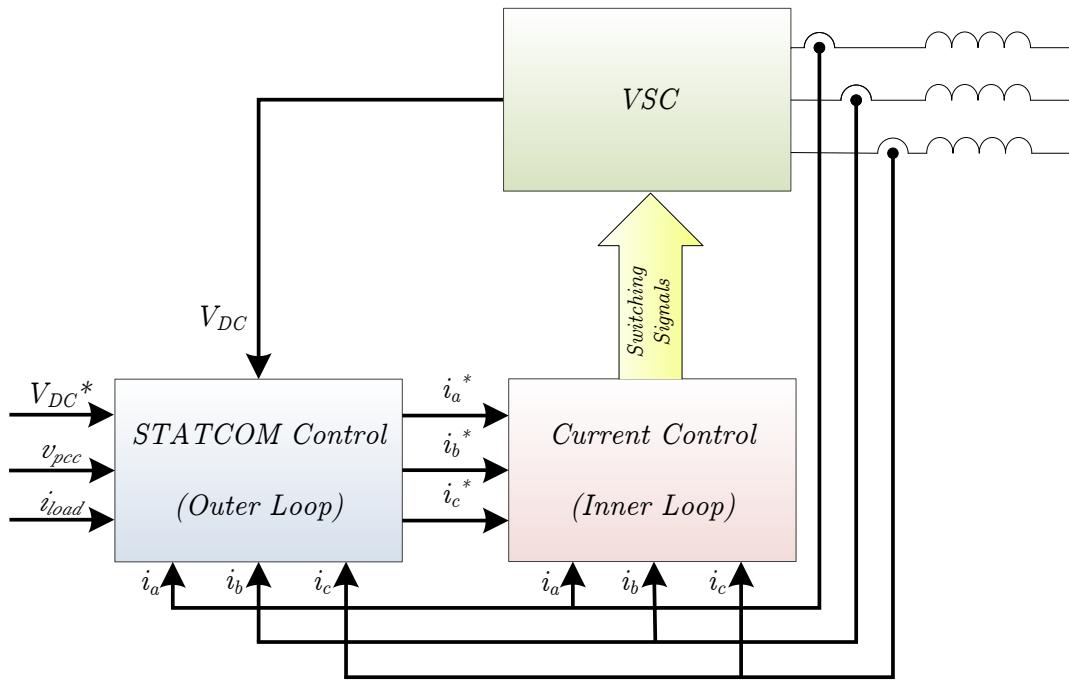


Figure 5.2: High level control block diagram for the Advanced STATCOM

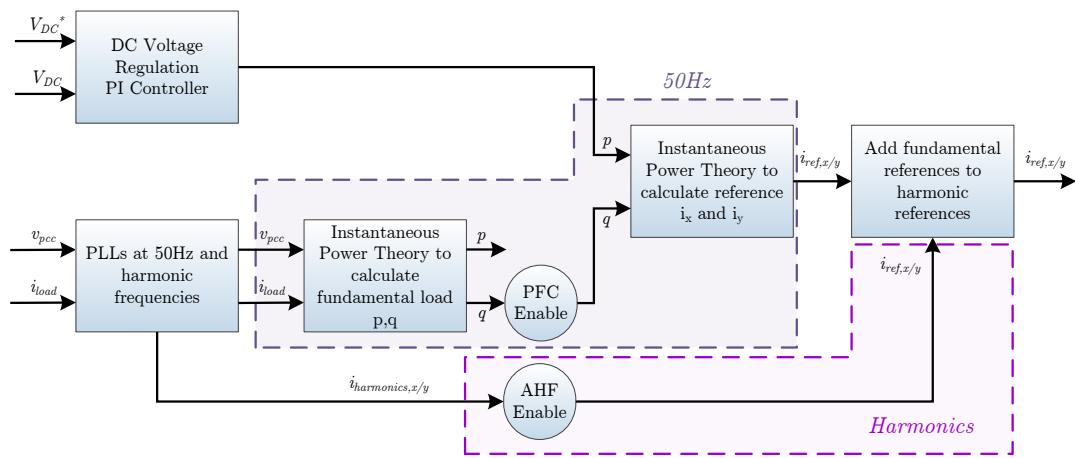


Figure 5.3: Block diagram of outer loop control

## 5.2 Voltage Regulation of the DC Bus

Though the STATCOM is used to provide harmonic and reactive power (which average no real power), there is still some real power consumption due to the losses in the various components of the VSC and inherent resistance of the output filter. For this reason, the STATCOM must draw a level of real power from the network in order to maintain the voltage of the DC bus. A design consideration is the size of the capacitors used for the DC bus, which affects both cost and performance. Larger capacitors are more expensive, however, they provide better regulation, reduce variations during transients and can store more real power for the filtering of harmonics[59]. The aim when designing the converter is to use the smallest capacitance necessary to store the energy in the real power oscillations of the harmonics.

To achieve voltage regulation, a reference DC bus voltage must be selected as the PI controller reference. For stable operation, the DC bus voltage is typically selected to be  $1.5 \times$  nominal AC peak-to-peak RMS voltage[53, 60]. Lower DC bus voltages do not provide sufficient overhead for the STATCOM to output the necessary voltages for stable operation. Conversely, higher DC bus voltages allow the VSC to output larger voltages, however, to synthesise smaller voltages (which are more common) the converter operates at relatively low duty cycles, reducing the utilisation of the entire duty cycle range[43]. Additionally, by operating at lower duty cycles, the impacts of dead time outlined in Section 3.4 become more apparent.

As the DC bus voltage drops below the reference value, the STATCOM must draw real power from the network to charge the bus capacitor and boost the DC voltage. Conversely, as the DC bus voltage increases about the reference value, the STATCOM must export real power to the network to discharge the bus capacitor and decrease the DC voltage.

The reference power,  $p$ , generated by the PI controller can be used to determine reference currents by using the inverse power transformation given in Equation 4.6 (which is restated below for convenience). The  $q$  component comes from the power factor correction block, which is later discussed in Section 5.4.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix}$$

The output of the PI controller forms the real power reference in p-q Theory which can then be used to calculate the reference currents for the inner control loop.

## 5.3 Extraction of Fundamental and Harmonic Frequency Components

One of the most complex and difficult aspects of the STATCOM controller is the challenge of identifying and isolating the fundamental component and each of the harmonic components to be compensated. This process needs to be fast, accurate and highly selective in order to enable

proper cancellation of the specified harmonics[54]. This section involves a brief overview of some common harmonic detection methods, followed by an in-depth analysis of the selected method, including simulations.

### 5.3.1 Methods for Selective Frequency Extraction

There are several methods of fundamental and harmonic extraction, which can be broadly classed into frequency-domain or time-domain methods[61].

Frequency-domain methods include using a fast Fourier transform (FFT) or discrete Fourier transform (DFT) to obtain the frequency spectrum[59].

Time-domain methods include synchronous fundamental dq-frame, synchronous harmonic dq-frame, PLLs in a parallel structure, and PLLs in a cascade structure[62].

PLLs in a parallel structure have the advantage that each frequency's PLL operates completely independently of the others. The input to all PLLs is the “raw” load current, and each PLL outputs only the component of the load current at the specified frequency. The disadvantage to this system, however, is that for the higher order harmonics, the desired harmonic signal is very small compared with the input signal, causing difficulties in locking and isolating the signal[27]. For example, the 7th harmonic may have an amplitude of 1A, while the fundamental has an amplitude of 15A, resulting in a very poor signal-to-noise ratio (SNR).

By placing PLLs in a cascaded (series) structure, with the lower frequency (larger amplitude) PLLs coming first, followed by the other frequencies in order of increasing harmonic number (decreasing amplitude), this issue can be mitigated[63]. The fundamental frequency PLL inputs the unfiltered load current, and outputs the 50Hz component of the load current. The input to the next PLL is the unfiltered load current with the 50Hz component subtracted, greatly increasing the SNR to improve the PLL performance. This continues throughout the cascade structure, with the input to each successive PLL being the original load current with the upstream PLL outputs removed. The main drawback to a structure like this is that the performance of downstream PLLs is dependent on the upstream PLLs, which could possibly cause locking delays during large transients. Overall, this is the harmonic extraction method that delivers the best performance and it is therefore used in this project.

### 5.3.2 Phase-Locked Loop Design and Simulation

In order to design and analyse the PLL, an efficient method of simulation and testing is needed, where a variety of input signals can be easily generated to study the effects of distorted conditions. These distorted conditions may include higher levels harmonics (that aren't being filtered), deviations of the supply frequency away from the nominal value, and unbalance due to the presence of negative sequence components[64].

The PLL functions are written in C++ so that they can be used in the hardware controller implementations with minimal modifications. Using the Saber platform to test the functions with a variety of inputs would be very inflexible, so a different approach is required. To overcome these issues a DLL file is generated from the C++ code, and a Python script is written to interface with this DLL file. Though time-consuming to set up initially, the script allows simulations to be carried out quickly, and modifications to the C++ code and/or Python script can be made easily. The actual PLL code written in this section is completely identical to the code that is later used in the hardware implementation - the only difference being that in this implementation the inputs come from the Python script, whereas in the hardware implementation the inputs come from current sensors.

Once the PLL gives satisfactory performance at the fundamental frequency alone, the harmonics also need to be extracted. Though PLLs are highly selective, the presence of significant amounts of noise can cause issues when attempting to lock on to the desired signal. For example, the fundamental frequency signal may be 20 times bigger than the 7th harmonic which the PLL is attempting to track. The method chosen to overcome this problem involves cascaded PLLs, where the input to successive PLLs has had the previous PLL signals removed. The input to the first PLL (fundamental frequency) is the total input signal, however, the input to the second PLL (5th harmonic) is the total input signal with the fundamental frequency removed. The disadvantage of this system is that the “upstream” PLLs must be locked before the “downstream” PLLs can lock, which can possibly cause locking delays during large transients.

Figure 5.4 on the next page shows the final results of the PLL system designed. The top, middle and bottom graphs show the fundamental, 5th, and 7th harmonic PLLs respectively. The blue and dark green signals are the generated inputs, and the red and light green signals are the PLL outputs. It is clear that the PLLs are accurately tracking the inputs, with minimal steady-state error.

### 5.3.3 Novel Karimi-Ghatemani Phase-Locked Loop

An alternative method of harmonic extraction was investigated which used single-phase PLLs instead of three-phase PLLs. A novel adaptation of the Karimi-Ghatemani PLL was designed and tested which provided significant performance benefits over the traditional PLL in the presence of harmonics. The PLL structure contains a gain component which affects the transient and steady-state performance[65]. A high gain will amplify errors in transient states to cause the PLL to shift faster and re-lock in a shorter period of time[65]. A negative impact this causes is in steady-state when the error caused through the presence of harmonics is amplified, as this presents a ripple on the output. To overcome these issues and take advantage of both the high and low gain scenarios, a dynamic gain PLL was designed. By using a basic low-pass filter to reduce harmonics, an estimation of the error can be obtained. When the error is large, a transient condition is assumed and hence, the gain in the PLL is increased. As the error signal

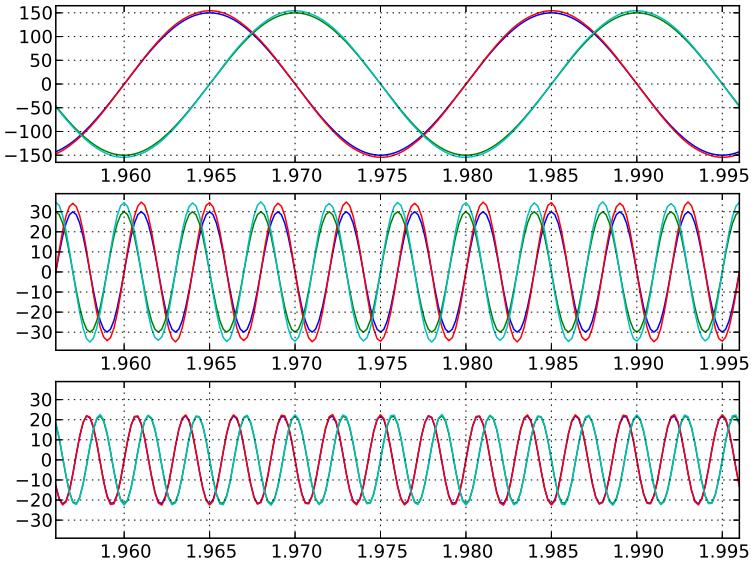


Figure 5.4:  $\alpha\beta$  components of fundamental, 5th, and 7th harmonics: Generated input vs. PLL output

becomes smaller, it is assumed that the output is locked to the input correctly, and the gain term reduces.

An example is provided where the fundamental frequency component has a magnitude of 20V and the 5th harmonic component has a magnitude of 5V. The results of this are shown in Figure 5.5 on the following page, where the magnitude output of the PLL is shown for 3 different scenarios. The low gain PLL output (green) shows a long time to reach the actual value, though presents a small steady-state ripple. Conversely, the high gain PLL output (red) shows a very fast response, however, the presence of harmonics causes a large steady-state ripple. The novel dynamic gain PLL output (blue) demonstrates the fast response time of the high gain PLL combined with the small steady-state ripple of the low gain PLL. Despite this significant improvement in PLL performance, the three-phase PLL structure in the previous section was chosen due to the computational efficiency of using 1 PLL instead of 3 PLLs, and the ability to provide positive sequence detection with ease[66, 67].

## 5.4 Power Factor Correction

Power factor correction is achieved by providing the fundamental frequency reactive power demands of the load, so that only real power flows through the transmission network to the

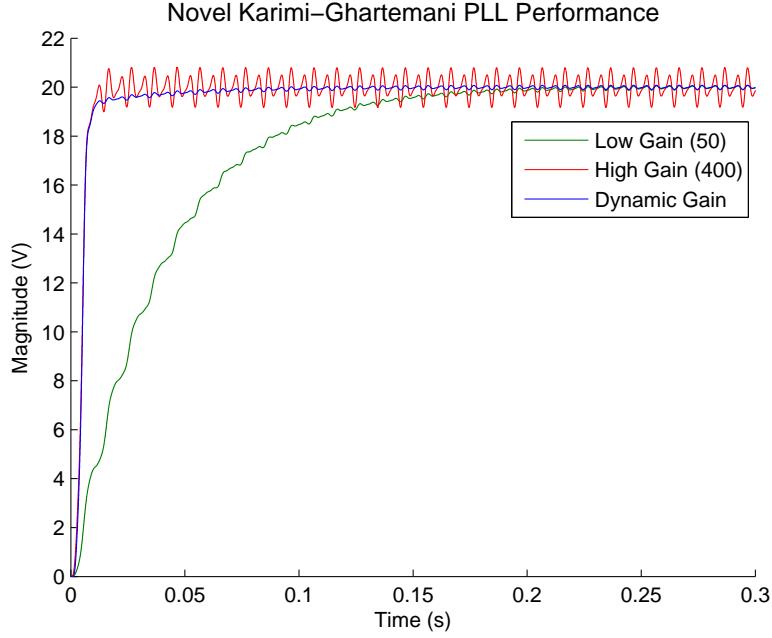


Figure 5.5: Karimi-Ghartermani PLL performance: low gain, high gain and dynamic gain

STATCOM connection point[19].

In order to achieve this, the fundamental frequency component of the load current may be decomposed into real and imaginary parts, which are in phase with the voltage, and 90 degrees out of phase with the voltage respectively. If the imaginary component of the load current is provided at the load terminals itself, then only the real component must be provided through the transmission network.

The most common method to separate the real and imaginary components involves the Park transform ( $abc$  to  $dq$ ), where the angle used for the transformation is the angle of the voltage at the point of common coupling, usually estimated by a PLL[68]. In this method, the  $q$ -axis component represents the imaginary current, and the  $d$ -axis component represents the real current. This  $q$ -axis component may be used as the input to a PI controller which then forms a reference for the current control loop.

This method produces excellent results in steady-state conditions, however, the inclusion of a PI controller impacts on transient performance[51]. Additionally, this project deals with the presence of harmonics and this significantly impacts steady-state performance as the  $q$ -axis component is no longer constant, but will have oscillations from the harmonic components. These two problems leave this method unable to satisfy the performance objectives of the STATCOM designed in this project.

To improve on the shortcomings of this Park transformation-based method, an alternate method based on p-q Theory can be utilised. As discussed in Chapter 4, instantaneous real and imaginary

powers can be calculated using Equation 4.5 on page 37. In a scenario without any harmonics, this method would provide outstanding performance as the p and q calculated would be equal to the fundamental real and imaginary powers, and thus reference currents could be calculated based on the imaginary power of the load. This method would also have excellent performance in transient conditions, as the calculated powers are purely a function of present inputs[32]. However, since this project deals with harmonic load currents too, the calculated real and imaginary powers will have oscillating components and therefore cannot be directly used for power factor correction, as power factor correction deals only with fundamental frequencies. This problem can be overcome through the use of a low-pass filter which can separate the calculated powers into their fundamental and harmonic components. It is then possible to use the fundamental imaginary power to calculate reference currents for the inner current control loop. Another problem arises, however, as the use of a low-pass filter introduces inherent delays which impact on both steady-state and transient performance[48].

Thus, a novel adaptation of p-q Theory was developed to meet the high steady-state and transient performance goals of the STATCOM. To obtain the fundamental frequency real and imaginary powers without the need for a low-pass filter, the power calculations must be performed with inputs that contain no harmonic components. To achieve this, PLL filters are used to obtain the 50Hz component of the voltages and currents which will then be used to determine the fundamental frequency real and imaginary power. As discussed in Section 4.3, the imaginary component of this power can be used to calculate reference currents for the current controller to achieve power factor correction using Equation 4.6 on page 38. As well as outstanding steady-state and transient performance, the use of PLLs provides an additional benefit which will become apparent in the discussion of the deadbeat current controller, where accurate future estimations provide optimal operation.

Instead of using the power invariant Clarke (and inverse) transformation usually used with p-q Theory, this controller uses the power variant transformation. The reason for this is to provide a computational advantage as the use of square root functions is removed. To allow generated references to be the same however, a scaling factor of 1.5 is used to account for the different constants:

$$\frac{3/2 \times 3/2}{\sqrt{3/2} \times \sqrt{3/2}} = 1.5$$

## 5.5 Harmonic Filtering

A typical method of reference generation for active harmonic filters comes from the use of high-pass filters combined with either the Park transform or p-q Theory[32]. The use of high-pass filters introduces delays which negatively impacts on both steady-state and transient performance. A modification of p-q Theory has been developed for the STATCOM to give significant benefits, in both performance and functionality.

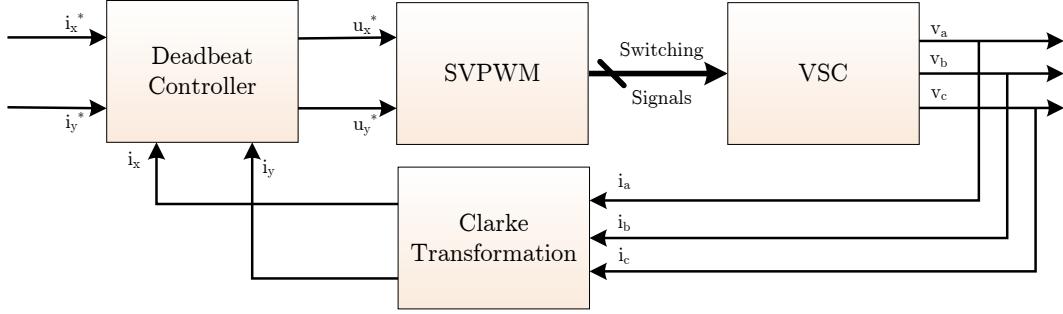


Figure 5.6: STATCOM current control loop

By using the PLLs discussed in Section 5.3, very significant performance gains can be made during both steady and transient states by removing the inherent delays introduced by high-pass filters. The other major source of increased performance is the ability of PLLs to provide accurate estimations of future currents. These benefits will become apparent when the deadbeat current controller is studied.

The functionality benefits arise from the PLLs at each harmonic frequency of interest, allowing independent control over which harmonics are filtered, and to what degree they are filtered. The traditional method of using a high-pass filter to separate the harmonics from the fundamental frequency provides no selectivity over individual harmonics. By carrying out the p-q Theory calculations on each harmonic frequency of interest, reference currents can be determined and summed with the previous reference currents (from DC bus regulation and power factor correction).

The active harmonic filtering in this project compensates for both the real and imaginary power, and so a more computationally efficient method involves simply summing the PLL estimated currents with the previously calculated reference currents. The process of extracting these harmonics has been previously covered in Section 5.3.

## 5.6 STATCOM Current Controller

As discussed in Section 3.5, the voltage source converter can be controlled to effectively act as a current source. Figure 5.6 presents the block diagram for the STATCOM's current controller which consists of a deadbeat controlled SVPWM scheme utilising an inductive output filter. These elements are further explored in the following subsections.

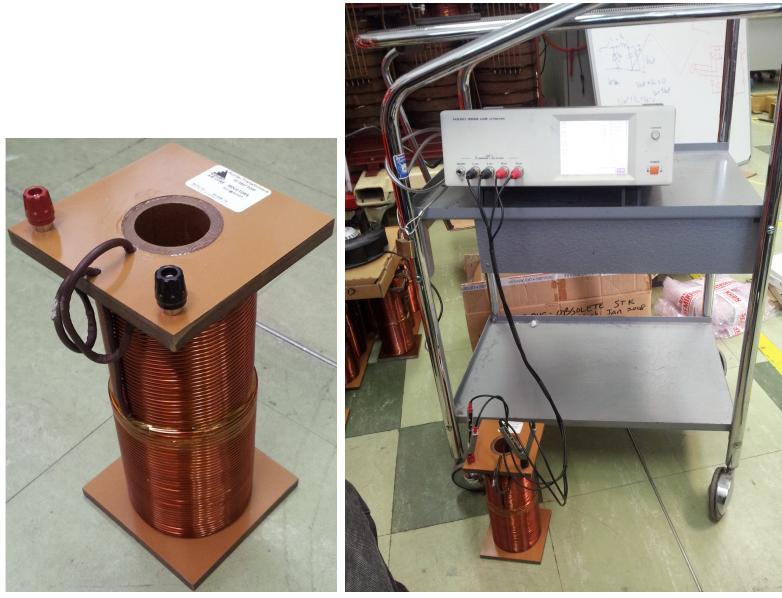


Figure 5.7: 5mH inductor and LCR testing

### 5.6.1 STATCOM Output Filter

The electrical grid voltages have a sinusoidal shape, however the phase voltage outputs of the voltage source converter are square waves. To connect the two, an output filter should be used which smooths the current flow and allows the converter to act as a controllable current source.

There are many possible output filter topologies including L filters, LC filters, LCL filters or even transformers in high voltage applications[50]. LC and LCL filters offer slightly improved current smoothing capabilities, however, they introduce potentially damaging resonances into the system[59]. LCL filters typically also require additional voltage measurements in the filter for deadbeat control purposes[59]. For these reasons, a purely inductive output filter was chosen for this project.

The sizing of the filter inductor is a trade-off between reducing switching noise and harmonic tracking ability. A larger inductor provides greater smoothing of the output currents, which reduces the switching noise present in the grid. If the level of inductance is too high however, the output currents may not be able to change fast enough which could limit the ability to control higher order harmonics[69]. Larger inductors are typically created by adding windings around a core, which also increases the resistance and hence real power losses.

The inductors used in this project are shown in Figure 5.7.

The rated inductance of these inductors is  $5mH$ , and ideally they will have no resistance. Upon measurement with an LCR meter the actual inductance was found to be approximately  $5.2mH$  with a winding resistance of  $0.37\Omega$ . The per-phase transfer function of the output filter which

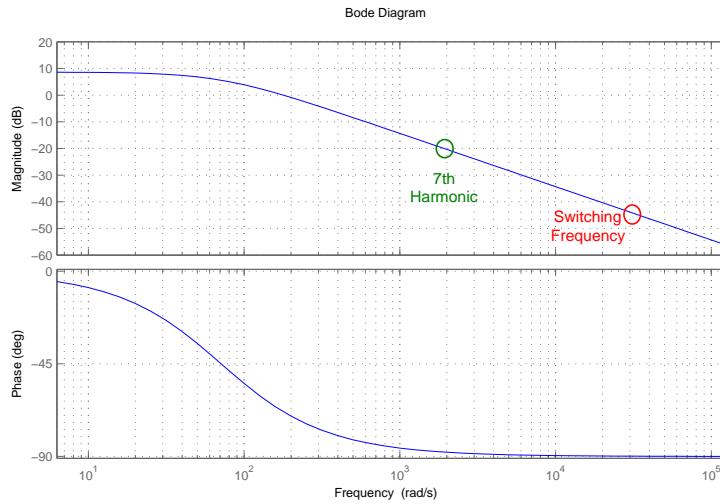


Figure 5.8: Bode plot of filter indicating highest harmonic and switching frequency

relates current to voltage can be found as follows:

$$\begin{aligned} V &= IZ \\ \frac{I}{V} &= \frac{1}{Z} \\ \frac{I}{V} &= \frac{1}{R + jwL} \\ H(s) &= \frac{1}{R + sL} \end{aligned}$$

The bode plot of this filter is shown in Figure 5.8 and demonstrates the large attenuation of the 5kHz switching frequency compared to the highest frequency harmonic of 350Hz.

### 5.6.2 Deadbeat Predictive Control

*Deadbeat predictive control*, or simply deadbeat control, involves determining the optimal input signal that will bring the output to a desired value in the minimum number of time steps[70]. The response to deadbeat control has the following characteristics:

- zero steady-state error,
- minimum rise time,
- minimum settling time,
- minimal overshoot/undershoot,

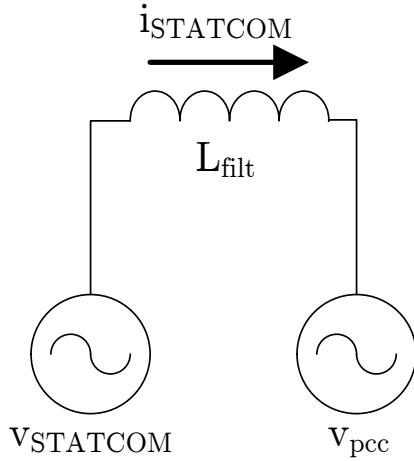


Figure 5.9: Simplified model of the deadbeat system

- very high control signal output[29].

It is necessary to create a model of the system in order to determine the deadbeat control algorithms. A simplified model of the system is shown in Figure 5.9, with the STATCOM and point of common coupling both being represented by voltage sources. The deadbeat control equations will give the STATCOM voltages that need to be applied in order to make the desired current flow from the STATCOM to the point of common coupling. The equations can be derived by considering the differential equation describing an inductor:

$$v = L \frac{di}{dt}$$

Converting to discrete time:

$$\begin{aligned} v_L &= L \frac{\Delta i}{\Delta t} \\ v_{STATCOM} - v_{pcc} &= L \frac{\Delta i}{\Delta t} \\ v_{STATCOM} &= L \frac{\Delta i}{\Delta t} + v_{pcc} \end{aligned}$$

The time difference being considered is the control period,  $T_s$ , and  $\Delta i$  is the change in current desired over this period. The aim of the deadbeat controller in this project is to reach the desired current,  $i^*$  by the end of each control interval, so the  $\Delta i$  must be  $i^*$  (at the end of the control interval) minus  $i_{measured}$  (at the start of the control interval), giving:

$$v_{STATCOM} = L \frac{i^*[k+1] - i_{measured}[k]}{T_s} + v_{pcc}$$

The point of common coupling voltage will vary slightly over the control interval, however, a single value must be used for the deadbeat algorithms. The most accurate and commonly used value, is the value at the middle of the control interval,  $v_{pcc}[k + 0.5]$ . This will give an expression for the average voltage that must be applied during the entire control interval:

$$\begin{aligned} v_{STATCOM}[k, k+1] &= L \frac{i^*[k+1] - i_{measured}[k]}{T_s} + v_{pcc}[k, k+1] \\ v_{STATCOM}[k, k+1] &= \frac{L}{T_s} (i^*[k+1] - i_{measured}[k]) + v_{pcc}[k+0.5] \end{aligned} \quad (5.1)$$

Now the above equation is technically correct, however this deadbeat controller could not be practically implemented in its current form due to causality limitations. This is because the calculations for the STATCOM output voltage during the period  $[k, k+1]$  cannot include the value,  $v_{pcc}[k+0.5]$ , as it will not have occurred at the time the calculations are being executed. In fact, even  $i_{measured}[k]$  cannot be included, as the sampling process and calculations take some finite amount of time, and hence must be carried out prior to the start of the period  $[k, k+1]$ . Since the controller updates once per control interval, all calculations are made during the interval  $[k-1, k]$  and can include measurements up to  $[k-1]$  only.

The use of PLLs in the outer loop controller provides an elegant solution to the  $v_{pcc}$  causality problem. The PLLs in this project are designed in such a way that they are able to generate future estimations, which are significantly more accurate than estimations provided by other methods such as linear or quadratic extrapolation. Therefore, a highly accurate value for  $v_{pcc}[k+0.5]$  can be determined at  $v_{pcc}[k-1]$ .

The remaining issue is how to determine  $i_{measured}[k]$ . Unfortunately, this cannot be estimated in the same way as  $v_{pcc}$ , since PLLs are not used on the STATCOM output current. Implementing PLLs simply for this purpose would generally not be possible due to the computational limitations of most microprocessor systems. In fact, PLLs are not needed at all as  $i_{measured}[k]$  can be estimated quite accurately using the same inductor differential equation:

$$\begin{aligned} v_L &= L \frac{\Delta i}{\Delta t} \\ v_{STATCOM}[k-1, k] - v_{pcc}[k-1, k] &= L \frac{i[k] - i[k-1]}{T_s} \\ v_{STATCOM}[k-1, k] - v_{pcc}[k-0.5] &= L \frac{i[k] - i[k-1]}{T_s} \\ \frac{T_s}{L} (v_{STATCOM}[k-1, k] - v_{pcc}[k-0.5]) &= i[k] - i[k-1] \\ i[k] &= \frac{T_s}{L} (v_{STATCOM}[k-1, k] - v_{pcc}[k-0.5]) + i[k-1] \end{aligned} \quad (5.2)$$

Note that the above value of  $i[k-1]$  can be used in the calculation, and the value of  $v_{STATCOM}[k-1, k]$  is also known as it is the applied voltage for the  $[k-1, k]$  interval that was calculated in the

Vector	Switching Pattern			Phase-to-Neutral Voltages			Phase-to-Phase Voltages		
	Leg A	Leg B	Leg C	$V_{AN}$	$V_{BN}$	$V_{CN}$	$V_{AB}$	$V_{BC}$	$V_{CA}$
$V_0$	0	0	0	0	0	0	0	0	0
$V_1$	0	0	1	$-1/3V_{DC}$	$-1/3V_{DC}$	$2/3V_{DC}$	0	$-V_{DC}$	$V_{DC}$
$V_2$	0	1	0	$-1/3V_{DC}$	$2/3V_{DC}$	$-1/3V_{DC}$	$-V_{DC}$	$V_{DC}$	0
$V_3$	0	1	1	$-2/3V_{DC}$	$1/3V_{DC}$	$1/3V_{DC}$	$-V_{DC}$	0	$V_{DC}$
$V_4$	1	0	0	$2/3V_{DC}$	$-1/3V_{DC}$	$-1/3V_{DC}$	$V_{DC}$	0	$-V_{DC}$
$V_5$	1	0	1	$1/3V_{DC}$	$-2/3V_{DC}$	$1/3V_{DC}$	$V_{DC}$	$-V_{DC}$	0
$V_6$	1	1	0	$1/3V_{DC}$	$1/3V_{DC}$	$-2/3V_{DC}$	0	$V_{DC}$	$-V_{DC}$
$V_7$	1	1	1	0	0	0	0	0	0

Table 5.1: Space vector combinations for a three-phase VSC

period before.

Substituting Equation 5.2 into Equation 5.1 and simplifying, the final, causal deadbeat algorithm is obtained:

$$v_{STATCOM} [k, k+1] = \frac{L}{T_s} (i^* [k+1] - i [k-1]) + v_{pcc} [k+0.5] + v_{pcc} [k-0.5] - v_{STATCOM} [k-1, k]$$

To summarise, this is the expression for the average voltage that must be applied by the STATCOM during the  $[k, k+1]$  interval to ensure that the output current reaches its desired value by the end of the control interval. Once this applied voltage has been calculated, the voltage source converter needs some way to synthesise it. This is discussed in the following section on space vector PWM.

It should be noted that the deadbeat algorithm ignores the resistance of the filter. This generally has no effect on the overall performance of the controller as the resistance is typically negligible. The sensitivity of the deadbeat algorithm to the inductance is also quite low[52]. If the inductance is underestimated there will be a slight decrease in performance as the voltage applied won't be sufficient to achieve the end-of-interval target current, however, this effect is not compounded as the actual currents are measured and fed back into the controller. The main issue with parameter sensitivity comes of the inductance is overestimated, producing larger than necessary voltages which can lead to instabilities in the controller[69].

### 5.6.3 Space Vector Pulse Width Modulation

The inverter can be controlled with *space vector modulation* (SVM) to operate a pulse-centred pulse width modulation switching scheme. This entire process, called space vector pulse width modulation (SVPWM), is an algorithm for the control of PWM used to generate AC waveforms[71]. As discussed in Section 3.2, for a three-phase two-level there are  $2^3$  legitimate switching states, which generate voltage space vectors  $V_0$  to  $V_7$ , as shown in Table 5.1. Also shown in this table are the equivalent phase-to-neutral voltages and phase-to-phase voltages of each state.

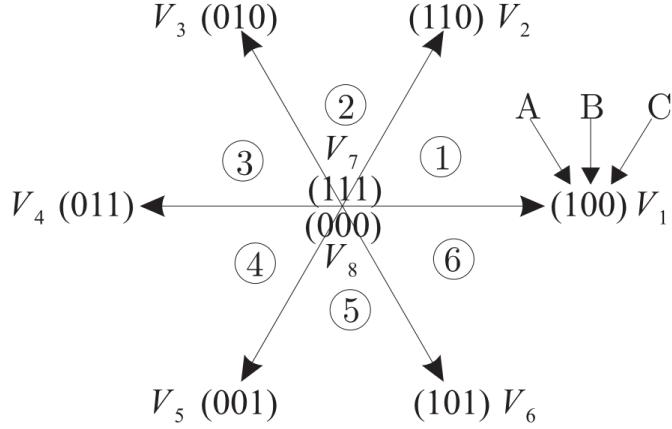


Figure 5.10: Graphical Representation of the Space Vectors[36]

Figure 5.10 shows a graphical representation of the 8 possible switching vectors. Note that although there are only 8 switching patterns, vectors can be formed anywhere in the 6 sectors by switching between the 8 available states to form an average vector. By utilising this PWM process, it is possible to create voltage and current vectors that rotate in time[34].

The space vector PWM scheme is a symmetrical scheme which provides lower harmonic distortion compared with asymmetrical PWM methods[43].

Table 5.2 shows a summary of the switching times and the switching order for the voltage vectors for each sector[36]. A derivation of these switching times is provided in Section A.1.

Sector	Switching Order	$t_0$	$t_1$	$t_2$
1	$V_0 V_1 V_2 V_7 V_7 V_2 V_1 V_0$	$\frac{T}{4} \left( 1 - \alpha - \frac{\beta}{\sqrt{3}} \right)$	$\frac{T}{2} \left( \alpha - \frac{\beta}{\sqrt{3}} \right)$	$\frac{\beta T}{\sqrt{3}}$
2	$V_0 V_3 V_2 V_7 V_7 V_2 V_3 V_0$	$\frac{T}{4} \left( 1 - \frac{2\beta}{\sqrt{3}} \right)$	$\frac{T}{2} \left( -\alpha + \frac{\beta}{\sqrt{3}} \right)$	$\frac{T}{2} \left( \alpha + \frac{\beta}{\sqrt{3}} \right)$
3	$V_0 V_3 V_4 V_7 V_7 V_4 V_3 V_0$	$\frac{T}{4} \left( 1 + \alpha - \frac{\beta}{\sqrt{3}} \right)$	$\frac{\beta T}{\sqrt{3}}$	$\frac{T}{2} \left( -\alpha - \frac{\beta}{\sqrt{3}} \right)$
4	$V_0 V_5 V_4 V_7 V_7 V_4 V_5 V_0$	$\frac{T}{4} \left( 1 + \alpha + \frac{\beta}{\sqrt{3}} \right)$	$\frac{-\beta T}{\sqrt{3}}$	$\frac{T}{2} \left( -\alpha + \frac{\beta}{\sqrt{3}} \right)$
5	$V_0 V_5 V_6 V_7 V_7 V_6 V_5 V_0$	$\frac{T}{4} \left( 1 + \frac{2\alpha}{\sqrt{3}} \right)$	$\frac{T}{2} \left( -\alpha - \frac{\beta}{\sqrt{3}} \right)$	$\frac{T}{2} \left( \alpha - \frac{\beta}{\sqrt{3}} \right)$
6	$V_0 V_1 V_6 V_7 V_7 V_6 V_1 V_0$	$\frac{T}{4} \left( 1 - \alpha + \frac{\beta}{\sqrt{3}} \right)$	$\frac{T}{2} \left( \alpha + \frac{\beta}{\sqrt{3}} \right)$	$\frac{-\beta T}{\sqrt{3}}$

Table 5.2: Switching Details for Each Sector for SVPWM

By using the switching orders shown in Table 5.2, the pulse-centred PWM scheme also guarantees the application of the ‘000’ vector at the start of every interval and the ‘111’ vector at the midpoint of every interval. Knowing this, samples of the voltages and currents can be made at these instances in time, as it is guaranteed that there will be no switching transients. These switching orders also have the advantage of only having 1 leg switching per vector transition.

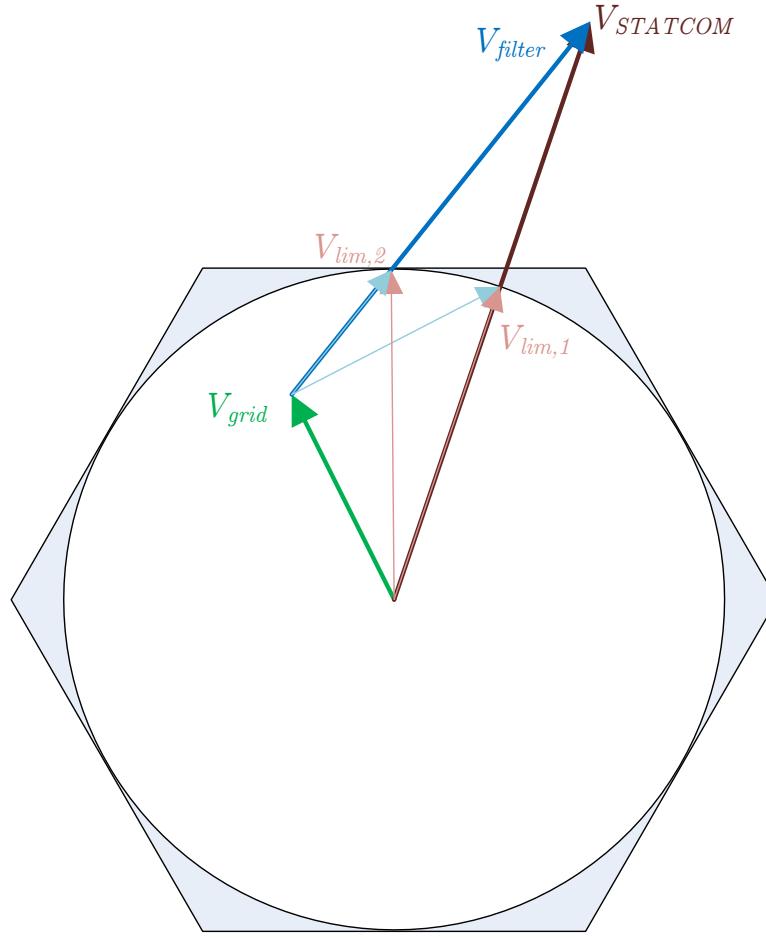


Figure 5.11: Voltage limiting techniques

#### 5.6.4 Voltage Limiting Techniques

As a result of the PWM process, the largest voltage vector obtainable is limited to the hexagon formed by joining the tips of the voltage vectors[43]. It is possible that the deadbeat controller can generate reference voltages that are outside the bounds of this hexagon, as the size of the hexagon is dependent on the DC bus voltage. Some method must be employed to limit these reference voltages to a vector that is able to be synthesised by SVPWM[72].

In this section, a comparison is provided between two common voltage limiting techniques (the limit hexagon and the limit circle), followed by the more sophisticated method used in this project which aims to overcome a shortcoming of the commonly used methods. Figure 5.11 shows a desired voltage vector,  $V_{STATCOM}$ , which lies outside the limit hexagon. This scenario is used as an example to provide a comparison of the 3 methods.

#### 5.6.4.1 Limit Hexagon

As the name suggests, the desired voltage vector,  $V_{STATCOM}$ , would simply be limited in magnitude to the hexagon that defines the maximum voltage that can be output by the VSC. The angle of the limited vector is the same as that of the original desired vector.

The limit hexagon method allows full utilisation of the converter capabilities. In using this limiting method however, a rotating vector that tracks the hexagon will have a magnitude that varies in time, and this introduces a 3rd harmonic component[43]. There are 6 separate limiting equations for this method, defining the individual lines for each sector.

#### 5.6.4.2 Limit Circle

To overcome the non-uniformity issue of the limit hexagon, a circle can be formed within the bounds of the hexagon, as shown in Figure 5.11. By using this limiting method, a rotating vector that tracks the circle will have a constant magnitude and hence there will be no 3rd harmonic introduced[43]. Another advantage of this method is that a single circle equation defines the boundary, rather than 6 separate equations as for the limit hexagon.

By limiting the excursion of the reference vector to a circle, the converter capabilities are underutilised as the shaded areas in Figure 5.11 are not used.

Like the limit hexagon, the limit circle preserves the angle of the original voltage reference vector, as shown by  $V_{lim,1}$  in Figure 5.11.

#### 5.6.4.3 Limit Circle with Current Angle Preservation

The problem in using the limit hexagon and limit circle method may not be obvious at first, so it is necessary to recall the aim of the original reference voltage vector. This vector was determined by calculating the voltage that needed to be applied across the filter, to generate a desired output current:

$$\begin{aligned} i_{STATCOM} &= \frac{V_{STATCOM} - V_{grid}}{Z_{filter}} \\ &= \frac{V_{filter}}{Z_{filter}} \end{aligned}$$

The angle of this desired current is dependent on both the voltage across the filter,  $V_{filter}$ , and the impedance of the filter,  $Z_{filter}$ , which is a constant. Figure 5.11 shows the desired voltage across the filter relating to the grid voltage and the STATCOM voltage. It can be seen that when the original reference vector is limited using the previous methods, the angle of the filter voltage (and hence filter current) will change, yet the angle of the desired vector will be preserved.

In fact, it is far more important that the angle of the output current is preserved, rather than the angle of the desired voltage vector[72]. This is a more complex method to implement, since it requires the additional knowledge of the grid voltage vector, whereas the previous methods only required the reference vector. The new reference voltage vector can be obtained by limiting the filter voltage to the circle. This new reference vector preserves the more important output current angle, rather than the STATCOM voltage angle.

It can be seen that there may be cases when it is impossible to preserve the current angle, such as when the grid voltage vector also lies outside the limit circle. For these cases, the previous limit circle method is utilised.

## 5.7 Chapter Summary

This chapter studied the Advanced STATCOM controller, which utilises PLLs to separate the fundamental, 5th and 7th harmonic load currents and the fundamental frequency voltage. The PLL structure used involves cascaded PLLs at each frequency of interest, which successively remove their frequencies to improve the SNR for the downstream PLLs.

This chapter also introduced a novel adaptation of the Karimi-Ghartemani PLL which implements dynamic gain. This combines the performance benefits of high gain (fast tracking) and low gain (noise immunity).

The filtered signals from the PLLs are used with a modified p-q Theory to determine the fundamental reactive power of the load. DC bus voltage regulation is accomplished with the use of a PI controller that generates the fundamental active power reference. These active and reactive power components are used to determine the 50Hz reference currents for the STATCOM.

Depending on the control objectives, the 5th and 7th harmonic currents may be added to the 50Hz references to achieve active harmonic filtering. The resulting current references are passed to a deadbeat controller which determines the necessary voltage that needs to be synthesised by the STATCOM.

A sophisticated voltage limiting method is then used to preserve the phase angle of the desired output current. Finally, this voltage is synthesised using space vector modulation to generate symmetrical PWM waveforms to minimise harmonic distortion.



## Chapter 6

# Simulations of the Advanced STATCOM

*The previous chapter explored the entire control system design for the STATCOM, including the output filter, current controller, DC bus voltage regulation, power factor correction and harmonic cancellation. This chapter involves simulation of the STATCOM in a test power system to highlight its effectiveness in improving power quality.*

### 6.1 Simulation Package and Test System

The Saber simulation package is used for the modelling and simulation of the STATCOM as it is a proven platform, has excellent model accuracy and an extensive device library[73]. Saber has support for digital control through the use of dynamic-link libraries (.dll files), can perform a range of analyses and results can be studied in-depth using CosmosScope.

The STATCOM was simulated in a basic three bus radial power system as shown in Figure 6.1 on the following page.

The set-up is chosen to represent a real world scenario, where:

- The source and transmission network provide a Thevenin equivalent of the entire network,
- The point of common coupling (PCC) connects the STATCOM to the network,
- The load consists of both linear and non-linear components,
- The impedance between the PCC and the load is negligible.

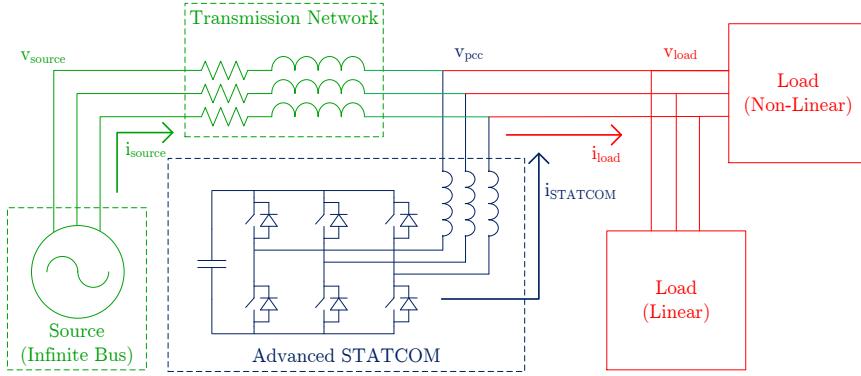


Figure 6.1: Simulation power system

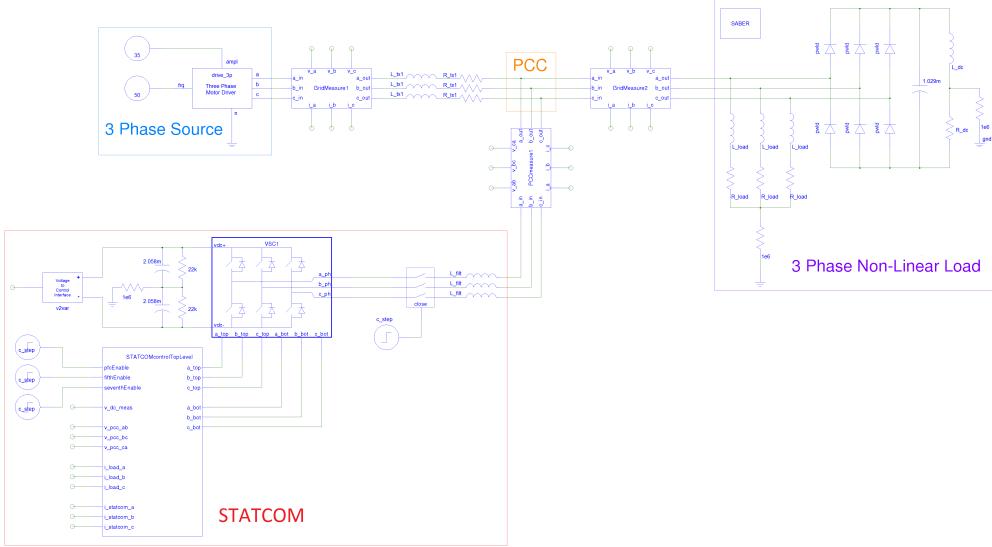


Figure 6.2: Saber screenshot: Top level

A screenshot of the top level simulation designed in Saber is shown in Figure 6.2 on the preceding page.

### 6.1.1 Source and Transmission Network

In real power systems, the bulk generators, transmission companies and distributors maintain control over the network to ensure the frequency is very close to nominal (generally 49.95 Hz to 50.05 Hz). The relative angles of each phase are also maintained very accurately[50]. Thus, it is valid to model the generation as ideal three-phase sine wave voltage sources.

The power network itself is a mesh of many transmission and distribution feeders, connecting to multiple bulk generators as well as many other forms of smaller-scale generation. Thus, the

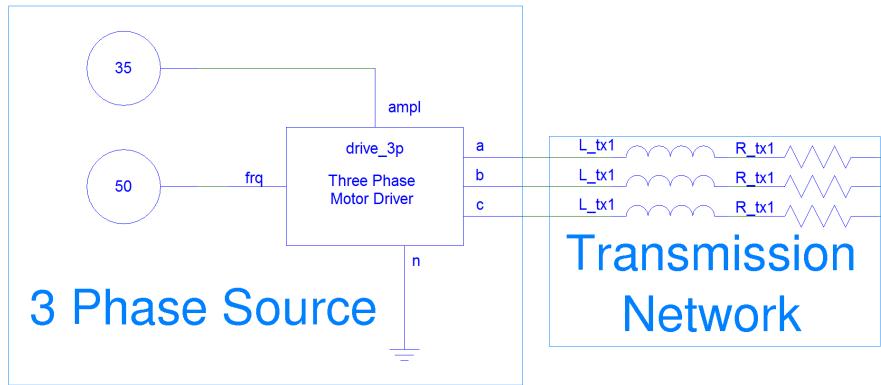


Figure 6.3: Saber screenshot: Source and transmission network

Thevenin impedance is very small and since the majority of the feeders are overhead lines, the impedance is largely inductive[5].

To simplify the top-level diagram in Saber, the generators are modelled with a motor driver voltage source, which provides ideal three-phase sinusoidal voltages that are separated by  $120^\circ$  and have controllable amplitude and frequency. The power network Thevenin impedance is modelled as a  $5mH + 0.5\Omega$  impedance per phase. A screenshot of the source and transmission network in Saber is shown in Figure 6.3.

### 6.1.2 Voltage Source Converter

The VSC sub-block simulates a two-level three-phase voltage source converter. The main simplification made is in the modelling of each IGBT module as single-pole switch with an anti-parallel diode. The purpose of this is to increase the ease of performing switching by removing the need to implement gate drive circuitry for the IGBTs. This simplification does reduce the model accuracy slightly, so it would be important to model the IGBTs correctly if the focus was on fine details, such as transients in the transistor current waveforms. The focus of this project, however, is on the higher level control so the difference between using IGBTs and switches is not important. Some non-ideal effects are introduced in the basic switch models, such as non-zero on-state resistance, finite off-state resistance, and non-zero open and close times. With these non-ideal inclusions, the difference between using IGBTs and switches is negligible, especially compared to other estimations made when modelling the physical system (such as ignoring parasitic impedances).

The other components included in the VSC sub-block are switch driver interfaces which generate position output states based on digital (logic 4) input values. Screenshots of the VSC symbol and sub-block are shown in Figure 6.4.

The VSC is connected to the network with filters that are modelled on the physical inductors

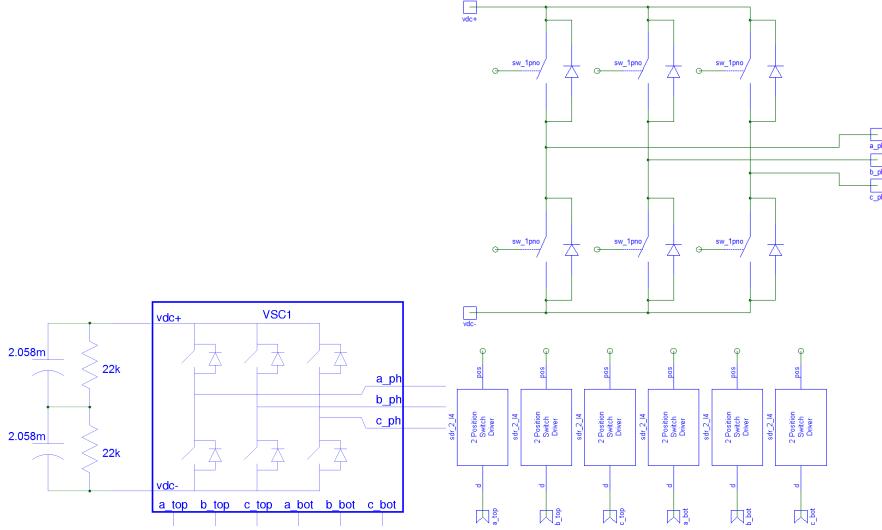


Figure 6.4: Saber screenshot: VSC symbol and sub-block

from Section 5.6.1. These inductors have an inductance of  $5.2mH$  and a winding resistance of  $0.37\Omega/\text{phase}$ .

### 6.1.3 STATCOM Controller

The entire STATCOM controller is implemented in a single DLL file to improve simulation speed and reduce the possibility of simulation errors. A drawback of implementing the entire controller in a single block is that it is not easy to view intermediate variables. For this purpose, 10 extra debug outputs are included, to which any variables can be assigned and viewed. Another significant inconvenience is time and difficulty involved if changes to the controller require modifications of the inputs/outputs from the DLL file. Screenshots of the STATCOM controller symbol and sub-block are shown in Figure 6.5 on the facing page.

### 6.1.4 Measurement Blocks

In order to have a neat and clear top-level diagram, all the Saber measurement components have been included in ‘Grid Measure’ sub-blocks. These blocks contain current-to-control interfaces to measure the current flowing through each phase, and voltage-to-control interfaces to measure the voltage of each phase. The voltages are measured as phase-to-phase values since a three-wire system being considered, and so it is not possible to measure voltages which are referenced to the source ground. Screenshots of the ‘Grid Measure’ symbol and sub-block are shown in Figure 6.6.

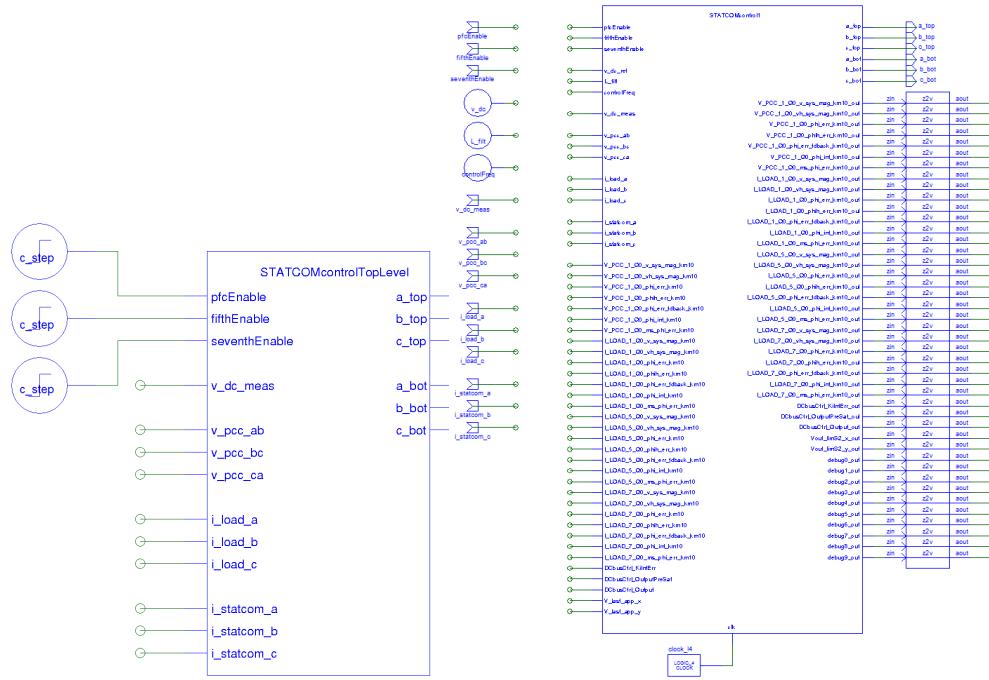


Figure 6.5: Saber screenshot: STATCOM controller symbol and sub-block

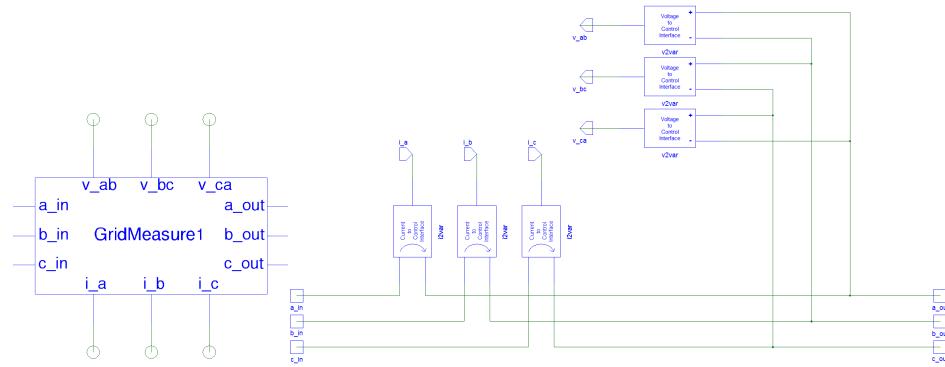


Figure 6.6: Saber screenshot: 'Grid Measure' symbol and sub-block

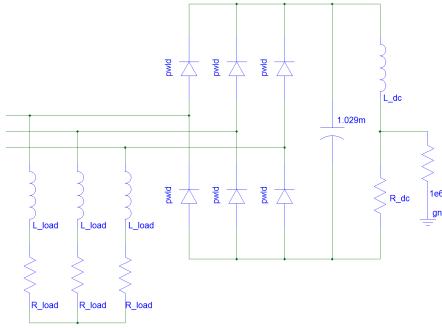


Figure 6.7: Saber screenshot: linear and non-linear loads

### 6.1.5 Load Modelling

To demonstrate both power factor correction and harmonic filtering, the load consists of both linear and non-linear components:

- The **linear component** consists of a star-connected load, with a series inductor and resistor on each phase,
- The **non-linear component** consists of an uncontrolled three-phase diode rectifier with a DC bus capacitor and a resistive load.

A screenshot of these load components in Saber is given in Figure 6.7. A  $1M\Omega$  resistor is included on the DC side of the rectifier to allow the simulation algorithms to converge to a solution. Without this resistor, there is no reference to ground and the simulator will generate an error.

## 6.2 Simulations and Results

This section provides various simulations to demonstrate:

1. DC bus voltage regulation,
2. Power factor correction,
3. Active harmonic filtering,
4. Combined power factor correction and active harmonic filtering.

For the first simulation, the DC bus voltage starts from 0 to show the controller's ability to regulate the voltage to the reference value. For simulations 2-4, the initial DC bus voltage is set to the reference value, since the focus of these scenarios is not on the voltage regulation. For simplicity, only phase 'a' currents and voltages have been shown in simulations 2-4, however it

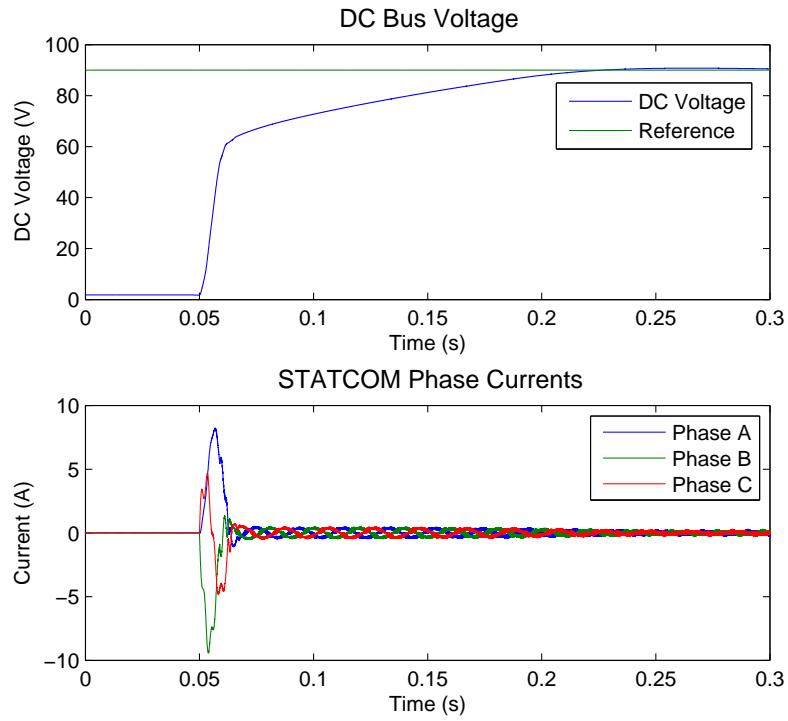


Figure 6.8: Simulation of STATCOM DC bus regulation

is important to note that this is a balanced three-phase system, so the phase ‘b’ and ‘c’ signals are similar, though phase shifted by  $\pm 120^\circ$ .

### 6.2.1 DC Bus Voltage Regulation

This simulation involves STATCOM initially disconnected from the network, then connected at  $t = 50ms$ . The top graph in Figure 6.8 shows a sharp increase in DC voltage when the STATCOM is connected, due to the uncontrolled rectifier action of the anti-parallel diodes in the VSC. The STATCOM currents in the bottom graph cause a steady increase in the bus voltage until it reaches the reference value, approximately 0.15 seconds after connecting to the network. There is no noticeable overshoot or steady-state error in the voltage regulation, validating the parameter selection in the controller design.

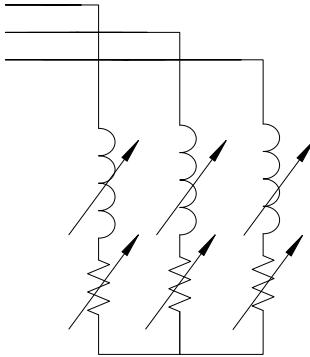


Figure 6.9: Load for power factor correction scenario

### 6.2.2 Power Factor Correction

A three-phase star connected load is used to demonstrate power factor correction, with a series inductor and resistor per phase, as shown in Figure 6.9. This load only draws fundamental frequency currents, and varying the inductance and resistance allows the real and reactive power to be altered. The inductance and resistance values selected for this test are  $100mH$  and  $25\Omega$  respectively, as these values replicate the physical system that is later constructed.

The top graph in Figure 6.10 on the facing page shows the source current (green), load current (red) and STATCOM current (blue). Prior to the STATCOM being turned on, the source and load currents are the same, since the STATCOM current is zero. When the STATCOM is turned on at  $t = 45ms$ , an initial rise in source current can be seen as the capacitor needs to regulate the DC bus. Once the bus is charged it can be seen that the source current is lower than the load current, since the STATCOM current is providing all the reactive power demands of the load. The bottom graph shows the source current and a scaled version of the grid voltage, and it is clear that the power factor is unity as the signals overlap.

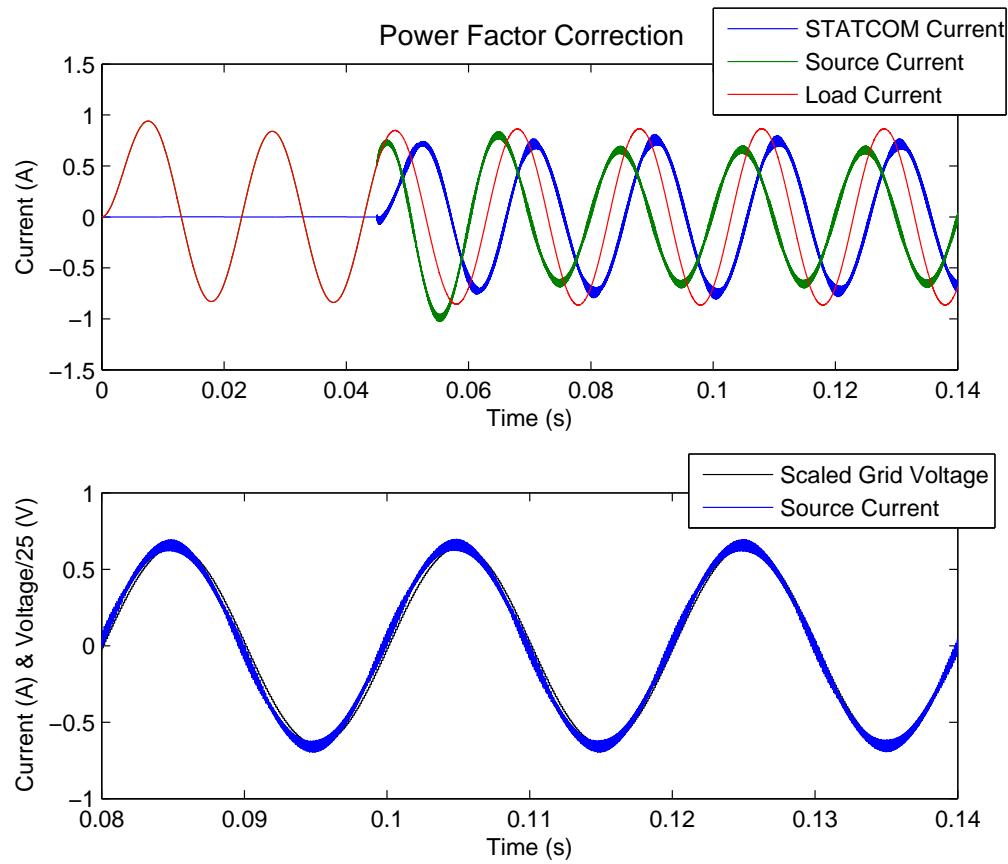


Figure 6.10: Power factor correction simulation

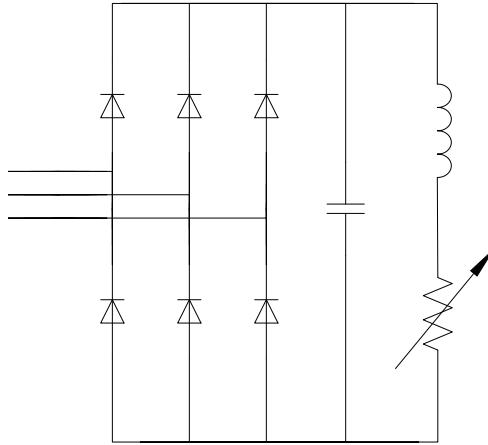


Figure 6.11: Load for active harmonic filtering scenario

### 6.2.3 Active Harmonic Filtering

A rheostat load on the DC side of an uncontrolled diode rectifier load, as shown in Figure 6.11, is used to demonstrate active harmonic filtering due to the large presence of 5th and 7th harmonics. The DC-side load is a  $50\Omega$  rheostat which has a winding inductance of  $20mH$ .

The top graph in Figure 6.12 on the facing page shows that the load current (red) draws significantly more harmonics when the STATCOM is switched on at  $t = 45ms$ . This is because the process of harmonic filtering removes notching and distortion present in the supply voltage, allowing the rectifier to draw even more harmonics. The current injected by the STATCOM (blue) is the sum of the 5th and 7th harmonic components that are consumed by the source. It is clear that the source current (green) becomes considerably more sinusoidal once the STATCOM is turned on, with the remaining distortion mainly resulting from the uncompensated higher order harmonics. The bottom graph shows a comparison of the source and load currents which clearly demonstrates the lower distortion and smaller peak of the source current compared with the load current.

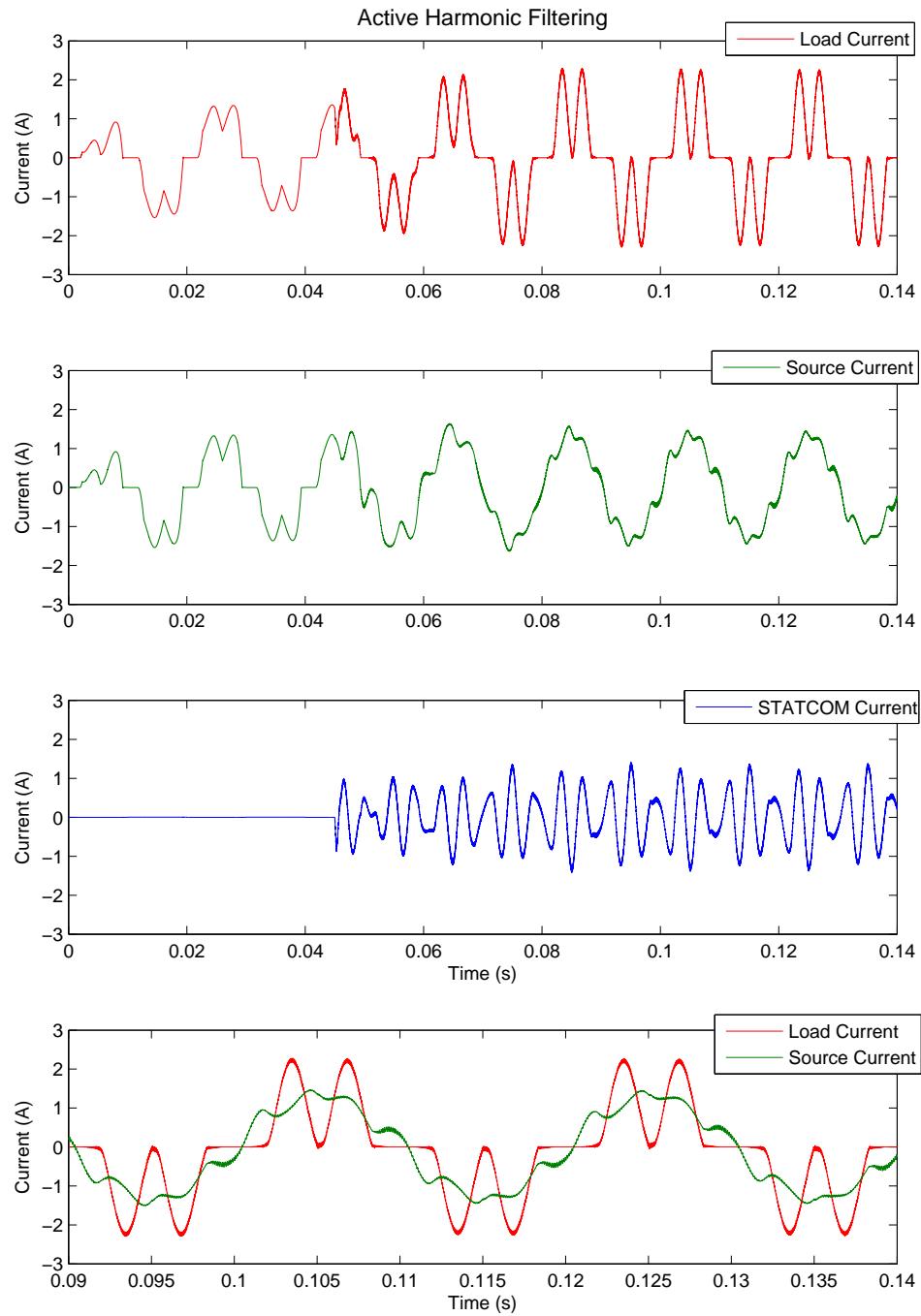


Figure 6.12: Active harmonic filtering simulation

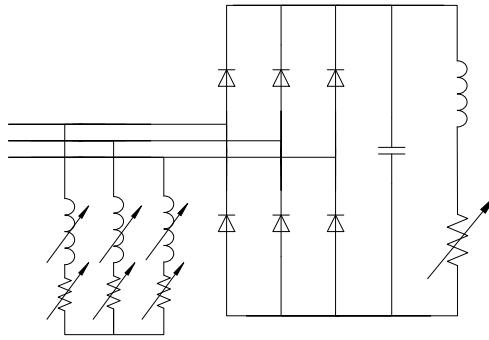


Figure 6.13: Load for combined PFC and AHF scenario

#### 6.2.4 Combined PFC and AHF

To demonstrate simultaneous power factor correction and active harmonic filtering, both of the previous loads are connected, as shown in Figure 6.13. This load draws a combination of fundamental frequency active power, fundamental frequency reactive power, harmonic active power and harmonic reactive power.

Like the previous simulation, the top graph in Figure 6.14 on the facing page shows that the load current (red) draws significantly more harmonics when the STATCOM is switched on at  $t = 45ms$ , as a result of the decrease in grid voltage distortion. This load current also has a superimposed fundamental frequency component from the star-connected resistors and inductors. The current injected by the STATCOM (blue) is the sum of the fundamental reactive current, as well as the 5th and 7th harmonic components that are consumed by the source. Again, the source current becomes considerably more sinusoidal, with the remaining distortion primarily resulting from the uncompensated high order harmonics. The bottom graph shows that the source current has far less distortion than the load current, and that the peak value is also smaller. A scaled grid voltage is also shown to indicate that the source current is in phase with the grid voltage, demonstrating the simultaneous power factor correction capabilities of the STATCOM.

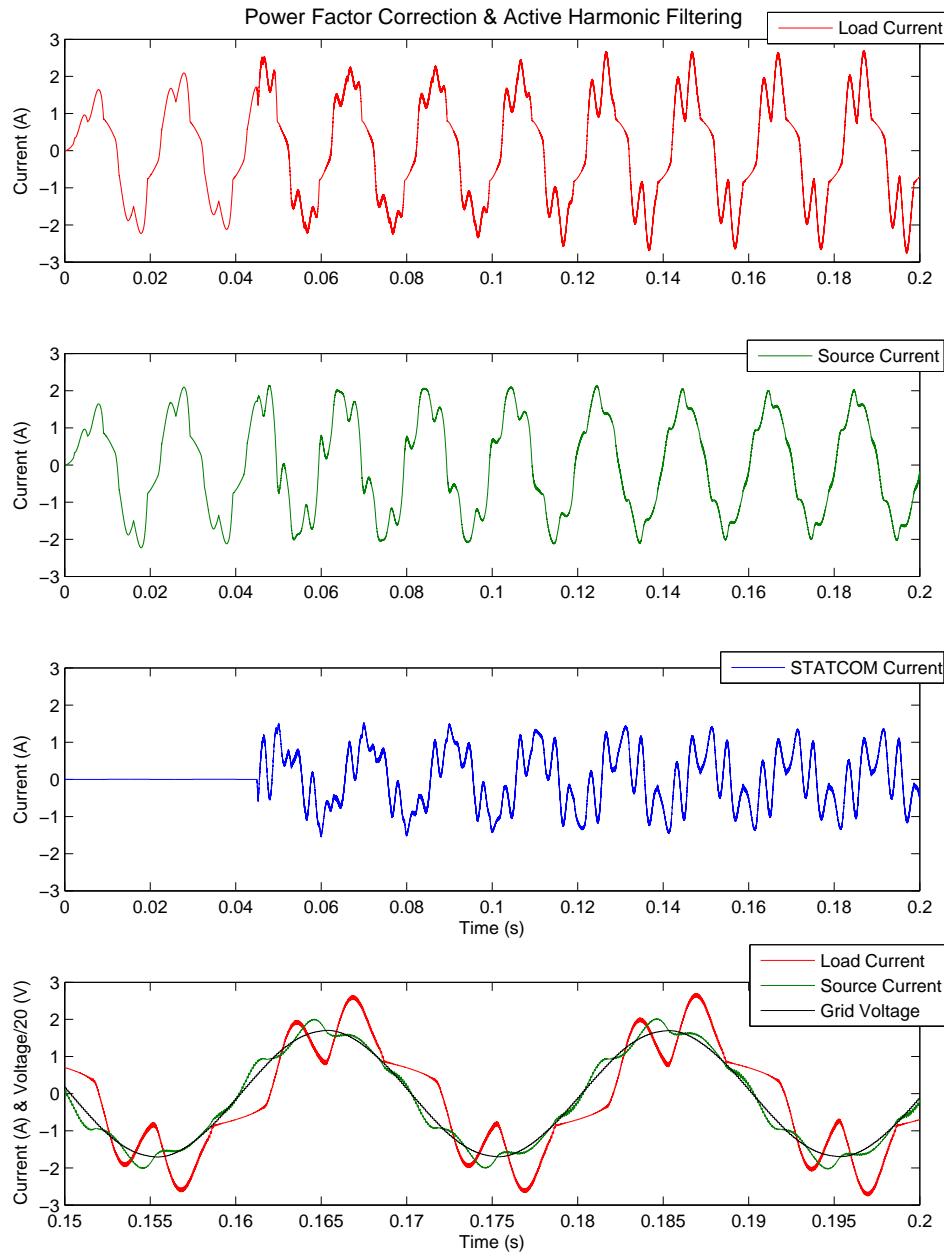


Figure 6.14: Simultaneous power factor correction and active harmonic filtering simulation

### 6.3 Chapter Summary

This chapter involved simulations of the Advanced STATCOM in a test power system using the Saber platform. An outline of the engineering process in designing the various simulation components (including source, transmission network, VSC and load) was provided. The entire control scheme was written in C++ and compiled into a single DLL file to allow fully discrete control, accurately simulating a physical real-time digital controller.

Simulations were performed to prove the STATCOM's functionality in DC bus voltage regulation, power factor correction and active harmonic filtering. The results of these simulations demonstrated the STATCOM's significant impact in improving power quality.

## Chapter 7

# Experimental Demonstration of the Advanced STATCOM

*The previous chapter provided simulation results of the STATCOM using the Saber simulation platform. This chapter discusses the physical construction of the STATCOM and a power system test bed to provide a practical demonstration of its functionality. The chapter investigates the design choices for selecting equipment, the construction process, and results of the completed project.*

### 7.1 STATCOM and Test Bed Design

Figure 7.1 on the next page shows the entire power system test bed constructed for this project. This section outlines the hardware design for the following components:

- Power converter,
- STATCOM controller,
- Voltage and current measurement,
- Transmission network,
- Loads.

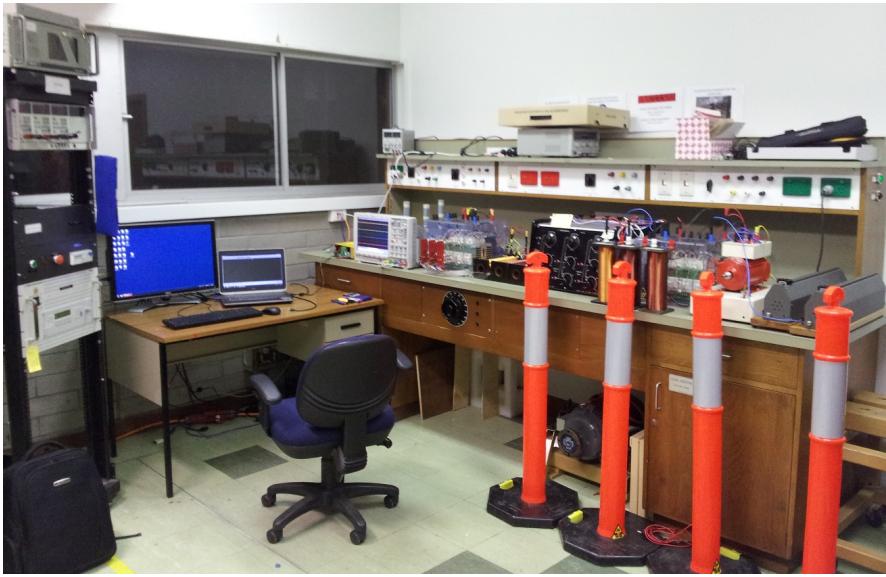


Figure 7.1: Experimental test bed

### 7.1.1 Converter Selection

The power converter used is the Semistack by Semikron, as shown in Figure 7.2 on the facing page. This product, which is designed as an educational unit, is very flexible as it has many components (including a rectifier, three inverter legs, a chopper leg, DC bus capacitors, snubber circuits and IGBT drivers)[35]. Due to the number of components and ease at which they can be accessed, the Semistack is able to simulate many industrial applications including rectifiers, inverters, back-to-back converters and motor drives. For the STATCOM, three inverter legs and the DC bus capacitors are used. Each inverter leg uses a single Semitrans module (SKM 50GB123D) consisting of 2 IGBTs and their associated anti-parallel diodes. The DC bus contains two large  $2200\mu F$  capacitors in series with  $22k\Omega$  resistors across the terminals of each capacitor for voltage balancing and to serve as bleed resistors which discharge the capacitors when the converter is not in use[74]. The 23kVA Semistack used is rated to  $440V_{ac}$ ,  $750V_{dc}$ ,  $30A_{rms}$ , which is sufficient for this project with some additional overhead to allow for future modifications in specifications.

The design decision to use this converter was predominantly made due to the highly time-constrained nature of the project. The all-in-one aspect of the Semistack removes many of the trivial yet time-consuming challenges, such as individual component selection, ordering and waiting during lead times. The converter is also very flexible, with the connections being easily accessible, and the transition from extra-low voltage to low voltage requiring no hardware changes. Finally, the knowledge and experience of others at the university with the device, made the Semistack the optimal choice for use in the STATCOM.

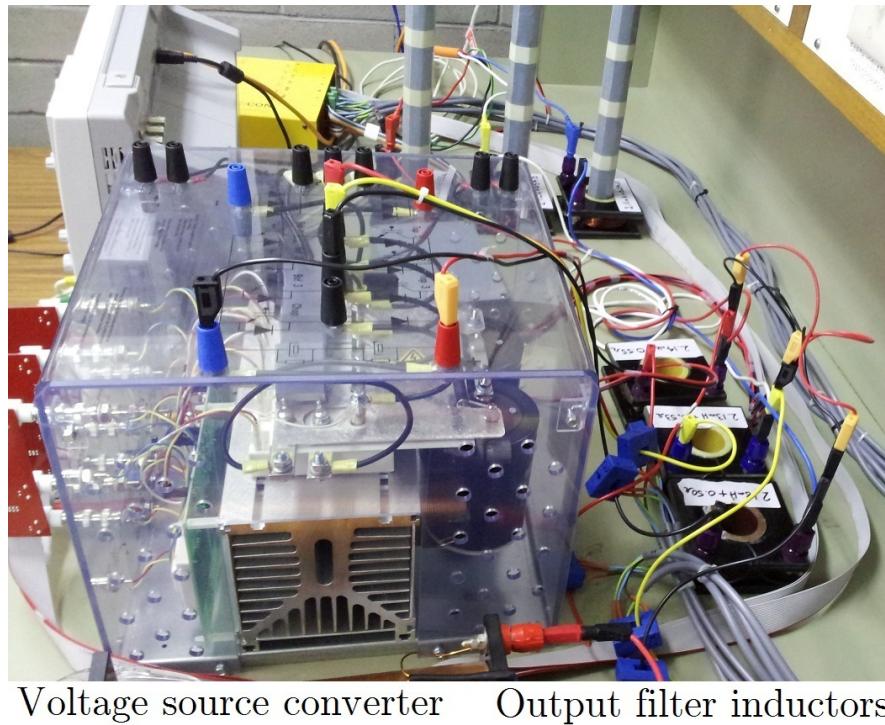


Figure 7.2: Semistack (used as VSC) and filter inductors

### 7.1.2 Controller Selection

The controller used for the STATCOM is a PwrCON unit, which contains a Texas Instruments Delfino F28335 microcontroller. The PwrCON box, shown in Figure 7.3 on the next page, contains a base board which connects the microcontroller card (TMS320F28335 ControlCARD) to the various peripheral cards. Table 7.1 on the following page lists the peripheral cards in the PwrCON box and details their usage.

The microcontroller was chosen because it is a digital signal controller which has excellent floating-point performance and a high clock speed processor, necessary for the computational load of the STATCOM controller[75]. Another important consideration when choosing this controller was the ability to perform simultaneous high precision ADC samples required for the performance objectives of the controller.

### 7.1.3 Voltage and Current Measurement

Accurate voltage and current measurements are essential to the proper operation of the STATCOM. The DC bus and grid voltages may be in excess of 100V, so an interface is needed for connection to the  $\pm 10\text{V}$  inputs of the AIVC card. The ‘X002’ card (four-channel voltage sensing

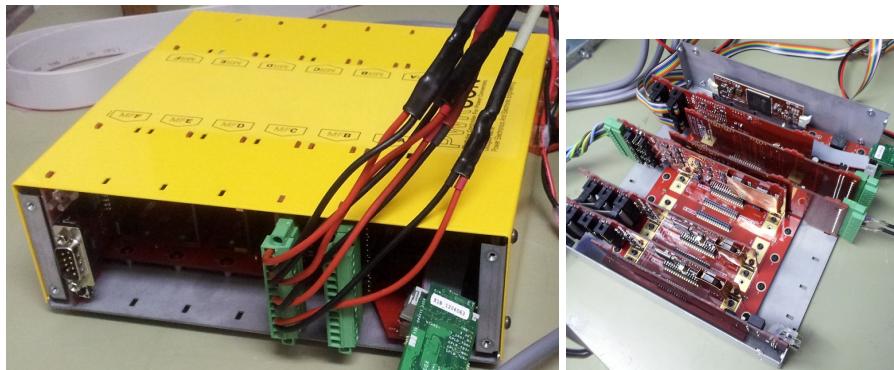


Figure 7.3: PwrCON controller - outside and inside

Port	Card	Use
B - Rear	AIVC	Voltage feedback for PCC phase-to-phase voltages and DC bus voltage
B - Front	AIOA	Analogue outputs connected to oscilloscope for debugging purposes
C - Rear	AICA	Current feedback of STATCOM currents
C - Rear	AICA	Current feedback of load currents
E - Rear	GDCE	IGBT drivers for the three legs of the inverter
F - Front	SERA.CAN	Isolated CANinterface for computer communications

Table 7.1: PwrCON Peripheral Cards and Uses

board) is used for this purpose, which is essentially a voltage divider circuit. Figure 7.4 shows this interface card with the high voltage inputs on the right, and the low voltage signals going to the controller on the left. The voltages on the card are potentially dangerous so the entire interface card is enclosed in a box, which is also shown in Figure 7.4.

Current measurements are provided by LEM LA 55-P Hall effect current transducers. These transducers were chosen as they have a large frequency bandwidth (DC - 200kHz), appropriate current range ( $\pm 70\text{A}$ ), high current resolution, and a convenient interface with the AICA current sensing peripheral cards.



Figure 7.4: Voltage sensing board and current sensor



Figure 7.5: California Instruments 4500Lx programmable supply and lab set-up

#### 7.1.4 Source Selection (Transmission Network)

A programmable three-phase supply (California Instruments 4500Lx) connected to inductors form the Thevenin equivalent source for the test bed, as shown in Figure 7.5. The programmable supply is completely microprocessor controlled and allows different supply conditions to be set so that the effects of harmonics, unbalance and transients can be analysed. The supply has built-in measurement and power analyser capabilities so the benefits of the STATCOM are easily seen and quantified.

#### 7.1.5 Load Design

The load, shown in Figure 7.6 on the following page, is formed by a parallel connection of linear and non-linear components. The linear component is formed with a series connection of active and reactive loads:

- The active power component of the load is a star-connected load bank (with the star point left unconnected). The per-phase resistance of the load bank is configurable between  $24\Omega$  and  $288\Omega$ .
- The reactive power component of the load is a set of inductors, where the inductance can be varied by moving ferromagnetic cores within the centre of the inductors. The inductance range is  $5mH$  with the core removed, and  $60mH$  with the core fully inserted.

The harmonic components are provided by an uncontrolled three-phase rectifier with two types of load connected at the DC terminals:

- A constant impedance rheostat,
- A compound DC motor with the input terminals connected in series with a rheostat to provide a simplistic method of speed control.



Fundamental reactive load      Fundamental real load      Uncontrolled three-phase rectifier      DC compound motor      Rheostat on DC terminals

Figure 7.6: Load set-up for practical demonstration

The harmonic spectrum of this load contains significant amounts of 5th, 7th, 11th and 13th harmonics, allowing a clear demonstration of the harmonic filtering capabilities of the STATCOM.

## 7.2 PC Interface and Communications

### 7.2.1 Computer Application

A computer program was designed and coded in C# to manage the STATCOM. Two-way communications with the PwrCON box enabled control of the STATCOM, as well as real-time feedback of system information.

The application (as shown in Figure 7.7 on the next page) provides the ability to control the objectives and functionality of the STATCOM, as well as view real-time data of the power system and controller. The graphical user interface shows real-time graphs of the PCC voltage, grid frequency, DC bus voltage, power factor and PLL statuses. The functions of power factor correction and harmonic filtering can be independently enabled or disabled, with each harmonic independently controllable. Each of the outputs connected to the oscilloscope can also be configured from an extensive list of options, to make the debugging and fault-finding process considerably easier and more streamlined.

### 7.2.2 Communications with the Advanced STATCOM

The SERA.CAN peripheral card in the PwrCON unit provides a CAN (Controller Area Network) communications interface, which is a standard designed to communicate with other CAN ports

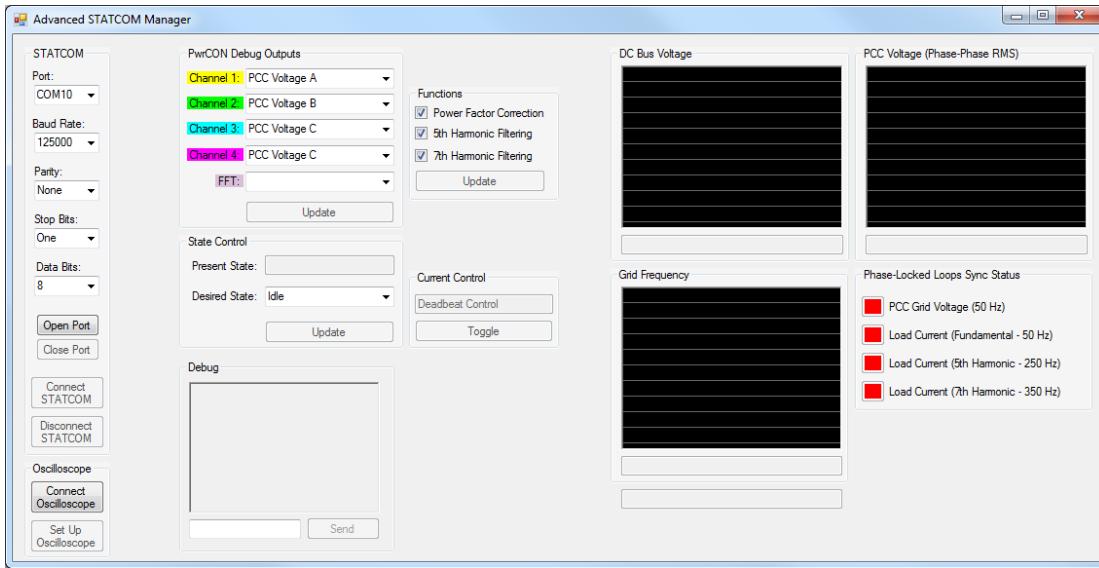


Figure 7.7: Computer application: ‘Advanced STATCOM Manager’



Figure 7.8: CANUSB converter

(and not specifically with PCs)[76]. This protocol is capable of a 1Mbps throughout, enabling real-time transmission of large amounts of data. To facilitate communications with a PC, a special ‘CANUSB’ interface device is required, as shown in Figure 7.8.

The far left of the application is used for managing the connection to the PwrCON controller. This interface is achieved with the computer application communicating directly with the CANUSB module, which is set up as a virtual COM port (VCP). The application sets up the appropriate VCP information (such as baud rate and parity) and sends the specific packets to establish a connection through to the PwrCON unit. Messages being sent to the STATCOM controller from the PC need to be wrapped with additional data to instruct the CANUSB to forward the messages to the PwrCON unit.

A proprietary protocol for exchanging data with the PwrCON unit was developed, with the objective of minimising resource usage on the PwrCON unit due to the importance and pro-

cessing power required by other control tasks. Due to the nature of the CAN communications protocol and limitations of the CANUSB module, packet sizes in excess of 4 bytes incur larger overheads, so it was desired that all data be transmitted in 4 byte packets. 1 byte was reserved as a function byte, so a special 3 byte data type, similar to a float, was developed to allow complete transmission of a function and associated data within the 4 byte limit. This new data type provides a resolution of 0.001 and a range of  $\pm 8388.607$ , which is suitable for all data variables anticipated for communications.

The communications code on both the computer and PwrCON unit is fully interrupt-driven, allowing it to run very efficiently, which is critical given the computational intensity of other tasks being carried out simultaneously by the STATCOM controller.

### 7.2.3 Communications with the Oscilloscope

The oscilloscope primarily used in this project is an Agilent InfiniiVision MSO7104B, which has a network and USB port, allowing it to be accessed and controlled via a PC. Control is achieved using the SCPI (Standard Commands for Programmable Instruments) syntax with the VISA I/O API (Virtual Instrument Systems Architecture input/output application programming interface).

This method of control was integrated into the computer application to allow a specific set-up to be applied (as shown in Figure 7.9 on the next page) for easily viewing the STATCOM signals:

- Enable all four channels,
- Label all four channels,
- Configure the horizontal time division scaling,
- Configure the vertical voltage division scaling,
- Configure the triggering,
- Set the terminating impedance for each channel.

In addition, the channel labels are renamed when the debug outputs are changed, such that the oscilloscope will always show what is being displayed on each channel to make investigations of systems behaviour more polished and streamlined. Functionality is also provided to view the FFT of the signals on any channel.



Figure 7.9: Default oscilloscope set-up

#### 7.2.4 STATCOM State Control

The STATCOM may be in one of five states:

1. **Null:** The STATCOM is not switching. This state is the first state the STATCOM enters when powered up. The sensors are zeroed in this state.
2. **Idle:** The STATCOM is not switching. There will still be a DC voltage on the DC bus due to the anti-parallel diodes acting as an uncontrolled rectifier. The PLLs are still running to monitor the system parameters.
3. **DC Regulation:** The STATCOM is being controlled to regulate the DC bus.
4. **Active:** The STATCOM is being controlled to regulate the DC bus, as well as to perform additional functionality as determined by the Functionality Selector, outlined in Section 7.2.5. The STATCOM cannot enter this state unless the DC bus is within 5% of its nominal value.
5. **Fault:** The STATCOM protection has tripped the STATCOM due to the detection of a fault in the converter. As there is no circuit breaker connected between the STATCOM and the grid, the fault detection simply disables all switching. For this project, the faults are defined as an overcurrent in any phase output (in excess of 10A), or an overvoltage of the DC bus (in excess of 20V).

The STATCOM state control part of the application allows the user to select the operating mode of the STATCOM.

### 7.2.5 STATCOM Functionality Selector

When the STATCOM is operating in the ‘Active’ state, it can perform:

- Power factor correction,
- 5th harmonic filtering,
- 7th harmonic filtering.

The functionality selector allows any combination of these functions to be enabled. If all functions are disabled, the STATCOM simply performs DC bus regulation.

### 7.2.6 PwrCON Debug Outputs

The debug output drop-down lists enable the user to select what to view on each channel of the oscilloscope from an extensive list of important controller and power system signals. As the user changes what variable is being displayed, the application also communicates with the oscilloscope to update the channel labels appropriately.

The FFT drop-down list enables the display of the frequency content of any channel. The application also configures the FFT scaling on the oscilloscope to view the spectrum from 0 to 500Hz to easily see the fundamental, 5th and 7th harmonic components.

### 7.2.7 Real-Time Graphs

Real-time graphs were included to display the:

- STATCOM DC bus voltage,
- Point of common coupling voltage (phase-to-phase RMS voltage),
- Grid frequency.

All the graphs have automatic vertical scaling to accurately show all information, even when there are large changes in the displayed values. The horizontal axis spans approximately 10 seconds, so that “old” information isn’t kept, as it would decrease the time resolution for “new” information.

### 7.2.8 Phase-Locked Loop Status Indicators

Indicators were implemented to display the status of the various PLLs utilised in the controller:

- Fundamental (50Hz) point of common coupling voltage,
- Fundamental (50Hz) load current,
- 5th harmonic (250Hz) load current,
- 7th harmonic (350Hz) load current.

The indicators are:

- **Red**, if the PLL is not locked,
- **Yellow**, if the PLL is in a capture state,
- **Green**, if the PLL is locked.

## 7.3 Experimental Results

This section presents 6 sets of results, relating to the most common scenarios the Advanced STATCOM may be implemented in:

1. DC bus regulation
2. Power factor correction
3. Active harmonic filtering (without DC bus capacitor)
4. Active harmonic filtering (with DC bus capacitor)
5. Power factor correction + active harmonic filtering (without DC bus capacitor)
6. Power factor correction + active harmonic filtering (with DC bus capacitor)

For simplicity, only phase ‘a’ currents and voltages have been shown in the simulations, however it is important to note that this is a balanced three-phase system, so the phase ‘b’ and ‘c’ signals are similar, though phase shifted by  $\pm 120^\circ$ .

### 7.3.1 DC Bus Regulation

This set of results simply presents the DC bus voltage regulation of the STATCOM, while performing no other functions. Figure 7.10 on the following page shows that the STATCOM rises from its unregulated value (approximately 50V due to the grid voltage) to the reference value of 90V in less than 0.2 seconds with no overshoot. During the later testing scenarios, as

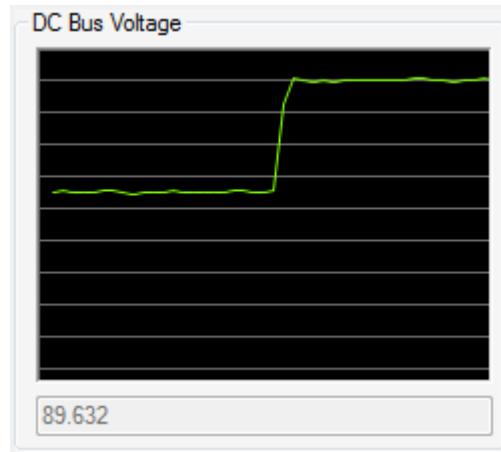


Figure 7.10: DC bus regulation

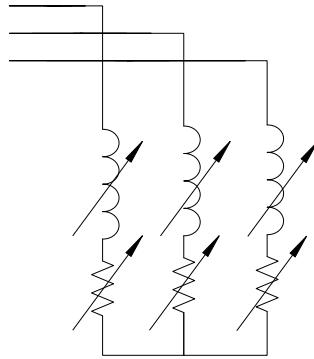


Figure 7.11: Load for power factor correction scenario

the STATCOM is made to perform power factor correction and active harmonic filtering, there are still no perturbations from this regulated voltage.

### 7.3.2 Power Factor Correction

This scenario shows the power factor correction capabilities of the Advanced STATCOM. As shown in Figure 7.11, the load connected consists of three  $60mH$  inductors (with variable inductance by altering the iron core position) connected in series with a star-connected load bank, set with a resistance of approximately  $25\Omega/\text{phase}$ .

Oscilloscope screen captures during operation are shown in Figure 7.12 on the facing page. The image on the left clearly shows a phase shift between the PCC voltage (yellow trace), and the load current (purple trace). The reactive current injected by the STATCOM (pink trace) is  $90^\circ$  out of phase with the voltage, leaving the source current (green trace) in phase with the voltage.

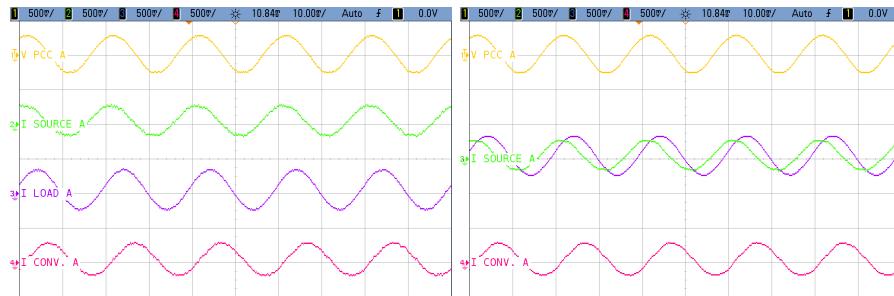


Figure 7.12: Power factor correction waveforms

	Without compensation	With compensation
Power (VA)	12.4	10.3
Power Factor	0.7	0.99
$THD_I (\%)$	0.55	3.45
$THD_V (\%)$	0.3	0.86

Table 7.2: Source measurements: before and after power factor correction

The screen capture on the right shows a clear decrease in the current magnitude in the source current when compared to the load current. This image is very similar to the simulation results obtained in Figure 6.10 on page 69.

Table 7.2 shows a drastic increase in the power factor from 0.7 to 0.99. This power factor is slightly below unity as it is the power factor as seen by the source, including the source inductors. The phase of the source voltages and PCC voltages are therefore different, so although the source currents are in phase with the PCC voltages, they are not in phase with the source voltages.

Slight increases in both current and voltage THDs are also observed as a result of the switching processes in the VSC.

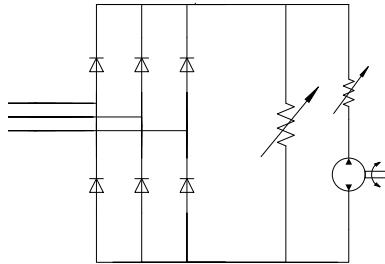


Figure 7.13: Load for active harmonic filtering scenario

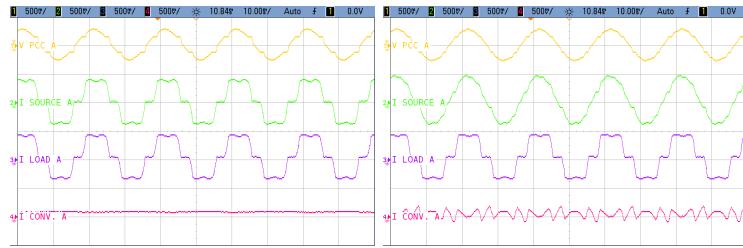


Figure 7.14: Active harmonic cancellation waveforms: capacitor not connected on DC side

### 7.3.3 Active Harmonic Filtering (Without DC Bus Capacitor)

To investigate active harmonic filtering, this scenario (as shown in Figure 7.13) uses a rectifier with the following loads connected on the DC side:

- a constant resistance,
- a compound wound DC motor in series with a variable resistor for basic speed control.

This rectifier does *not* have a bus capacitor as this will be investigated in a later scenario. Thus, the current drawn by the rectifier approximates having a constant current load connected to the DC terminals.

Oscilloscope screen captures during operation are shown in Figure 7.14. The left image shows the source current (green) equalling the load current (purple) as the STATCOM is not enabled. It is also worth noting the large notches in the point of common coupling voltage (yellow). These notches present significant problems to other customers connected to the grid, as discussed in Section 2.4. The image on the right shows the STATCOM injecting the 5th and 7th harmonic components of the load current, leaving the source current as an almost pure sinusoid. It can also be seen that the voltage notching is significantly reduced.

Table 7.3 on the next page shows a drastic decrease in the level of current harmonic distortion, from 22.3% to 6.5% (as seen by the programmable source, using harmonics up to the 50th for THD calculations). A decrease in the voltage harmonic distortion is also seen, due to the

	Without compensation	With compensation
Power (VA)	18.7	19.2
Power Factor	0.95	0.99
$THD_I$ (%)	22.3	6.5
$THD_V$ (%)	1.3	0.9

Table 7.3: Source measurements: before and after active harmonic cancellation

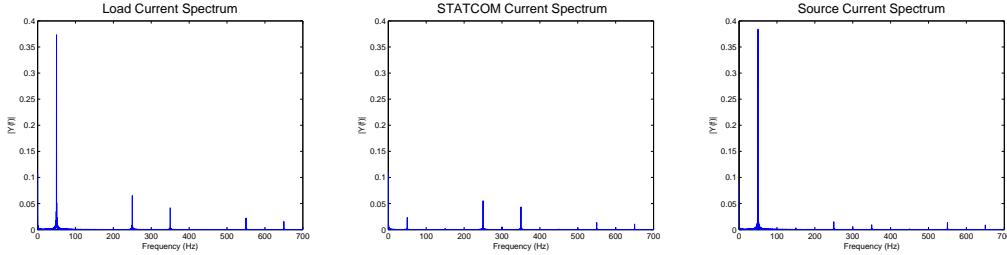


Figure 7.15: FFT for AHF with no DC capacitor: load, STATCOM, source

minimisation of the notching.

Figure 7.15 shows the frequency spectrum for the load, STATCOM and source respectively, as calculated with an FFT in MATLAB using oscilloscope data. It can be seen that the frequency spectrum of the injected current (middle graph) contains most of the 5th and 7th harmonic components of the load (left graph), leaving the source (right graph) with very little harmonic distortion.

The left image in Figure 7.16 compares the harmonic levels of the 5th, 7th, 11th and 13th harmonics to the fundamental frequency component. The level of 11th and 13th are relatively small compared to the 5th and 7th, confirming the justification for the STATCOM compensating 5th and 7th harmonics. The right image shows the harmonic levels of the load (blue) and source (red) as a fraction of their fundamental frequency component, confirming the reduction in THD due to the STATCOM.

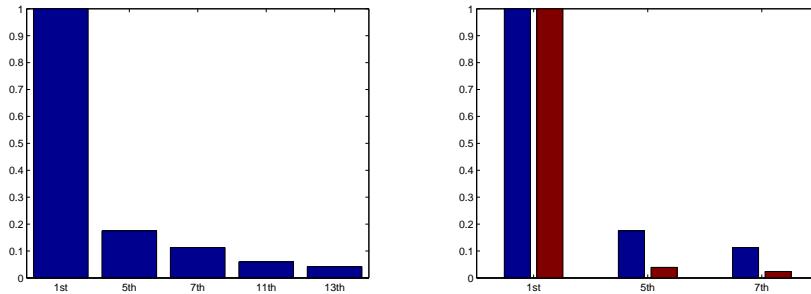


Figure 7.16: Harmonic spectrum of load; and a before/after comparison of source harmonics with AHF

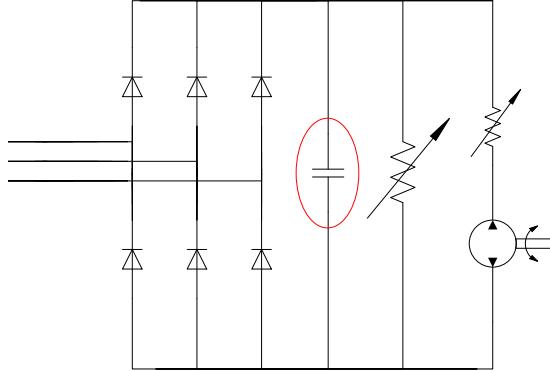


Figure 7.17: Load for active harmonic filtering scenario, with DC rectifier capacitor

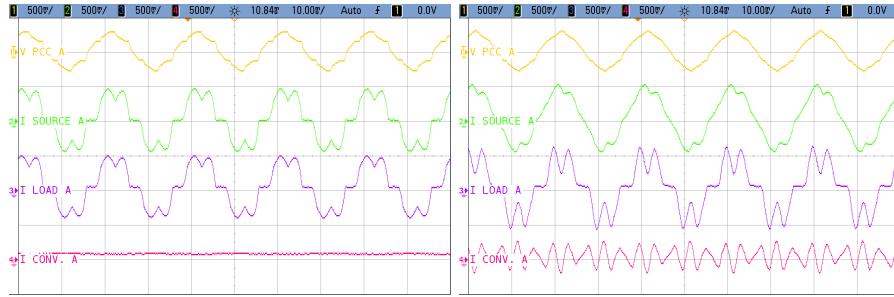


Figure 7.18: Active harmonic cancellation waveforms: capacitor connected on DC side

### 7.3.4 Active Harmonic Filtering (With DC Bus Capacitor)

To further investigate active harmonic filtering, this scenario (as shown in Figure 7.17) uses the same load as the previous test, however, a capacitor is connected to the DC bus, causing the currents drawn to contain much higher levels of harmonics. This test essentially represents the worst case scenario for active harmonic filtering.

Oscilloscope screen captures during operation are shown in Figure 7.18. The left image is similar to the previous scenario, however, the load current (purple trace) contains much more distortion. When active harmonic filtering is enabled (right image) the voltage notching (yellow waveform) is substantially decreased, causing even larger harmonic currents to be drawn by the rectifier as observed in the earlier simulations. Due to the increased distortion, the resulting source current (green waveform) is less sinusoidal when compared to the previous scenario, however a significant improvement is still made when compared to the load current. The right image shows a high correlation with the simulation results obtained in Figure 6.12 on page 71.

Table 7.4 on the next page shows a drastic decrease in the level of current harmonic distortion, from 25.6% to 10.9%. An associated decrease in the voltage harmonic distortion is also seen,

	Without compensation	With compensation
Power (VA)	19.2	19.8
Power Factor	0.93	0.99
$THD_I$ (%)	25.6	10.9
$THD_V$ (%)	1.3	0.9

Table 7.4: Source measurements: before and after active harmonic cancellation

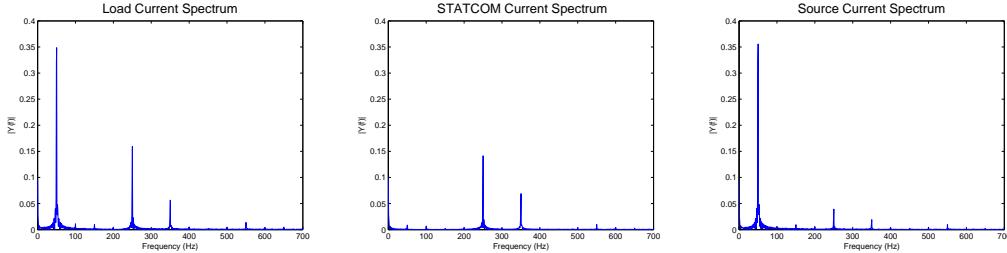


Figure 7.19: FFT for AHF with DC capacitor: load, STATCOM, source

due to the minimisation of the notching.

Figure 7.19 confirms that the 5th harmonic in the load current (left graph) has increased significantly compared to the previous scenario. Again, the frequency spectrum of the STATCOM current (middle graph) matches the harmonic components of the load current. The resulting source current frequency spectrum (right graph) shows very little remaining harmonic components.

The left image in Figure 7.20 shows the magnitude of the 5th harmonic is almost 50% of the fundamental. The right image shows the comparative harmonic levels of the load (blue) and source (red), confirming the dramatic reduction in the 5th and 7th harmonics due to the STATCOM. Bandwidth limitations of the controller prevent the harmonic components from being completely eliminated..

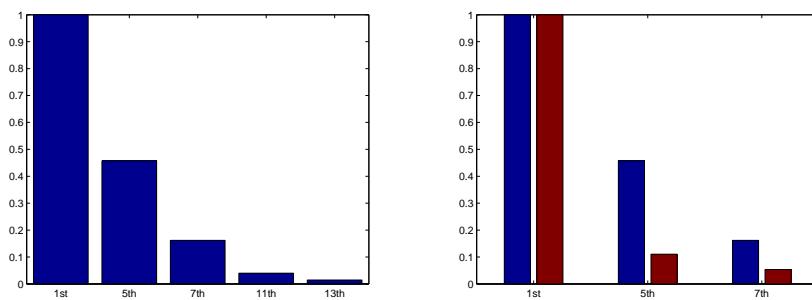


Figure 7.20: Harmonic spectrum of load; and a before/after comparison of source harmonics with AHF

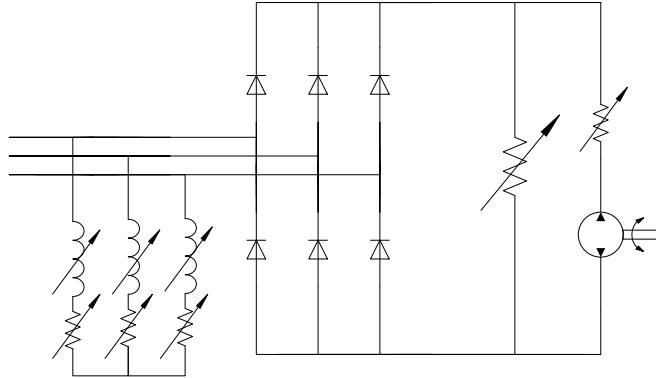


Figure 7.21: Load for power factor correction and active harmonic filtering scenario

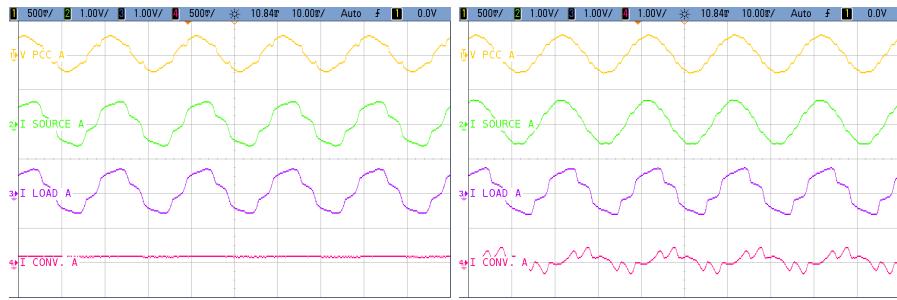


Figure 7.22: Power factor correction and active harmonic cancellation waveforms: capacitor not connected on DC side

### 7.3.5 Power Factor Correction and Active Harmonic Filtering (Without DC Bus Capacitor)

This scenario involves the parallel connection of the loads used in scenario 2 and 3, as shown in Figure 7.21, to demonstrate simultaneous power factor correction and harmonic cancellation.

Oscilloscope screen captures during operation are shown in Figure 7.22. The image on the left shows the system without compensation and the distortion of the source green (green waveform) is clearly evident. The image on the right shows the STATCOM injecting the fundamental reactive component of the load, in addition to the 5th and 7th harmonics, leaving the source current as an almost pure sinusoid in phase with the PCC voltage. Again, it can also be seen that the voltage notching is significantly reduced.

Table 7.5 on the facing page shows a considerable decrease in the level of current harmonic distortion, from 13.2% to 4.4%. A decrease in the voltage harmonic distortion is also seen, due to the minimisation of the notching. Power factor correction results in a power factor of 0.99 as seen by the programmable source.

	Without compensation	With compensation
Power (VA)	28.6	28.6
Power Factor	0.87	0.99
$THD_I$ (%)	13.2	4.4
$THD_V$ (%)	1.1	0.9

Table 7.5: Source measurements: before and after power factor correction + active harmonic cancellation

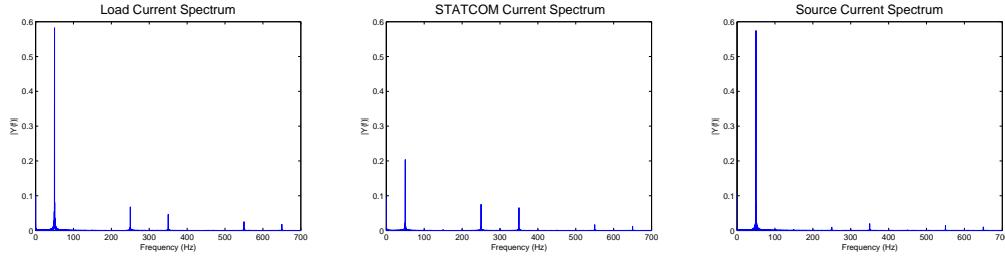


Figure 7.23: FFT for PFC + AHF with no DC capacitor: load, STATCOM, source

Figure 7.23 shows a larger fundamental frequency in the load spectrum (left graph) compared to the previous scenarios, due to the addition of the star-connected load. The frequency spectrum of the STATCOM current (middle graph) shows the 5th and 7th harmonics of the load as before, but now also includes a 50Hz component which is related to the fundamental reactive current. The source current frequency spectrum (right graph) shows the minimal harmonic content remaining.

The left image in Figure 7.24 confirms the relative decrease in the size of the harmonic components compared to the fundamental frequency, resulting from the addition of the linear load. The right image confirms that the 5th and 7th harmonic components have almost been completely eliminated from the source currents.

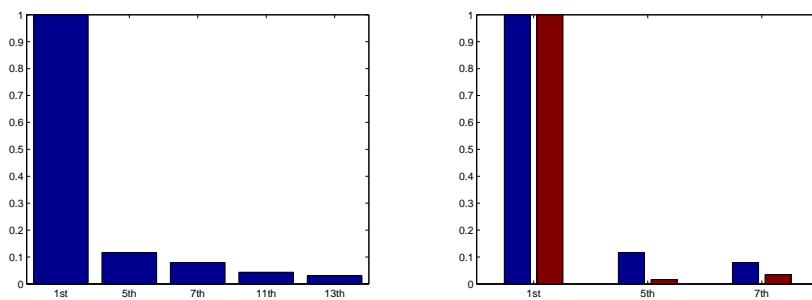


Figure 7.24: Harmonic spectrum of load; and a before/after comparison of source harmonics with PFC & AHF

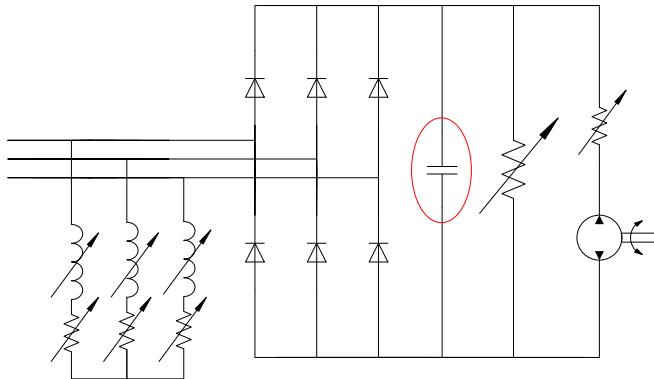


Figure 7.25: Load for power factor correction and active harmonic filtering scenario, with DC rectifier capacitor

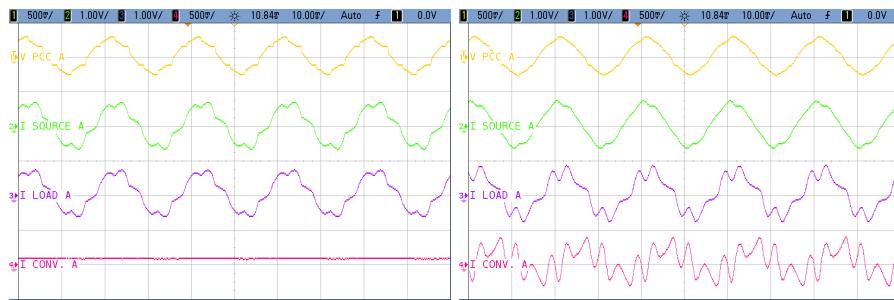


Figure 7.26: Power factor correction and active harmonic cancellation waveforms: capacitor connected on DC side

### 7.3.6 Power Factor Correction and Active Harmonic Filtering (With DC Bus Capacitor)

This final scenario, as shown in Figure 7.25, is based on the previous configuration, with the addition of a DC bus capacitor to produce larger harmonics.

Oscilloscope screen captures during operation are shown in Figure 7.26. The left image is similar to the previous scenario, however the current distortions are far worse due to the presence of the DC bus capacitor. The image on the right shows the STATCOM current (pink) being injected to ensure that the source current (green) is sinusoidal and in phase with the PCC voltage (yellow). A marked improvement can be seen when comparing the source current to the load current (purple). As with the previous scenarios, the voltage distortions are almost completely eliminated. The right image shows a high correlation with the simulation results obtained in Figure 6.14 on page 73.

Table 7.6 on the facing page shows a significant decrease in the level of current harmonic distortion, from 15.5% to 6.5%, and an associated decrease in the voltage harmonic distortion, from

	Without compensation	With compensation
Power (VA)	29	28.9
Power Factor	0.87	0.99
$THD_I$ (%)	15.5	6.5
$THD_V$ (%)	1.2	0.9

Table 7.6: Source measurements: before and after power factor correction + active harmonic cancellation

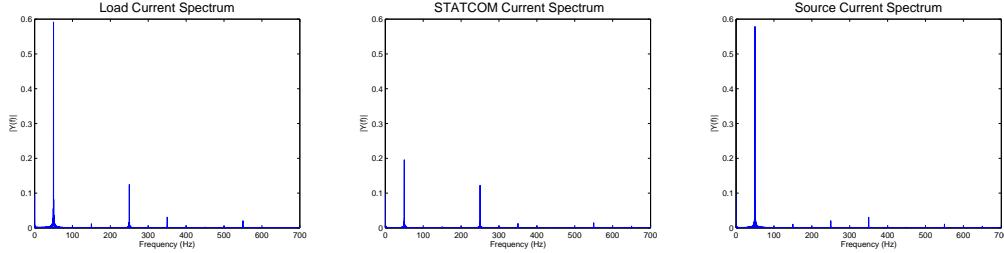


Figure 7.27: FFT for PFC + AHF with DC capacitor: load, STATCOM, source

1.2% to 0.9%. The power factor is increased from 0.87 to 0.99 due to the power factor correction functionality.

Figure 7.27 shows the frequency spectrum of the load current (left), STATCOM current (middle) and source current (right). The results are similar to the previous scenario, however the 5th harmonic component of the load current and STATCOM current are significantly increased.

The left image in Figure 7.28 shows a relative increase in the harmonic content of the load, compared with the previous scenario. The right image shows that the STATCOM almost completely eliminates the 5th harmonic component of the source current. The 7th harmonic component however, is unchanged because it is already quite small and the STATCOM cannot provide further minimisation.

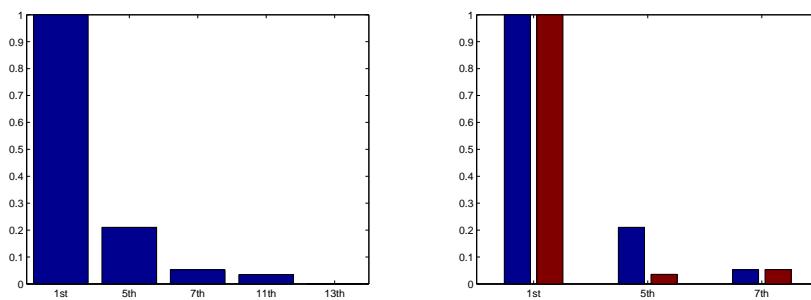


Figure 7.28: Harmonic spectrum of load; and a before/after comparison of source harmonics with PFC & AHF

## 7.4 Chapter Summary

This chapter discussed the design choices made during the physical construction of the configurable distribution system test bed. Overviews of the Semistack converter and PwrCON controller were given, followed by an outline of the physical source and load design.

The computer application was then detailed, with an explanation of its various functions and underlying communications protocols.

Finally, experimental results were obtained for 6 different test set-ups relating to the most common real world scenarios. The results demonstrated that power factor correction increased the total load power factor to unity in all scenarios. Active harmonic filtering performed equally well, with total harmonic current distortion dropping by 60-70% compared with the uncompensated value. This decrease in distortion was a direct result of filtering the 5th and 7th harmonics, and most of the remaining distortion was caused by uncompensated higher order harmonics. A corresponding improvement in the grid voltage waveforms was visible, with a significant decrease in the notching caused by the three-phase rectifier. These experimental outcomes accurately supported the simulated results previously obtained in Chapter 6.

# Chapter 8

## Conclusions and Extensions

*This chapter provides a summary of the project and concluding comments on the outcomes attained. The chapter closes with a discussion of possible future works that could extend on the achievements of this project.*

### 8.1 Conclusions

This project aimed to provide a working demonstration of a power electronics-based device that can optimise the utilisation of existing power system capabilities. This FACTS device, known as an ‘Advanced STATCOM’, uses sophisticated control techniques to combine the functionality of a traditional STATCOM and an active harmonic filter. The project goals have been exceeded with the addition of substantial extra features and more innovative control techniques than originally anticipated.

An initial background of the issues facing today’s power systems was established. This was followed by a discussion of several methods to minimise these problems. An analysis of the voltage source converter was then provided as it forms the “engine” of the Advanced STATCOM. Instantaneous power theory was examined as it underpins the entire outer loop control scheme of the device.

The Advanced STATCOM controller was introduced, including a considerable discussion of harmonic extraction techniques and PLL system simulations. A novel adaptation of the Karimi-Ghartemani PLL was presented which clearly demonstrated substantial improvements. A high performance deadbeat current controller was then developed and analysed prior to the entire system being examined, using the Saber simulation platform. These simulation results illustrated the significant power quality gains achieved by the STATCOM.

Following a discussion of these simulation results, the STATCOM controller was implemen-

ted using a PwrCON control box with a Texas Instruments Delfino microcontroller card. A communications protocol and computer application were developed to facilitate analysis and control of the STATCOM, as well as to provide the ability to view important power system parameters. The GUI also incorporated communications and control of an Agilent oscilloscope to provide a streamlined process of investigating the STATCOM's behaviour. A physical test bed (consisting of a programmable supply, source inductors, resistive load bank, load inductors, a rectifier, a rheostat, and a speed-controllable DC compound motor) was set up to allow a practical demonstration of the STATCOM's functionality.

When power factor correction was enabled, the benefits were significant with the source currents becoming in phase with the point of common coupling voltages, resulting in the programmable supply displaying a power factor of 0.99, and a substantial drop in apparent power delivered.

When harmonic cancellation was enabled, measurement of the source currents showed almost pure sinusoids compared with the heavily distorted load currents. Most of the remaining harmonic distortion was a result of the uncompensated harmonics, rather than shortcomings of the STATCOM itself. With a more powerful microprocessor system, it could be reasonably anticipated that higher order harmonics could also be compensated, further decreasing the level of total harmonic distortion.

It was also shown power factor correction and harmonic cancellation could be simultaneously achieved, such that a non-linear load with a poor displacement power factor would draw similar current waveforms to a pure resistor. The quality and performance of this completed system surpassed expectations of what could be achieved during the span of the project.

## 8.2 Future Extensions

The large scope of this project allows it to be extended in numerous ways. The existing functionality could be further investigated as follows:

- Analysis of transient states (such as fault conditions or large loads switching) with an investigation into the stability enhancements provided by the STATCOM,
- Supply voltage unbalance (presence of negative sequence components),
- High power testing to assess operational and performance limits,
- Load unbalance.

A list of ways the functionality could be extended include, but are not limited to:

- Addition of energy storage (such as a battery) on the DC bus, to provide real power control and peak power smoothing,
- Four-wire application (zero sequence inclusion),
- Load current balancing with the injection of negative sequence currents,
- Multilevel converter for larger powers and voltages,
- Obtain a more powerful microprocessor to allow higher order harmonics to be cancelled, and to allow inclusion of voltage harmonics in the deadbeat algorithms.



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## Appendix A

# Proofs and Derivations

### A.1 SVPWM Switching Times

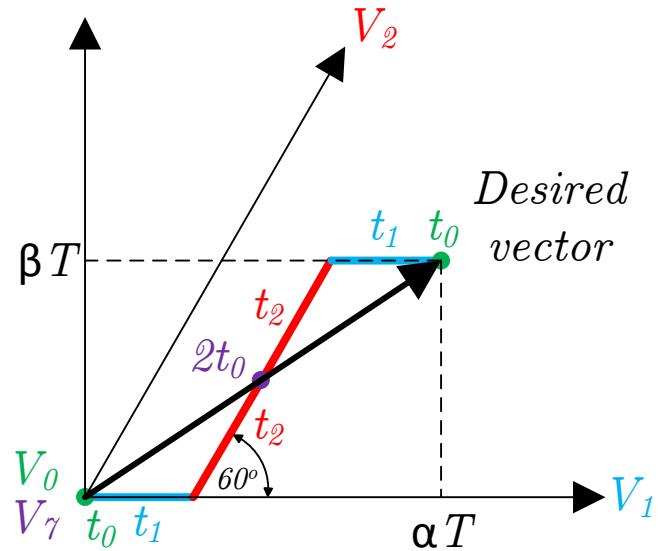


Figure A.1: Reference vector in sector 1

$$\begin{aligned}\alpha &= \frac{2t_1 + 2t_2 \cos 60}{T} \\ \alpha &= \frac{2t_1 + t_2}{T}\end{aligned}\tag{A.1}$$

and

$$\begin{aligned}\beta &= \frac{2t_2 \sin 60}{T} \\ t_2 &= \frac{\beta}{2 \sin 60} \\ t_2 &= \frac{\beta T}{\sqrt{3}}\end{aligned}\tag{A.2}$$

Substituting Equation A.2 into Equation A.1 gives:

$$\begin{aligned}\alpha &= \frac{2t_1 + \frac{\beta T}{\sqrt{3}}}{T} \\ t_1 &= \frac{\alpha T - \frac{\beta T}{\sqrt{3}}}{2} \\ t_1 &= \frac{T}{2} \left( \alpha - \frac{\beta}{\sqrt{3}} \right)\end{aligned}\tag{A.3}$$

The individual switching intervals must sum to equal the total period, giving:

$$\begin{aligned}4t_0 + 2t_1 + 2t_2 &= T \\ 2t_0 &= \frac{T}{2} - t_1 - t_2 \\ t_0 &= \frac{1}{2} \left( \frac{T}{2} - t_1 - t_2 \right)\end{aligned}\tag{A.4}$$

Substituting Equation A.2 and Equation A.3 into Equation A.4 gives:

$$\begin{aligned}t_0 &= \frac{1}{2} \left[ \frac{T}{2} - \frac{T}{2} \left( \alpha - \frac{\beta}{\sqrt{3}} \right) - \frac{\beta T}{\sqrt{3}} \right] \\ t_0 &= \frac{T}{2} \left( \frac{1}{2} - \frac{\alpha}{2} + \frac{\beta}{2\sqrt{3}} - \frac{\beta}{\sqrt{3}} \right) \\ t_0 &= \frac{T}{4} \left( 1 - \alpha - \frac{\beta}{\sqrt{3}} \right)\end{aligned}\tag{A.5}$$

In summary, the switching times are:

$$\begin{aligned}t_0 &= \frac{T}{4} \left( 1 - \alpha - \frac{\beta}{\sqrt{3}} \right) \\ t_1 &= \frac{T}{2} \left( \alpha - \frac{\beta}{\sqrt{3}} \right) \\ t_2 &= \frac{\beta T}{\sqrt{3}}\end{aligned}$$

Similar calculations are performed to determine the equations for the switching times for the other 5 sectors. The results are shown in Table A.1.

Sector	Switching Order	$t_0$	$t_1$	$t_2$
1	$V_0 V_1 V_2 V_7 V_7 V_2 V_1 V_0$	$\frac{T}{4} \left(1 - \alpha - \frac{\beta}{\sqrt{3}}\right)$	$\frac{T}{2} \left(\alpha - \frac{\beta}{\sqrt{3}}\right)$	$\frac{\beta T}{\sqrt{3}}$
2	$V_0 V_3 V_2 V_7 V_7 V_2 V_3 V_0$	$\frac{T}{4} \left(1 - \frac{2\beta}{\sqrt{3}}\right)$	$\frac{T}{2} \left(-\alpha + \frac{\beta}{\sqrt{3}}\right)$	$\frac{T}{2} \left(\alpha + \frac{\beta}{\sqrt{3}}\right)$
3	$V_0 V_3 V_4 V_7 V_7 V_4 V_3 V_0$	$\frac{T}{4} \left(1 + \alpha - \frac{\beta}{\sqrt{3}}\right)$	$\frac{\beta T}{\sqrt{3}}$	$\frac{T}{2} \left(-\alpha - \frac{\beta}{\sqrt{3}}\right)$
4	$V_0 V_5 V_4 V_7 V_7 V_4 V_5 V_0$	$\frac{T}{4} \left(1 + \alpha + \frac{\beta}{\sqrt{3}}\right)$	$\frac{-\beta T}{\sqrt{3}}$	$\frac{T}{2} \left(-\alpha + \frac{\beta}{\sqrt{3}}\right)$
5	$V_0 V_5 V_6 V_7 V_7 V_6 V_5 V_0$	$\frac{T}{4} \left(1 + \frac{2\alpha}{\sqrt{3}}\right)$	$\frac{T}{2} \left(-\alpha - \frac{\beta}{\sqrt{3}}\right)$	$\frac{T}{2} \left(\alpha - \frac{\beta}{\sqrt{3}}\right)$
6	$V_0 V_1 V_6 V_7 V_7 V_6 V_1 V_0$	$\frac{T}{4} \left(1 - \alpha + \frac{\beta}{\sqrt{3}}\right)$	$\frac{T}{2} \left(\alpha + \frac{\beta}{\sqrt{3}}\right)$	$\frac{-\beta T}{\sqrt{3}}$

Table A.1: Switching Details for Each Sector for SVPWM



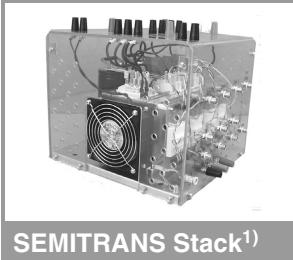
## Appendix B

# Supplemental Information

Odd harmonics: non-multiple of 3		Odd harmonics: multiple of 3		Even harmonics	
Order	Distortion (%)	Order	Distortion (%)	Order	Distortion (%)
5	2	3	2	2	1.5
7	2	9	1	4	1
11	1.5	15	0.3	6	0.5
13	1.5	21	0.2	8	0.4
17	1	>21	0.2	10	0.4
19	1			12	0.2
23	0.7			>12	0.2
25	0.7				
>25	$0.2 + 0.5 \frac{25}{h}$				

Table B.1: Harmonic voltage limits for networks over 35kV (total THD = 3%)[30]

## SEMISTACK - IGBT

SEMISTRANS Stack<sup>1)</sup>

**Three-phase rectifier + inverter with brake chopper**

**SEMITEACH - IGBT**  
**SKM 50 GB 123D**  
**SKD 51**  
**P3/250F**

### Features

- Multi-function IGBT converter
- Transparent enclosure to allow visualization of every part
- IP2x protection to minimize safety hazards
- External banana/BNC type connectors for all devices
- Integrated drive unit offering short-circuit detection/cut-off, power supply failure detection, interlock of IGBTs + galvanic isolation of the user
- Forced-air cooled heatsink

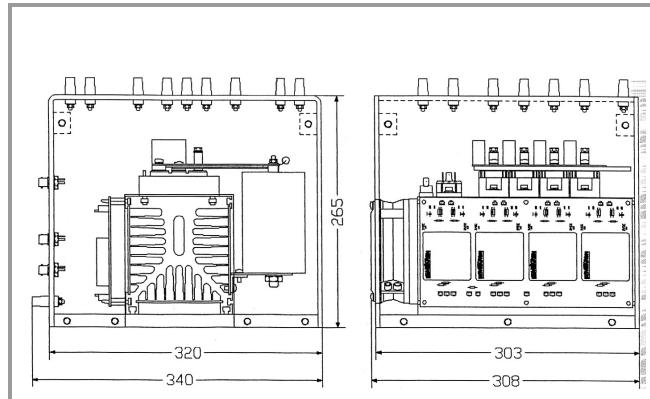
### Typical Applications

- Education: One stack can simulate almost all existing industrial applications:
  - 3-phase inverter+brake chopper
  - Buck or boost converter
  - Single phase inverter
  - Single or 3-phase rectifier

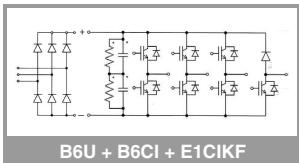
<sup>1)</sup> Photo non-contractual

Circuit	I <sub>rms</sub> (A)	V <sub>ac</sub> / V <sub>dcmax</sub>	Types
B6CI	30	440 / 750	SEMITEACH - IGBT

Symbol	Conditions	Values	Units
I <sub>rms</sub>	no overload	30	A
V <sub>CES</sub>	IGBT - 4x SKM 50 GB 123D	1200	V
V <sub>CE(SAT)</sub>	I <sub>c</sub> = 50A, V <sub>GE</sub> = 15V, chip level; T <sub>j</sub> = 25(125)°C	2,7 (3,5)	V
V <sub>GES</sub>		±20	V
I <sub>c</sub>	T <sub>case</sub> = 25 (80)°C	50 (40)	A
I <sub>CM</sub>	T <sub>case</sub> = 25 (80)°C; t <sub>p</sub> = 1ms	100 (80)	A
V <sub>in(max)</sub>	Rectifier - 1x SKD 51/14 without filter	3 x 480	V
	with filter	3 x 380	V
C <sub>eqv</sub>	DC Capacitor bank - Electrolytic 2x 2200µF/400V	1100 / 800	µF / V
V <sub>DCmax</sub>	total equivalent capacitance max. DC voltage applied to the capacitor bank	750	V
Power supply	Driver - 4x SKH 22	0 / 15	V
Current consumption	max; per driver	16	mA
Thermal trip	Normally Open type (NO)	71	°C



General dimensions



This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee expressed or implied is made regarding delivery, performance or suitability.

Figure B.1: Semistack power converter data sheet[35]