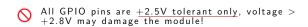


## BOARD OFFICIAL PINOUT



Absolute MAX per pin 24mA, recommended 10mA

GPIO0..28 are available, except GPIO25, which does not exist!
GPIOs can be set as input or output (GPIO13..17 are outputs only), but they cannot be put into 3-state (high impedance or disconnected)

All GPIOs are multiplexed with other functions, except GPIO24, which can be used to control SPI FLash Write Protection when looped back externally to the FLASH\_WP signal.

Boostrap settings must be effective at boot time in order for the module to boot corectly.

LED0..6 are also used for bootstrap settings. To avoid applying a wrong voltage on the I/O pin coming from the LED, these GPIOs should be sourcing current only, not sinking current.

For normal operation, both +5V pins or the Micro USB +VUSB pin must be connected to a +5V power supply

The +2.5V and +2VA\_ETH\_OUT are internally generated power supplies for powering external I/O voltage translators and Ethernet transformer bias, respectively.

GPIO	Bootstrap Function	Pulled Down	Pulled Up
GPIO0	Crystal frequency	25 MHz	40 MHz
GPIO1	Boot from	ROM [	SPI Flash
GPIO11	ICE interface	JTAG	CPU ICE
GPIO12	Memory type LSB	SDRAM/DDR2	DDR1
GPIO13	USB Mode	Device _	Host
GPIO14	Chip Mode LSB	0	1
GPIO15	Chip Mode MSB	0	1
GPIO16	Firmware download	from USB	from MDIO
GPIO17	Ethernet	off (	on
GPIO28	Memory type MSB	SDRAM/DDR1	DDR2

LED5

LED6

LED7

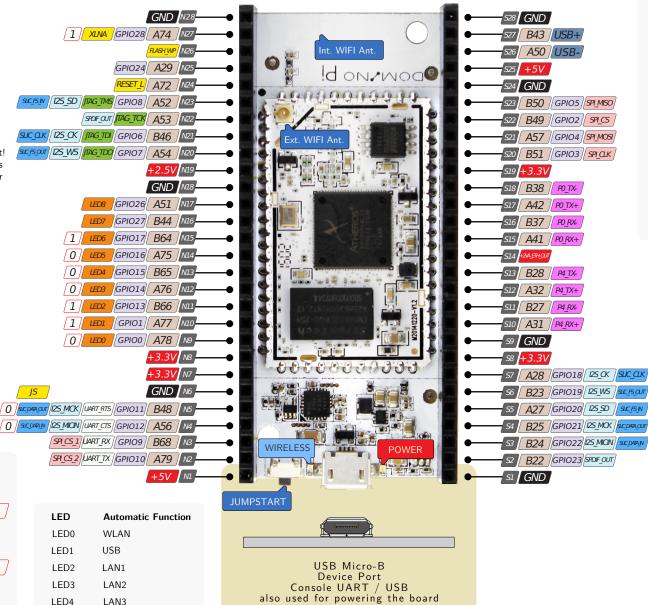
LED8

LAN4

WAN

(SYS)

(WPS)



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06 APR 2015

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**P**Ower **■**GND

GPIO

 $\square JTAG$ 

LED

**UART** 

SLIC

SPI

USB

Ethernet

Antenna

Bootstrap

Control

7125 Audio

ModulePin

AR9331Pin