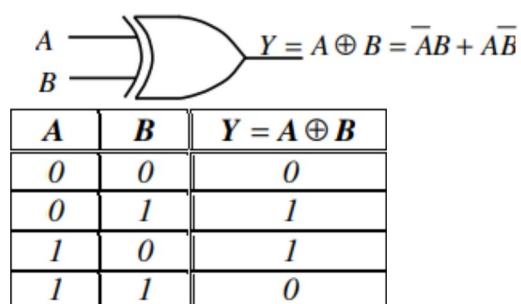


LABORATOR 3

1. Scopul lucrării

Lucrarea își propune studierea detectoarelor de imparitate/paritate și sintetizarea unui astfel de detector cu 4 variabile de intrare.

Detectorul de imparitate/paritate este un circuit logic combinațional la ieșirea căruia trebuie să se obțină 1 logic dacă numărul variabilelor de intrare egale cu 1 logic este impar/par. El are la bază poarta SAU-EXCLUSIV (XOR) cu două intrări, (**fig. de mai jos**)



tabelul de adevăr - (tabelul de mai sus). La ieșirea XOR-ului se obține 1 logic atunci când intrările sunt diferite (01 sau 10 - deci număr impar de 1 logic la intrări) și 0 logic atunci când intrările coincid (00 sau 11 - deci număr par de 1 logic la intrări).

. Detectorul de imparitate-paritate comandat

În sinteza detectorului este necesar să se țină seama de următoarele condiții:

- 1) Transformarea detectorului de imparitate (fig. 3.4) în detector de paritate trebuie realizată prin schimbarea valorii logice a unei singure bare de comandă;
- 2) Indiferent de regimul de "imparitate" sau "paritate" în care lucrează detectorul, ieșirea acestuia trebuie să fie 1 logic în momentul detecției. Rezultă că pentru regimul de imparitate, ieșirea $Y' = Y$, iar pentru regimul de paritate, $Y' = Y$ (vezi tab. 3.3). Este deci necesară utilizarea proprietății nr. 3 (XOR-ul ca detector de imparitate/paritate - comandat) de maniera din fig. 3.5.

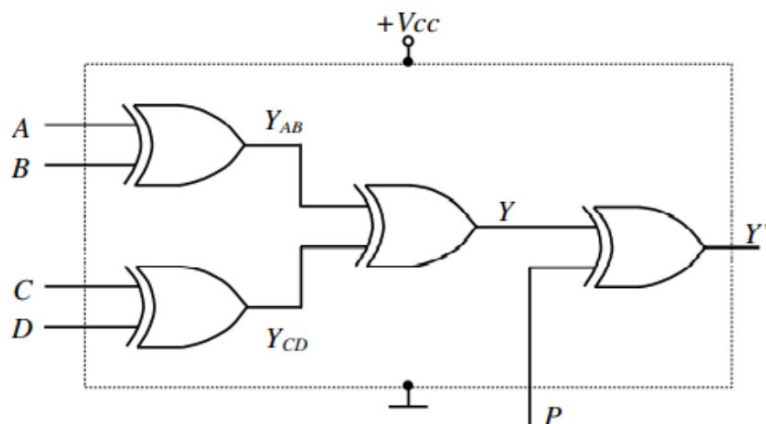


Fig. 3.5. Schema detectorului de imparitate/paritate comandat

$$Y' = Y \oplus P = \begin{cases} Y, & \text{daca } P = 0 (\text{detector de imparitate}); \\ \bar{Y}, & \text{daca } P = 1 (\text{detector de paritate}). \end{cases}$$

Tab. 3.3. Tabelul de adevăr al detectorului de imparitate/paritate comandat

<i>D</i>	<i>C</i>	<i>B</i>	<i>A</i>	<i>Y</i>	<i>P</i>	<i>Y'</i>
0	0	0	0	0	0	0
0	0	0	1	1	0	1
0	0	1	0	1	0	1
0	0	1	1	0	0	0
0	1	0	0	1	0	1
0	1	0	1	0	0	0
0	1	1	0	0	0	0
0	1	1	1	1	0	1
1	0	0	0	1	0	1
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	1	0	1
1	1	1	0	1	0	1
1	1	1	1	0	0	0
0	0	0	0	0	1	1
0	0	0	1	1	1	0
0	0	1	0	1	1	0
0	0	1	1	0	1	1
0	1	0	0	1	1	0
0	1	0	1	0	1	1
0	1	1	0	0	1	1
0	1	1	1	1	1	0
1	0	0	0	1	1	0
1	0	0	1	0	1	1
1	0	1	0	0	1	1
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	0	1	1

. Conținutul referatului

1. Schema din fig. 3.5, completată cu numărul pinilor respectivi;
2. Tabelul 3.3;
3. Tabelul care rezultă în urma experimentului de la pct. 3.1.7;
4. Observații personale ale studentului.

1)

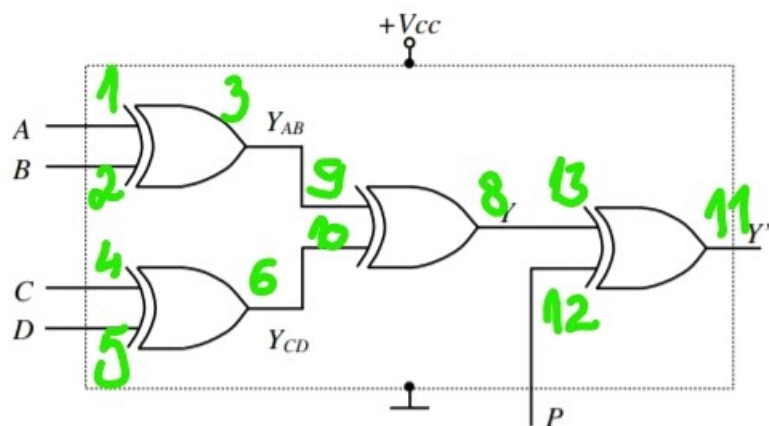


Fig. 2.5. Schema logică a detectorului de paritate comandat cu variabila P.

Mai jos am implementat un detector de paritate/imparitate comandat cu variabila P cu ajutorul unui circuit integrat **74HC86** care conține **4 porte XOR**.
Cand variabila P=1 atunci avem paritate

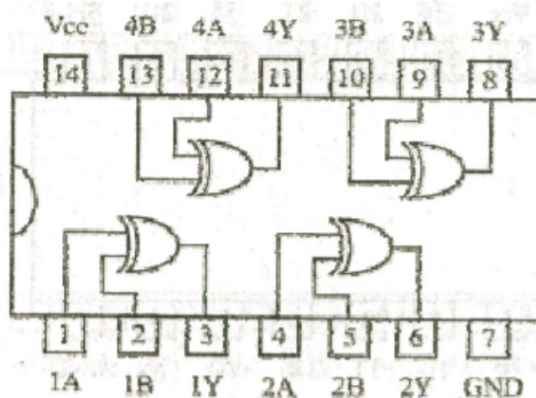
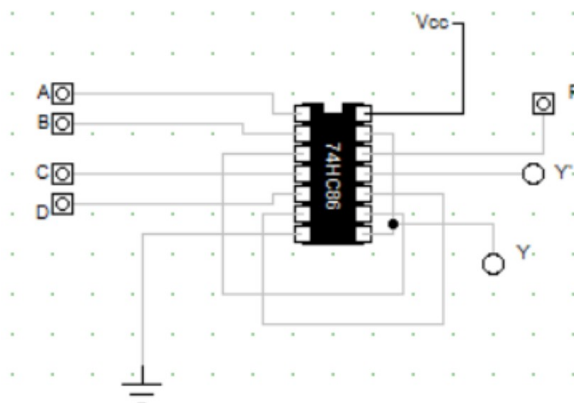
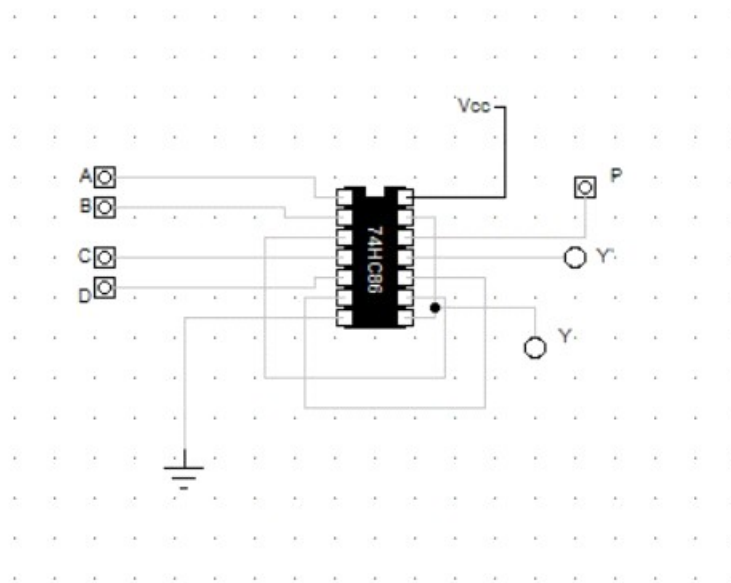


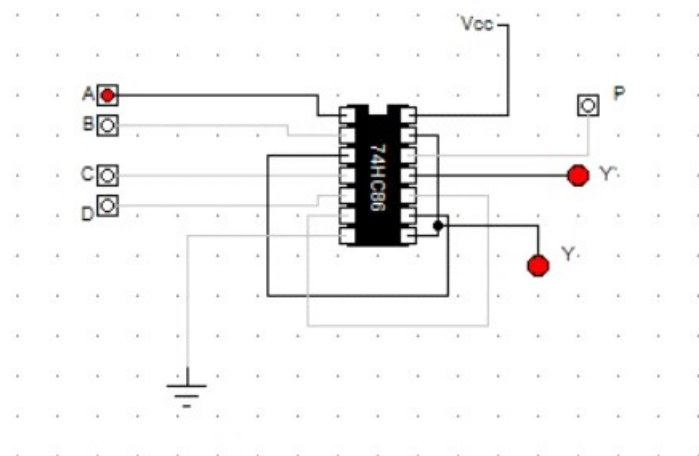
Fig. A.13. CDB 486 (patru operatori XOR cu câte 2 intrări)

2) Tabelul de adevar este prezentat mai sus . De asemenea am verificat pe schema mea tabelul de adevar dupa cum se vede in reprezentarile de mai jos:

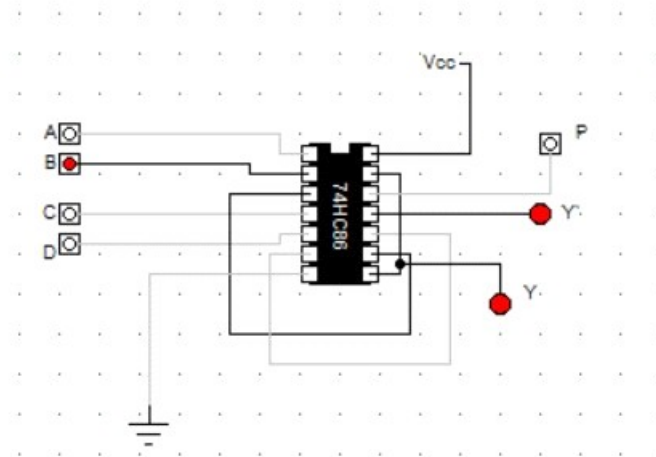
D=0 C=0 B=0 A=0 P=0 =>Y=0 Y'=0



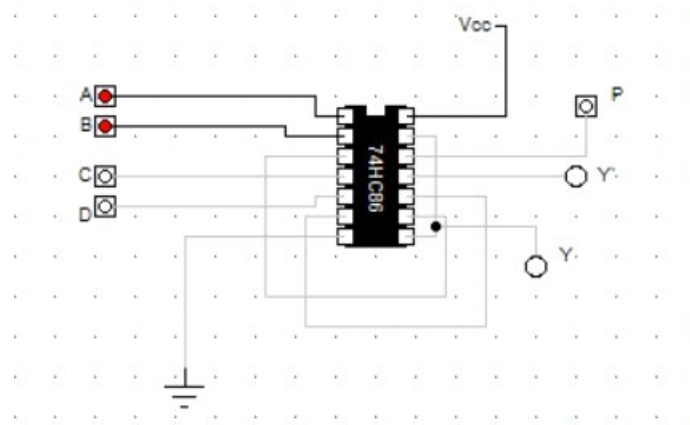
D=0 C=0 B=0 A=1 P=0 =>Y=1 Y'=0



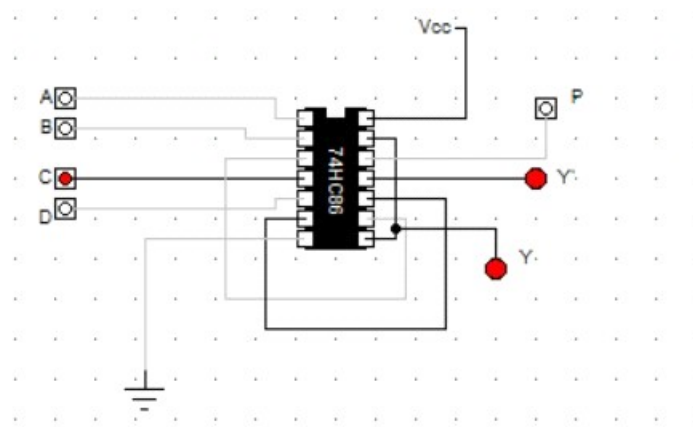
D=0 C=0 B=1 A=0 P=0 =>Y=1 Y'=0



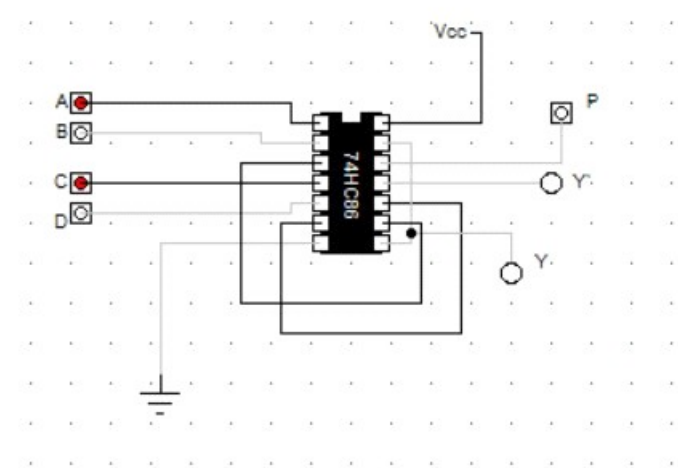
D=0 C=0 B=1 A=1 P=0 =>Y=0 Y'=1



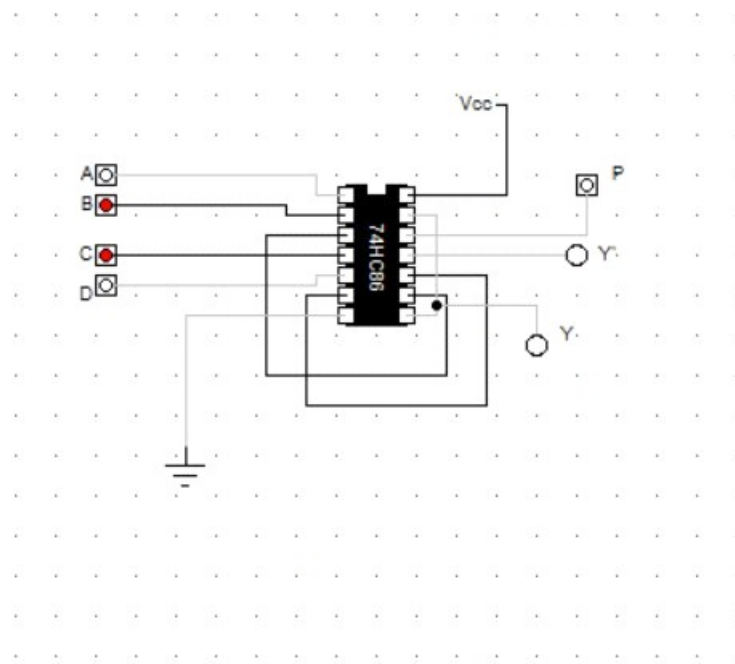
D=0 C=1 B=0 A=0 P=0 $\Rightarrow Y=1$ $Y'=1$



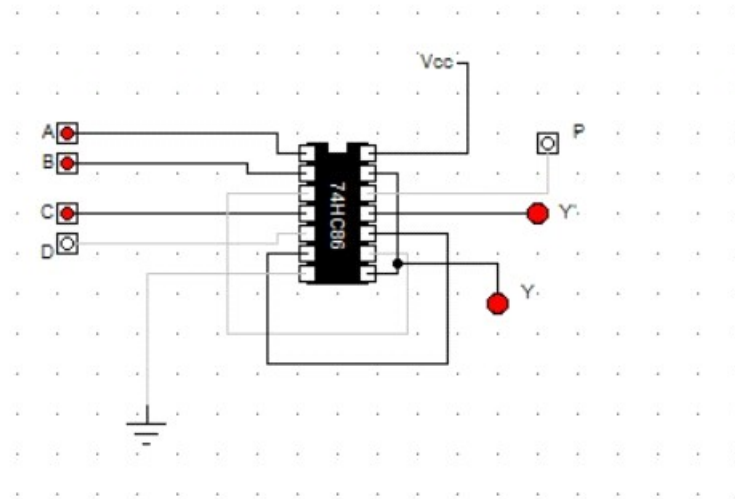
D=0 C=1 B=0 A=1 P=0 $\Rightarrow Y=0$ $Y'=0$



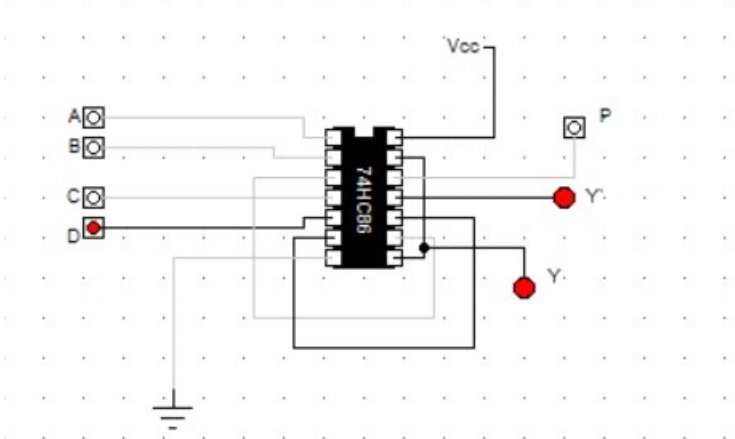
D=0 C=1 B=1 A=0 P=0 $\Rightarrow Y=0$ $Y'=1$



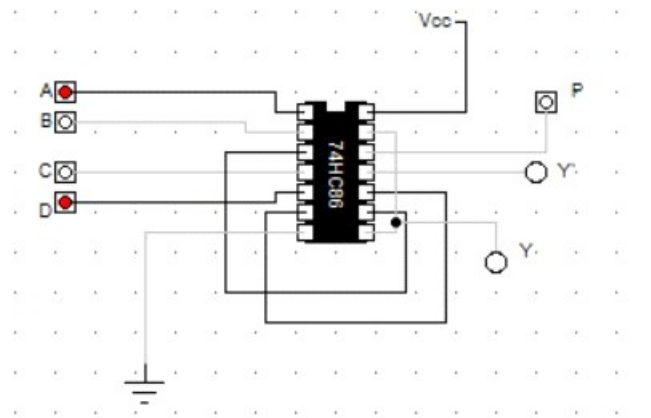
D=0 C=1 B=1 A=1 P=0 \Rightarrow Y=1 Y'=0



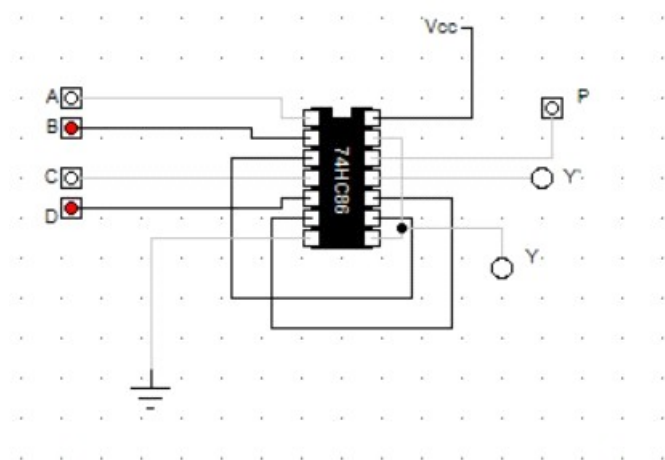
D=1 C=0 B=0 A=0 P=0 \Rightarrow Y=1 Y'=0



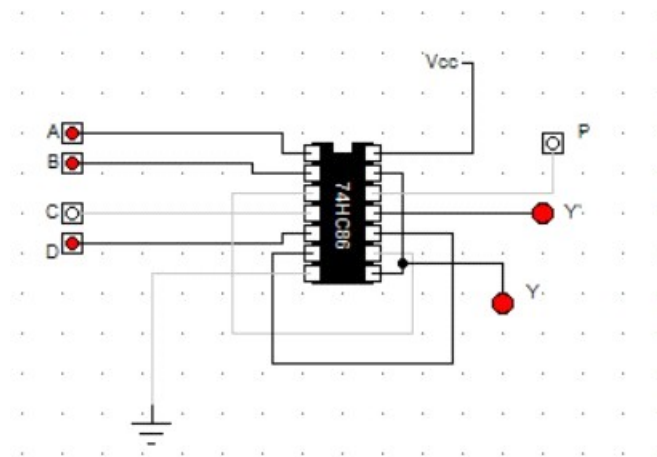
D=1 C=0 B=0 A=1 P=0 \Rightarrow Y=0 Y'=1



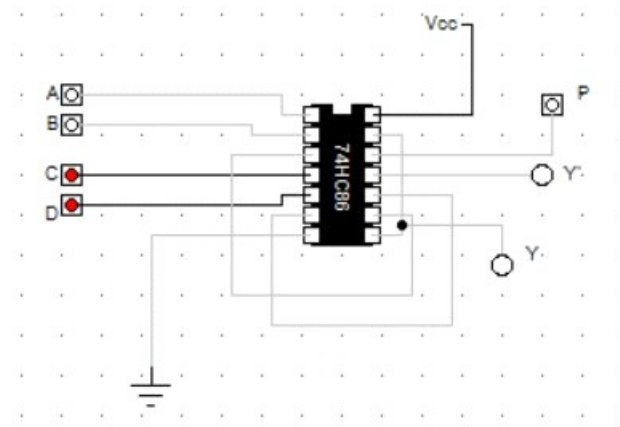
D=1 C=0 B=1 A=0 P=0 \Rightarrow Y=0 Y'=1



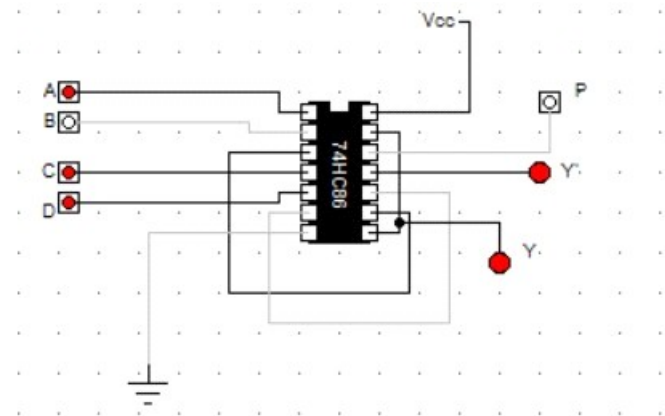
D=1 C=0 B=1 A=1 P=0 \Rightarrow Y=1 Y'=0



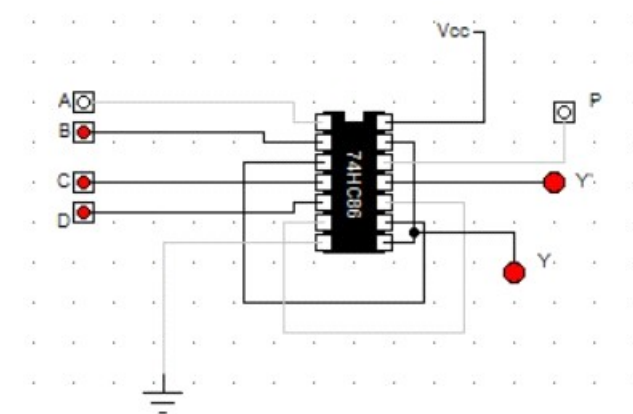
D=1 C=1 B=0 A=0 P=0 \Rightarrow Y=0 Y'=0



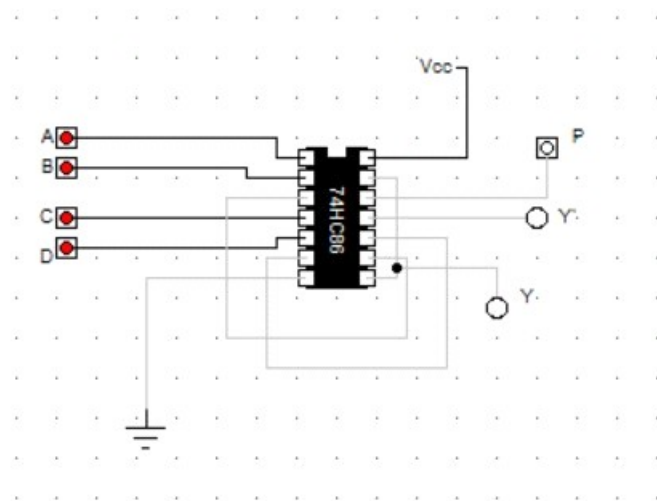
D=1 C=1 B=0 A=1 P=0 $\Rightarrow Y=1$ $Y'=1$



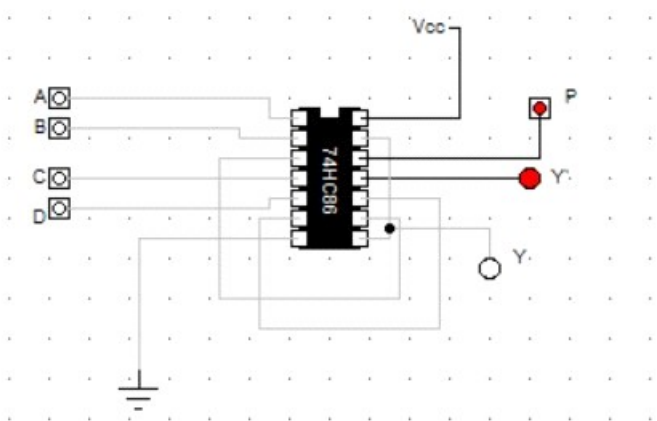
D=1 C=1 B=1 A=0 P=0 $\Rightarrow Y=1$ $Y'=1$



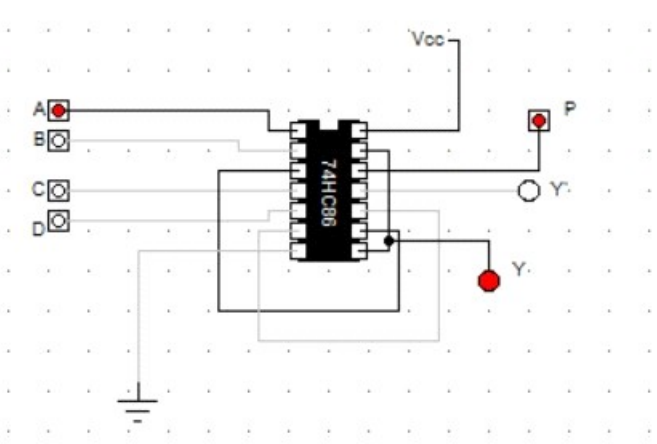
D=1 C=1 B=1 A=1 P=0 $\Rightarrow Y=0$ $Y'=1$



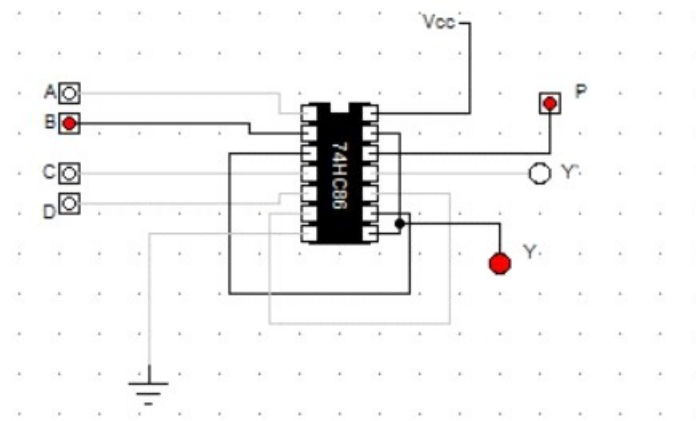
D=0 C=0 B=0 A=0 P=1 \Rightarrow Y=0 Y'=1



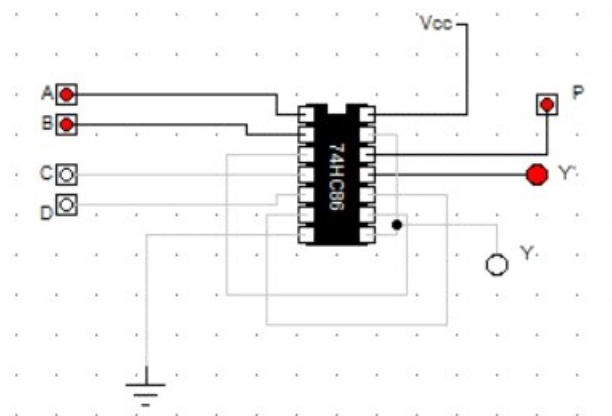
D=0 C=0 B=0 A=1 P=1 \Rightarrow Y=1 Y'=0



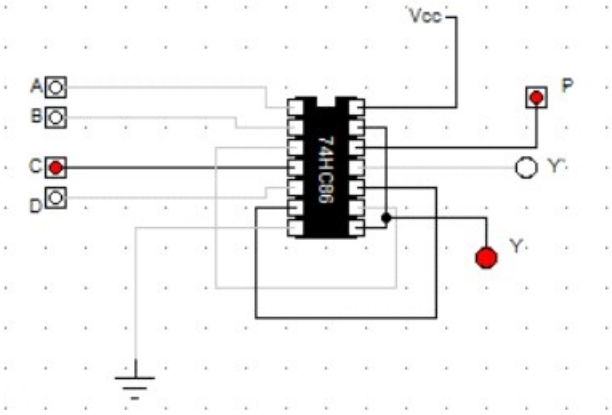
D=0 C=0 B=1 A=0 P=1 \Rightarrow Y=1 Y'=0



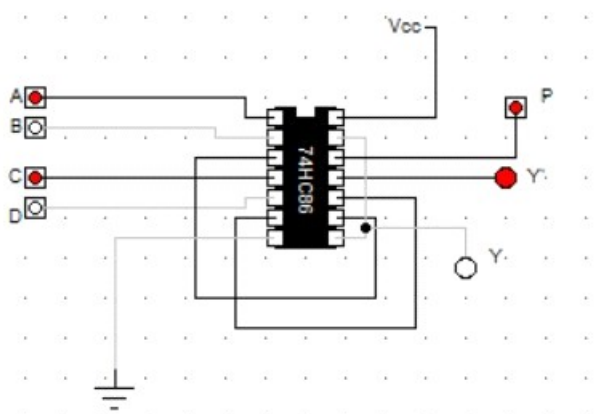
D=0 C=0 B=1 A=1 P=1 $\Rightarrow Y=0$ $Y'=1$



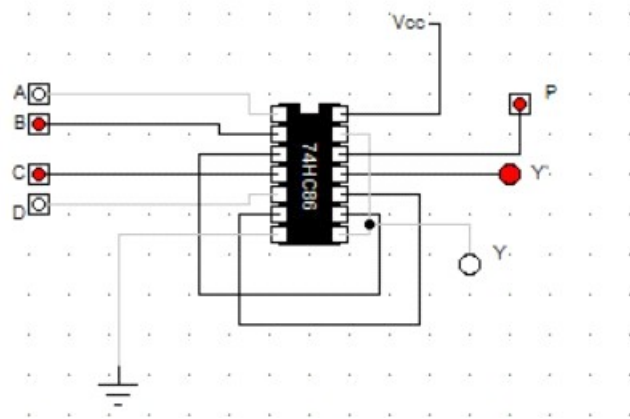
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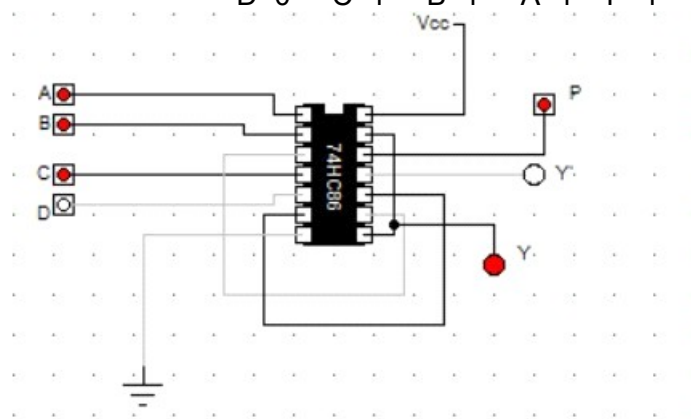
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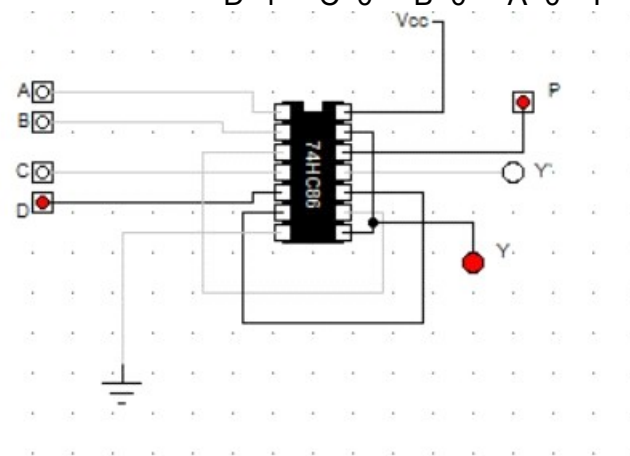
D=0 C=1 B=1 A=0 P=1 $\Rightarrow Y=0$ $Y'=1$



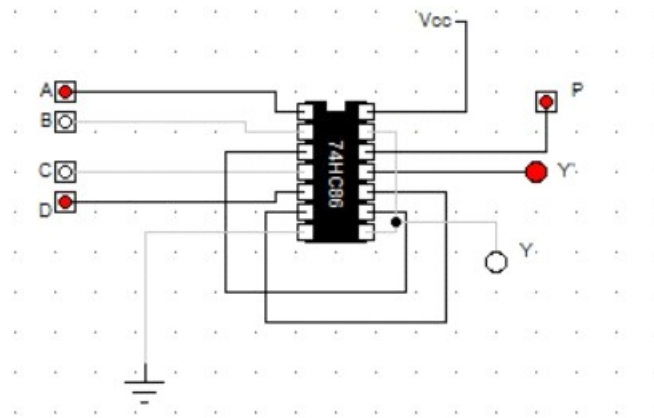
D=0 C=1 B=1 A=1 P=1 $\Rightarrow Y=1$ $Y'=0$



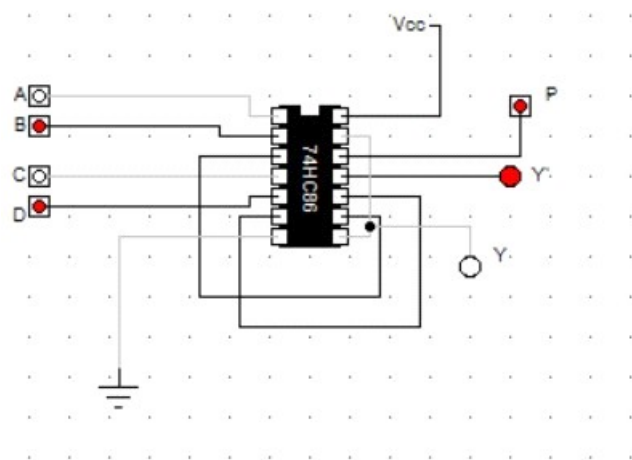
D=1 C=0 B=0 A=0 P=1 $\Rightarrow Y=1$ $Y'=0$



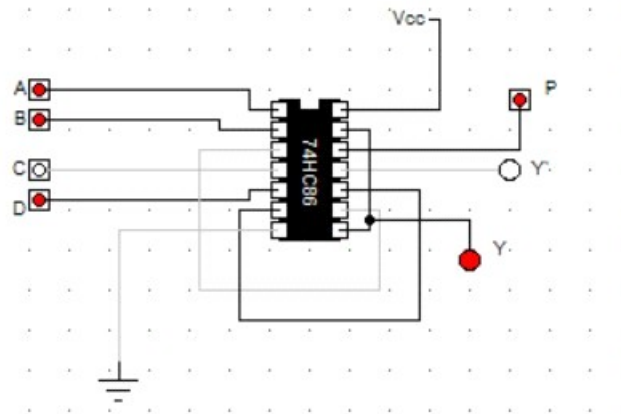
D=1 C=0 B=0 A=1 P=1 $\Rightarrow Y=0$ $Y'=1$



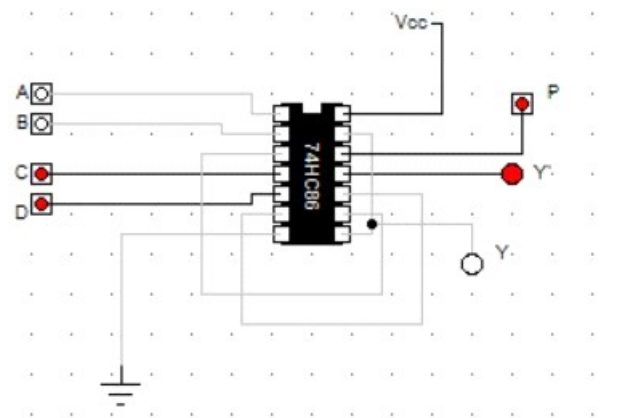
D=1 C=0 B=1 A=0 P=1 $\Rightarrow Y=0$ $Y'=1$



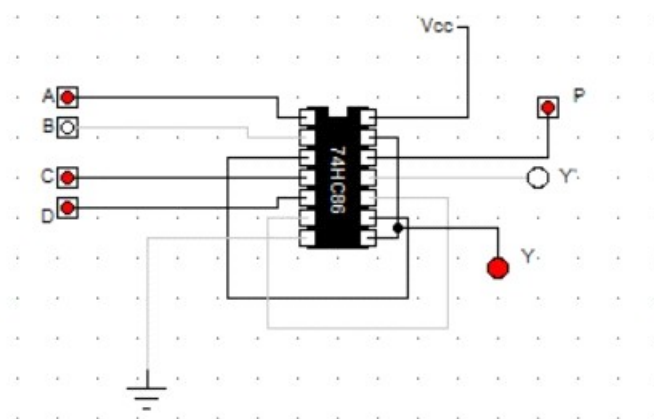
D=1 C=0 B=1 A=1 P=1 $\Rightarrow Y=1$ $Y'=0$



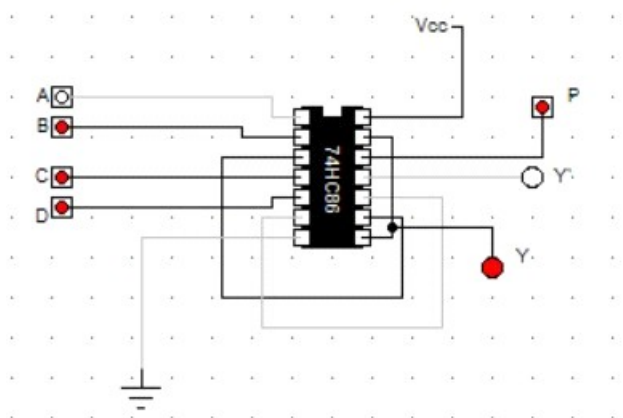
D=1 C=1 B=0 A=0 P=1 $\Rightarrow Y=0$ $Y'=1$



D=1 C=1 B=0 A=1 P=1 \Rightarrow Y=1 Y'=0



D=1 C=1 B=1 A=0 P=1 \Rightarrow Y=1 Y'=0



D=1 C=1 B=1 A=1 P=1 \Rightarrow Y=0 Y'=1

