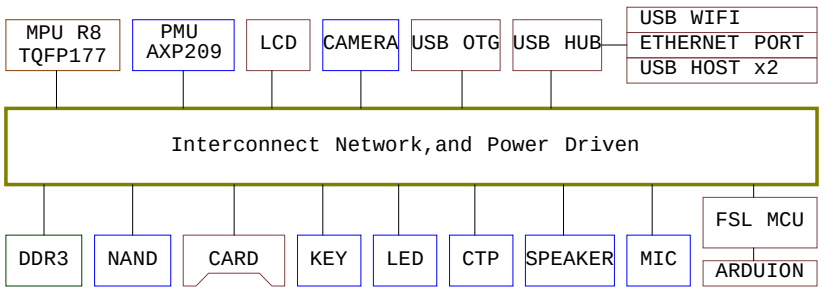
COVER

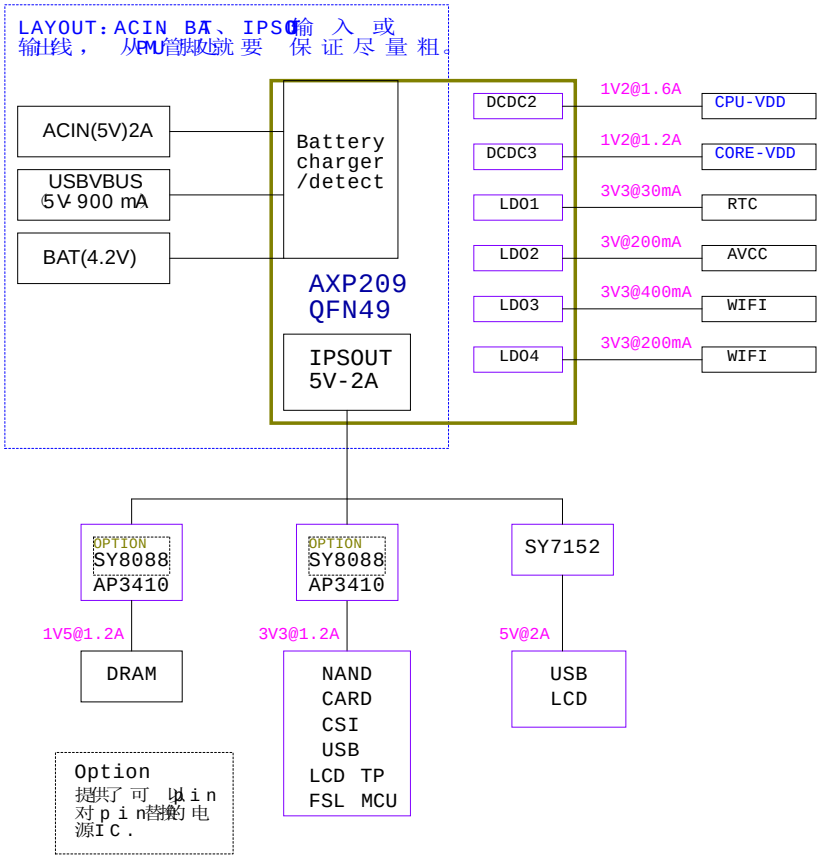
Schematics Index

特别提醒：
1:PG0 / PG1 / PG2这3个PIN脚
默认有INPUT下拉有功能。
2:PMU的GPIO0/1/2这3个PIN脚
默认GPIO-OUTPUT功能
3:PG10 / PG11 / PG12这3个PIN脚
的功能可改变。
4:CSI-PCLK / CSI-MCLK这2个PIN脚
默认有INPUT下拉有功能。
5:CSI-HSYNC默认有INPUT下拉有功能，
不建议用途。

BLOCK



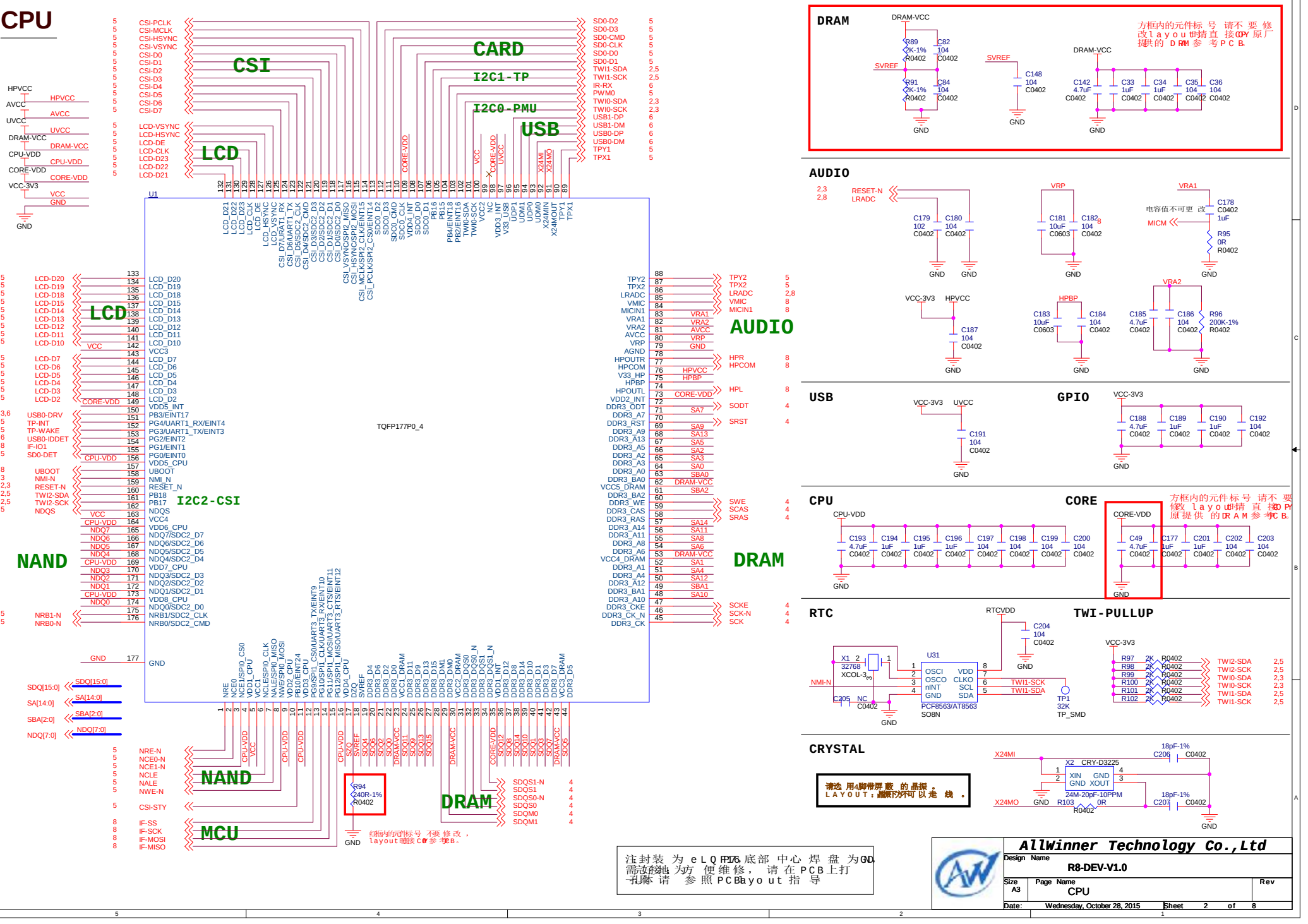
POWER TREE



REVISION HISTORY

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	R8-DEV-V1.0	2015-09-23	CHS		

AllWinner Technology Co.,Ltd
Design Name: R8-DEV-V1.0
Size: A3 | Page Name: COVER | Rev:
Date: Wednesday, October 28, 2015 | Sheet 1 of 8


CPU
CSI
CARD
I2C1-TP
I2C0-PMU
USB
LCD
AUDIO
NAND
I2C2-CSI
DRAM
MCU
TQFP177P0_4
DRAM
AUDIO
USB
GPIO
CPU
CORE
RTC
TWI-PULLUP
CRYSTAL
方框内的元件标号 请不要修改layout时请直接COPY原厂提供的DRAM参考PCB.
请选用4脚带屏蔽的晶振。
LAYOUT：晶振下方不可以走线。
注封装为eLQFP176底部中心焊盘为GND需就近地为方便维修，请在PCB上打孔接请参照PCB layout指导
AllWinner Technology Co.,Ltd
R8-DEV-V1.0
CPU
Wednesday, October 28, 2015

POWER

POWER LINE:Width>=80mil POWER LINE:Width>=50mil

BATTARY IN

5V DCIN

IPSOUT TO 1V6

IPSOUT TO 3V3

IPSOUT TO 5V

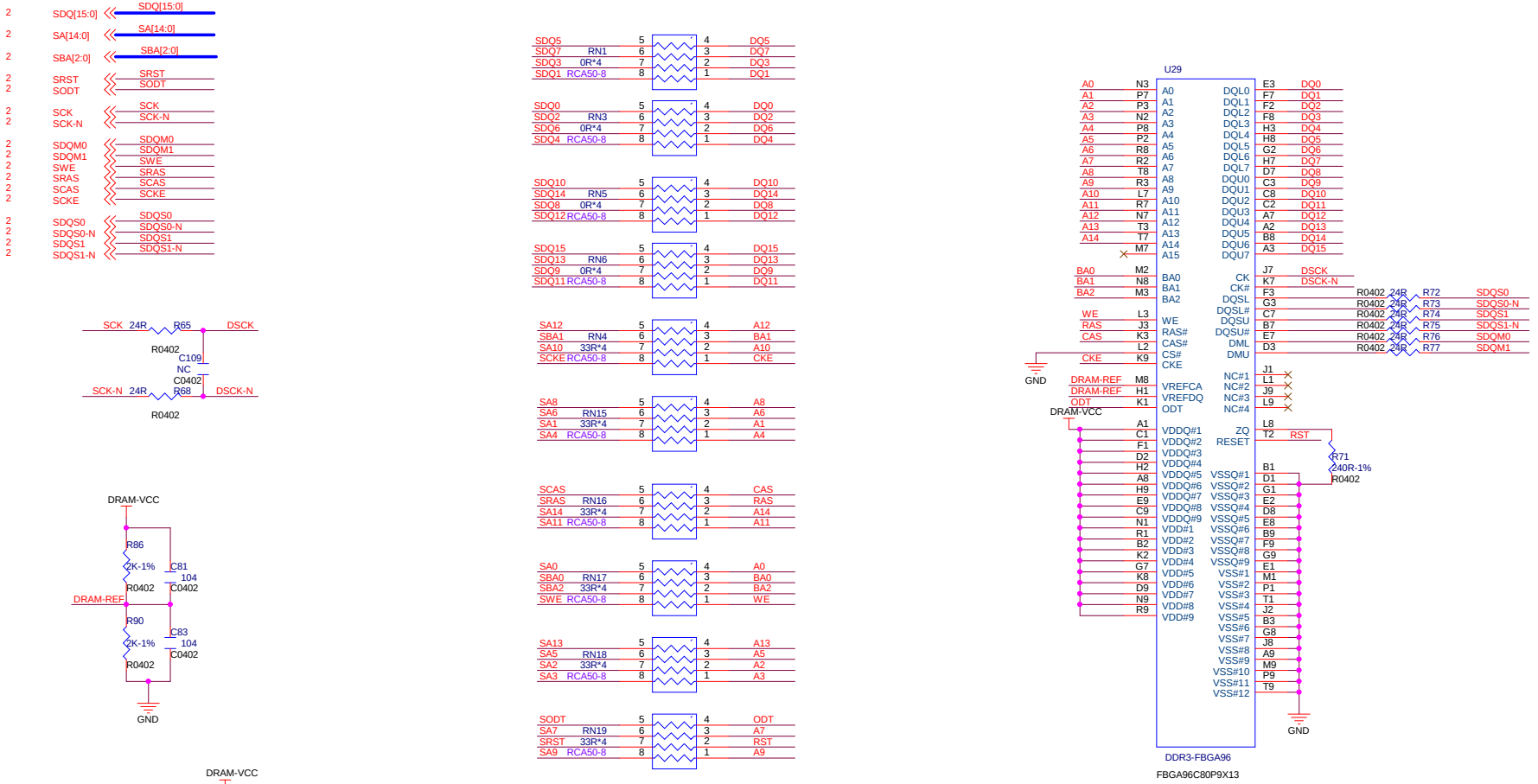
注2.2uH-DCR<0.1R-1.5A
表示在1.5A的电流电感感量还满足2.2uH
DCR<0.1R表示电流电阻要小于0.1欧姆

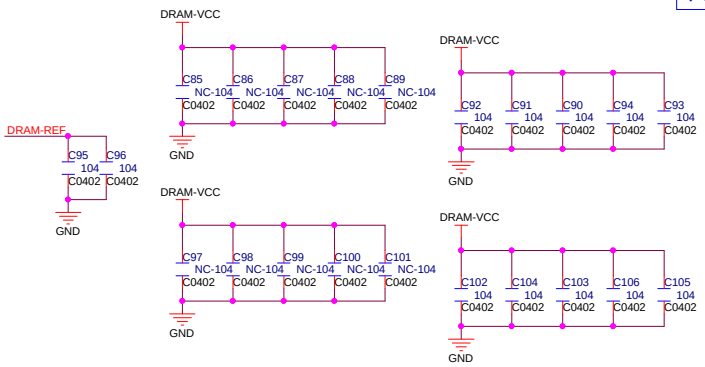
AllWinner Technology Co.,Ltd			
Design Name: R8-DEV-V1.0			
Size: A3	Page Name: POWER		Rev
Date: Wednesday, October 28, 2015	Sheet 3 of 8		

DDR3 16x1

DDR3

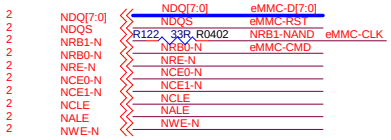
本页的元件标号 请 不要 修 改
layout时直 接 COPY原厂提 供
的DRAM参考 P C B



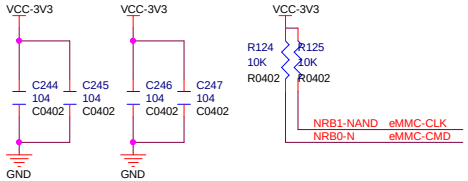


AllWinner Technology Co.,Ltd			
Design Name: R8-DEV-V1.0			
Size: A3	Page Name: DDR3 16x1		Rev
Date: Wednesday, October 28, 2015	Sheet 4 of 8		

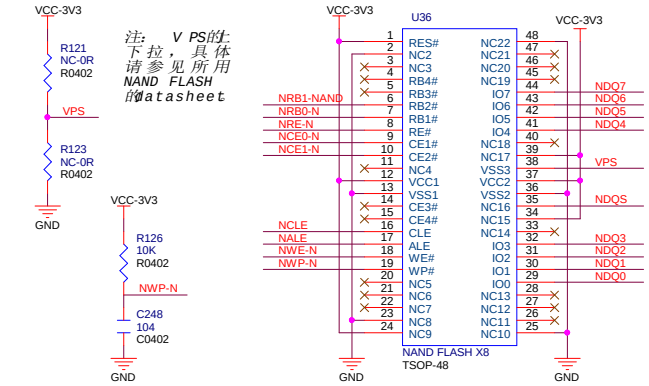
NAND/CARD/LCD TP/CAMERA



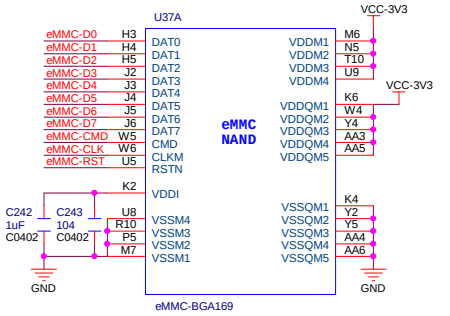
Put 33R close to CPU.



NAND

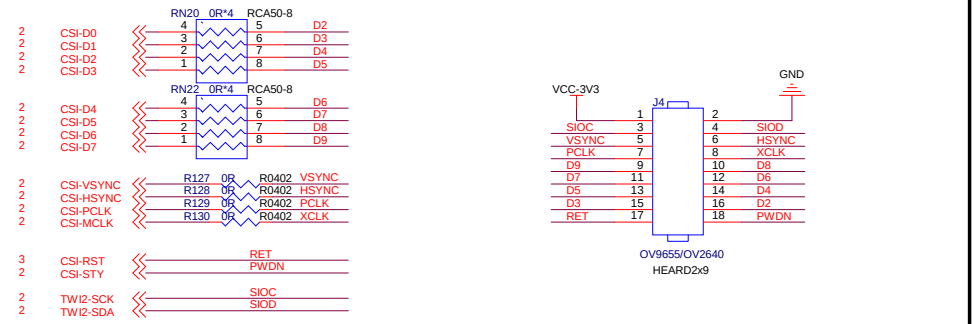


eMMC

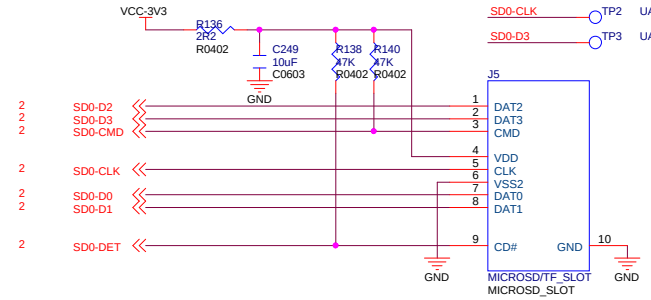


Both eMMC NAND and first TSOP NAND layout together

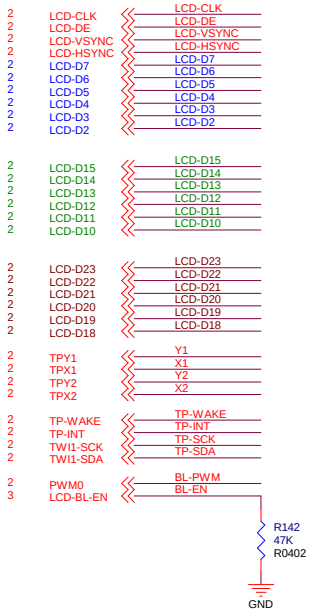
CSI

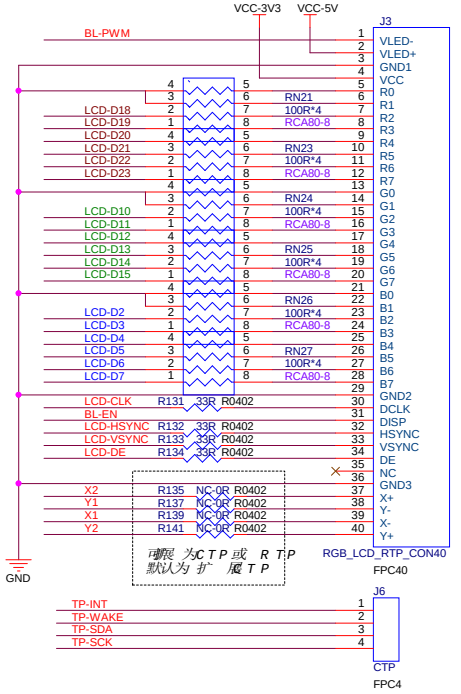


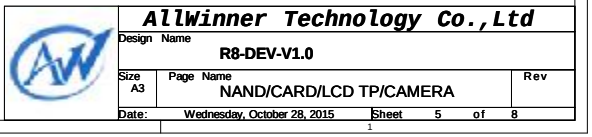
CARD



LCD TP

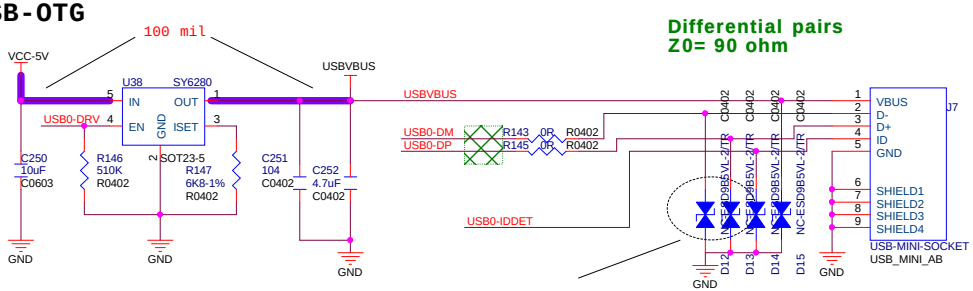






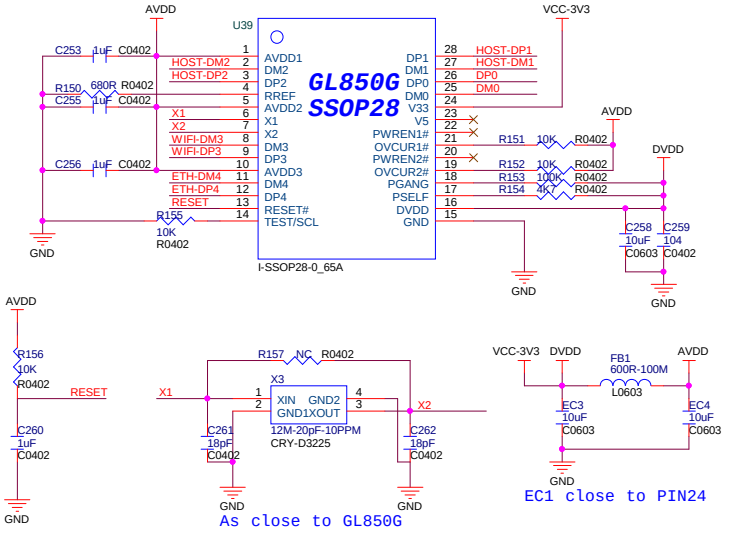
USB/WIFI/IR

USB-OTG

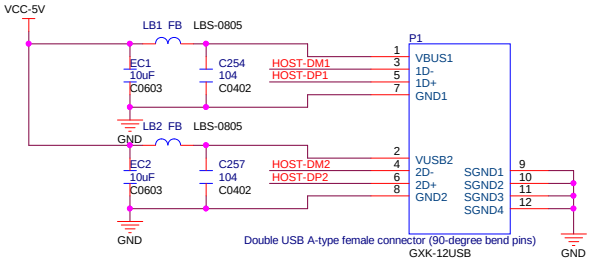


D+/D- 上的 ESD 器件电容小于等于 4 pF(包括了误差)。

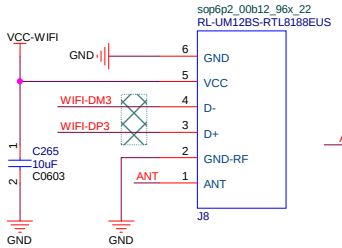
USB-HUB

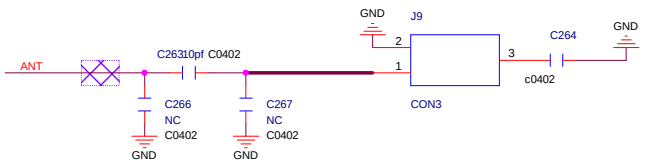


USB-HOST

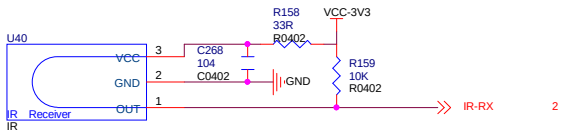


USB-WIFI





IR



USB-ETHERNET

AllWinner Technology Co.,Ltd			
Design Name: R8-DEV-V1.0			
Size: A3	Page Name: USB/WIFI/IR		Rev
Date: Wednesday, October 28, 2015	Sheet 6 of 8		

ETHERNET

*Note2-9:
For self-power applications, please refer to below suggestions to design the V_BUS signal circuit,
(1)While the USB interface was connected to USB host/hub controller, the V_BUS signal MUST be pulled high to set AX88772C/AX88772B at normal operation stage.
(2)While the USB interface was disconnected from USB host/hub controller, the V_BUS signal MUST be pulled down to set AX88772C/AX88772B at reset stage.

*Note2-1:
The C269 cap between the DP and DM pins is used to filter the common-mode noise and should be placed as close as pin #57 and #56.

USB to Ethernet

*Note2-9

*Note2-1

VCC-5V
ETH-DM
ETH-DP
C270 104 C0402
C271 4.7uF C0402
C269 3.3pF C0402
R160 4K7 R0402
R161 330 R0402
D16 LED-Y R0603
USB_ACT
VCC-3V3
GND

U41
V_BUS
DM
DP
MFA_3 / PHY_N
RESET_N
TEST1
TEST0
RREF
TCLK_EN
TCLK_0
TCLK_1
X2
X1
RSET_BG
EXTWAKEUP_N
EEDIO
EECK
EECS
GND18A_PLL
GND33A_H
GND33A_PLL
GND3R3
GND4
GND3
GND2
GND1
GND18A3
GND18A2
GND18A1
XTL25P
XTL25N
RXIN
RXIP
TXON
TXOP
MFB_0
MFB_1 / CRSDV
MFB_2 / TXEN
MFB_3 / TXD1
MFB_4 / TXD0
MFB_5 / REF50M
MFB_6 / RXD1
MFB_7 / RXD0
GPIO_0 / PME
GPIO_1
GPIO_2
SD
MFA_2 / RMII_N
MFA_1 / MDIO
MFA_0 / MDC
LINK
VCC3R3
VCC3A3
VCC33A_PLL
VCC33A_H
VCC3IO1
VCC3IO2
V18F
VCC18A1
VCC18A2
VCC18A_PLL
VCCK1
VCCK2
VCCK3
VCCK4
LQFP64_7X7

AX88772C
AX88772B

TP4 TP TP_SMD
TP5 TP TP_SMD
TP6 TP TP_SMD
TP7 TP TP_SMD
TP8 TP TP_SMD

*Note2-5:
The SD signal should be connected to GND directly or through a 4.7K resistor at copper mode.

D17 R0603 LED-G
R170330 R0402

*Note2-2:
The RC reset circuit is optional for AX88772C/AX88772B applications. You can reserve the RC reset circuit on your AX88772C/AX88772B schematic to fine tune the reset timing if necessary.

Reset Circuit

VCC-3V3
*Note2-2
R169 NC/39K R0402
RESET_N
C273 NC/0.47uF C0402
GND
Optional

93C56 or 93C66 EEPROM

U42
GND DO
ORG DI
NC SK
VCC CS
93C66
TSSOP_8
R166 4K7
R0402
C272 104 C0402
R165 22 R0402
R167 22 R0402
*Note2-3

*Note2-3:
The AX88772C/AX88772B supports 16-bit mode 93C56/93C66 EEPROM. The R166 resistor is mounted to set the ATMEL AT93C66A EEPROM to 16-bit mode.

J10 JUMPER
R0402
R163 12K1-1% R0402
R164 R0402 4K7

*Note2-6:
The 1M feedback resistor is necessary for 25MHz crystal circuit. The reference 25MHz crystal is the NSK NXH-32 SMD 25MHz crystal with CL 20pF and ESR max. 70 Ohm. The 25MHz clock signals should be within 25MHz +- 50ppm.
Please reserve the R171 0 Ohm resistor on 25MHz crystal circuit for fine tuning the 25MHz crystal circuit if necessary.

25MHz +- 30ppm Crystal *Note2-6

R168 1M R0402
R171 0R R0402
XTL25N
XTL25P
Y1
25M CRYSTAL
XTAL-5X3_2
NSK NXH-32 SMD
C274 33P C0402
C275 33P C0402

3.3V to 1.8V *Note2-4 On-chip Regulator

*Note2-4:
AX88772C/AX88772B on-chip 3.3V to 1.8V regulator is a low dropout regulator (LDO), which requires some large external compensating capacitors on its input (pin #52) and output (pin #51) pins. The C283, C284, C728 and C279 capacitors are the compensating capacitors for the on-chip regulator.
The analog powers and digital powers should be isolated with a Ferrite Bead (L7, L8).
The VC3R3 trace should be wider than 40mil for good power regulation.
The V18F trace should be wider than 20mil for good power regulation.

A3V3
L7 TI160808U110T L0603
C276 104 C0402
C277 4.7uF/10V C0603
D3V3
C283 4.7uF/10V C0603
C284 104 C0402
D1V8
L8 TI160808U110T L0603
C278 4.7uF/10V C0603
C279 104 C0402
C280 4.7uF/10V C0603
A1V8
C281 104 C0402

Power and by-pass capacitors

Close to pin 16.44
VCC-3V3
D3V3
C286 104 C0402
C287 104 C0402

Close to pin 6.59.60
A3V3
C288 104 C0402
C289 104 C0402

Close to pin 20.24.36.49
D1V8
C293 104 C0402
C294 104 C0402
C295 104 C0402
C296 104 C0402

Close to pin 1.11.64
A1V8
C297 104 C0402
C298 104 C0402
C299 104 C0402

RJ-45 Connector + Tranformer*Note2-7

*Note2-7:
Please refer to Section 4 of AX88772C/AX88772B USB to LAN Application Design Note for more details of the Ethernet magnetics reference circuits.

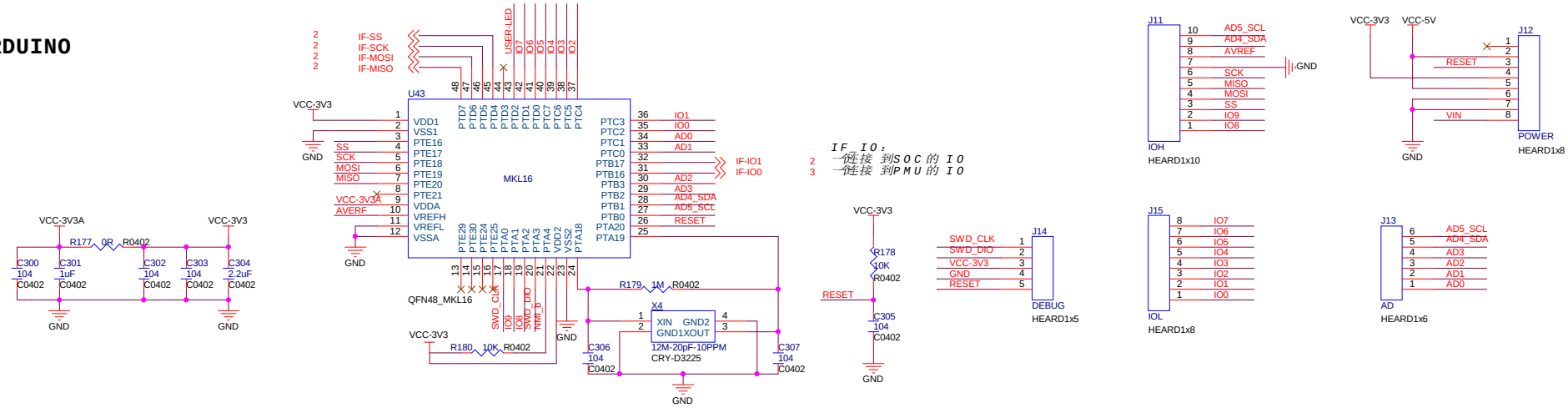
BOTHHAND NS0013LF Tranformer
(Turns Ratio 1CT:1CT,
without auto-MDIX)

C282 104 C0402
R172 49R9 R0402
R173 49R9 R0402
T1
GND1 RX-
GND2 RX+
RD+
RD- CRX
CRD CTX
CTD
TD+ TX-
TD- TX+
NC12
NC13
H1102NL
H1102NL
RXIP
RXIN
A3V3
C285 104 C0402
TXOP
TXON
R174 49R9 R0402
R175 49R9 R0402
C290 104 C0402
T2
NC4 E1
NC3
RX-
NC2
NC1
RX+
TX-
TX+ E2
C10001-108A4
RJ45-A
*Note2-8
RN28 75 RCA50-8
*Note2-8:
The C292 capacitor can be 1uF or 1000pF/2KV (for a better ESD protection)
C291 1000pF/2KV C1206
R176 1M R1206
C292 1000pF/2KV C1206
ETH_CHASSIS_GND

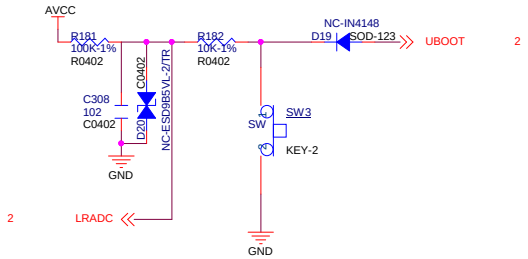
AllWinner Technology Co.,Ltd		
Design Name: R8-DEV-V1.0		
Size: A3	Page Name: ETHERNET	Rev
Date: Wednesday, October 28, 2015	Sheet 7 of 8	

ARDUINO/KEY/LED/AUDIO

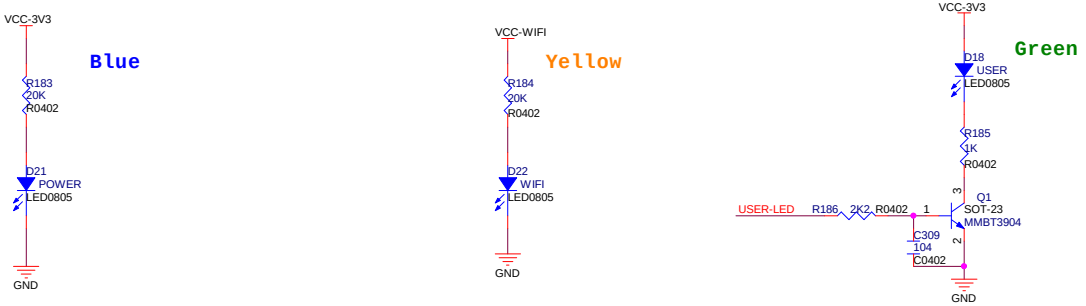
ARDUINO



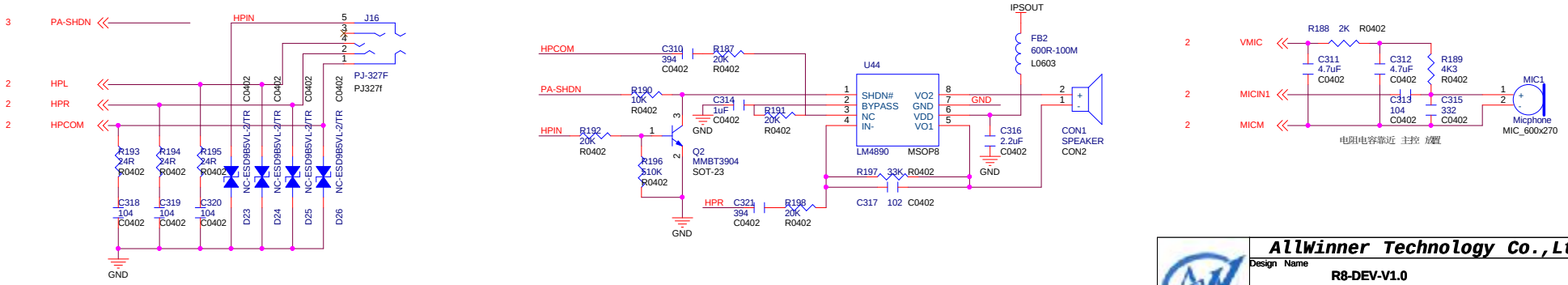
KEY



LED



HEADPHONE & SPEAKER & MIC



AllWinner Technology Co.,Ltd		
Design Name: R8-DEV-V1.0		
Size: A3	Page Name: ARDUINO/KEY/LED/AUDIO	Rev
Date: Wednesday, October 28, 2015	Sheet 8 of 8	