

[illegible]

2 USB0-DM <<>
2 USB0-DP <<>
2 USB0-IDET <<> USB0-IDET

VCC-3V3
R99
10K
R0402

D⁺ / D⁻ 上的ES器件电容小于等于4 pF(包括了误差)。

DISPLAY

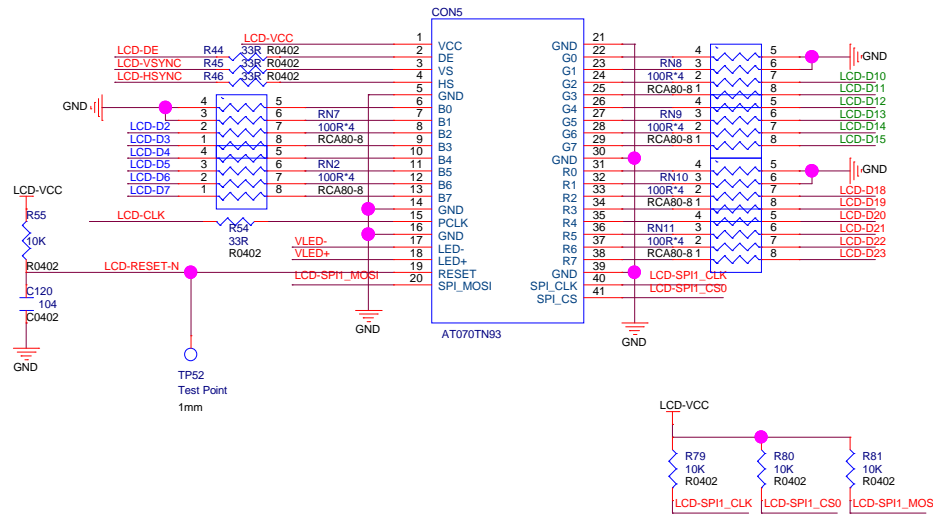
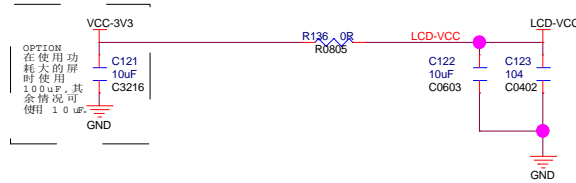
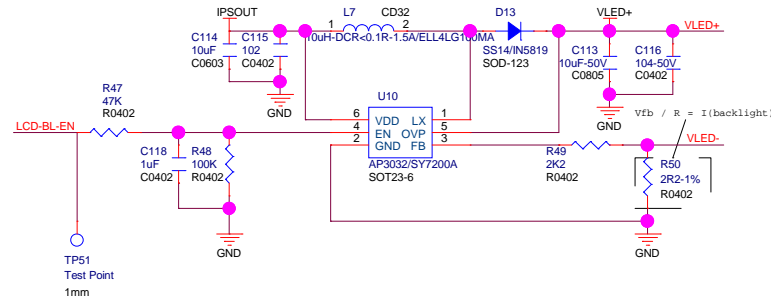
LCD

2 LCD-CLK
2 LCD-DE
2 LCD-VSYNC
2 LCD-HSYNC
2 LCD-D7
2 LCD-D6
2 LCD-D5
2 LCD-D4
2 LCD-D3
2 LCD-D2
2 LCD-D15
2 LCD-D14
2 LCD-D13
2 LCD-D12
2 LCD-D11
2 LCD-D10
2 LCD-D23
2 LCD-D22
2 LCD-D21
2 LCD-D20
2 LCD-D19
2 LCD-D18
2 LCD-BL-EN

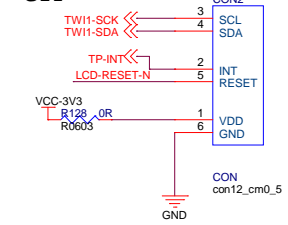
2 LCD-RESET-N

2 LCD-SPH1_CS0
2 LCD-SPH1_CLK
2 LCD-SPH1_MOSI

TP53 Test Point 1mm
TP54 Test Point 1mm
TP55 Test Point 1mm



CTP



电容屏信号连接示意图

FLASH/CARD

- 2

ND[7:0]

<<

ND[7:0]
- 2

NDQS

<<

NDQS
- 2

NRB0-N

<<

NRB0-N
- 2

NRE-N

<<

NRE-N
- 2

NCE0-N

<<

NCE0-N
- 2

NCE1-N

<<

NCE1-N
- 2

NCLE

<<

NCLE
- 2

NALE

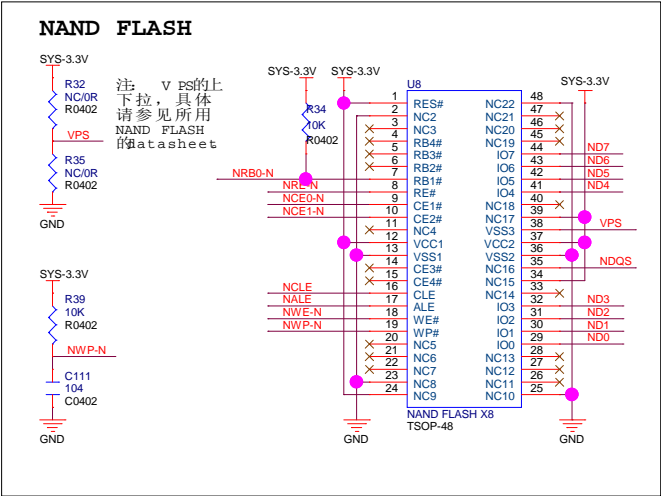
<<

NALE
- 2

NWE-N

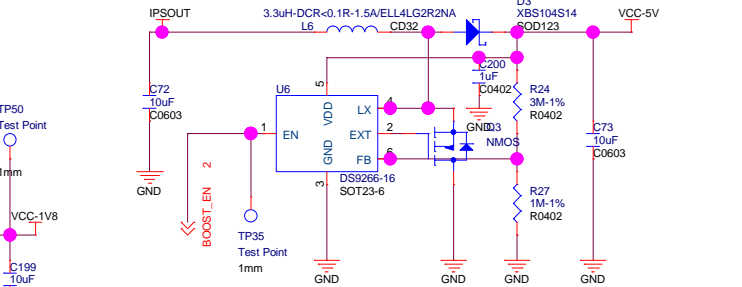
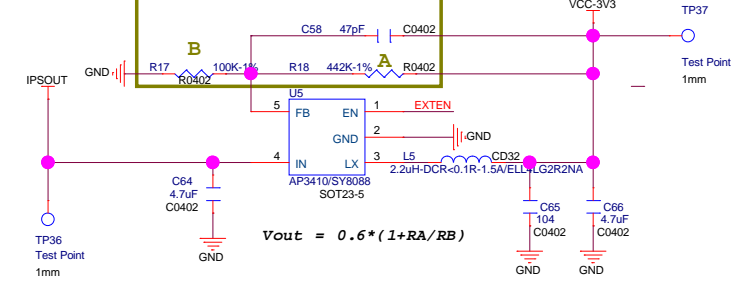
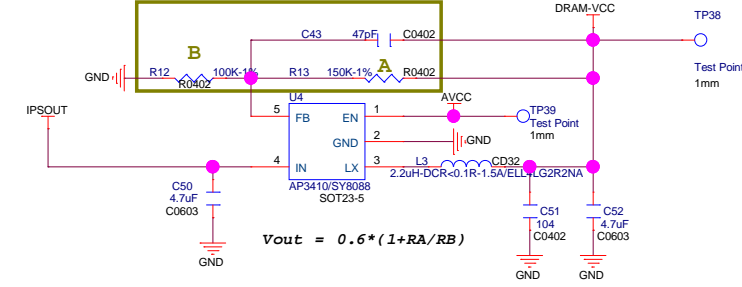
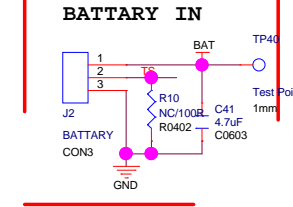
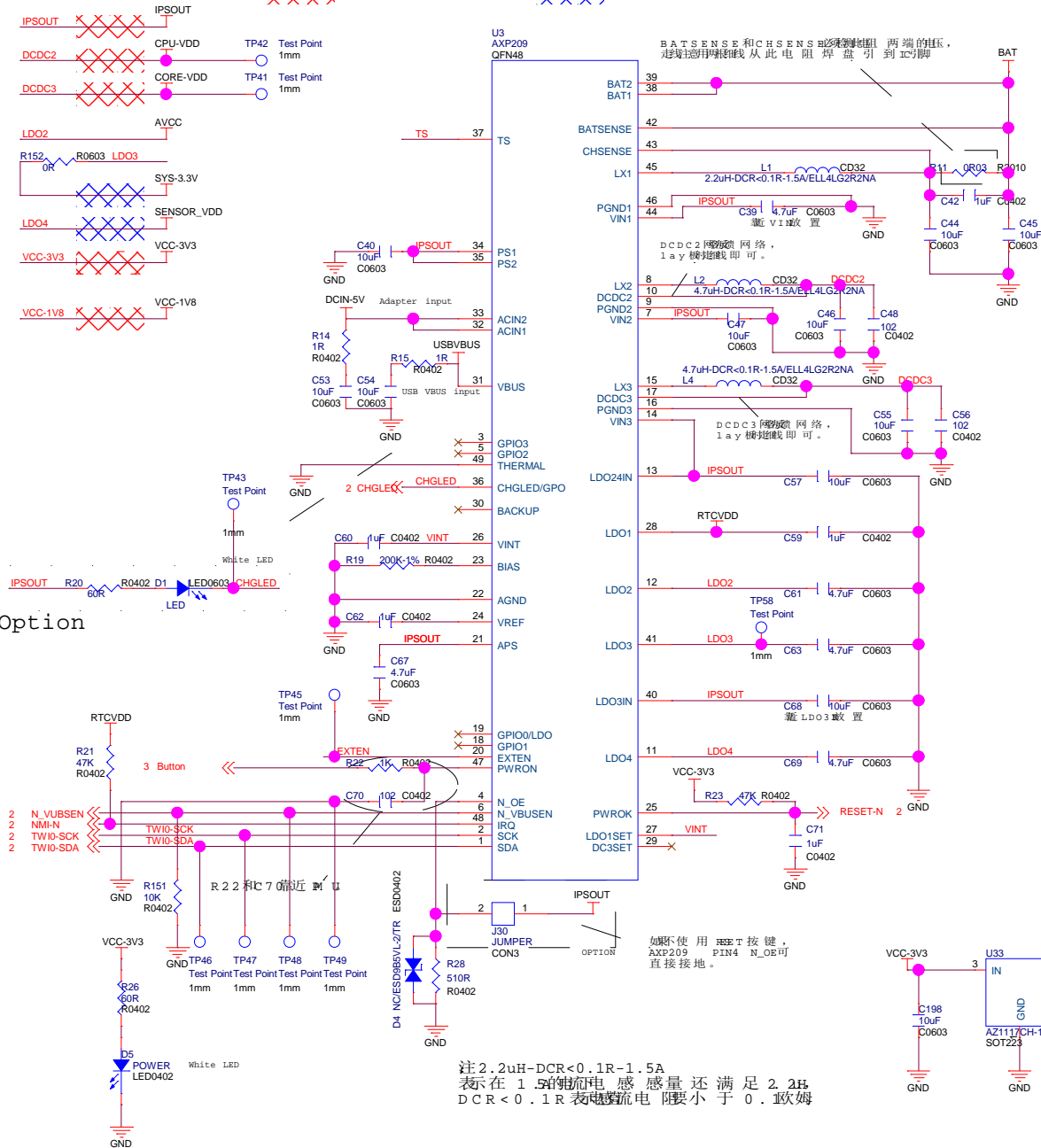
<<

NWE-N



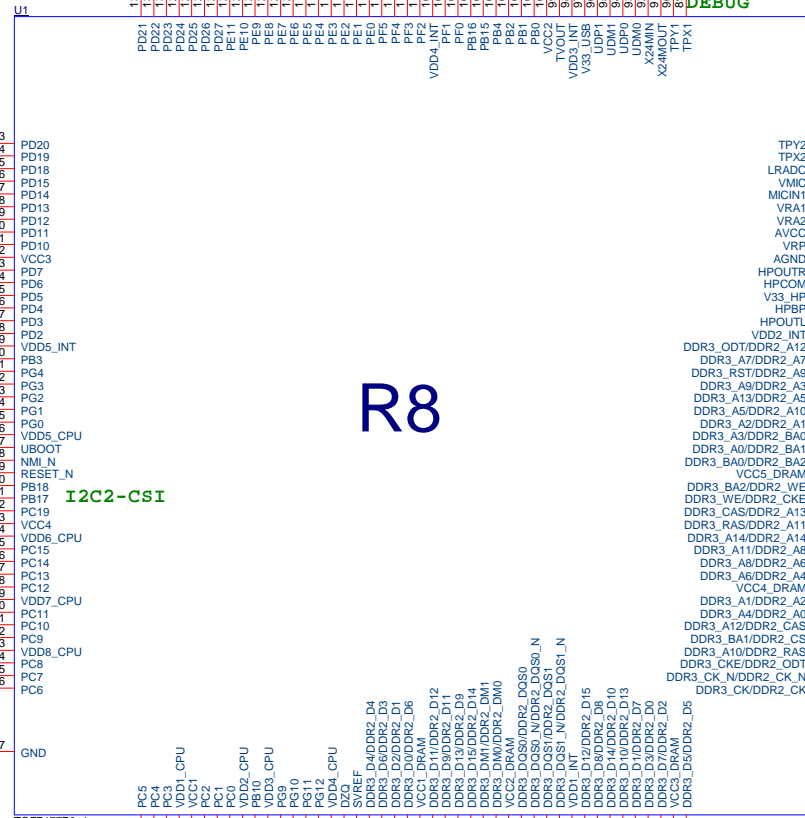
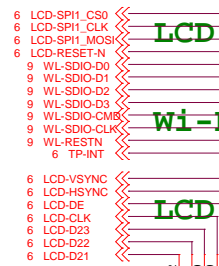
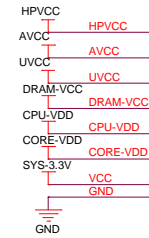
POWER

POWER LINE:Width>=80mil POWER LINE:Width>=50mil



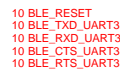
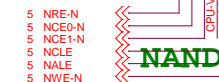
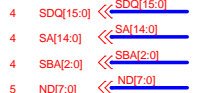
注2.2uH-DCR<0.1R-1.5A
表示在1.5A的电流下感量还满足2.2uH
DCR<0.1R表示感流阻要小于0.1欧姆

CPU



R8

NAND



NAND

BLE

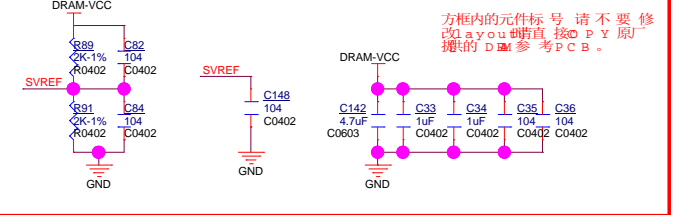
DRAM

红圈内的元件标号 不要修改，
Layout时请参考C参考图B。



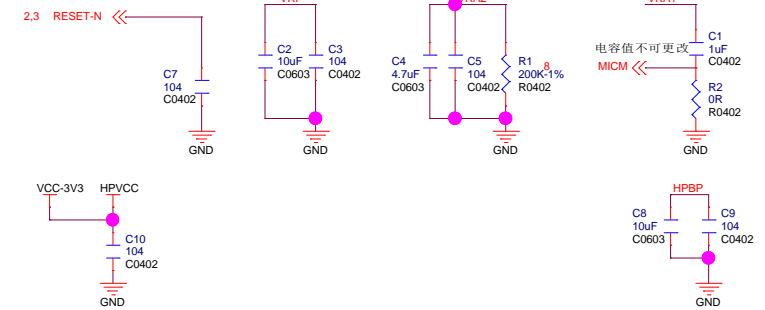
注封装为 eLQ BGA 底部中心焊盘为 GND
需焊接 为方便维修，请在 PCB 上打
孔 请参考 PCB layout 指导。

DRAM

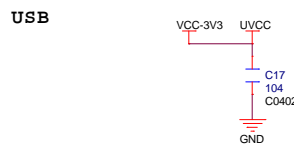


方框内的元件标号 请不要修
改 layout 时直接 COPY 原
图的 DRAM 参考 PCB。

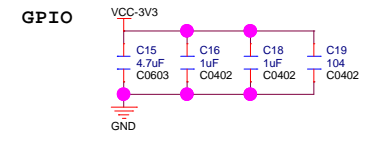
AUDIO-TP



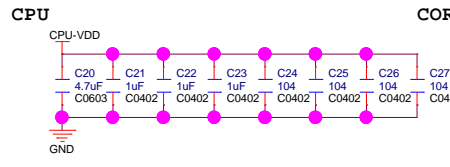
USB



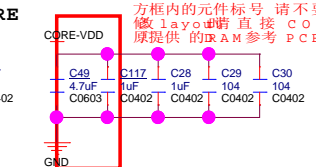
GPIO



CPU

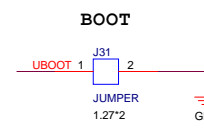


CORE

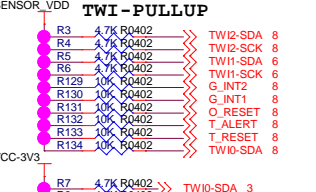


方框内的元件标号 请不要修
改 layout 时直接 COPY 原
图提供的 DRAM 参考 PCB。

BOOT

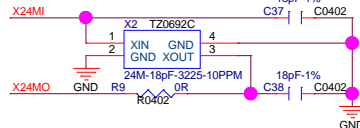


SENSOR_VDD



CRYSTAL

请选用 4脚带屏蔽的晶振。
Layout 时不可走线。



COVER

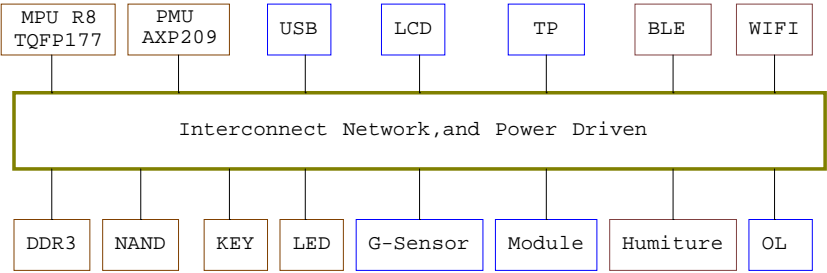
Schematics Index

Bran-Design

- 01 COVER
- 02 CPU
- 03 POWER
- 04 DDR3 16x1
- 05 FLASH
- 06 DISPLAY
- 07 PERIPHERS
- 08 SENSOR
- 09 WI-FI
- Option:
- 10 BLE

特别提醒：
1:PG0 / PG1 / PG这个IN脚
具有INPUT功能。
2:PM的GPIO0/1/2这四个IN脚
做GPIO-OUTPUT功能
3:PG10 / PG11 / PG1这个IN脚
的能可改变。
4:CSI-PCLK / CSI-MCLK这个IN脚
具有INPUT功能。
5:CSI-HSYNC具有INPUT功能，
不能用途。

BLOCK

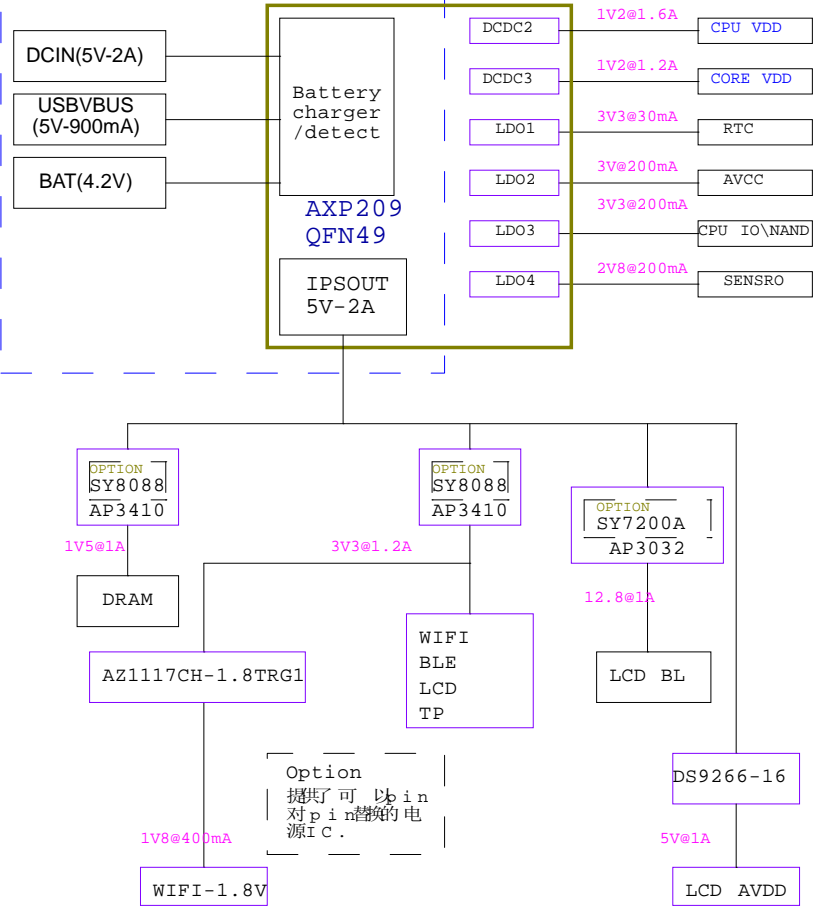


REVISION HISTORY

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Bran Main PCB ASSY	2016/6/2	Violet/Jemmey	Jemmey	

POWER TREE

LAYOUT: DCIN, BT, IPSOUT 输入或
输出线，从管脚处就要保证尽量粗。

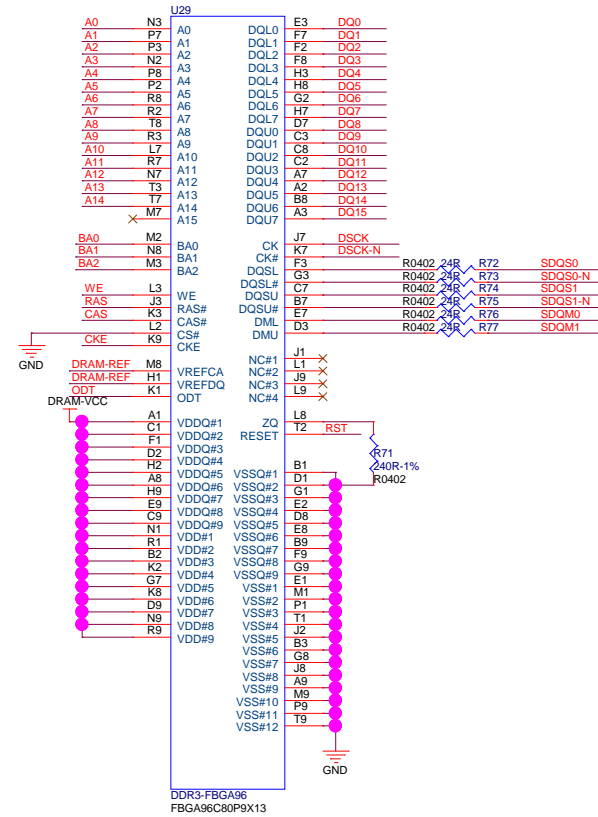
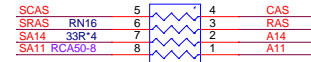
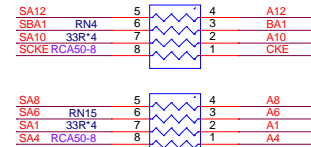
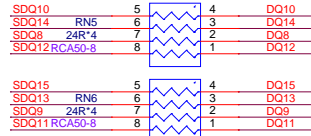
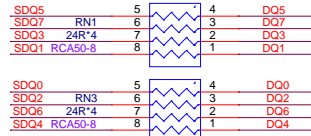
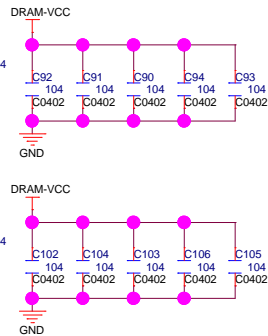
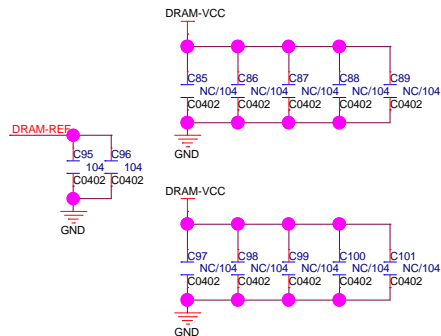
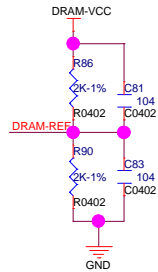
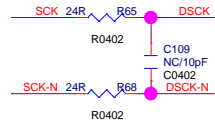


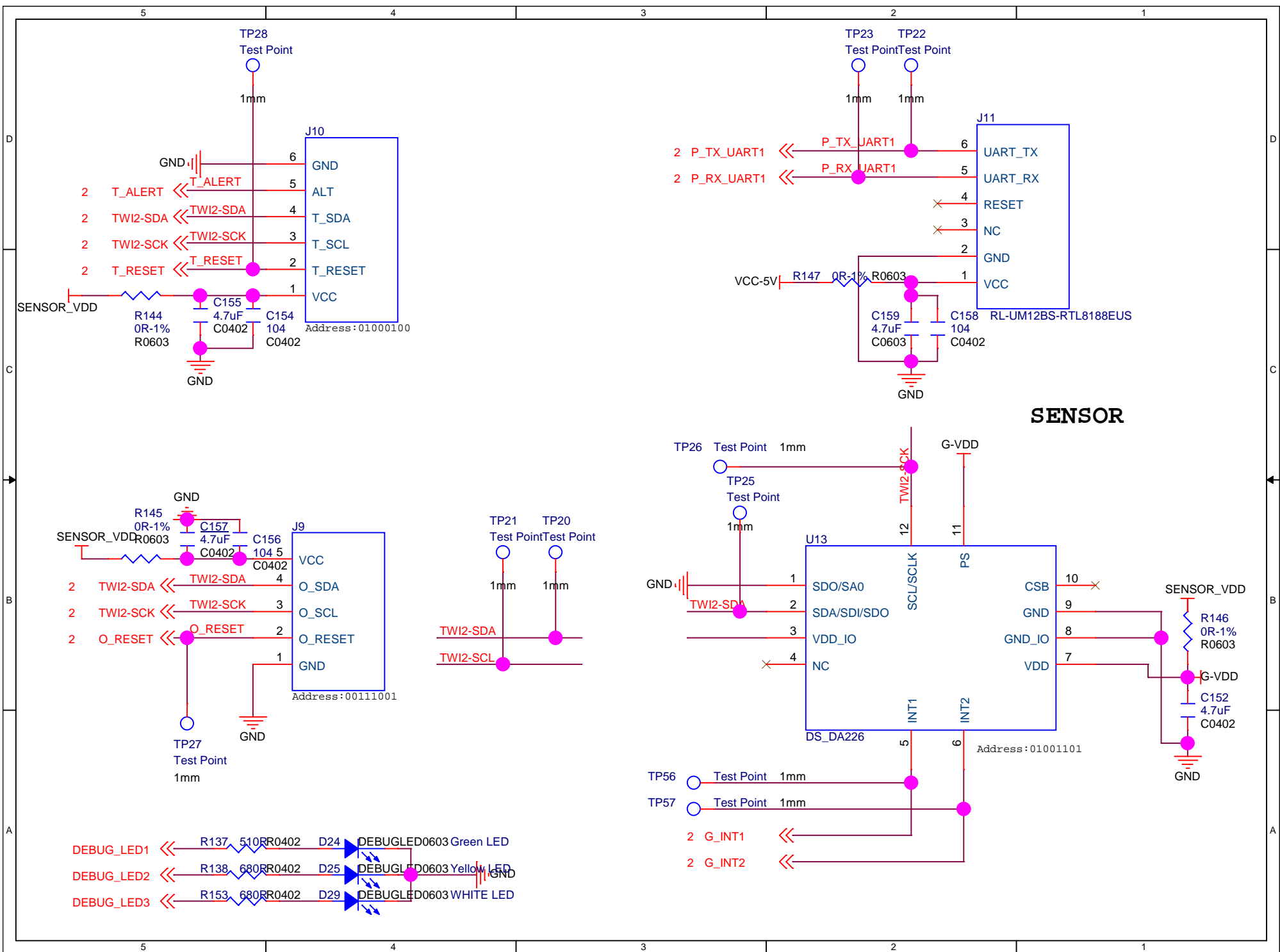
DDR3 16x1

DDR3

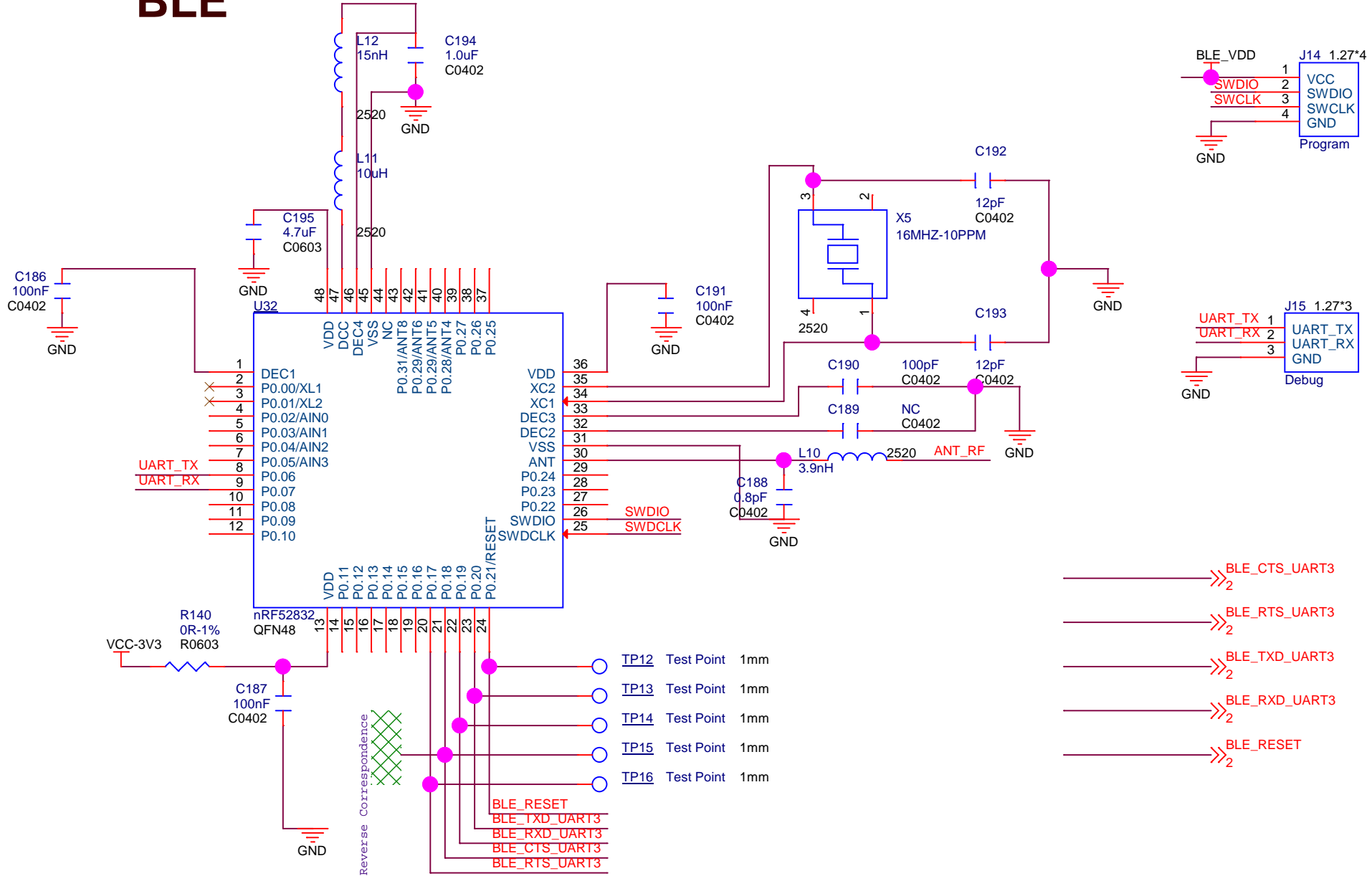
本页的元件标号 请 不要 修改
layout 时 直接 由 原厂 提供
的 参考 PCB

2	SDQ[15:0]	SDQ[15:0]
2	SA[14:0]	SA[14:0]
2	SBA[2:0]	SBA[2:0]
2	SRST	SRST
2	SODT	SODT
2	SCK	SCK
2	SCK-N	SCK-N
2	SDQM0	SDQM0
2	SDQM1	SDQM1
2	SWE	SWE
2	SRAS	SRAS
2	SCAS	SCAS
2	SCKE	SCKE
2	SDQS0	SDQS0
2	SDQS0-N	SDQS0-N
2	SDQS1	SDQS1
2	SDQS1-N	SDQS1-N

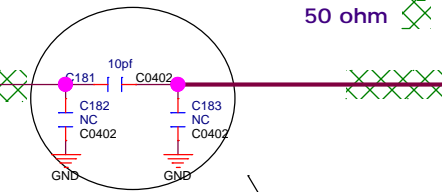
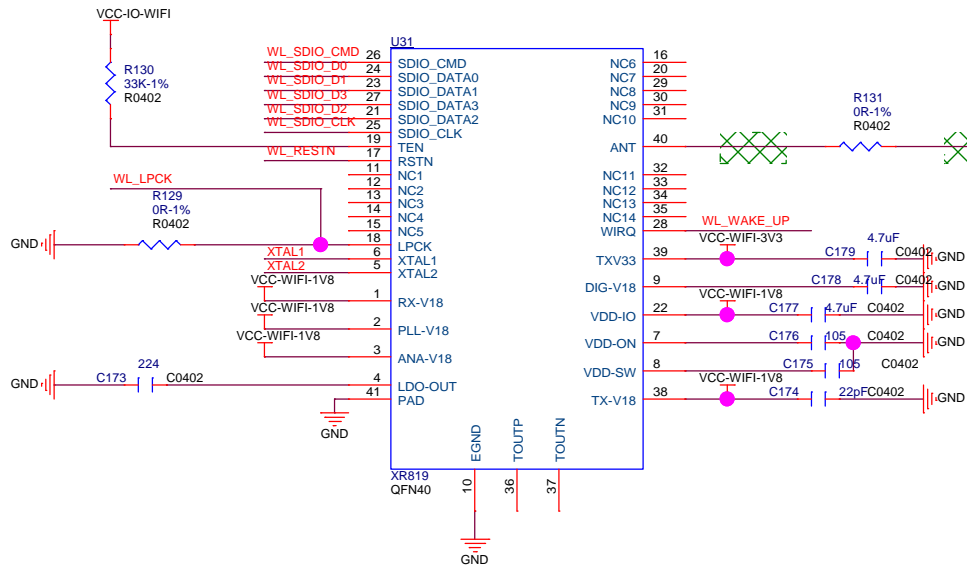




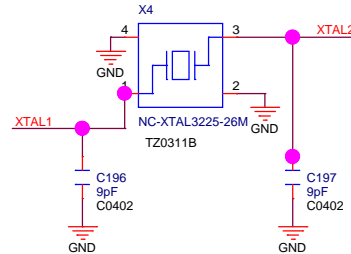
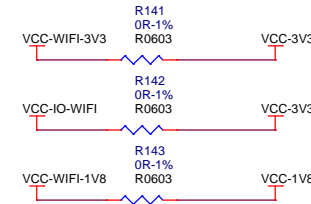
BLE



Wi-Fi



这部分电路根据天线的实际情况进行调整。



50 ohm

ANTA

J13 3216
ASC_RFANT3216120A5T_V07

- TP1 Test Point1mm VCC-3V3
- TP3 Test Point1mm VCC-1V8
- TP4 Test Point1mm WL-WAKE-AP
- IP5 Test Point1mm WL-RESTN
- TP29 WL-SDIO-D3
- TP30 WL-SDIO-D2
- TP31 WL-SDIO-D1
- TP32 WL-SDIO-D0
- TP33 WL-SDIO-CMD
- TP34 WL-SDIO-CLK

Title			<Title>
Size	Document	Number	Rev
B	<Doc>		<Rev Code>
Date:	Thursday, June 02, 2016	Sheet	1 of 1