

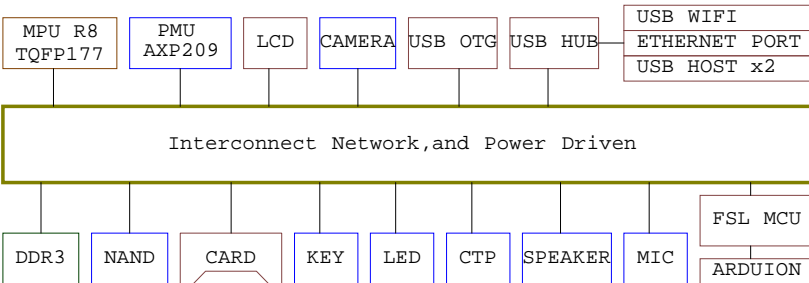
COVER

Schematics Index

- 01 COVER
- 02 CPU
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特别提醒：
1:PG0 / PG1 / PG2这个IN脚
具有INPUT功能。
2:PM的GPIO0/1/2这四个IN脚
做GPIO-OUT功能。
3:PG10 / PG11 / PG1这个IN脚
的能可改变。
4:CSI-PCLK / CSI-MCLK这个IN脚
具有INPUT功能。
5:CSI-HSYNC具有INPUT功能，
不做用途。

BLOCK

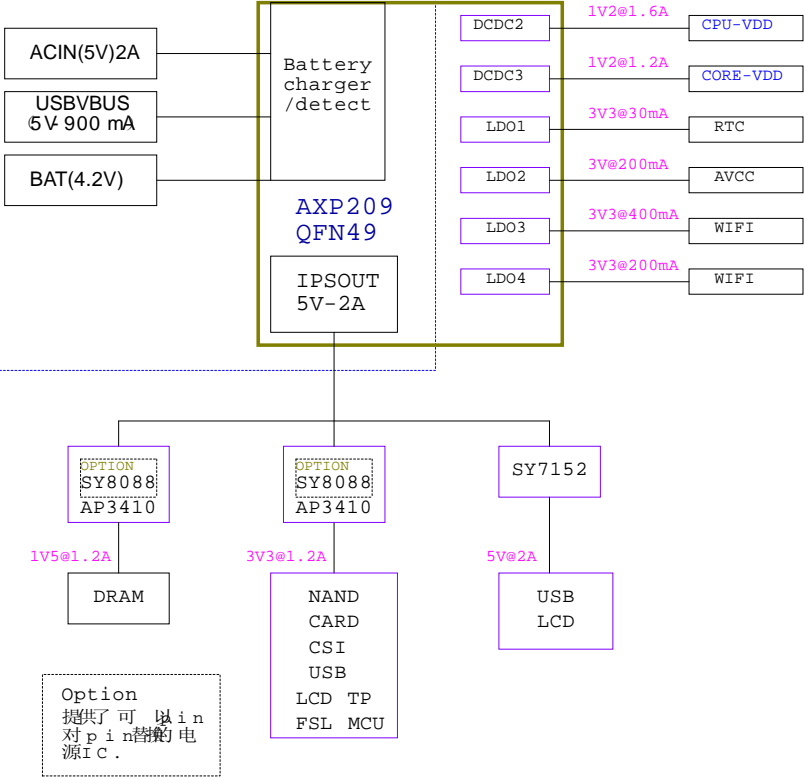


REVISION HISTORY

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	R8-DEV-V1.0	2015-09-23	CHS		

POWER TREE

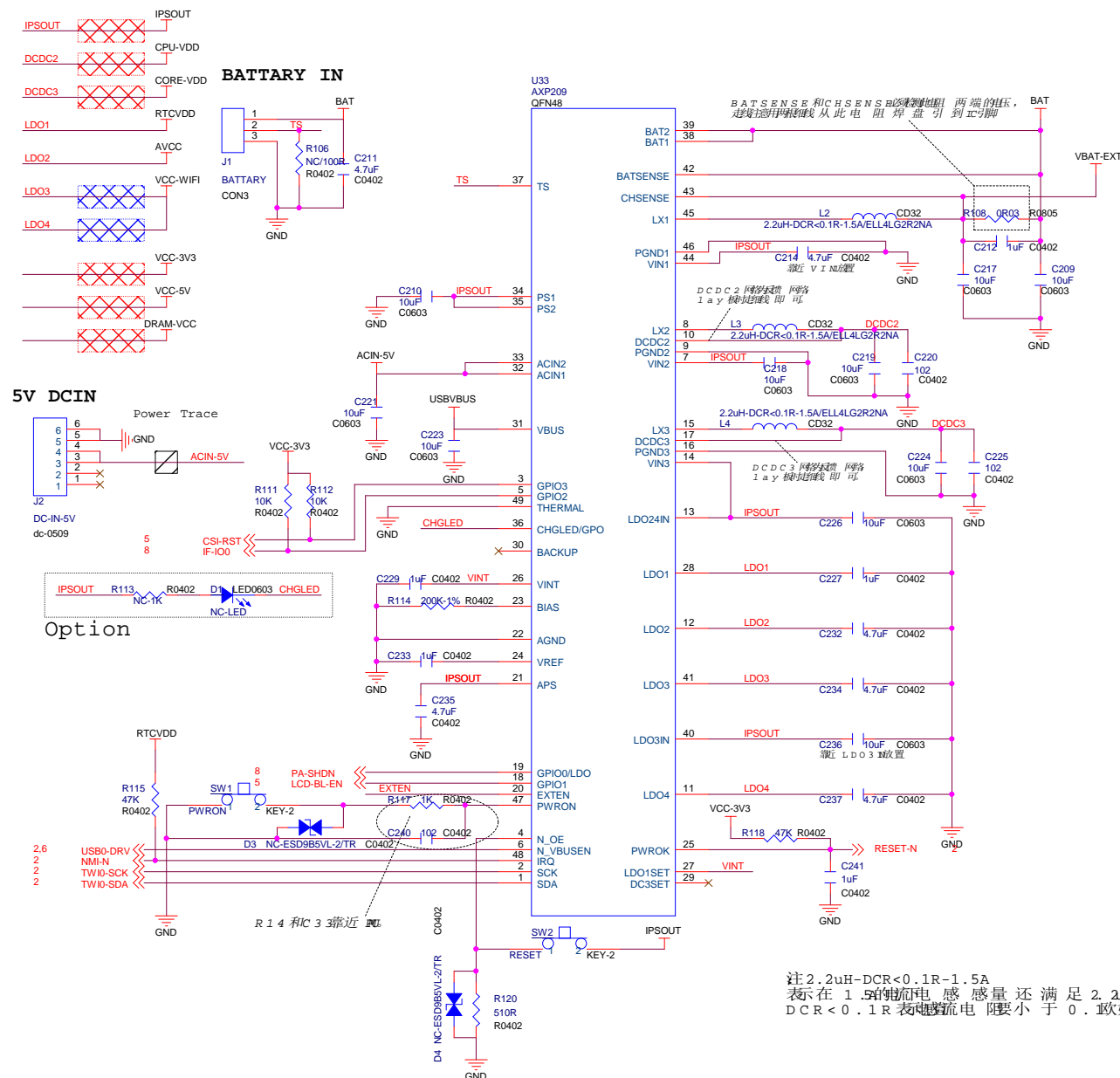
LAYOUT: ACIN BT、IPSC输入或
输出线，从管脚处就要保证尽量粗。



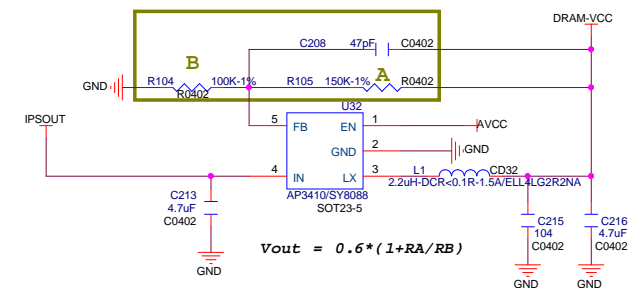


POWER

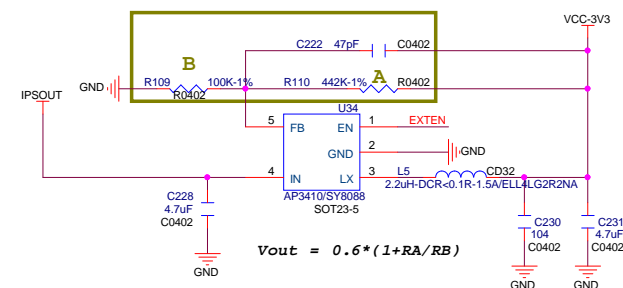
POWER LINE:Width>=80mil POWER LINE:Width>=50mil



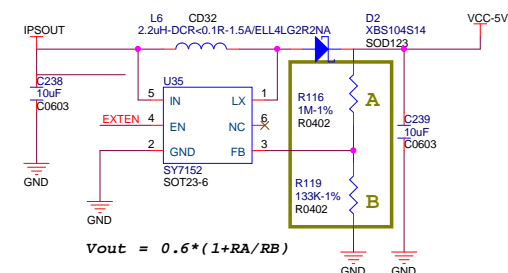
IPSOUT TO 1V6



IPSOUT TO 3V3



IPSOUT TO 5V

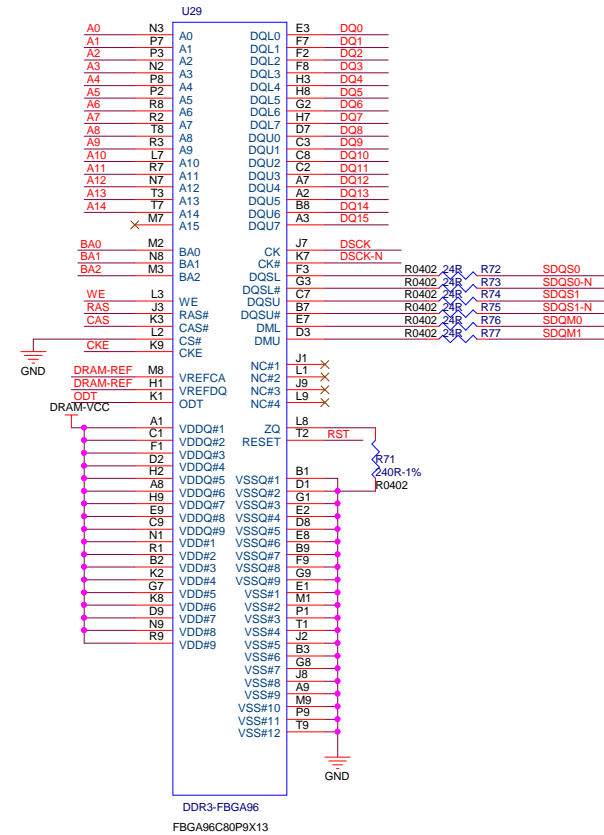
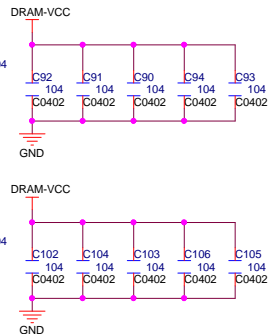
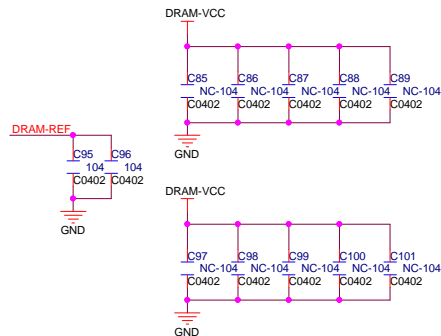
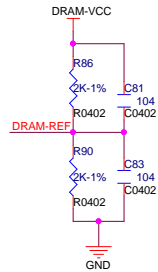
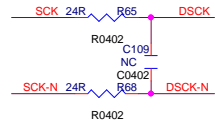
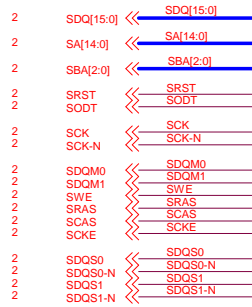


注2.2uH-DCR<0.1R-1.5A
表示在1.5A的电流电感感量还满足2.2uH
DCR<0.1R表示电感阻要小于0.1欧姆

DDR3 16x1

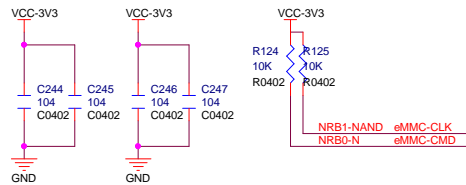
DDR3

本页的元件标号 请 不要 修改
layout时直接 由原厂提供
的DRAM参考PCB



N	NDQ[7:0]	NDQ[7:0]	eMMC-D[7:0]	
N	NDQS	NDQS	eMMC-RST	
N	NRB1-N	R122_33R_R0402	NRB1-NAND	eMMC-CLK
N	NRB9-N	NRB9-N	eMMC-CMD	
N	NRE-N	NRE-N		
N	NCE0-N	NCE0-N		
N	NCE1-N	NCE1-N		
N	NCLE	NCLE		
N	NALE	NALE		
N	NWE-N	NWE-N		

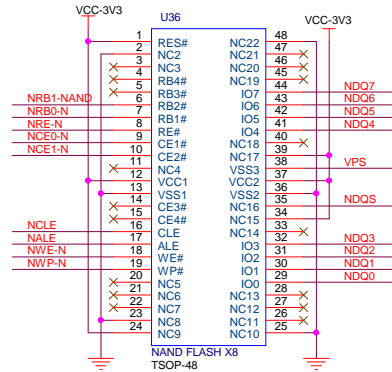
Put R33R close to CPU.



VCC-3V3

R121
NC-0R
R0402

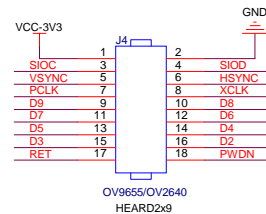
注: V_{PS}的上
下拉, 具体
请参见所用
NAND FLASH
的datasheet



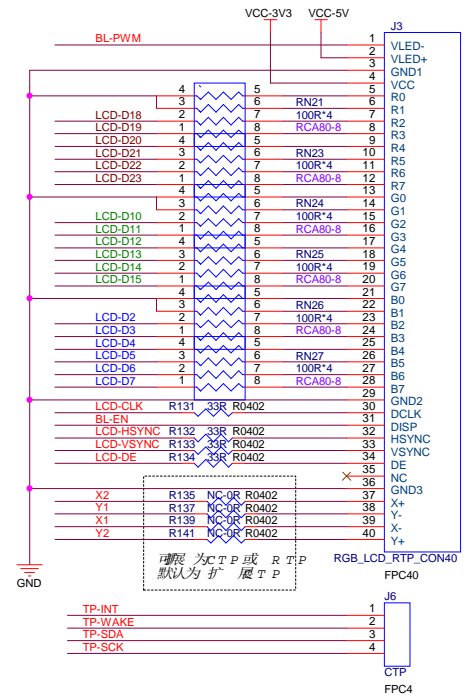
Both eMMC NAND and first TSOP NAND layout together

Pin configuration diagram for the RC501-8 package. The diagram shows two rows of pins. The top row (pins 1-8) includes CSI-D0, CSI-D1, CSI-D2, CSI-D3, CSI-D4, CSI-D5, CSI-D6, and CSI-D7. The bottom row (pins 9-16) includes CSI-VSYNC, CSI-HSYNC, CSI-PCCLK, CSI-MCLK, CSI-RST, CSI-STY, TWI2-SDA, and TWI2-SCL. Each pin is connected to a specific signal, with some pins having multiple connections. The diagram also shows the internal connections between the pins and the package pins.

Pin	Signal
1	CSI-D0
2	CSI-D1
3	CSI-D2
4	CSI-D3
5	CSI-D4
6	CSI-D5
7	CSI-D6
8	CSI-D7
9	CSI-VSYNC
10	CSI-HSYNC
11	CSI-PCCLK
12	CSI-MCLK
13	CSI-RST
14	CSI-STY
15	TWI2-SDA
16	TWI2-SCL

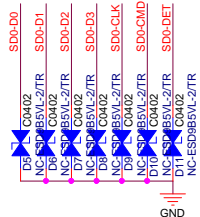


2	LCD-CLK	↔	LCD-CLK
2	LCD-D0E	↔	LCD-D0E
2	LCD-VSYN0	↔	LCD-VSYN0
2	LCD-HSYN0	↔	LCD-HSYN0
2	LCD-D7	↔	LCD-D7
2	LCD-D6	↔	LCD-D6
2	LCD-D5	↔	LCD-D5
2	LCD-D4	↔	LCD-D4
2	LCD-D3	↔	LCD-D3
2	LCD-D2	↔	LCD-D2
2	LCD-D15	↔	LCD-D15
2	LCD-D14	↔	LCD-D14
2	LCD-D13	↔	LCD-D13
2	LCD-D12	↔	LCD-D12
2	LCD-D11	↔	LCD-D11
2	LCD-D10	↔	LCD-D10
2	LCD-D23	↔	LCD-D23
2	LCD-D22	↔	LCD-D22
2	LCD-D21	↔	LCD-D21
2	LCD-D20	↔	LCD-D20
2	LCD-D19	↔	LCD-D19
2	LCD-D18	↔	LCD-D18

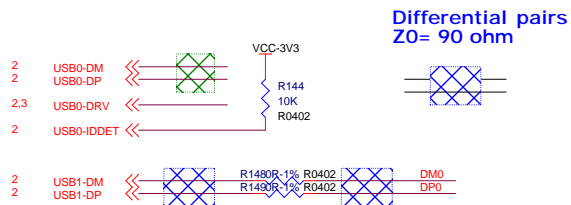


The schematic diagram illustrates the electrical connections for a microcontroller board. Key components and their values are as follows:

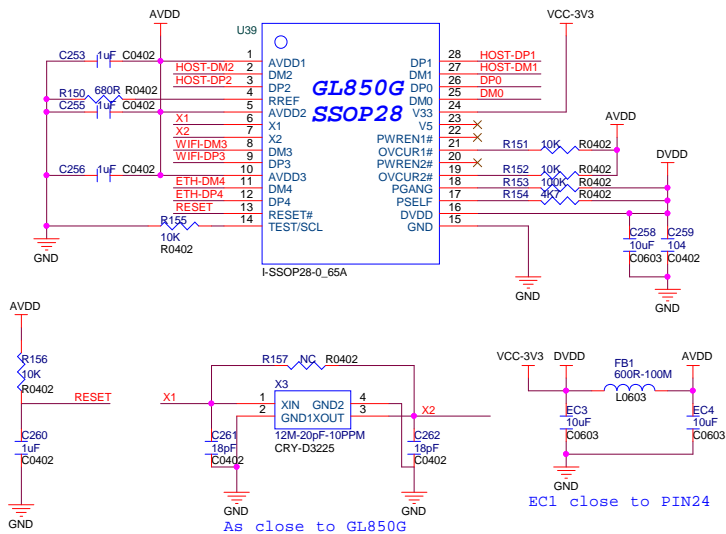
- VCC-3V3**: Power supply connection.
- Resistors**: R136 (2R2), R138 (47K), R140 (47K), and four R0402 surface-mount resistors.
- Capacitors**: C249 (10uF) and C0603.
- J5 Connector**: A 10-pin header with the following pin functions:
 - Pin 1: DAT2
 - Pin 2: DAT3
 - Pin 3: CMD
 - Pin 4: VDD
 - Pin 5: CLK
 - Pin 6: VSS2
 - Pin 7: DAT0
 - Pin 8: DAT1
 - Pin 9: CD#
 - Pin 10: GND
- SD Card Signals**:
 - SD0-D2, SD0-D3, SD0-CMD**: Connected to pins 1, 2, and 3 of J5.
 - SD0-CLK**: Connected to pin 5 of J5.
 - SD0-D0, SD0-D1**: Connected to pins 7 and 8 of J5.
 - SD0-DET**: Connected to pin 9 of J5.
- GND**: Ground connections at various points, including pin 10 of J5.



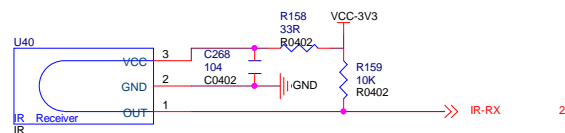
USB/WIFI/IR



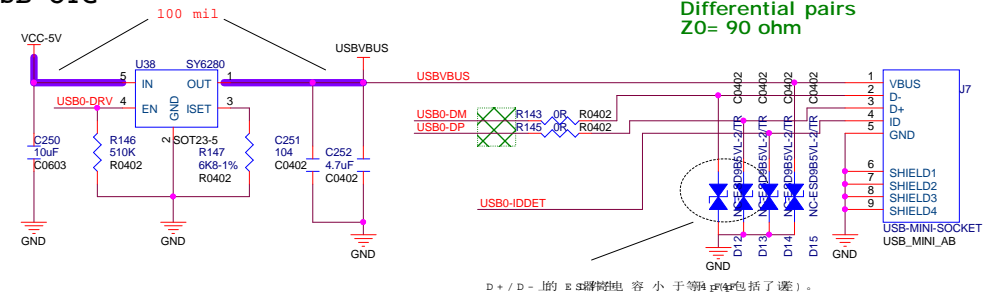
USB-HUB



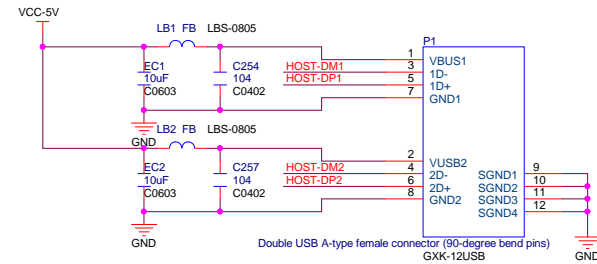
IR



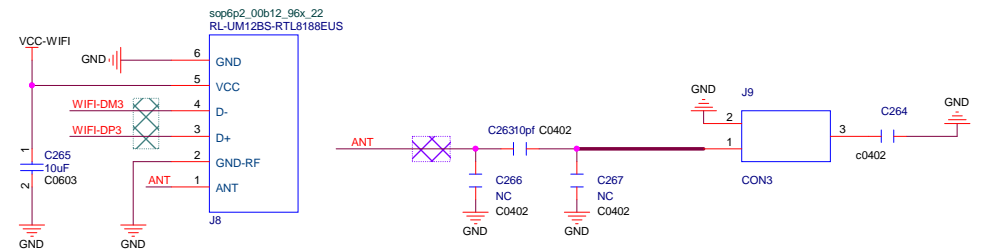
USB-OTG



USB-HOST



USB-WIFI



USB-ETHERNET



ETHERNET

USB to Ethernet

VCC-5V
ETH-DM
ETH-DP
C270 104 C0402
C271 4.7uF C0402
GND

***Note2-1:**
The C269 cap between the DP and DM pins is used to filter the common-mode noise and should be placed as close as pin #57 and #56.

***Note2-9:**
For self-power applications, please refer to below suggestions to design the V_BUS signal circuit.
(1) While the USB interface was connected to USB host/hub controller, the V_BUS signal MUST be pulled high to set AX88772C/AX88772B at normal operation stage.
(2) While the USB interface was disconnected from USB host/hub controller, the V_BUS signal MUST be pulled down to set AX88772C/AX88772B at reset stage.

***Note2-2:**
The RC reset circuit is optional for AX88772C/AX88772B applications. You can reserve the RC reset circuit on your AX88772C/AX88772B schematic to fine tune the reset timing if necessary.

Reset Circuit

VCC-3V3
R169 NC39K R0402
RESET_N
C273 NC0.47uF C0402
GND

***Note2-3:**
The AX88772C/AX88772B supports 16-bit mode 93C56/93C66 EEPROM. The R166 resistor is mounted to set the ATME16 AT93C56A EEPROM to 16-bit mode.

Optional

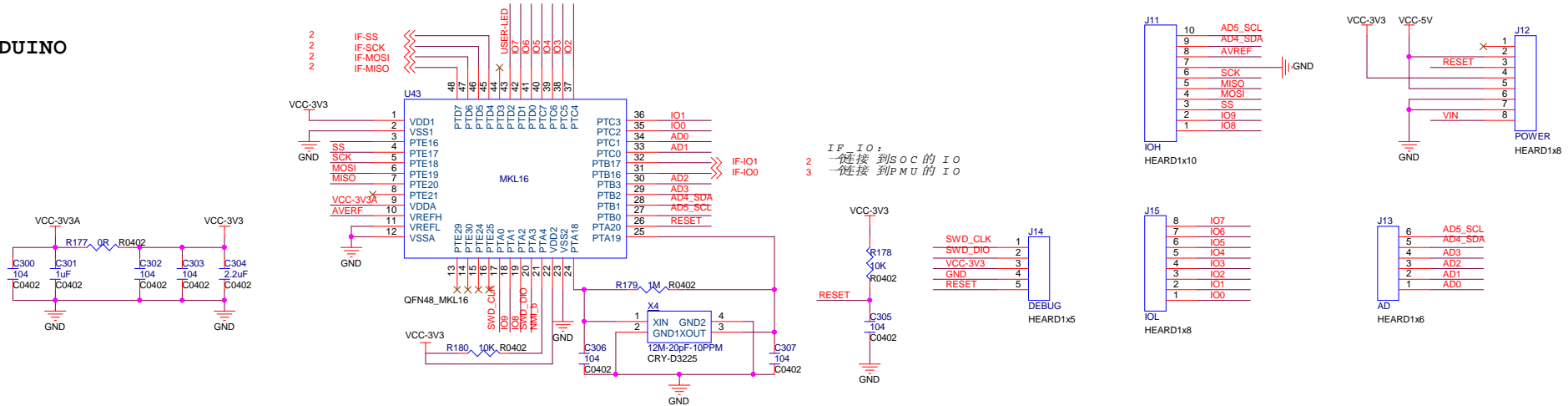
GND

3.3V to 1.8V On-chip Regulator

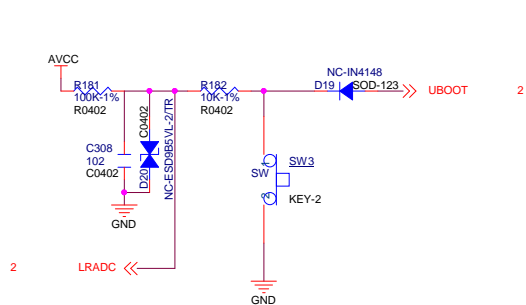
A3V3 L7 T1H6080U110T L0603
D1V8 L8 T1H6080U110T L0603
C276 104 C0402
C277 +4.7uF/10V C0603
C283 4.7uF/10V C0603
C284 104 C0402
C287 104 C0402
C288 104 C0402
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ARDUINO/KEY/LED/AUDIO

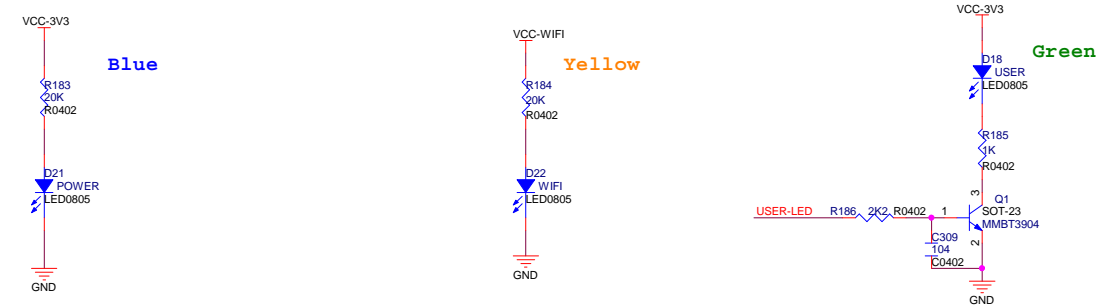
ARDUINO



KEY



LED



HEADPHONE & SPEAKER & MIC

