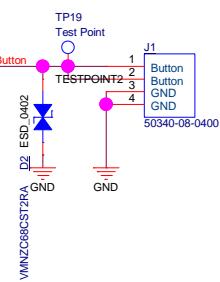
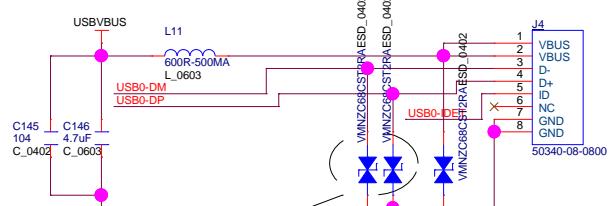


5 4 3 2 1

Button

3 Button

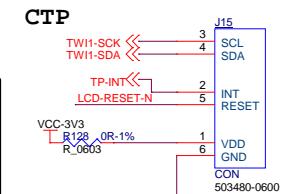
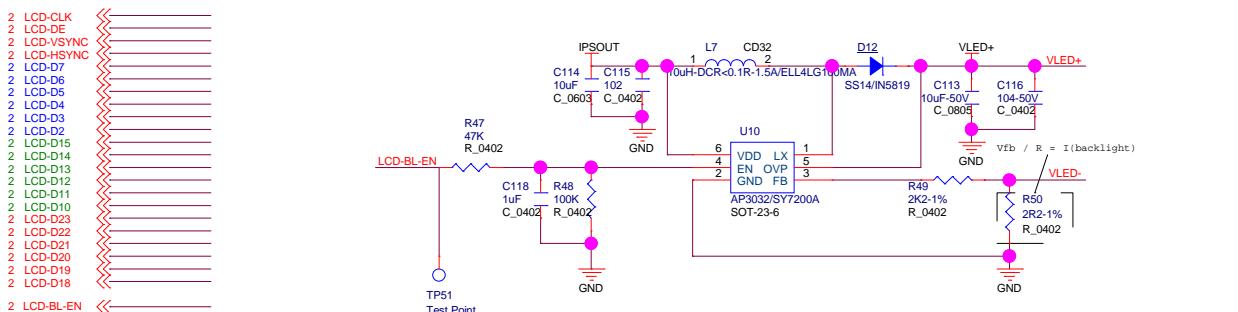
**PCB Power Assay**2 USB0-DM
2 USB0-DP
2 USB0-IDET**USB-DEVICE**Differential pairs
 $Z_0 = 90 \text{ ohm}$ 

D + / D - 上的 ESD 保护电容 小于等于 100 pF(包括了误差)。

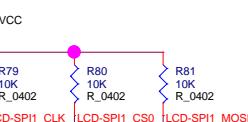
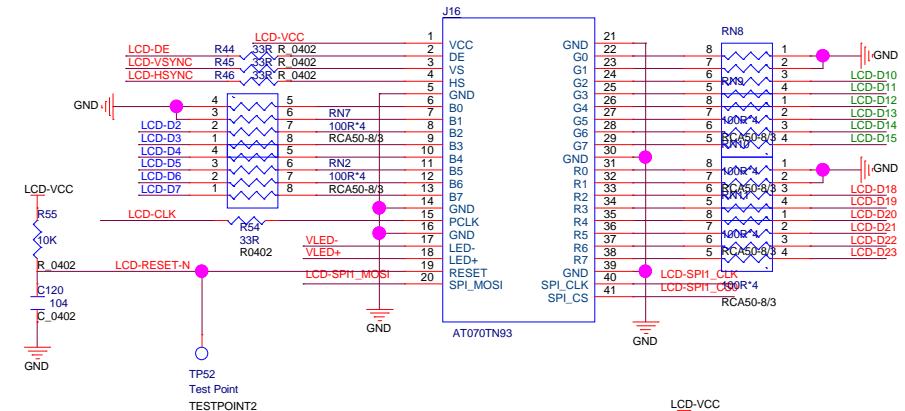
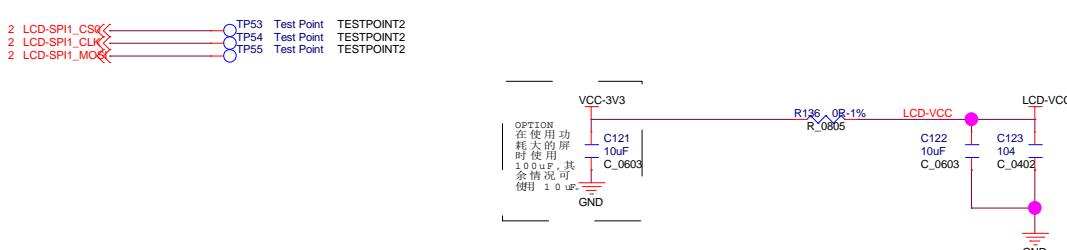
M1 Bad Mark
M2 Bad Mark

5 4 3 2 1

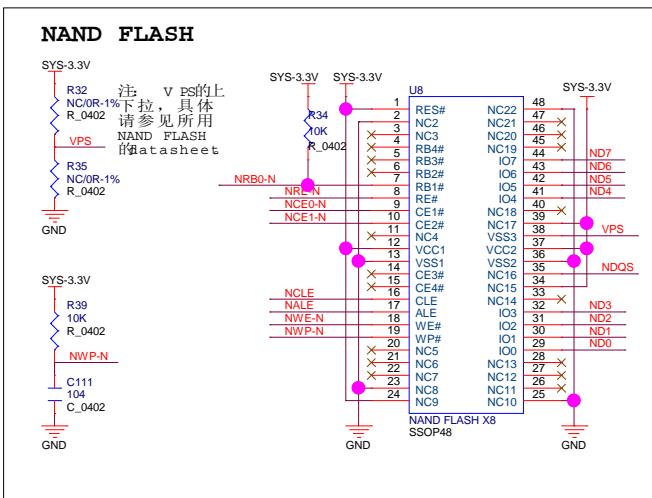
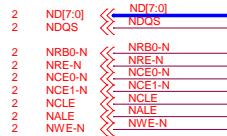
DISPLAY



电容屏信号连接示意图

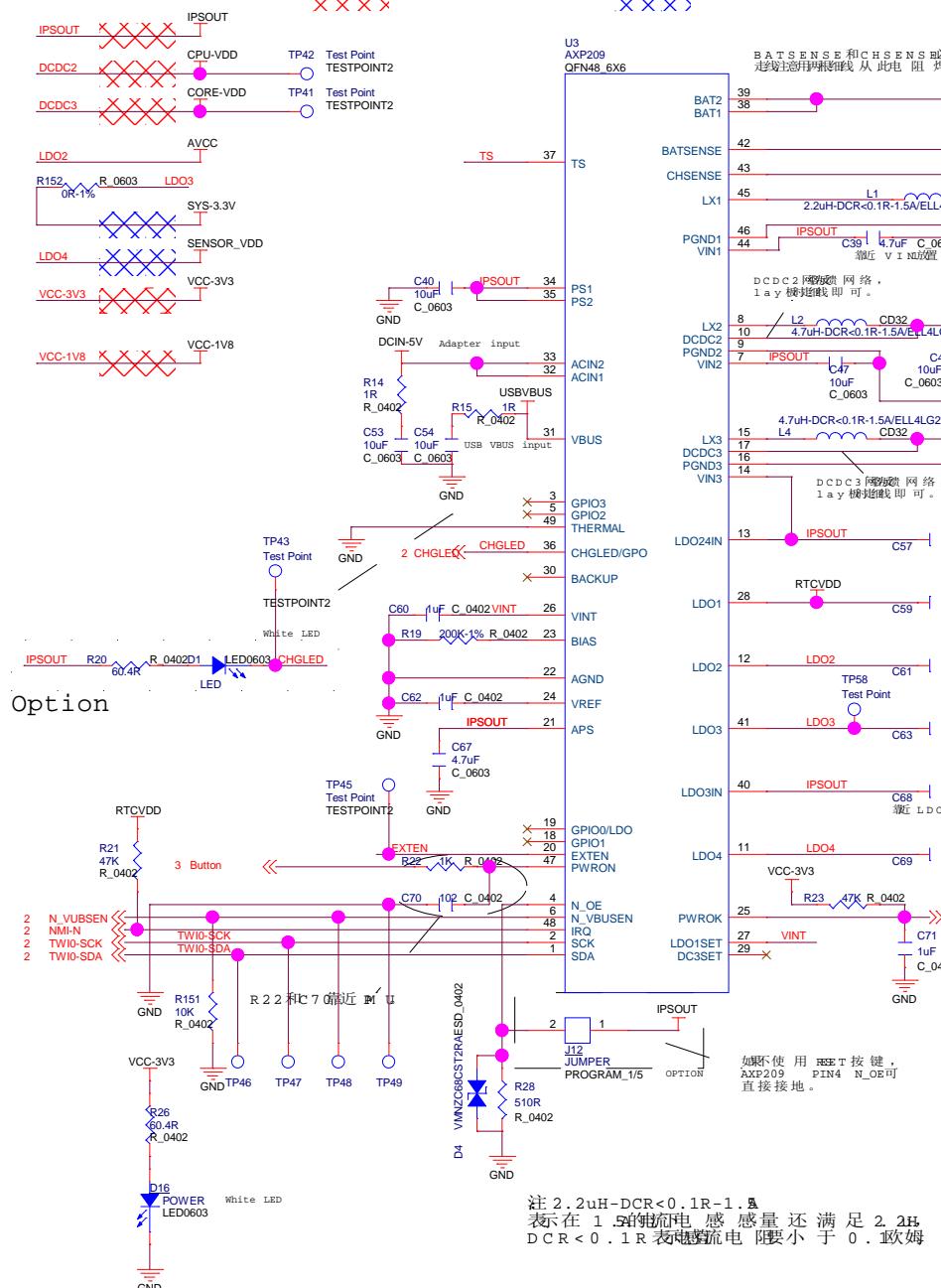


FLASH/CARD

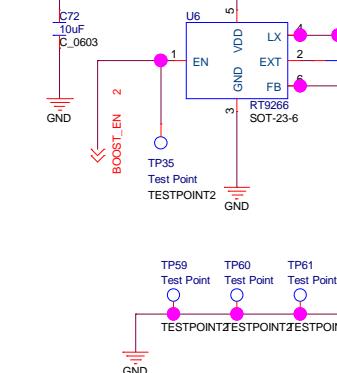
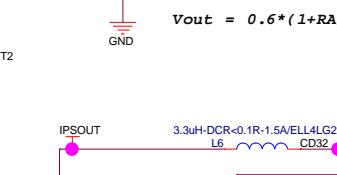
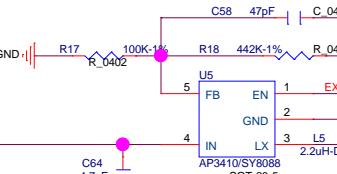
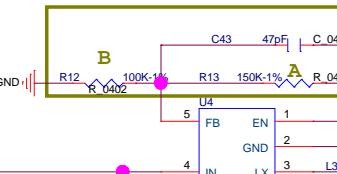
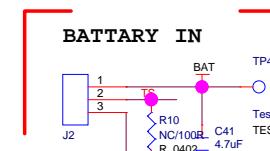


POWER

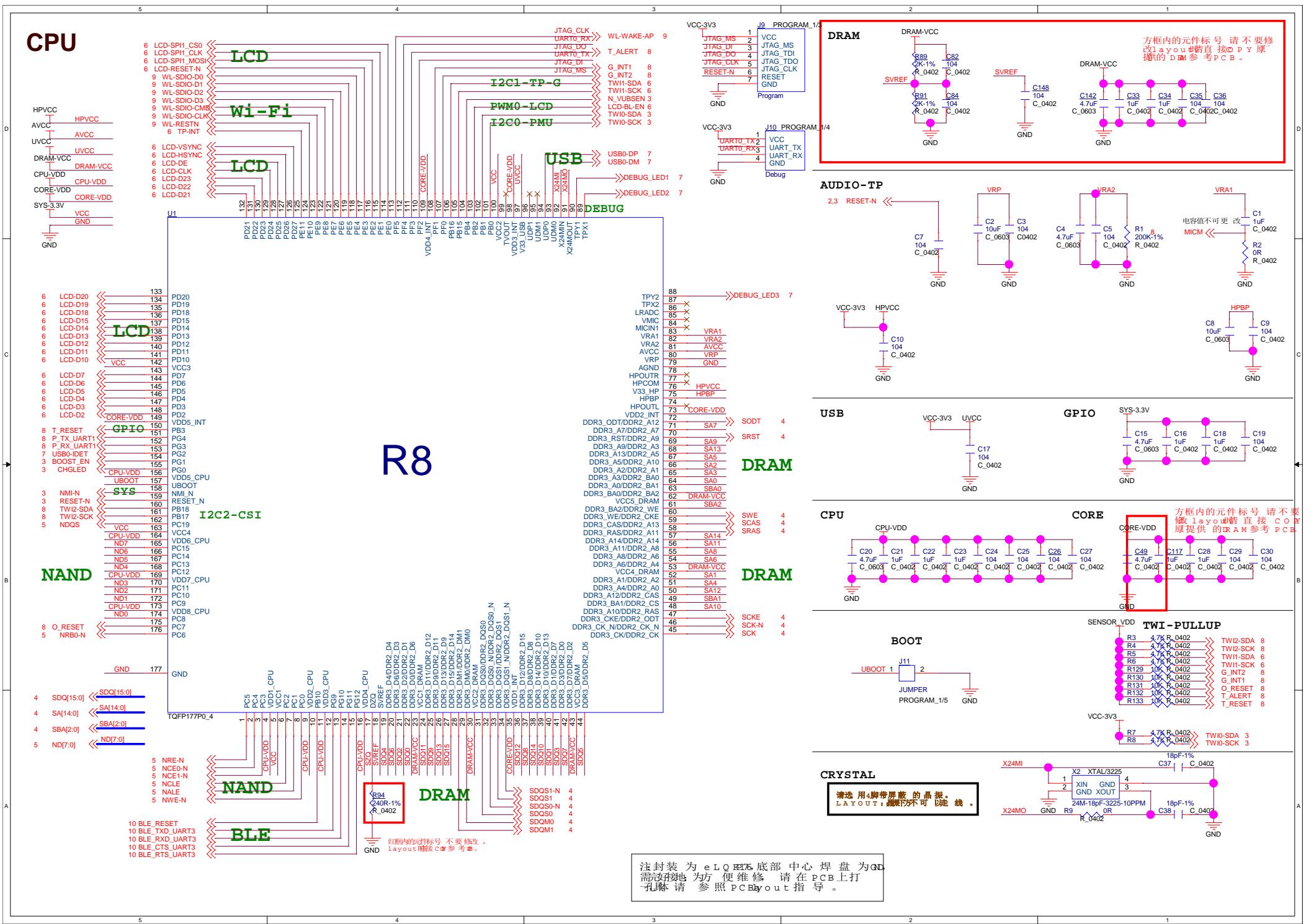
POWER LINE:Width>=80mil POWER LINE:Width>=50mil



注 2. 2uH-DCR<0.1R-1.5A
 表示在 1.5A 的输出电流感抗量还满足 2.2uH
 DCR < 0.1 R 表明输出电感要小于 0.1 欧姆



TP59 Test Point TESTPOINT2 TP60 Test Point TESTPOINT2 TP61 Test Point TESTPOINT2 TP62 Test Point TESTPOINT2 TP63 Test Point TESTPOINT2 TP64 Test Point TESTPOINT2 TP65 Test Point TESTPOINT2 TP66 Test Point TESTPOINT2



COVER

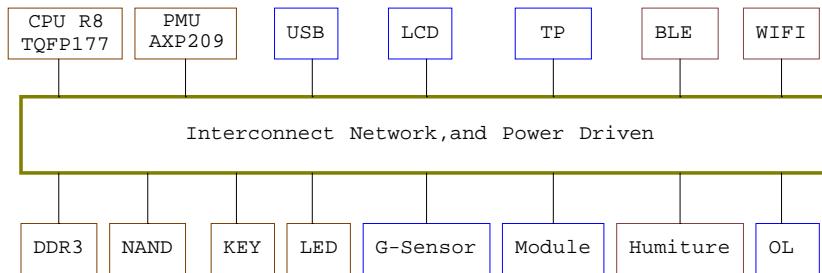
Schematics Index

Bran-Design

- 01 COVER
- 02 CPU
- 03 POWER
- 04 DDR3 16x1
- 05 FLASH
- 06 DISPLAY
- 07 PERIPHERS
- 08 SENSOR
- 09 WI-FI
- Option:
- 10 BLE

特别提醒：
 1: PG0 / PG1 / PG2 这三个IN脚
 具有 INPUT 和输出功能。
 2: PMU的GPIO0/1/2这三个IN脚
 做GPIO-OUT功能。
 3: PG10 / PG11 / PG12 这三个IN脚
 的输出可改变。
 4: CSI-PCLK / CSI-MCL这两个IN脚
 具有 INPUT 和输出功能。
 5: CSI-HSYNC 具有 INPUT 和输出功能，
 不他用途。

BLOCK

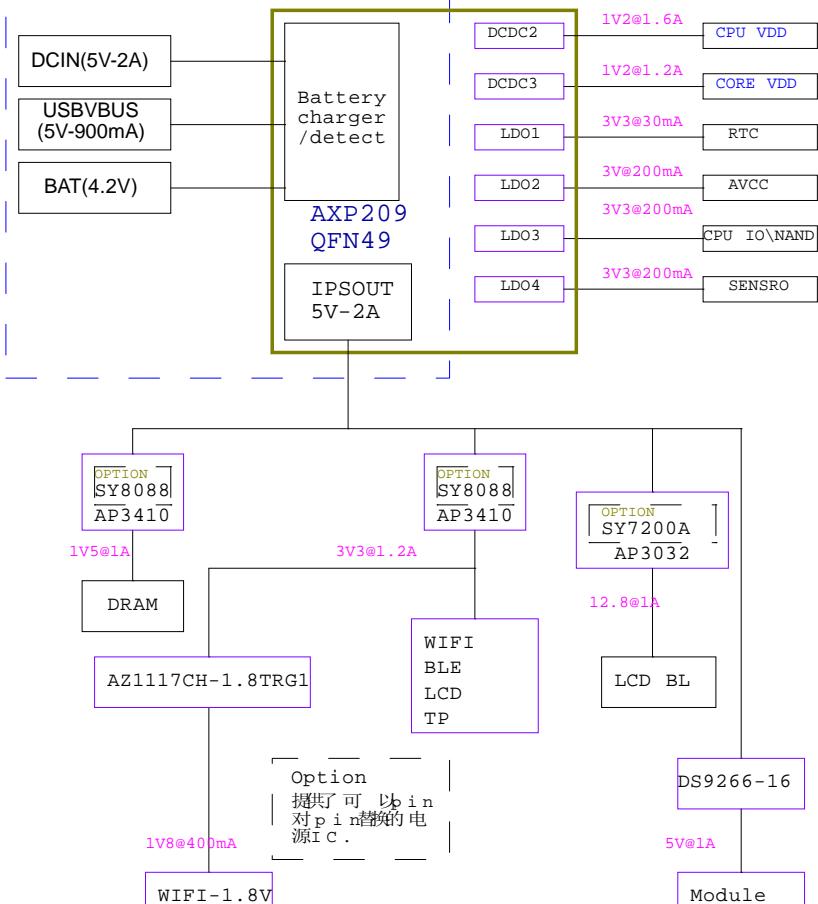


REVISION HISTORY

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Bran Main PCB ASSY	2016/6/2	Violet/Jemmey	Jemmey	

POWER TREE

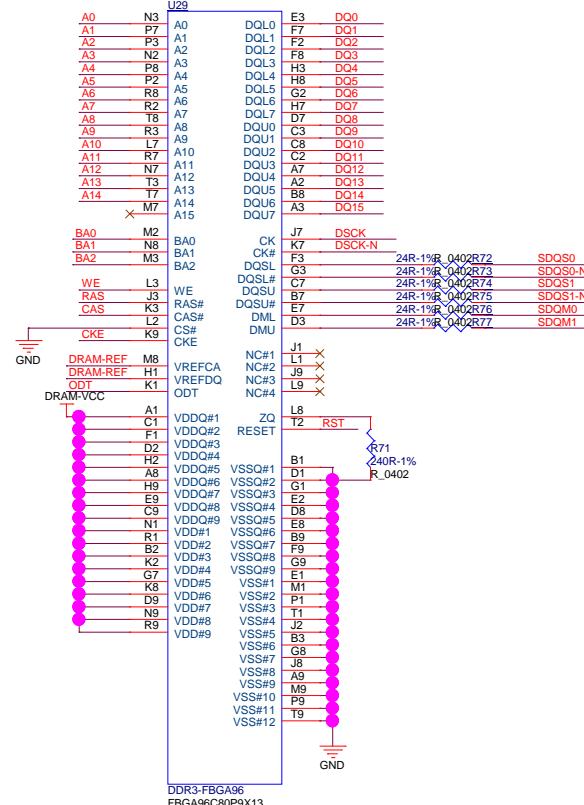
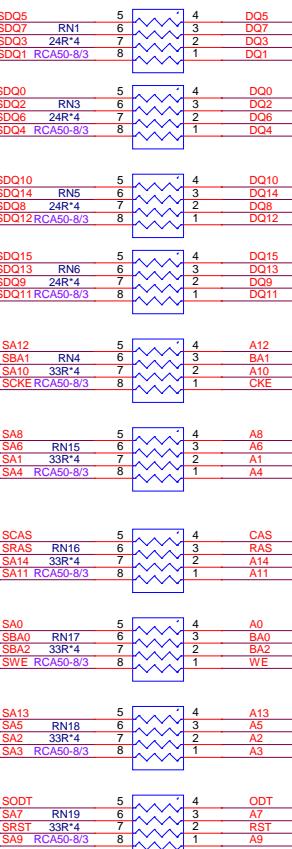
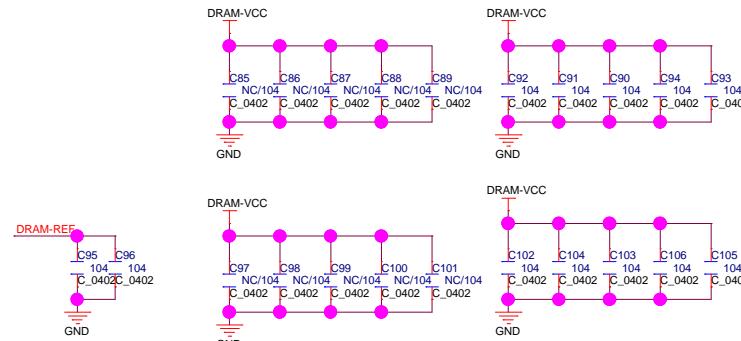
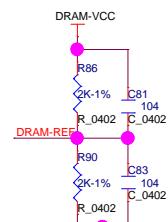
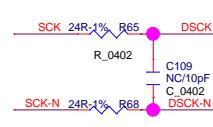
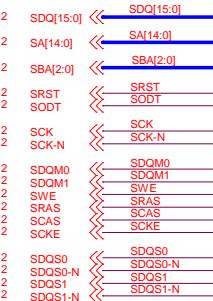
LAYOUT: DCIN BA、IPSO 输入或输出线，从PMU管脚处就要保证尽量粗。

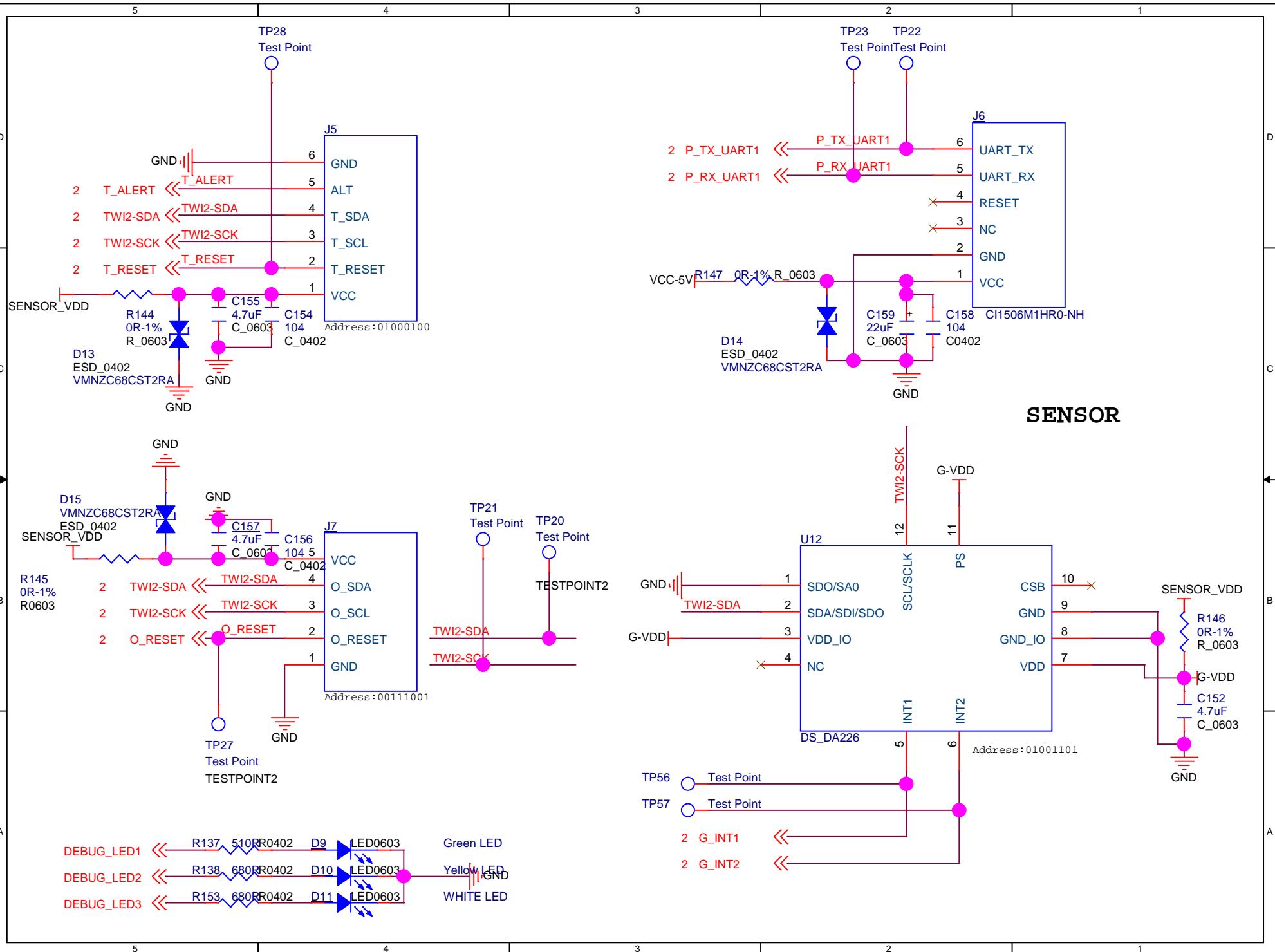


DDR3 16x1

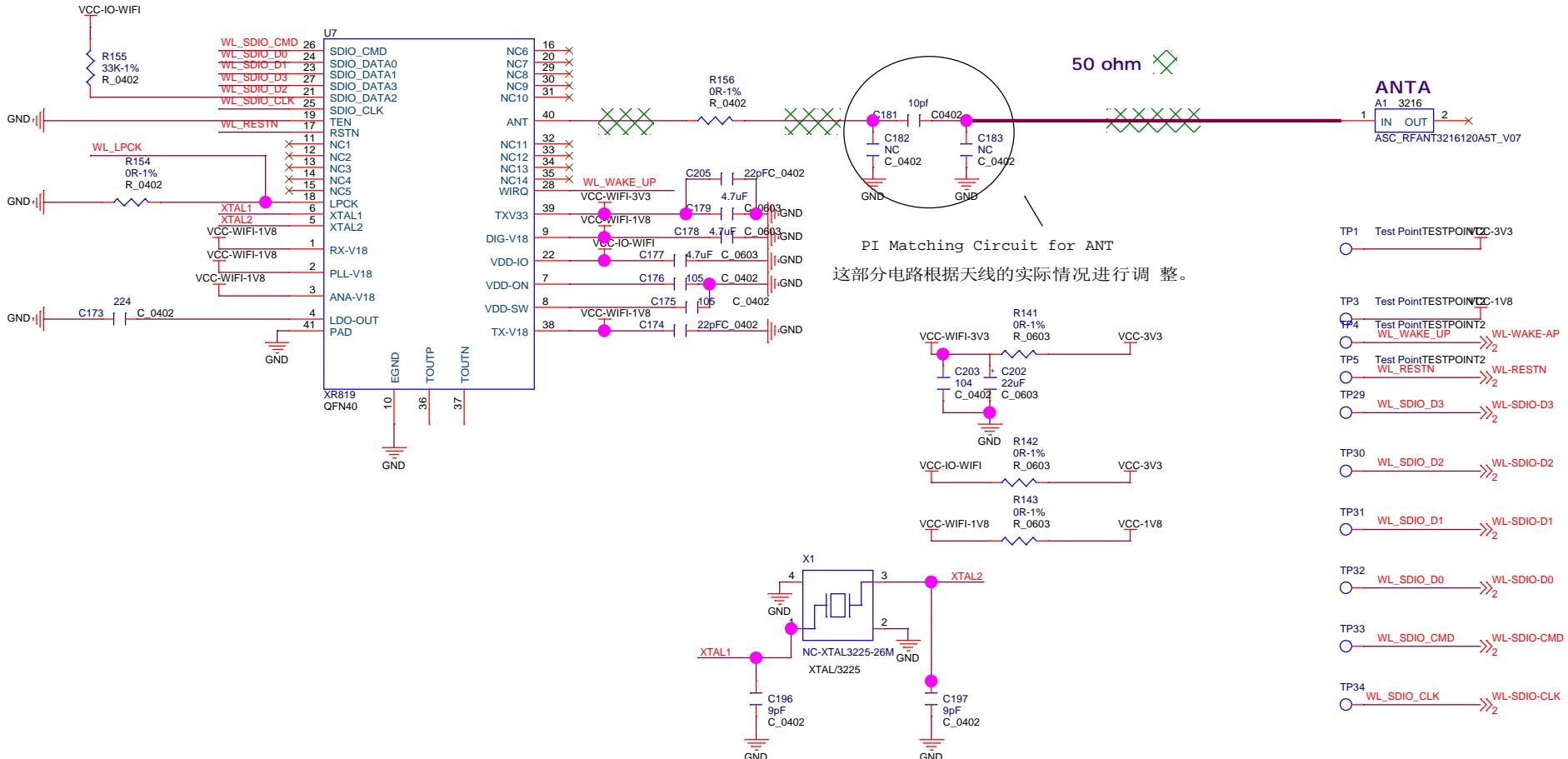
DDR3

本页的元件标号请不要修改
layout时直接用原厂提供的DRAM参考PCB





Wi-Fi



BLE

