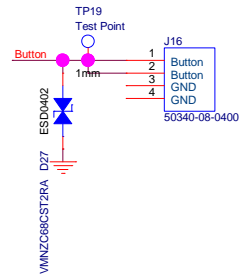
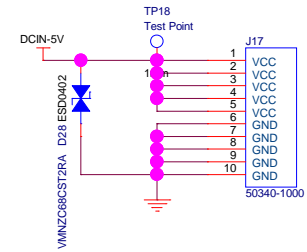


Button



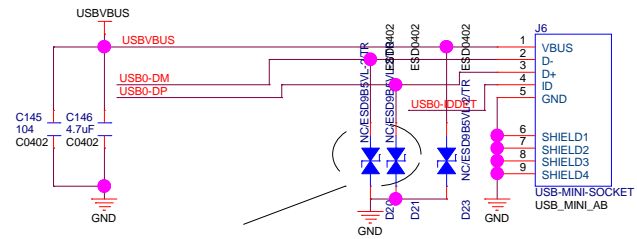
PCB Power Assay



USB-DEVICE



Differential pairs
Z0= 90 ohm



D^+ / D^- 上的ES器件电容小于等于4 pF(包括了误差)。

DISPLAY

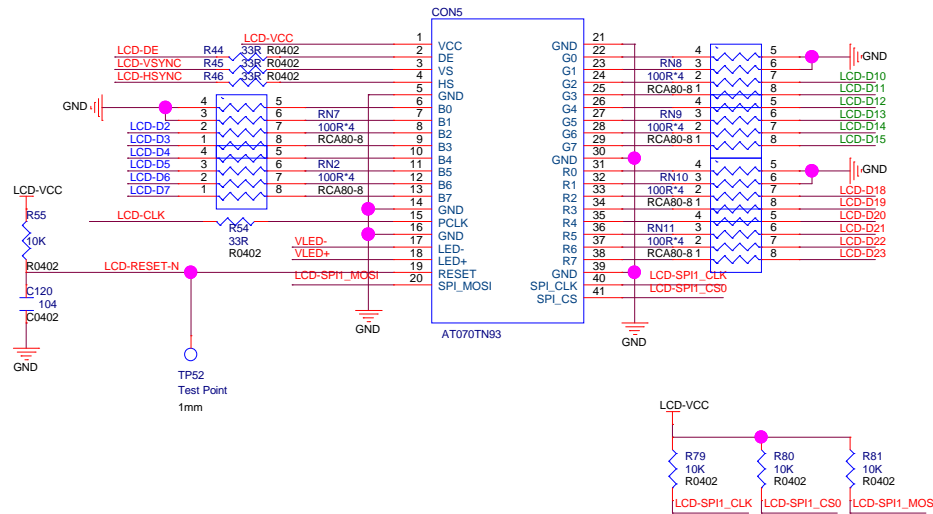
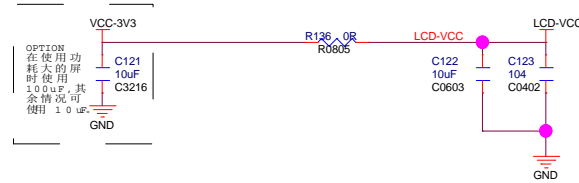
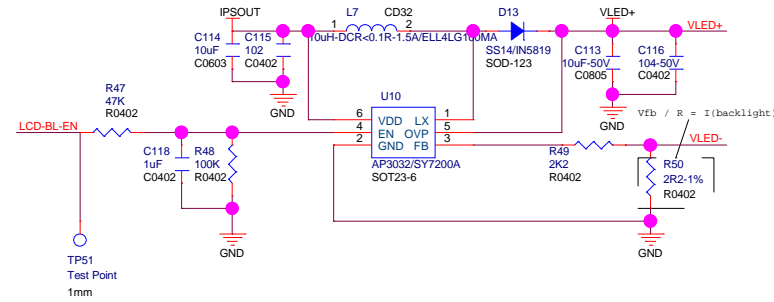
LCD

2 LCD-CLK
2 LCD-DE
2 LCD-VSYNC
2 LCD-HSYNC
2 LCD-D7
2 LCD-D6
2 LCD-D5
2 LCD-D4
2 LCD-D3
2 LCD-D2
2 LCD-D15
2 LCD-D14
2 LCD-D13
2 LCD-D12
2 LCD-D11
2 LCD-D10
2 LCD-D23
2 LCD-D22
2 LCD-D21
2 LCD-D20
2 LCD-D19
2 LCD-D18
2 LCD-BL-EN

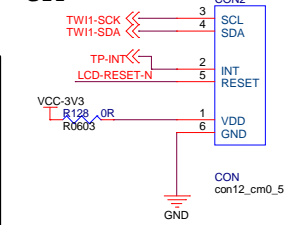
2 LCD-RESET-N

2 LCD-SPH1_CS0
2 LCD-SPH1_CLK
2 LCD-SPH1_MOSI

TP53 Test Point 1mm
TP54 Test Point 1mm
TP55 Test Point 1mm



CTP



电容屏信号连接示意图

FLASH/CARD

- 2

ND[7:0]

<<

ND[7:0]
- 2

NDQS

<<

NDQS
- 2

NRB0-N

<<

NRB0-N
- 2

NRE-N

<<

NRE-N
- 2

NCE0-N

<<

NCE0-N
- 2

NCE1-N

<<

NCE1-N
- 2

NCLE

<<

NCLE
- 2

NALE

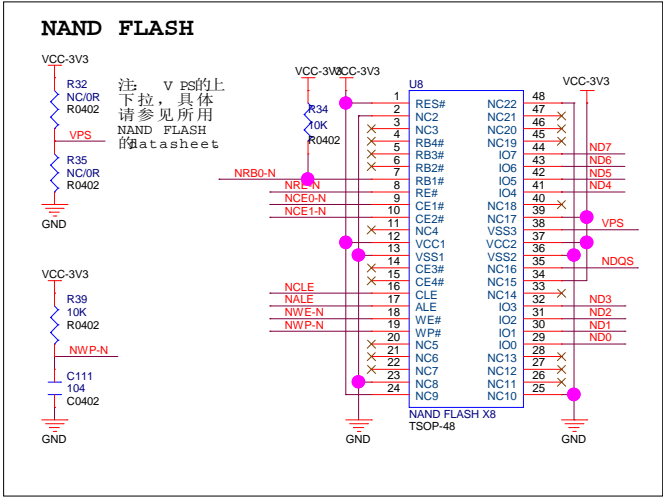
<<

NALE
- 2

NWE-N

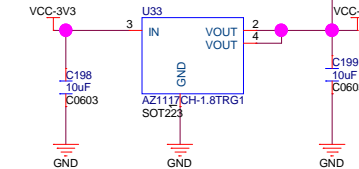
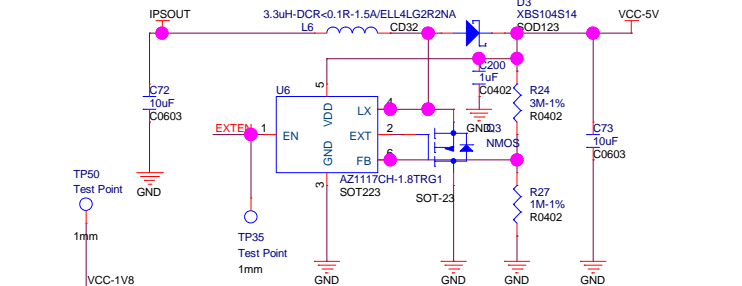
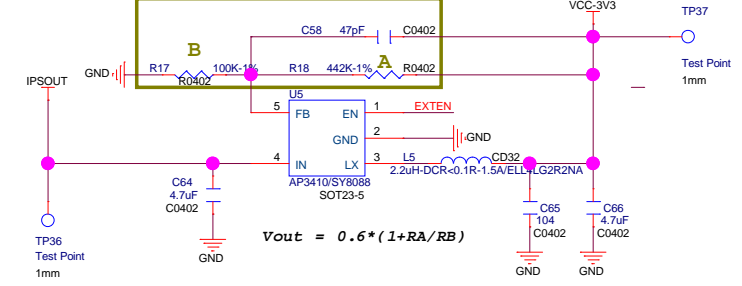
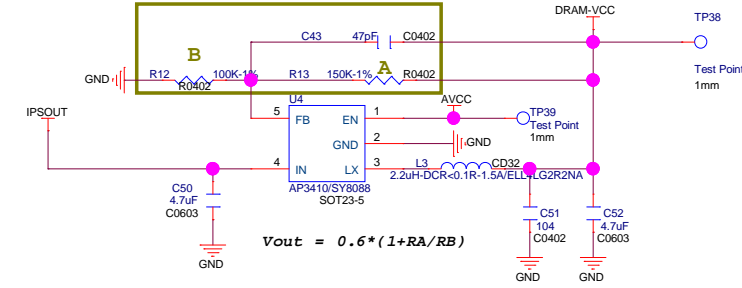
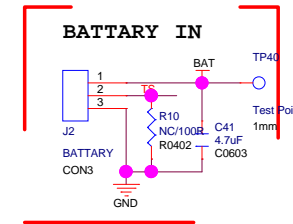
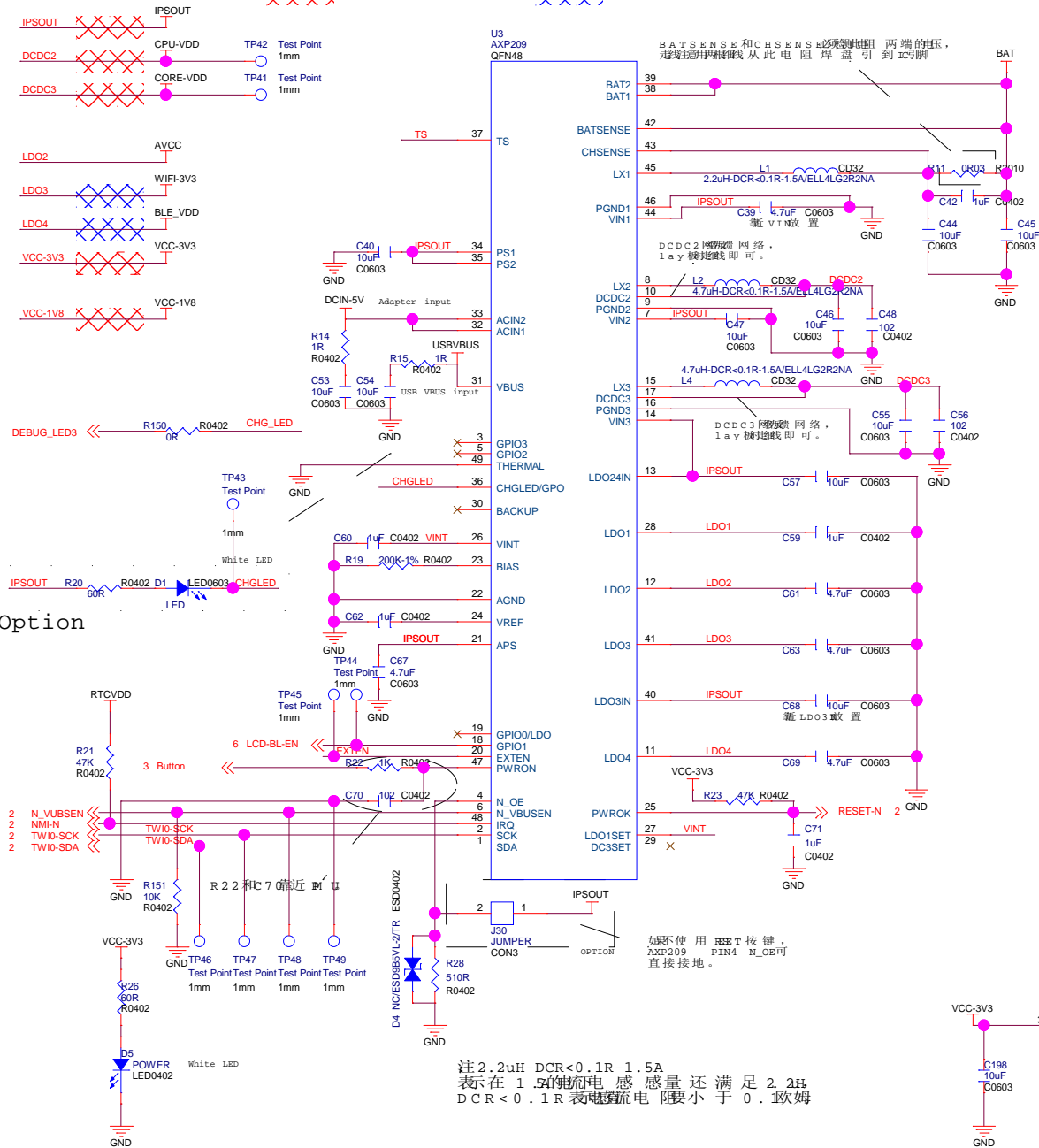
<<

NWE-N

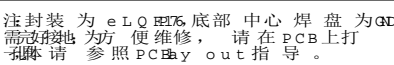


POWER

POWER LINE:Width>=80mil POWER LINE:Width>=50mil



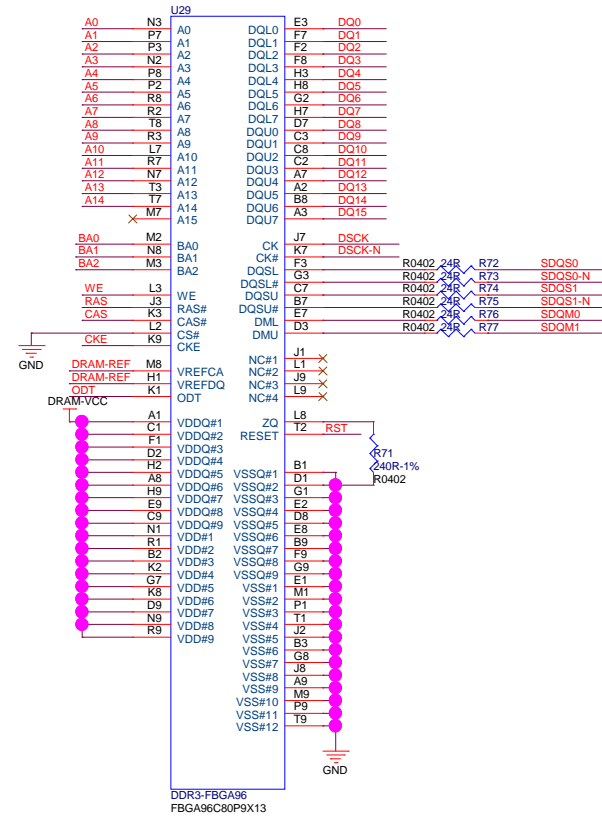
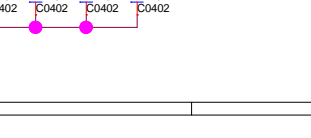
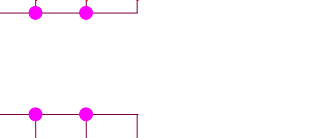
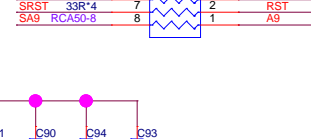
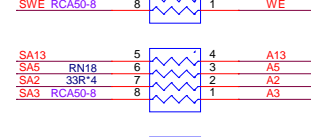
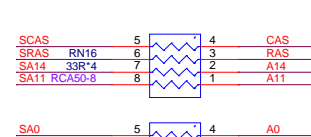
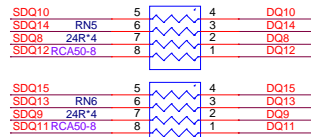
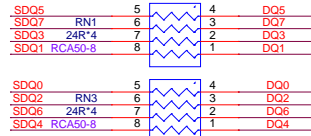
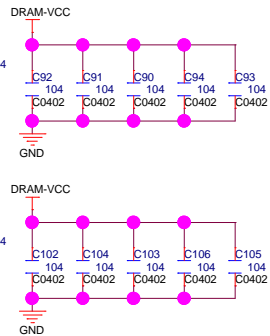
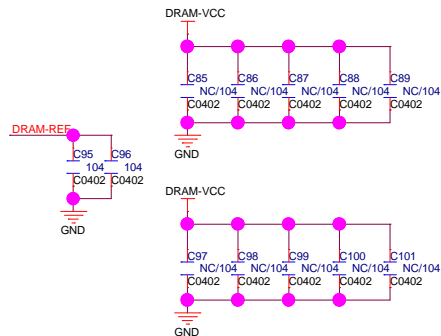
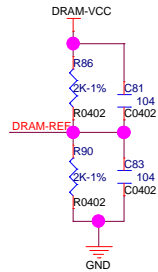
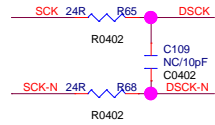
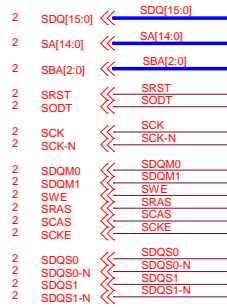
注 2.2uH-DCR<0.1R-1.5A
表示在 1.5A 电流电 感 感量 还 满 足 2.2uH
DCR<0.1R 表 示 电 流 电 阻 要 小 于 0.1 欧 姆

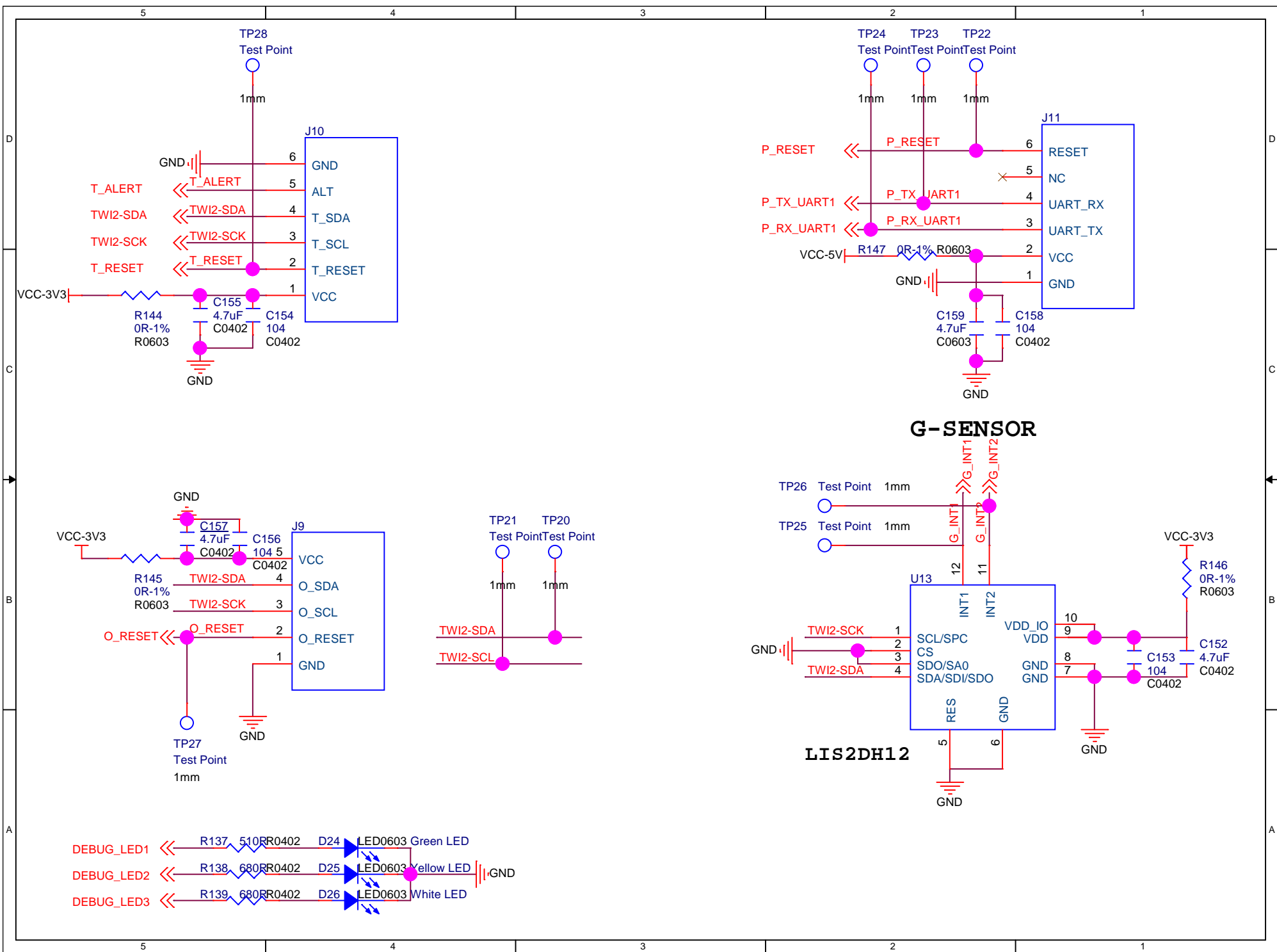


DDR3 16x1

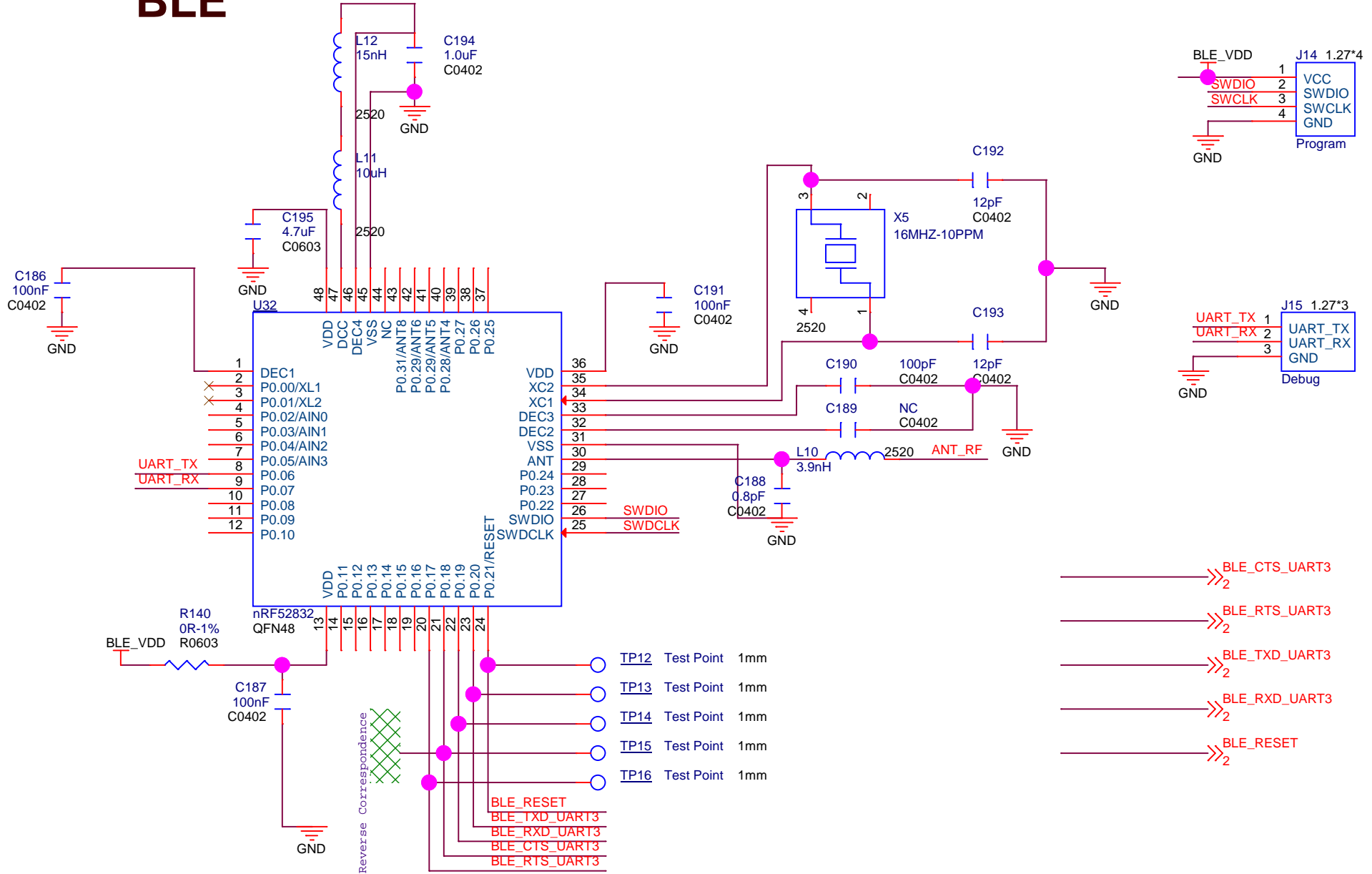
DDR3

本页的元件标号 请 不要 修改
layout 时 直接 由 原厂 提供
的 参考 PCB





BLE



COVER

Schematics Index

R8-REFERENCE-DESIGN

01 COVER
02 CPU
03 POWER
04 DDR3 16x1
05 FLASH/CARD
06 DISPLAY
07 USB-OTG/WIFI
08 MISC

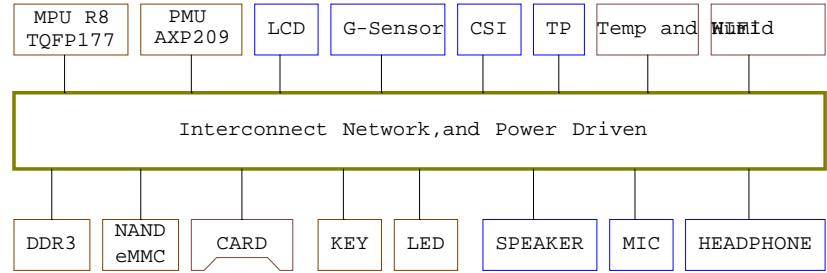
OPTION

09 DDR3 8x2
10 AUDIO

特别提醒:

- 1: PG0 / PG1 / PG2 这个 IN 脚 具有 INPUT 功能。
- 2: PMU 的 GPIO0/1/2 这三个 IN 脚 做 GPIO-OUTPUT 功能 的能可改变。
- 3: PG10 / PG11 / PG12 这个 IN 脚 具有 INPUT 功能。
- 4: CSI-PCLK / CSI-MCLK 这个 IN 脚 具有 INPUT 功能。
- 5: CSI-HSYNC 具有 INPUT 功能， 不能用途。

BLOCK



REVISION HISTORY

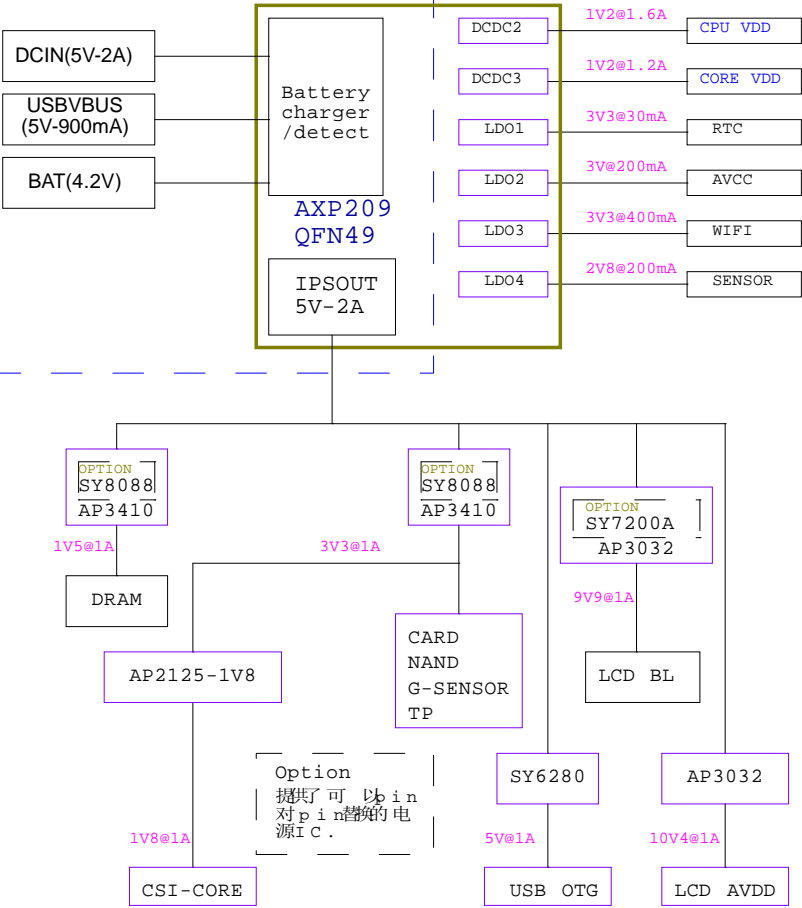
Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0					

GPIO ASSIGNMENT

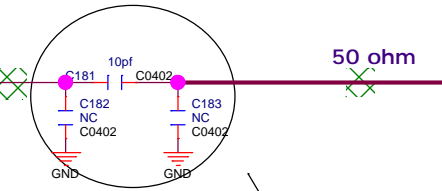
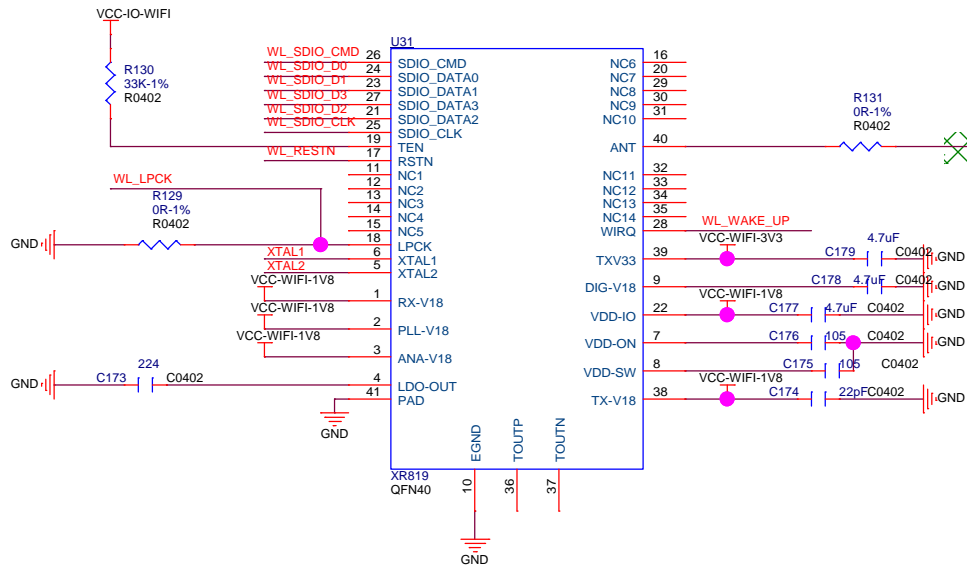
CPU	Define	Function
PB0	TWIO_SCK	TWIO-PMU
PB1	TWIO_SDA	
PB2	PWM0	LCD
PB3	GPIO-OUT	TP-WAKEUP
PB4	GPIO-OUT	USER-LED
PB10	GPIO-OUT	CSI-STY
PB15	TWII_SCK	TWII-TP-G
PB16	TWII_SDA	
PB17	TWII_SCK	
PB18	TWII_SDA	TWII-CSI
PG0	GPIO-IN	SD0-DET-N
PG1	NC	
PG2	GPIO-IN	USB0-IDDET
PG3	GPIO-OUT	CSI-STY-1
PG4	GPIO-OUT	CSI-RST-1
PG9	GPIO-OUT	ACIN-EN
PG10	GPIO-OUT	PA-SHDN
PG11	EINT	TP-INT
PG12	GPIO-OUT	USB0-DRV
PMU	Define	Function
GPIO0	GPIO-OUT	LCD-PWR
GPIO1	GPIO-OUT	LCD-BL-EN
GPIO2	GPIO-OUT	CSI-PWR-EN
GPIO3	GPIO-OUT	CSI-RST

POWER TREE

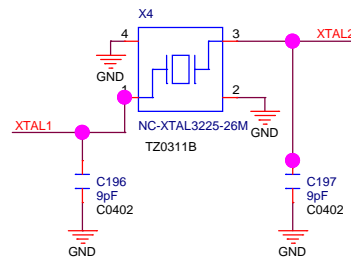
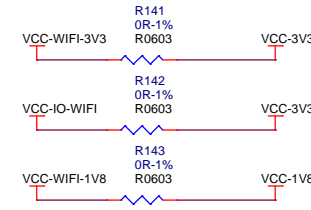
LAYOUT: DCIN, BT, IPSOUT 输入或输出线，从管脚处就要保证尽量粗。



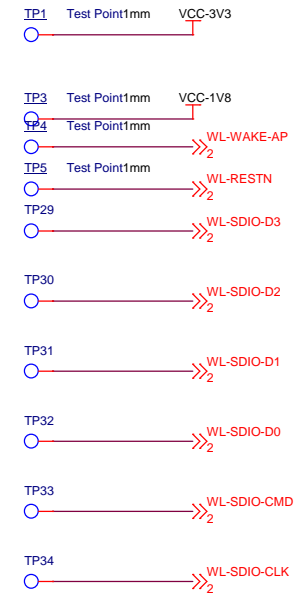
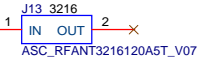
Wi-Fi



PI Matching Circuit for ANT
这部分电路根据天线的实际情况进行调整。



ANTA



Title			<Title>
Size	Document Number	Rev	
B	<Doc>	<Rev Code>	
Date:	Wednesday, June 01, 2016	Sheet	1 of 1