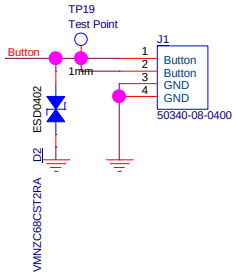
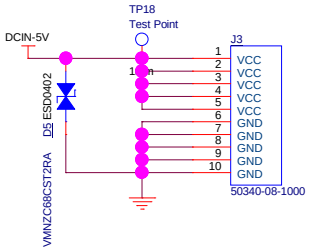
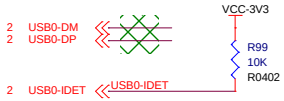
Button



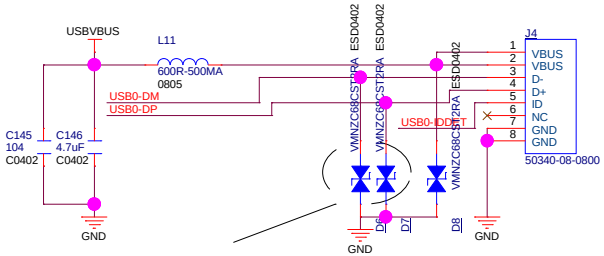
PCB Power Assay





USB-DEVICE

Differential pairs
Z0= 90 ohm



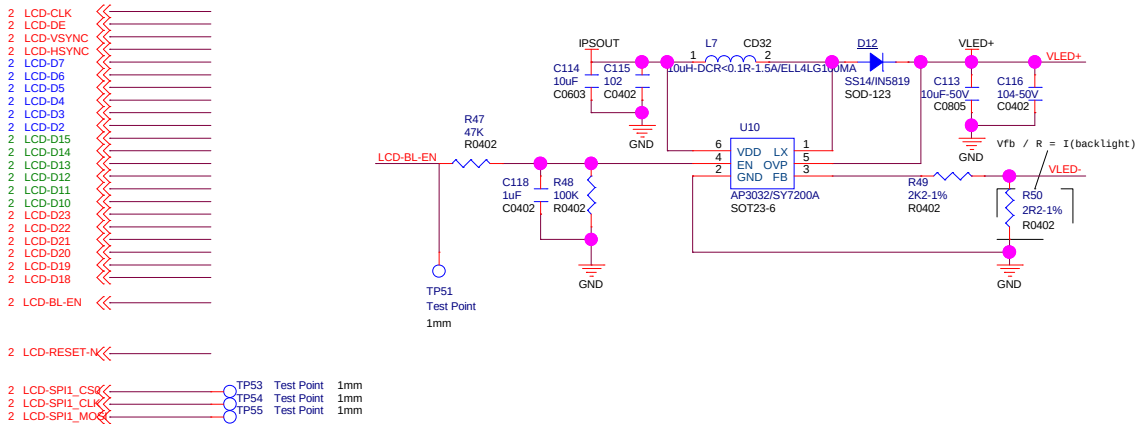
D+/D- 上的 ESD 器件电 容 小 于等于 4 pF(包括了误差)。

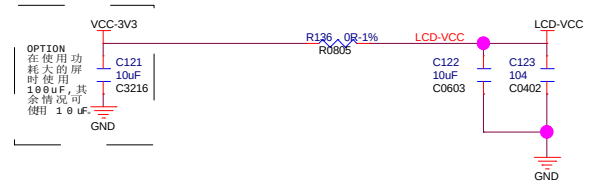
M1
Bad Mark

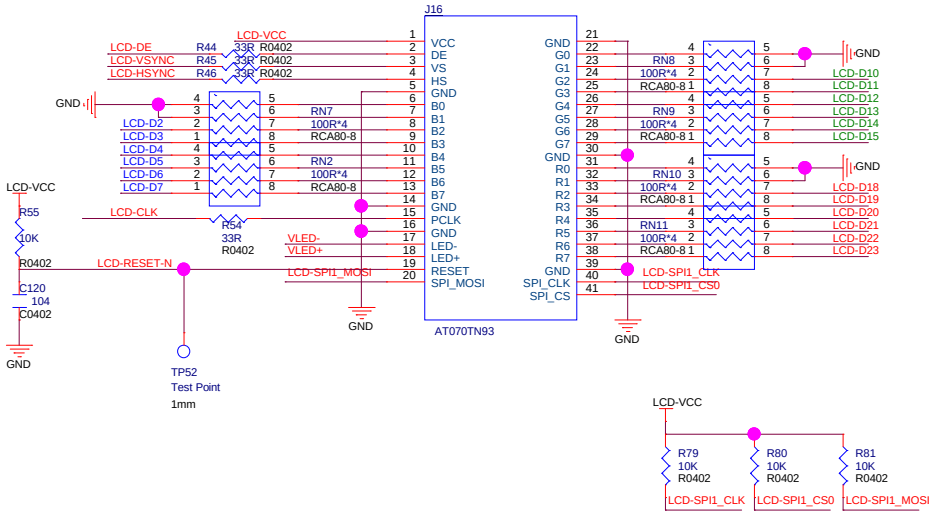
M2
Bad Mark

DISPLAY

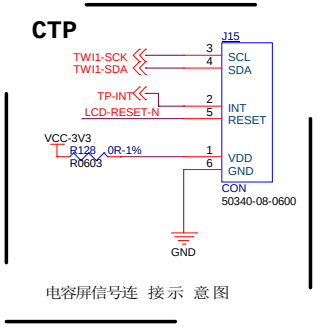
LCD







CTP

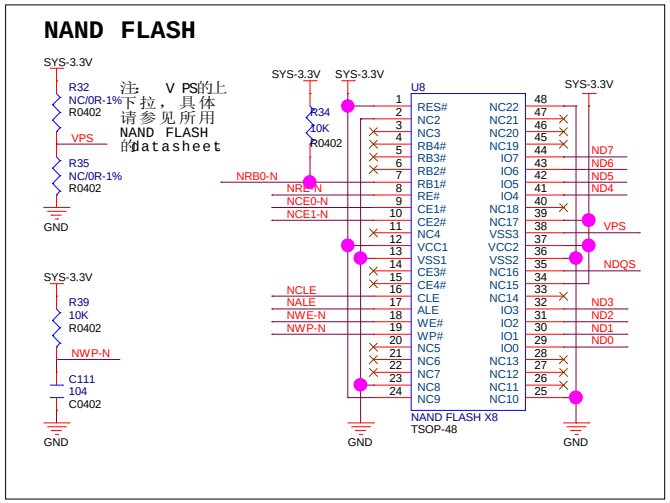


电容屏信号连 接示 意图

FLASH/CARD

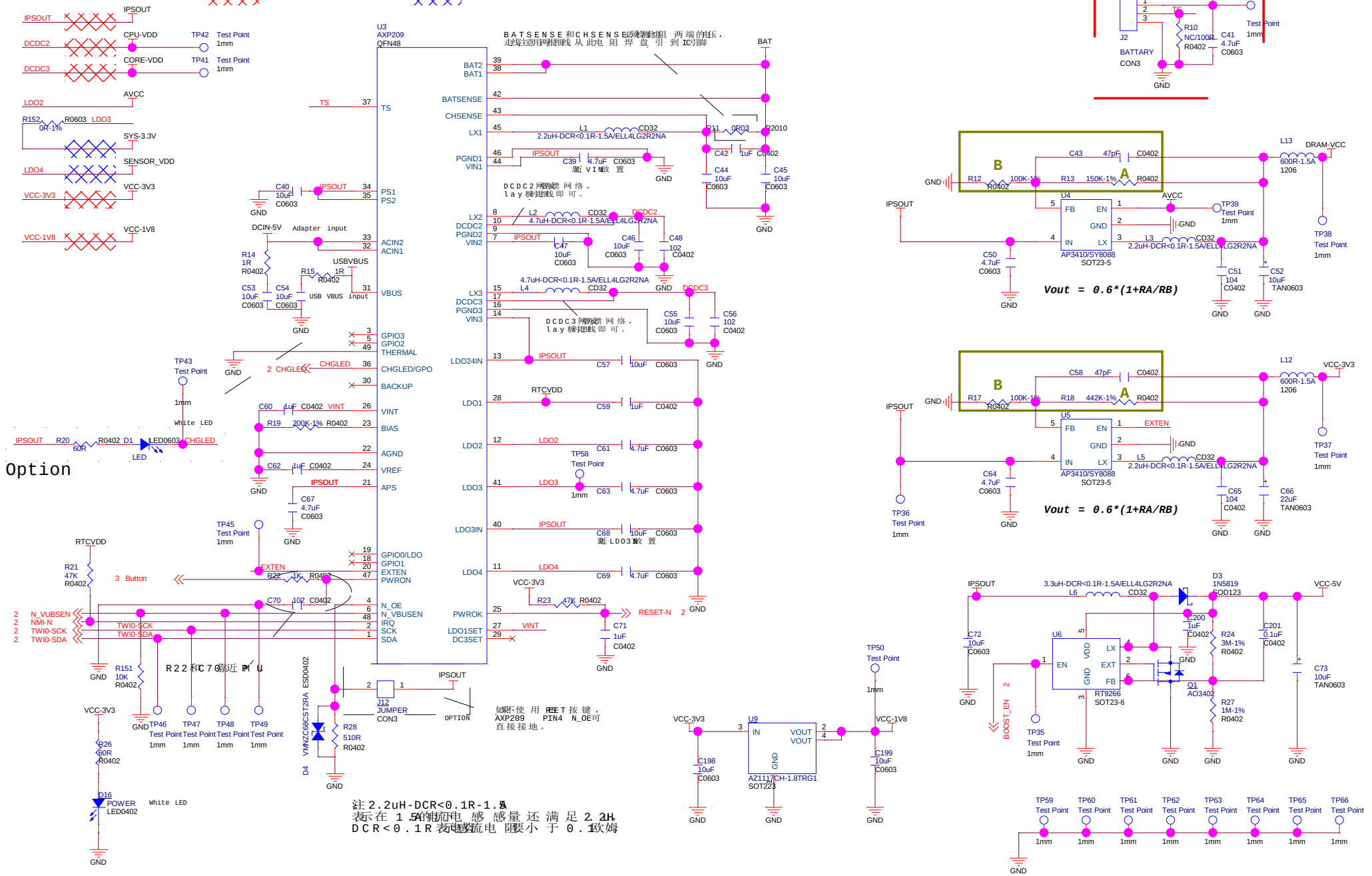
2 ND[7:0] — ND[7:0]
2 NDQS — NDQS

2 NRB0-N — NRB0-N
2 NRE-N — NRE-N
2 NCE0-N — NCE0-N
2 NCE1-N — NCE1-N
2 NCLE — NCLE
2 NALE — NALE
2 NWE-N — NWE-N



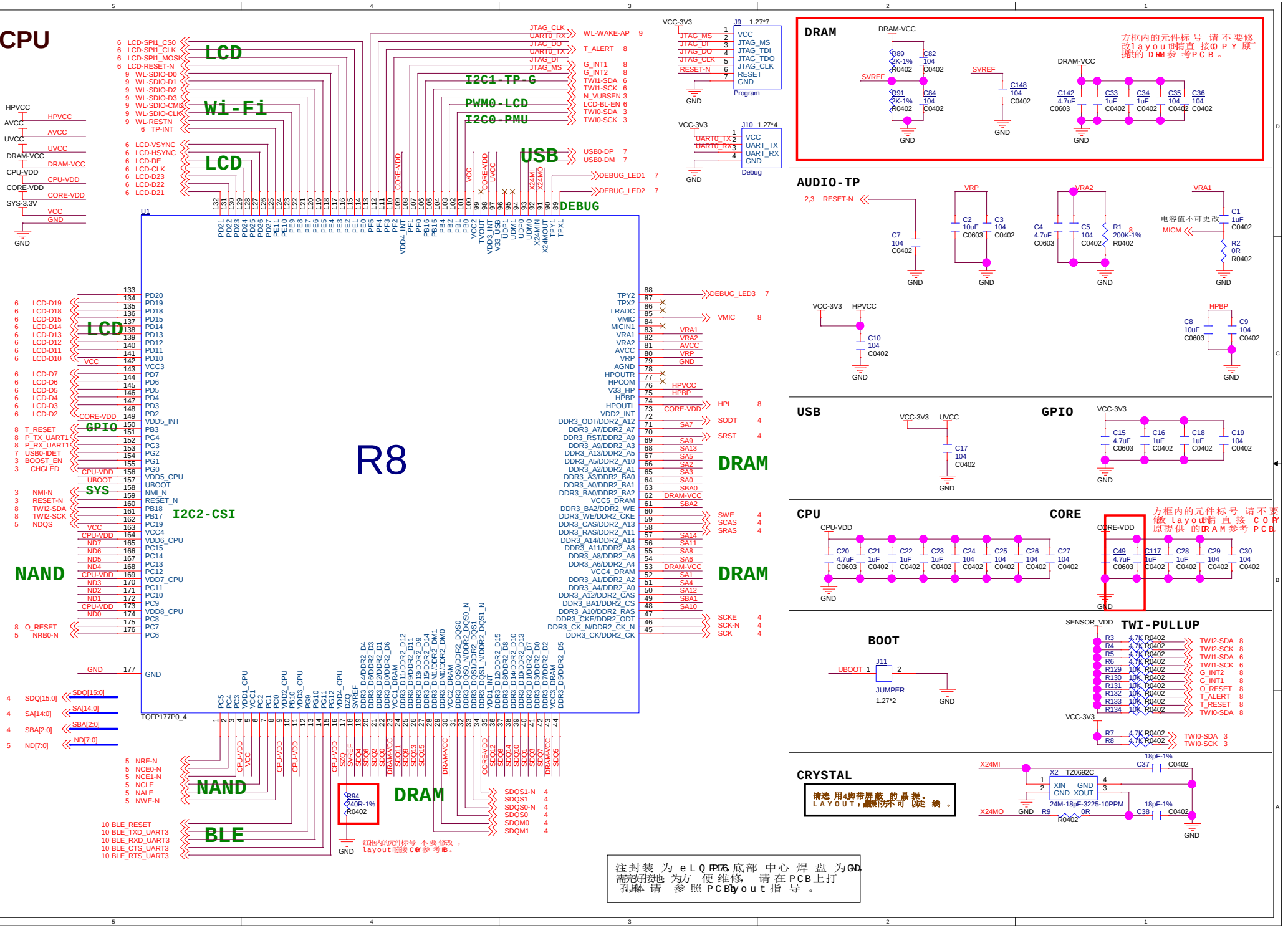
POWER

POWER LINE:Width>=80mil POWER LINE:Width>=50mil



Option

注 2.2uH-DCR<0.1R-1.5A
表示在 1.5A的额定电感量还满足2.2uH
DCR<0.1R表示额定电阻要小于0.1欧姆


CPU
R8
LCD
Wi-Fi
LCD
USB
DEBUG
I2C1-TP-G
PWM0-LCD
I2C0-PMU
LCD
GPIO
SYS
I2C2-CSI
NAND
NAND
BLE
DRAM
DRAM
DRAM
Program
Debug
DRAM
AUDIO-TP
USB
GPIO
CPU
CORE
BOOT
TWI-PULLUP
CRYSTAL
TQFP177P0_4
注封装为eLQFP176底部中心焊盘为GND需连接地，为方便维修，请在PCB上打孔，详请参照PCB layout指导。

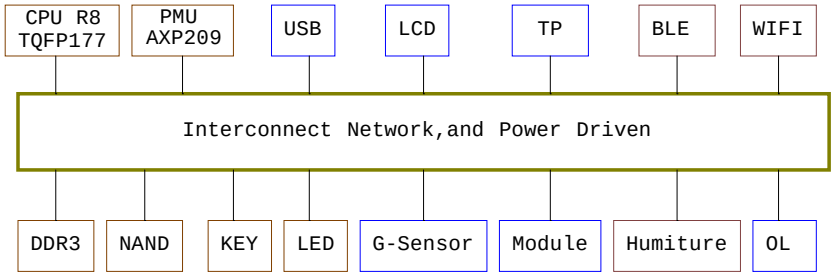
COVER

Schematics Index

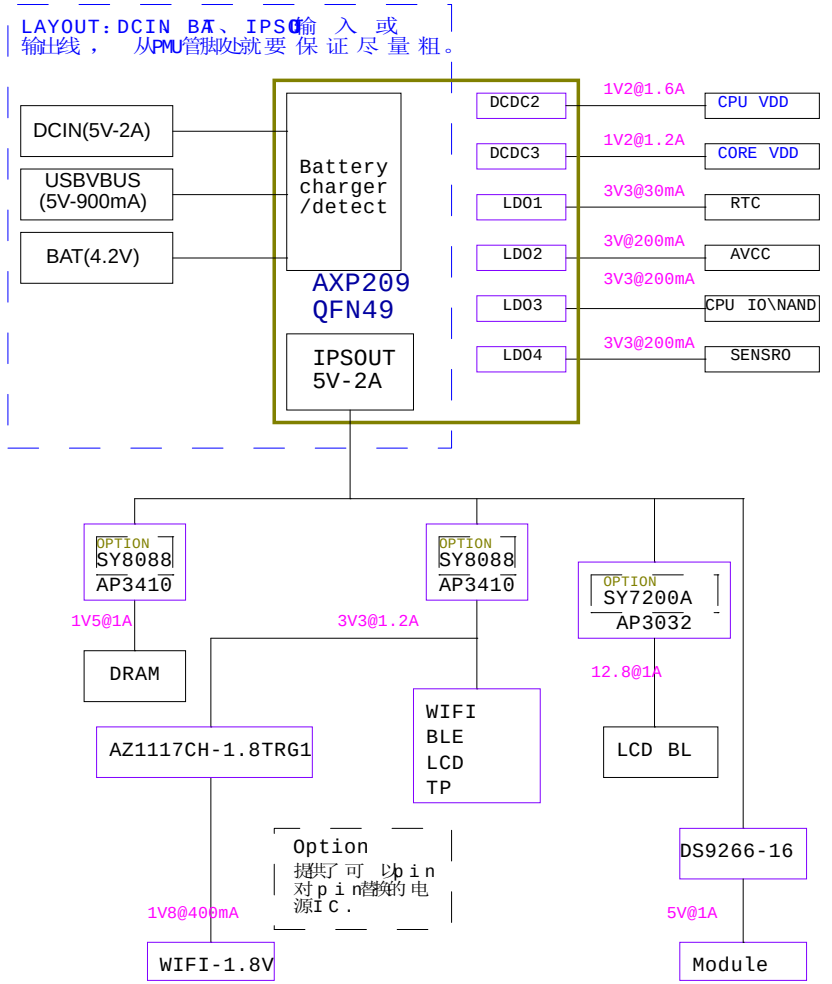
Bran-Design

特别提醒：
1:PG0 / PG1 / PG2这个PIN脚
如果有INPUT功能有 功 能 。
2：PMU的GPIO0/1/2这四个P IN 脚
做GPIO-OUTPUT功能
3:PG10 / PG11 / PG12这个PIN脚
的功能可改变。
4:CSI-PCLK / CSI-MCLK这个P I N 脚
如果有INPUT功能有 功 能 。
5：CSI-HSYNC如果有INPUT功有 功 能 ，
不能用途 。

BLOCK



POWER TREE



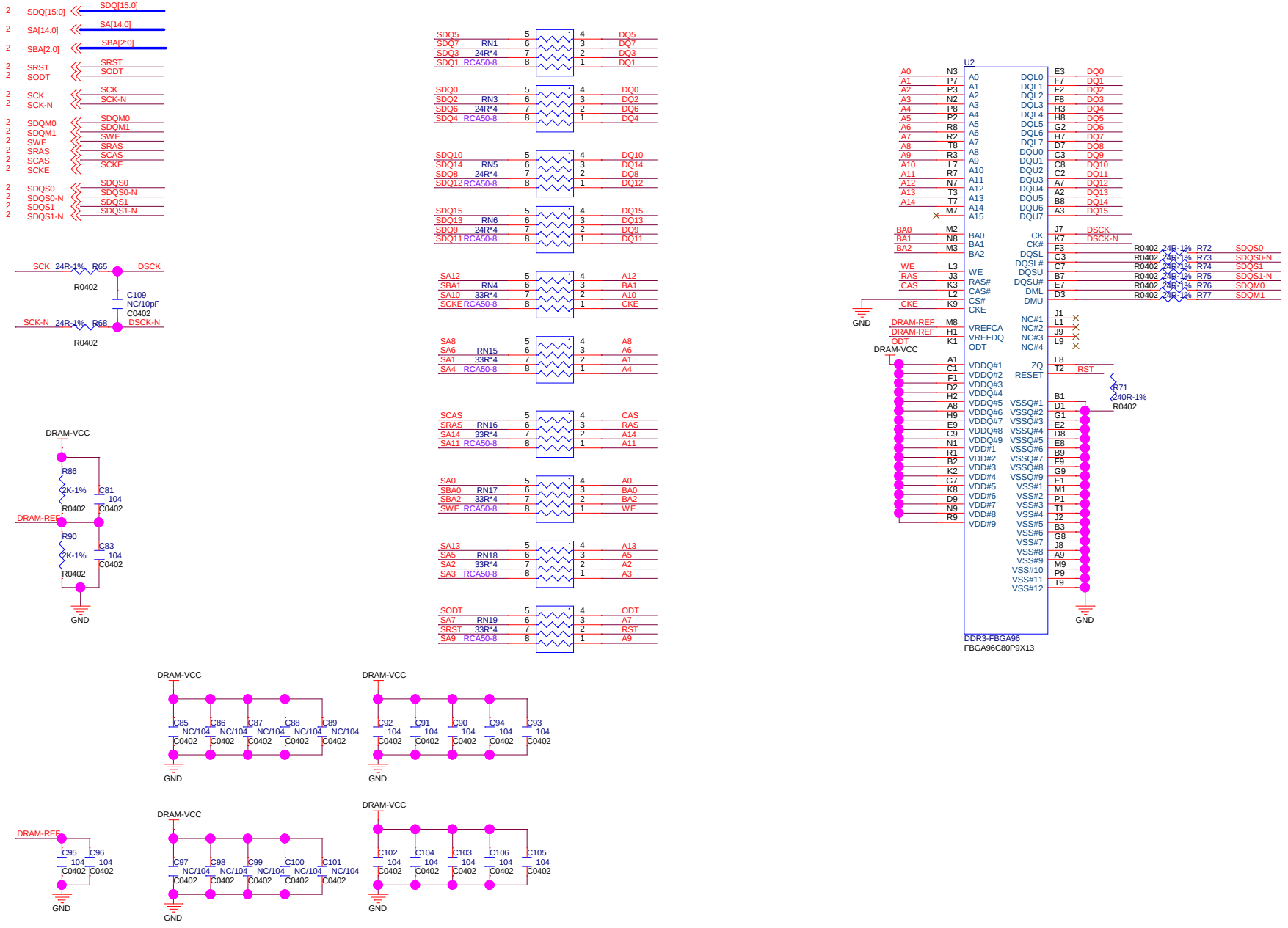
REVISION HISTORY

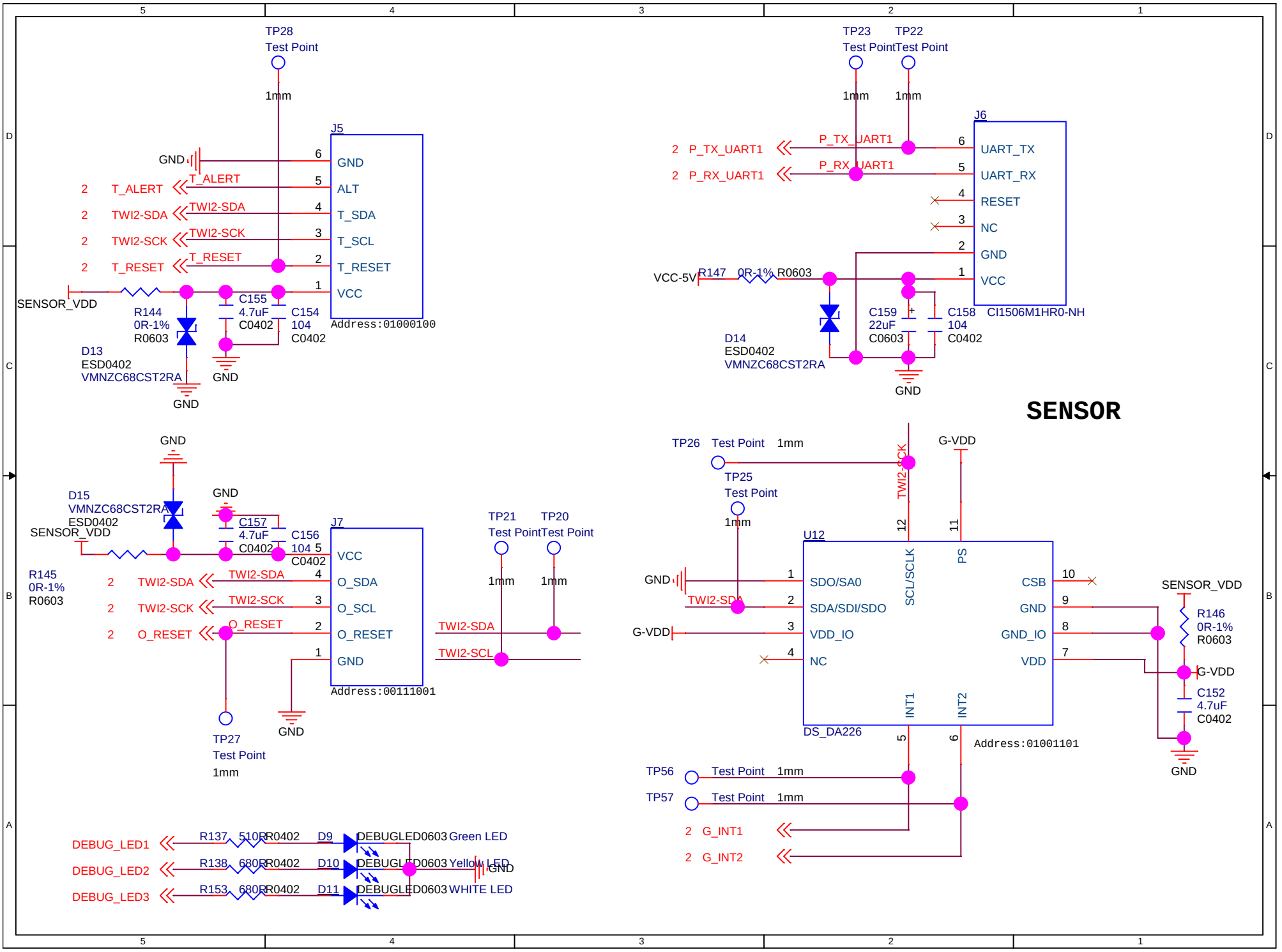
Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Bran Main PCB ASSY	2016/6/2	Violet/Jemmey	Jemmey	

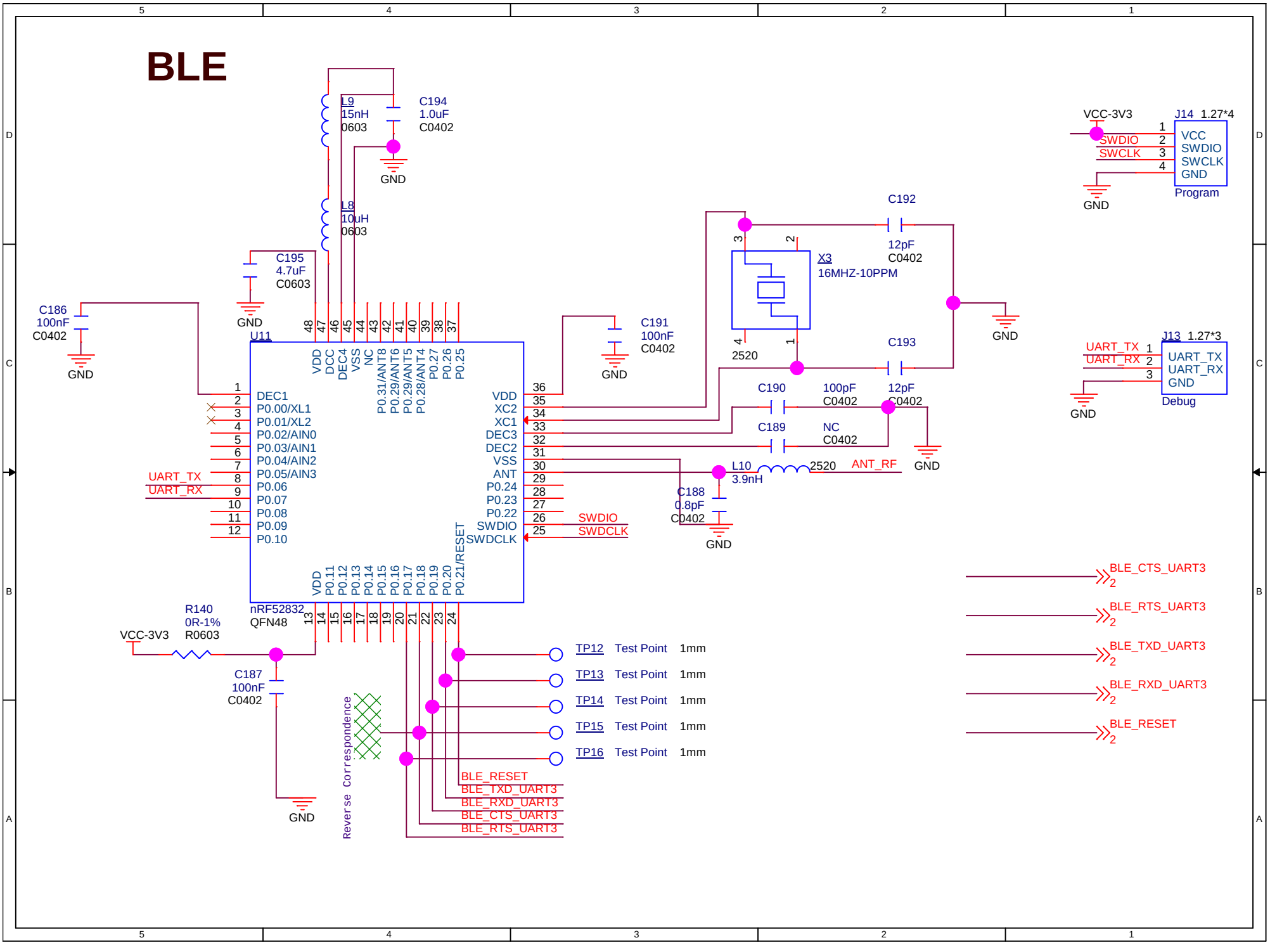
DDR3 16x1

DDR3

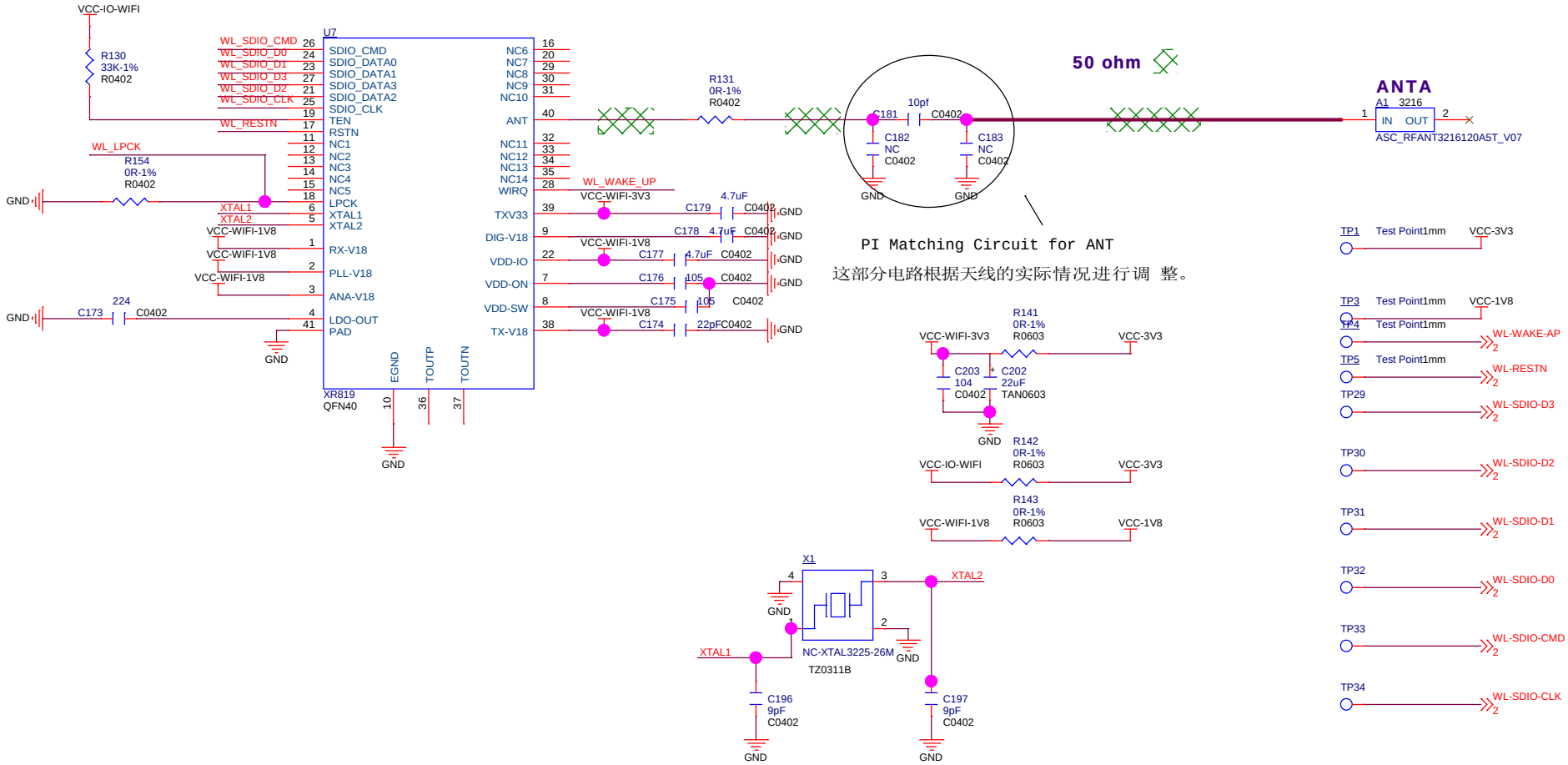
本页的元件标号请不要修改
layout时直接COPY原厂提供
的DRAM参考PCB




SENSOR
TP28
Test Point
1mm
J5
GND
T_ALERT
TWI2-SDA
TWI2-SCK
T_RESET
SENSOR_VDD
R144
0R-1%
R0603
C155
4.7uF
C0402
C154
104
C0402
D13
ESD0402
VMNZC68CST2RA
GND
Address:01000100
TP23
Test Point
TP22
Test Point
J6
P_TX_UART1
P_RX_UART1
UART_TX
UART_RX
RESET
NC
VCC-5V
R147
0R-1%
R0603
C159
22uF
C0603
C158
104
C0402
CI1506M1HR0-NH
D14
ESD0402
VMNZC68CST2RA
D15
VMNZC68CST2RA
ESD0402
C157
4.7uF
C0402
C156
104
C0402
J7
R145
0R-1%
R0603
O_RESET
TP21
Test Point
TP20
Test Point
TP27
Test Point
TP26
Test Point
TP25
Test Point
U12
SDO/SA0
SDA/SDI/SDO
VDD_IO
CSB
GND_IO
VDD
SCL/SCLK
PS
INT1
INT2
DS_DA226
Address:01001101
G-VDD
R146
0R-1%
R0603
C152
4.7uF
C0402
TP56
TP57
G_INT1
G_INT2
DEBUG_LED1
DEBUG_LED2
DEBUG_LED3
R137
510R
R138
680R
R153
680R
R0402
D9
D10
D11
DEBUGLED0603
Green LED
Yellow LED
WHITE LED


BLE
L9
15nH
0603
C194
1.0uF
C0402
GND
L8
10uH
0603
C195
4.7uF
C0603
C186
100nF
C0402
U11
nRF52832
QFN48
DEC1
P0.00/XL1
P0.01/XL2
P0.02/AIN0
P0.03/AIN1
P0.04/AIN2
P0.05/AIN3
P0.06
P0.07
P0.08
P0.09
P0.10
VDD
DCC
DEC4
VSS
NC
P0.31/ANT8
P0.29/ANT6
P0.29/ANT5
P0.28/ANT4
P0.27
P0.26
P0.25
VDD
XC2
XC1
DEC3
DEC2
VSS
ANT
P0.24
P0.23
P0.22
SWDIO
SWDCLK
P0.21/RESET
VDD
P0.11
P0.12
P0.13
P0.14
P0.15
P0.16
P0.17
P0.18
P0.19
P0.20
C191
100nF
C0402
C192
12pF
C0402
X3
16MHZ-10PPM
2520
C193
12pF
C0402
C190
100pF
C0402
C189
NC
C0402
L10
3.9nH
2520
ANT_RF
C188
0.8pF
C0402
UART_TX
UART_RX
SWDIO
SWDCLK
R140
0R-1%
R0603
VCC-3V3
C187
100nF
C0402
TP12 Test Point 1mm
TP13 Test Point 1mm
TP14 Test Point 1mm
TP15 Test Point 1mm
TP16 Test Point 1mm
Reverse Correspondence
BLE_RESET
BLE_TXD_UART3
BLE_RXD_UART3
BLE_CTS_UART3
BLE_RTS_UART3
J14 1.27*4
VCC
SWDIO
SWCLK
GND
Program
J13 1.27*3
UART_TX
UART_RX
GND
Debug
BLE_CTS_UART3
BLE_RTS_UART3
BLE_TXD_UART3
BLE_RXD_UART3
BLE_RESET

Wi-Fi



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Size B	Document Number <Doc>	Rev <RevCode>
Date: Saturday, June 04, 2016	Sheet 1 of 1	