XR819 Datasheet

Single-Chip IEEE 802.11 b/g/n WLAN

Version 1.1
May.3, 2016

Revision History

Version	Date	Notes
V1.0	Nov.18, 2015	Initial Release Version
V1.1	May.3, 2016	Change description on page 9

Declaration

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1 System Overview

1.1 General Description

This scope of document is to provide a specification of XR819 Wireless LAN SoC, that will be used by the system/design/development teams to detail the design requirements.

XR819 is a fully integrated 2.4G WLAN SoC to support 802.11 b/g/n. It is optimized for mobile applications such as PDAs and portable media players. The low power consumption and intelligent host off loading of beacon as well as the packet processing ensure better battery life. High sensitivity and transmitting power ensure long distance and robust connection. Highest level of integration allows very compact and cost effective reference designs delivering fast time-to-market for new WLAN enabled products. And small 5x5mm QFN package is suitable for very compact design.

1.2 Features

- Compatible with IEEE 802.11 b/g/n standard
- Clocks
  - – XTAL or external reference clock input from 13~52MHz
  - – Internal or external Low power clock at 32.768 kHz
- On-chip auto calibrations
- Intelligent adaptive power control for
  - – Saving power consumption
  - – Tolerating VSWR variation to maintain EVM performance
- WLAN solution with fully integrated
  - – High power PA
  - – TR switch
  - – Internal impedance matching network
  - – OFDM/CCK PHY processor
  - – SDIO 2.0 host interface
- Support for 6 Mbps to 65 Mbps OFDM
  - –11 Mbps and 5.5 Mbps CCK and legacy
  - – 2 Mbps and 1 Mbps DSSS data rates
- WiFi Direct support with concurrent operation
- Supports MAC enhancements including
  - – 802.11d - Regulatory domain operation
  - – 802.11e - QoS including WMM
  - – 802.11h – Transmit power control dynamic and frequency selection
  - – 802.11i - Security including WPA2 and WAPI compliance

– 802.11r - Roaming

– 802.11w - Management frame protection

1.3 Applications

- Tablet PC applications
- Portable media player(PMP) applications
- Portable gaming device(PGD) applications
- Smart internet TV box applications
- Internet of Thing (IOT)

1.4 Block Diagram

Top level block diagram of XR819 is shown in Figure 1-1.

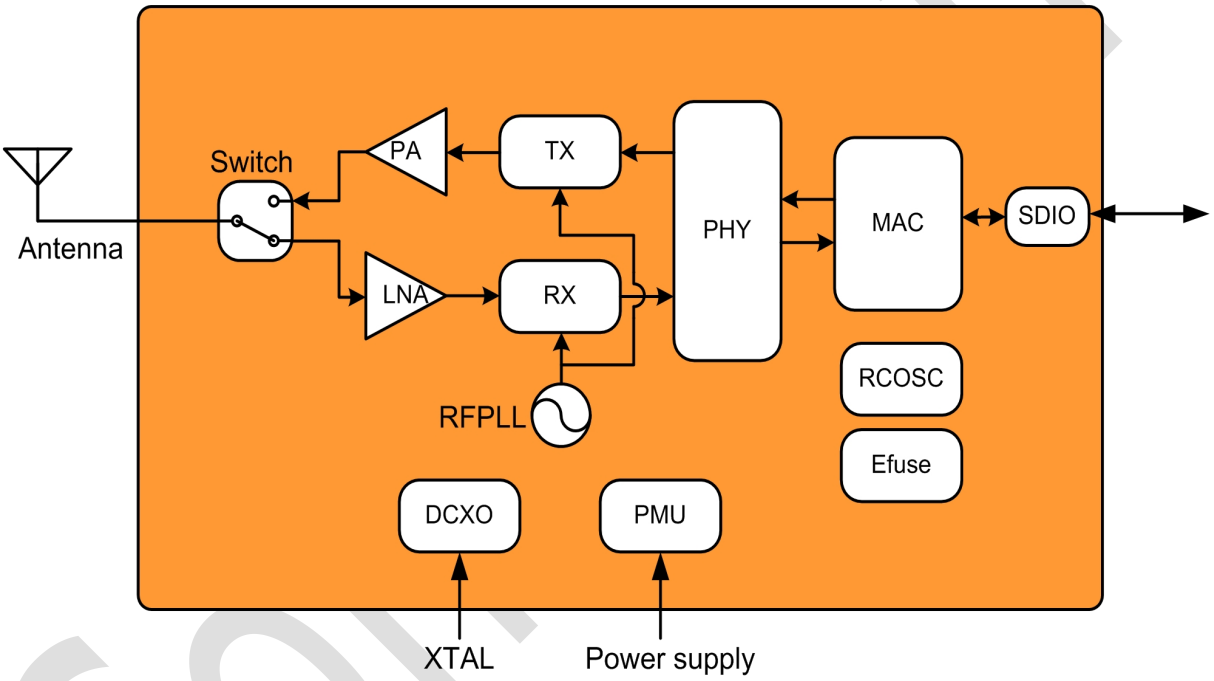


Figure 1-1 XR819 Block Diagram

The WLAN subsystem includes a single-band 2.4G RF transceiver (RX and TX), PA and LNA including RF switch, RFPLL, an OFDM/CCK PHY processor and PMU, that keep data communications with host using SDIO 2.0. This application has industry leading low cost BOM to simplify product development.

2 Pin Description

2.1 Pin Assignment

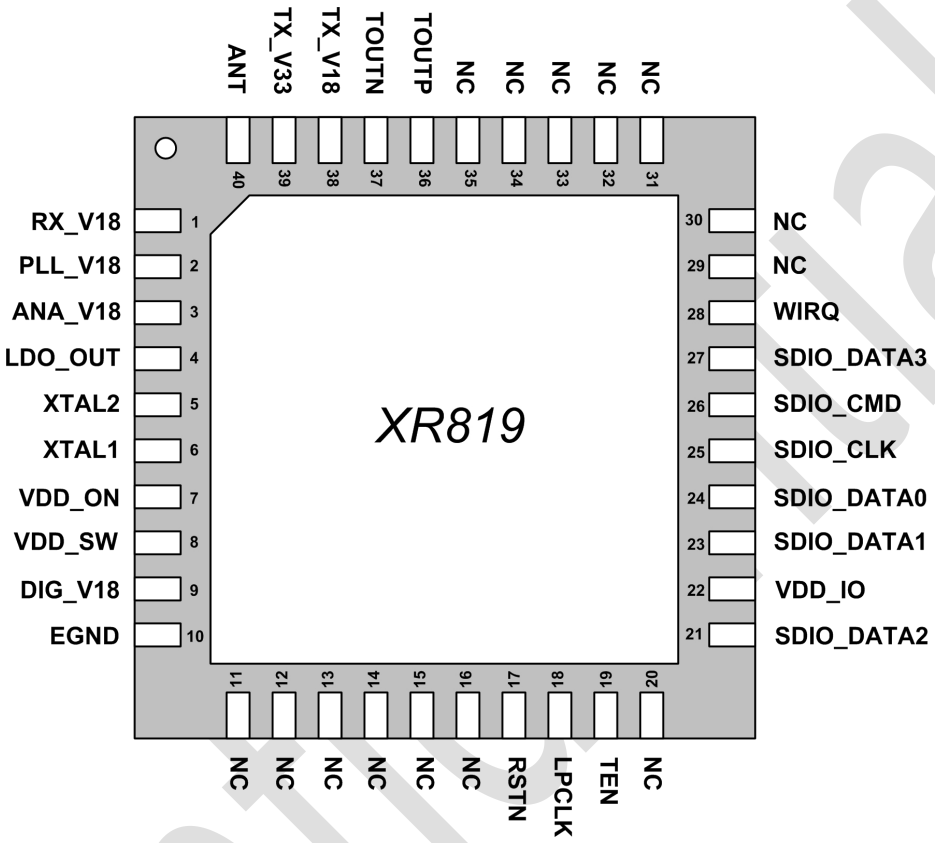


Figure 2- 1 Pin Assignment

2.2 Pin List

The following signal type codes are used in the table:

I: Input

O: Output

I/O: for Input/Output

P: Power pin

Table 2-1 Pin List

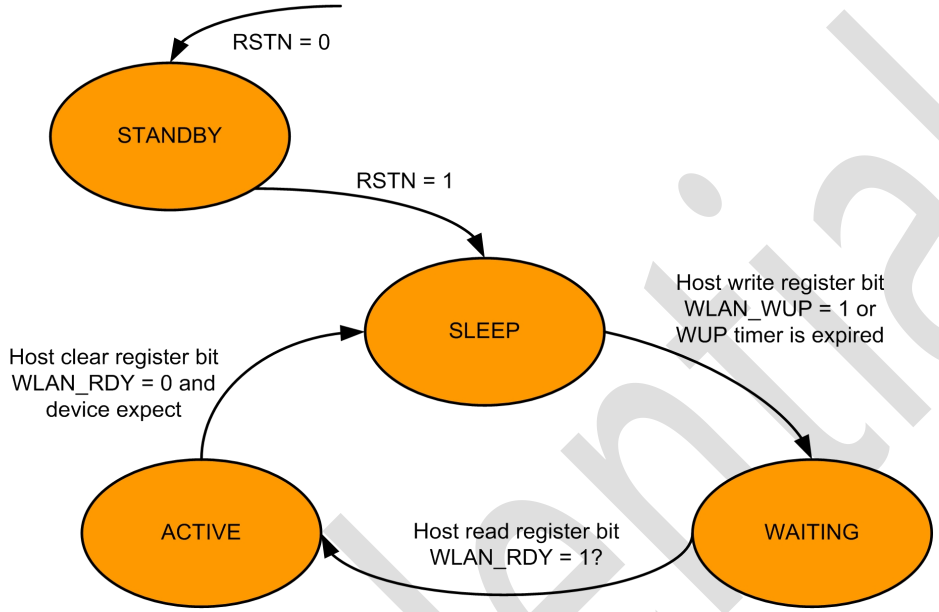
Name	Pin	Type	Description
Analog			

Name	Pin	Type	Description
XTAL1	6	I	Reference clock input or XTAL inputs
XTAL2	5	I	
LPCLK	18	I	Low power clock input, 32 kHz, external pull down
TOUTP	36	O	WLAN test output
TOUTN	35	O	
ANT	40	I/O	2.4 GHz RF input/output
Power			
RX_V18	1	P	Supply for WLAN RX (1.8V)
PLL_V18	2	P	PLL Supply
LDO_OUT	4	P	Internal supply Regulator output (1.2V)
EGND	10	P	Efuse programming supply, connected to GND at read mode
VDD_ON	7	P	Internal supply decoupling / Regulator output (1.1 V)
VDD_SW	8	P	Internal supply decoupling / Regulator output (1.1 V)
DIG_V18	9	P	Supply for WLAN digital LDOs (1.8 V)
VDD_IO	22	P	Supply for digital I/Os (3.3V/1.8 V)
ANA_V18	37	P	Analog supply
TX_V18	38	P	1.8 V Supply for 2.4G Integrated PA
TX_V33	39	P	3.3V Supply for 2.4G Integrated PA
Digital			
RSTN	17	I	Reset – active low
TEN	19	I	Test enable select, active high
WIRQ	28	O	WLAN interrupt request
SDIO_CMD	26	I	SDIO command
SDIO_CLK	25	I	SDIO clock
SDIO_DATA0	24	I/O	SDIO data
SDIO_DATA1	23	I/O	SDIO data
SDIO_DATA2	21	I/O	SDIO data
SDIO_DATA3	27	I/O	SDIO data
Not Used			
NC	11		Not Connected
NC	12		Not Connected
NC	13		Not Connected
NC	14		Not Connected
NC	15		Not Connected
NC	16		Not Connected
NC	20		Not Connected

Name	Pin	Type	Description
NC	29		Not Connected
NC	30		Not Connected
NC	31		Not Connected
NC	32		Not Connected
NC	33		Not Connected
NC	34		Not Connected
NC	35		Not Connected

3 Power Supply

3.1 Power Up and Power Down



There is no constraint on the power supplies (V18,V33 and VDD_IO) activation sequence. The device can start up without the reference clock being present. The platform is than expected to provide a stable clock within T_{stable} ms (see reference value in chapter 4) unless the built-in XTAL oscillator is used. A typical startup for the WLAN system is as follows:

(1) V18, V33, VDD_IO is applied.
(2) The RSTN pin is released after at least two LP_CLK cycles.
(3) The host should wait 30 ms after the RSTN release for the on-chip LDO to stabilize.
(4) The device is now in the Sleep state.
(5) The host should now wake the device by writing over the host interface SDIO, to the WUP bit.
(6) Within T_{stable} ms, the reference clock should be stable and the system can start using it.
(7) The device will set the RDY (ready) bit and assert WIRQ to the host.
(8) The host can download the firmware and release the CPU reset by further SDIO write.
(9) The host now waits for the XR819 to initialize and can clear the WUP bit.
(10) Once initialized, which includes a series of messages passing between the host and the WLAN, the WLAN may not have anything further to do and will enter the sleep state.

To power down the device, RSTN have to be set to 0. There are no constraints on other input pins (although it is recommended to give at least two LP_CLK cycles after asserting RSTN = 0). VDD_IO is allowed to go down 20 ms after all input signals have been set to 0(avoid the influent current).

3.2 Analog Power Supply

Table 3-1 Analog Power Supply

Symbol	Parameter	Min	Typ	Max	Unit
TX_V33	TX PA 3.3V power supply	3.0	3.3	3.6	V
RX_V18	RX LDO power supply	1.62	1.8	1.98	V
PLL_V18	PLL power supply	1.62	1.8	1.98	V
LDO_OUT	LDO 1.2V output	1.14	1.2	1.26	V
TX_V18	TX PA 1.8V power supply	1.62	1.8	1.98	V
ANA_V18	Analog power supply	1.62	1.8	1.98	V

3.3 Digital Power Supply

Table 3-2 Digital Power Supply

Symbol	Parameter	Min	Typ	Max	Unit
VDD_IO	IO power supply	2.5	3.0	3.6	V
DIG_V18	Digital LDO power supply	1.62	1.8	1.98	V
VDD_ON	Digital 1 supply (internal)	0.9	1.1	1.16	V
VDD_SW	Digital 2 supply (internal)	0.9	1.1	1.16	V

4 Clocks

XR819 uses two clocks,a reference clock and a low power clock.

For the reference clock, XR819 can either use an external reference clock source or generate its own reference using a XTAL and a built-in oscillator.

The low-power clock is used during power save modes and used only for power controller module.This clock will operate at about 32.768 KHz. If this clock is not available, XR819 will use the internal 32.768KHz clock coming from internal block. By this way, XR819 can still get a low power clock to function properly.

4.1 Reference Clock

Table 4-1 External Reference Clock Specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Clock input frequency list using an external clock source	13	26	52	MHz
	Clock input frequency list using a XTAL and the built-in oscillator	19.2	26	52	MHz
F_{INTOL}	Tolerance on input frequency without trimming	-20	-	+20	ppm
T_{stable}	Clock stabilization time	-	-	10	ms
I_{LEAK}	Input leakage current, both for analog and digital	-	-	1	uA

Clock frequency detection

An integrated automatic detection algorithm detects the reference clock frequency using the low power clock after a hardware reset.

Clock source detection

An integrated automatic detection mechanism detects the clock source from the connections of the XTAL1 and XTAL2 pins:

• When an external reference clock source is used, the clock input pin is XTAL2. The XR819 supports both an analog and digital source. An analog source shall be AC coupled to XTAL2 while a digital source shall be DC coupled to XTAL2. In both cases, XTAL1 shall be DC grounded.

• When a XTAL and the built-in oscillator are used, the XTAL shall be DC coupled to XTAL1 and XTAL2.

External Clock Source

• Requirements

Table 4-2 External Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
AC coupled signal					
F_{IN}	Frequency	13	26	52	MHz
V_{APP}	Peak-to-peak voltage range of the AC coupled analog input	0.4	0.5	1.2	Vpp
N_H	Total harmonic content of the input signal	-	-	-25	dBc
DC coupled signal					
V_{IL}	input low voltage on XTAL2	0	-	0.3*V18	V
V_{IH}	input low voltage on XTAL2	0.7*V18	-	V18	V
T_r/T_f	10%-90% rise and fall time	-	-	5	ns
Duty cycle	Cycle-to-cycle	40	50	60	%
Both analog and digital signals					
Z_{INRE}	Real part of parallel AC input impedance at the pin	30	-	-	KOhm
Z_{INIM}	Imaginary part of parallel AC input impedance at the pin	-	3.5	5	pF
Z_{DC}	DC input impedance	1	-	-	MOhm
Phase noise	Ref clock @ 26 MHz, 2.4 GHz 802.11b/g/n operation @1 kHz @10 kHz @100 kHz @1 MHz	-	-	 -123 -133 -138 -138	dBc/Hz

External XTAL and Built-in Oscillator

Table 4-3 External Crystal Characteristics Requirements

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range		13	-	52	MHz
ESR		-	-	60	Ohm
C_{in_xtal}(1)	Single-ended	3.5	7	11	pF
Load capacitance(1)		-	8	27	pF
Oscillator tuning range(2)		+/-20	+/-50	+/-70	ppm
Crystal frequency accuracy at nominal temperature	25 °C	-10	-	+10	ppm
Crystal drift due to temperature	-20 °C to +85 °C	-10	-	+10	ppm
Crystal pull ability		10	-	150	ppm/pF

(1). The load capacitance value (C_{load}) depends on XTAL model, XTAL1 and XTAL2 pin have extra

capacitance(C_{in_xtal}), so external added load capacitance value $C_{load\_ext}=C_{load}-C_{in\_xtal}$. C_{in_xtal} has tuning range about 7pF, which is controlled by software, for details please go to software user manual.

(2). Tuning range depends on XTAL load capacitance requirement, typical case is based on 26MHz XTAL, 8pF C_{load}.

4.2 Low Power Clock

Table 4-4 Low Power Clock Specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Frequency	-	32.768	-	KHz
F/F_{IN}	Frequency accuracy	-1000	-	+1000	ppm
Duty cycle		30	-	70	%
Jitter	Cycle-to-cycle	-40	-	+40	ns
R_{in}	Input resistance	1	-	-	MOhm
C_{in}	Input capacitance	-	-	5	pF
V_{IL}	Input low voltage on LPCLK	0	-	0.4	V
V_{IH}	Input high voltage on LPCLK	VDD_IO-0.4	-	VDD_IO	V

5 Electrical Characteristics

5.1 Absolute Maximum Rating

The Absolute Maximum Rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown).

Table 5-1 Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
V33	3.3V power supply	-0.3	4.0	V
V18	1.8V power supply	-0.3	2.5	V
VDD_IO	IO power supply	-0.3	4.0	V
Vin	Input voltage on any digital pin	-0.3	3.6	V
T_{stg}	Storage Temperature	-40	150	°C
T_a	Ambient Operating Temperature	-20	85	°C

5.2 Digital IO Pin DC Characteristics

Table 5-2 IO DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Input high voltage	2.06	3.3	3.6	V
V_{IL}	Input low voltage	--	0	1.32	V
V_{OH}	Output high voltage	2.9	--	3.3	V
V_{OL}	Output low voltage	0	--	0.4	V

5.3 ESD Threshold Voltages

Table 5-3 ESD Threshold Voltages

Parameter	Conditions	Value	Unit
ESD	HBM (JESD22-A114-F)	+/-3500	V
	CDM (JESD22-C101F)	+/-500	V

5.4 SDIO Interface AC Characteristics

The SDIO interface is a 4 or 6-wire data interface (SDIO_CLK, SDIO_CMD, SDIO_DATA0, SDIO_DATA1/INT, optional SDIO_DATA2 and SDIO_DATA3), compatible with SDIO 2.0 standard. In addition a 7th wire can be used for the optional WIRQ function.

The 7 signals of the SDIO interface are the following:

– SDIO_CLK: clock signal.

– SDIO_CMD: Bidirectional SDIO command line.

– SDIO_DATA0: Bidirectional data line.

– SDIO_DATA1/INT: Bidirectional data line. When no data is present on the line, it is used as interrupt from the slave, used to request an SDIO transfer from the slave to the master.

– SDIO_DATA2: Optional bidirectional data line.

– SDIO_DATA3: Optional bidirectional data line.

– WIRQ: Optional un-multiplexed INT (interrupt) to Host

The maximum operating frequency is 50 MHz. The SDIO interface in XR819 supports the timing defined below.

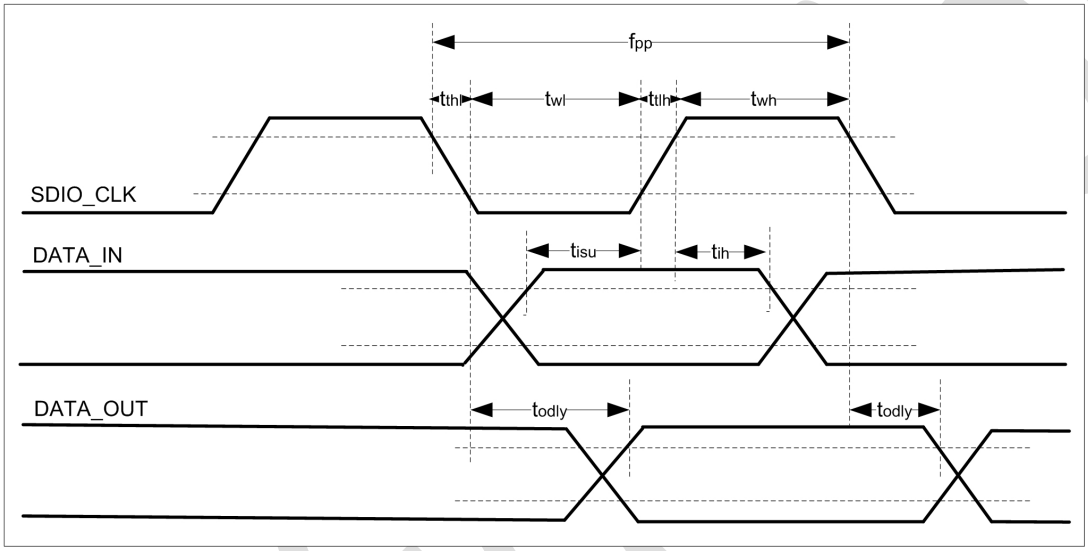


Figure 5-5 SDIO Interface Timing

Table 5-4 SDIO Interface AC Parameters

Symbol	Parameter	Min	Typ	Max	Unit
C_{in}	Input capacitance	-	-	5	pF
C_{load}	Driving load capacitance	10	-	-	pF
R_{in}	Input resistance	1	-	-	MOhm
R_{out}	Output resistance	35	50	115	Ohm
f_{pp}	Clock frequency	0	-	50	MHz
t_{thl}	Clock fall time	-	-	3	ns
t_{tlh}	Clock rise time	-	-	3	ns
t_{wl}	Clock low time	7	-	-	ns
t_{wh}	Clock high time	7	-	-	ns
t_{isu}	Input setup time	6	-	-	ns
t_{ih}	Input hold time	2	-	-	ns
t_{odly}	Output delay time	-	-	14	ns

6 WLAN Transceiver Performance

TBD.

7 Package Mechanical Dimensions

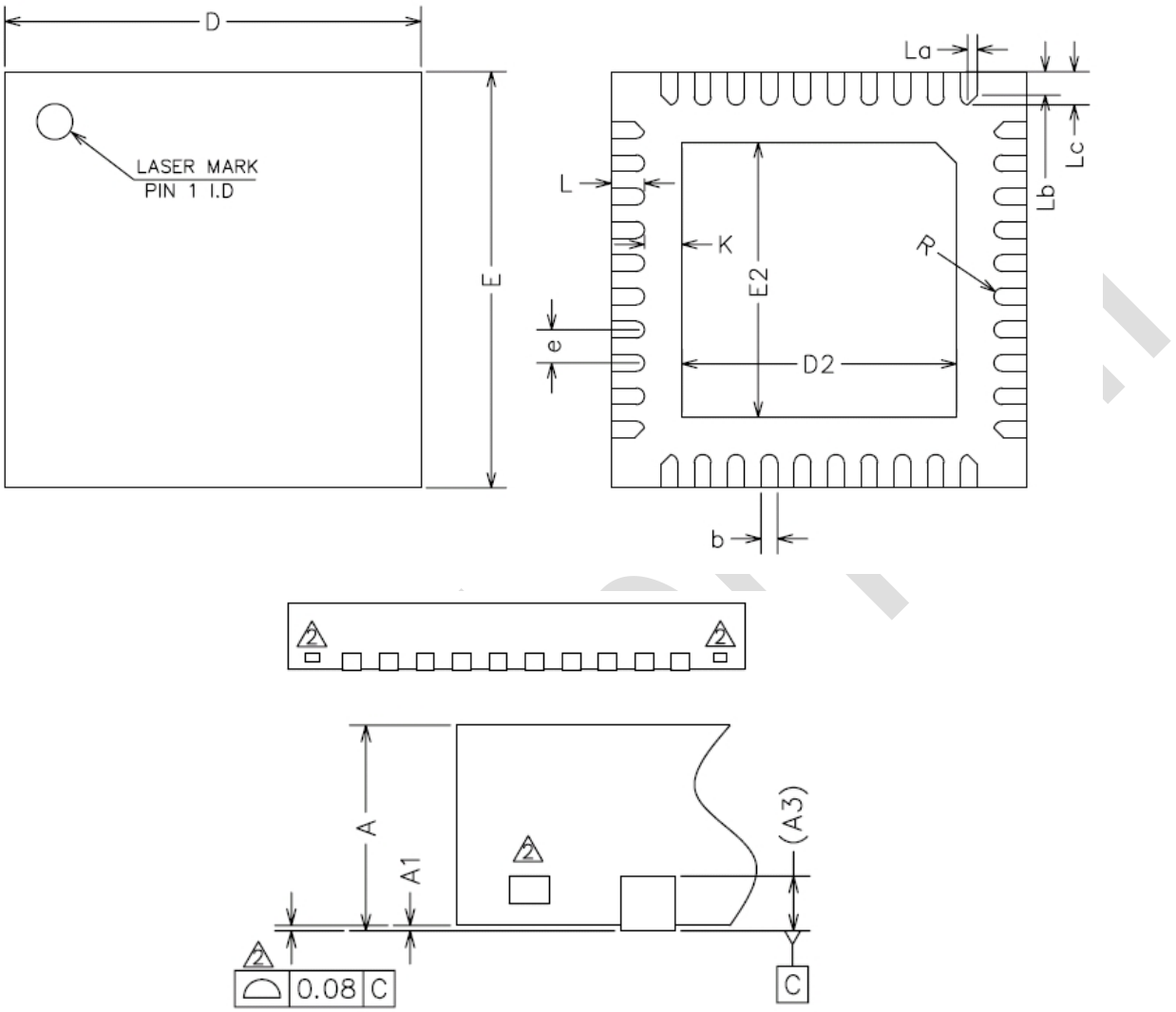


Figure 7-1 Package Dimensions

Table 7-1 Package Dimensions

Symbol	Min	Typ	Max	Unit
A	0.70	0.75	0.80	mm
A1	0	0.02	0.05	mm
A3	0.20REF			mm
b	0.15	0.20	0.25	mm
D	4.90	5.00	5.10	mm
E	4.90	5.00	5.10	mm
D2	3.15	3.30	3.45	mm

E2	3.15	3.30	3.45	mm
e	0.30	0.40	0.50	mm
K	0.20	-	-	mm
L	0.30	0.40	0.50	mm
R	0.09	-	-	mm
La	0.12	0.15	0.18	mm
Lb	0.23	0.26	0.29	mm
Lc	0.30	0.39	0.50	mm

8 Ordering Information

Table 8-1 Ordering Information

Part Number	Package	Status
XR819-xxx	5mm*5mm QFN 40 pin	MP

Glossary

ADC	Analog digital converter
AGC	Automatic Gain Control
APE	Application Engine
ABB	Analog BaseBand
BB	BaseBand (or DBB, Digital BB)
DAC	Digital -to-Analog Converter
DCO	DC Offset
DCXO	Digitally Controlled Crystal Oscillator
DSSS	Direct Sequence Spread Spectrum
ENOB	Effective Number Of Bits
ESD	Electro-Static Discharge
EVM	Error Vector Magnitude
FDD	Frequency Domain Duplex Mode
FEM	Front-End Module
FFT	Fast Fourier Transform
FM	Frequency Modulation
HBM	ESD standard (Human Body Model)
HIF	Host interface
IF	Intermediate Frequency
IIP3	Input referred third order Intercept Point
IM3	Third Order Inter-modulation product
IMD	Inter-modulation Distortion (expressed relative to the signal)
IP	Intellectual Proprietary
IPD	Integrated Passive Device
IP3	Third Order Intercept Point
LDO	Low Dropout Regulator
IF	Intermediate Frequency
I/O	Input(s) / Output(s)
LNA	Low noise amplifier
LO	Local oscillator
LSB	Least Significant Bit
MAC	Media Access Control
NF	Noise Figure
OFDM	Orthogonal Frequency Division Multiplexing

OIP3	Output referred third order Intercept Point
PA	Power Amplifier
PAR	Peak to Average power Ratio
PCB	Printed Circuit Board
PLL	Phase Lock Loop
PMA	Post Mixer Amplifier
PMU	Power Management Unit
PEP	Peak Envelope Power
IP1dB	Input referred 1-dB compression point
OP1dB	Output referred 1-dB compression point
RAM	Random access memory
RX	Reception
RMS	Root Mean Square
SMD	Surface Mounted Component
SQNR	Signal-to-Quantitation Noise Ratio
SoC	System On Chip
TBC	To Be Confirmed
TBD	To Be Defined
TDD	Time Domain Duplex Mode
TX	Transmission
TR	Transmission and Reception
VBAT	Battery voltage
VSWR	Voltage Stationary Wave Ratio
WLAN	Wireless Local Area Network
XTAL	Crystal
ZIF	Zero Intermediate Frequency

