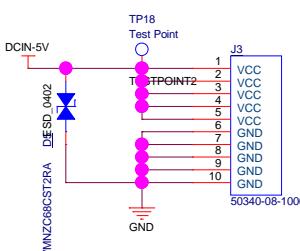
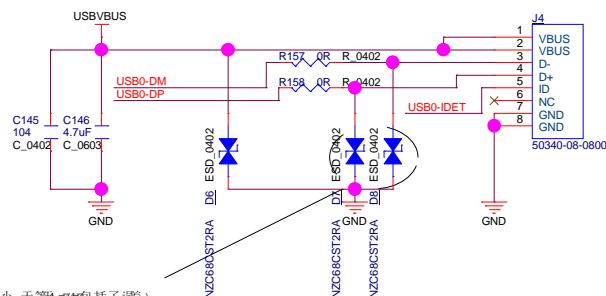


PCB Power Assay



USB-DEVICE

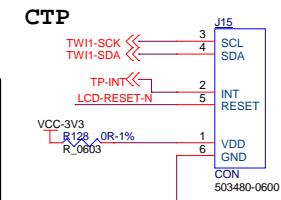
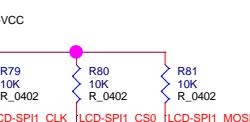
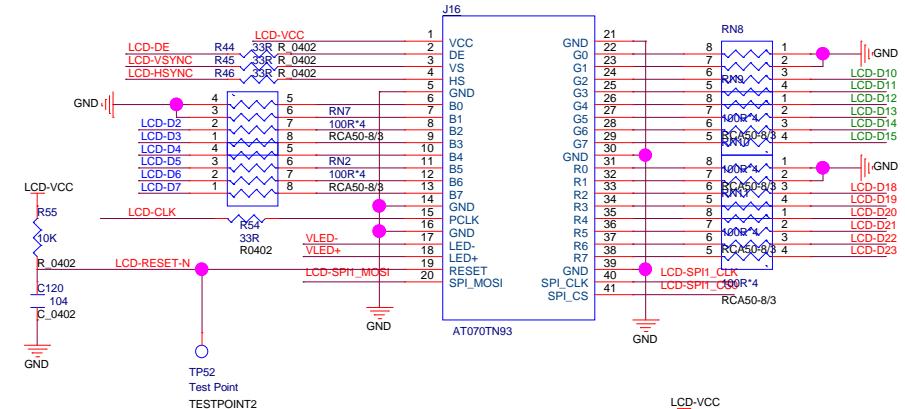
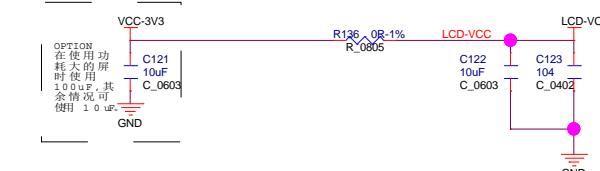
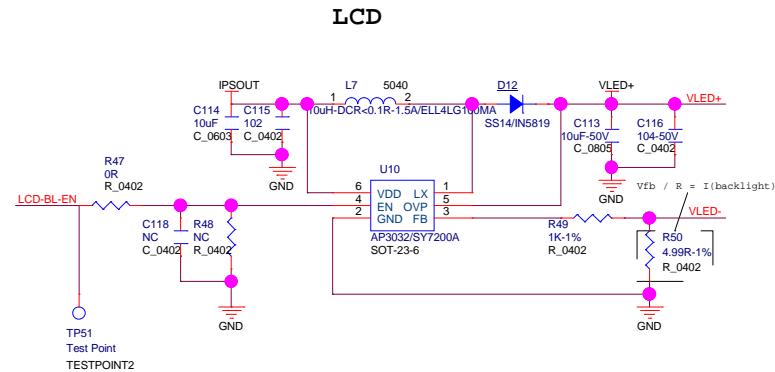
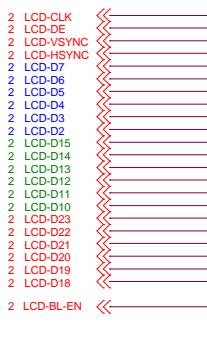
Differential pairs
 $Z_0 = 90 \text{ ohm}$



D⁺ / D⁻ 上的 ESD 器件电容 小于等4 pF(包括了误差)。



DISPLAY

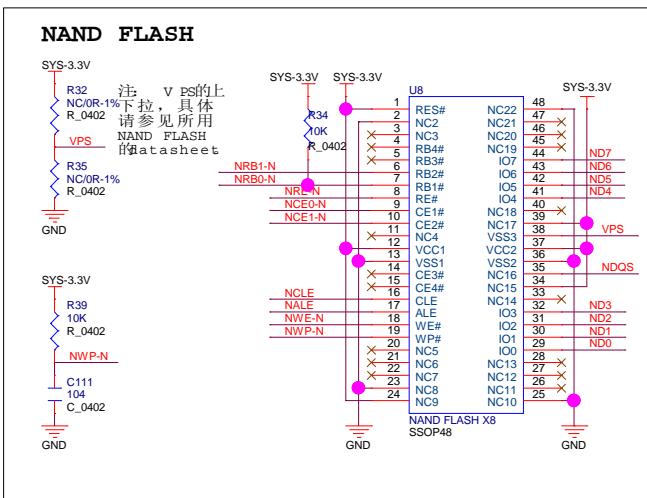


电容屏信号连接示意图

FLASH/CARD

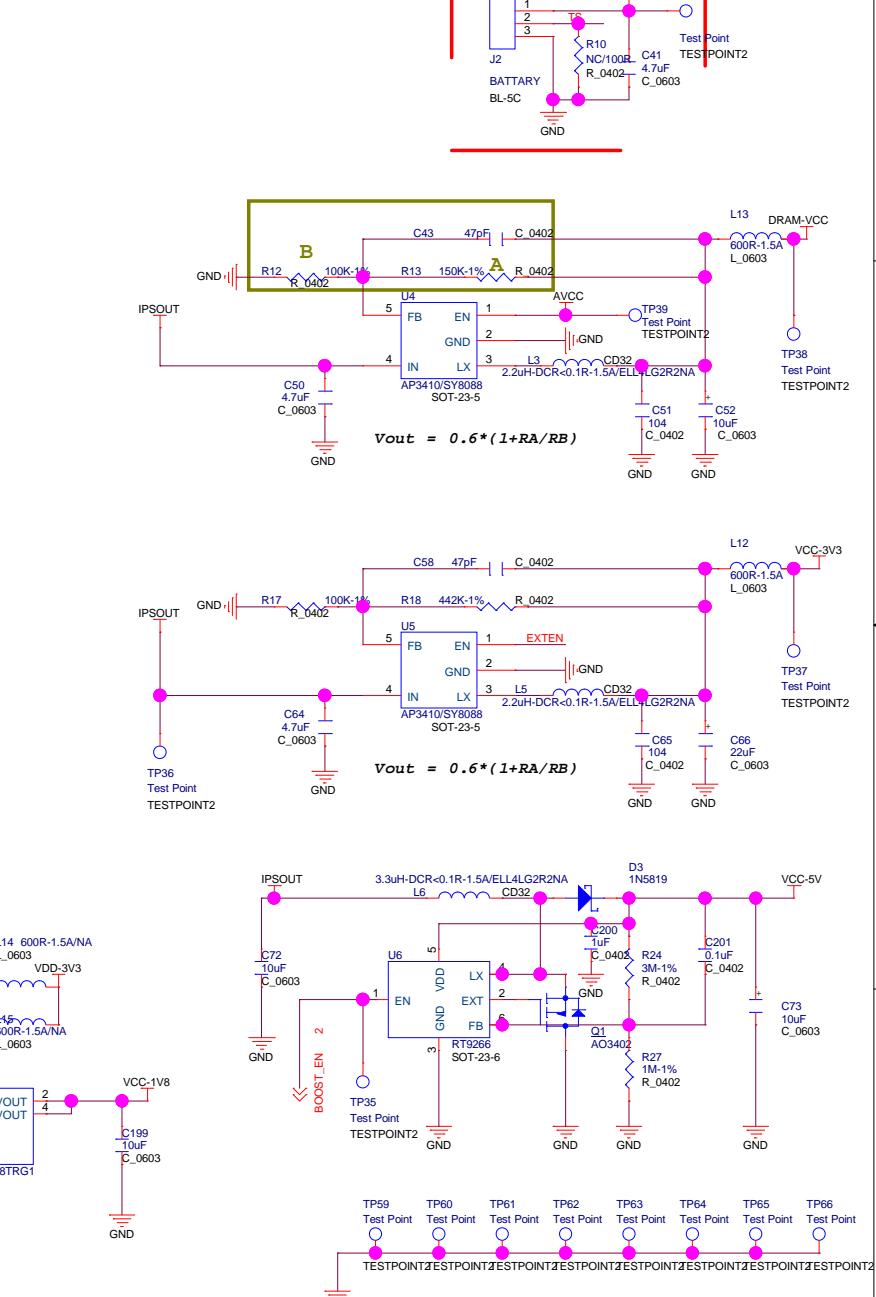
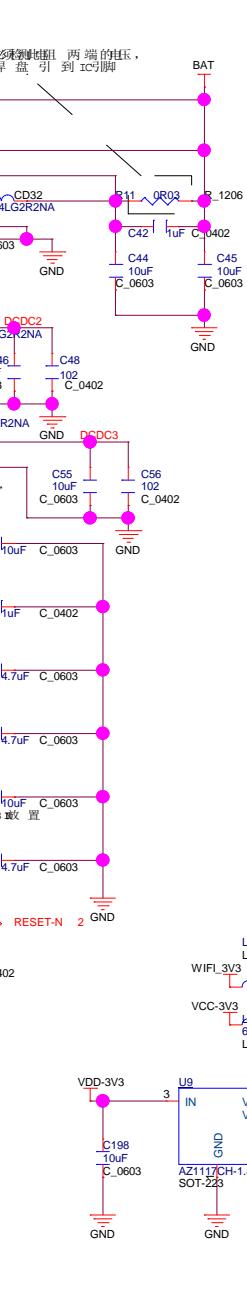
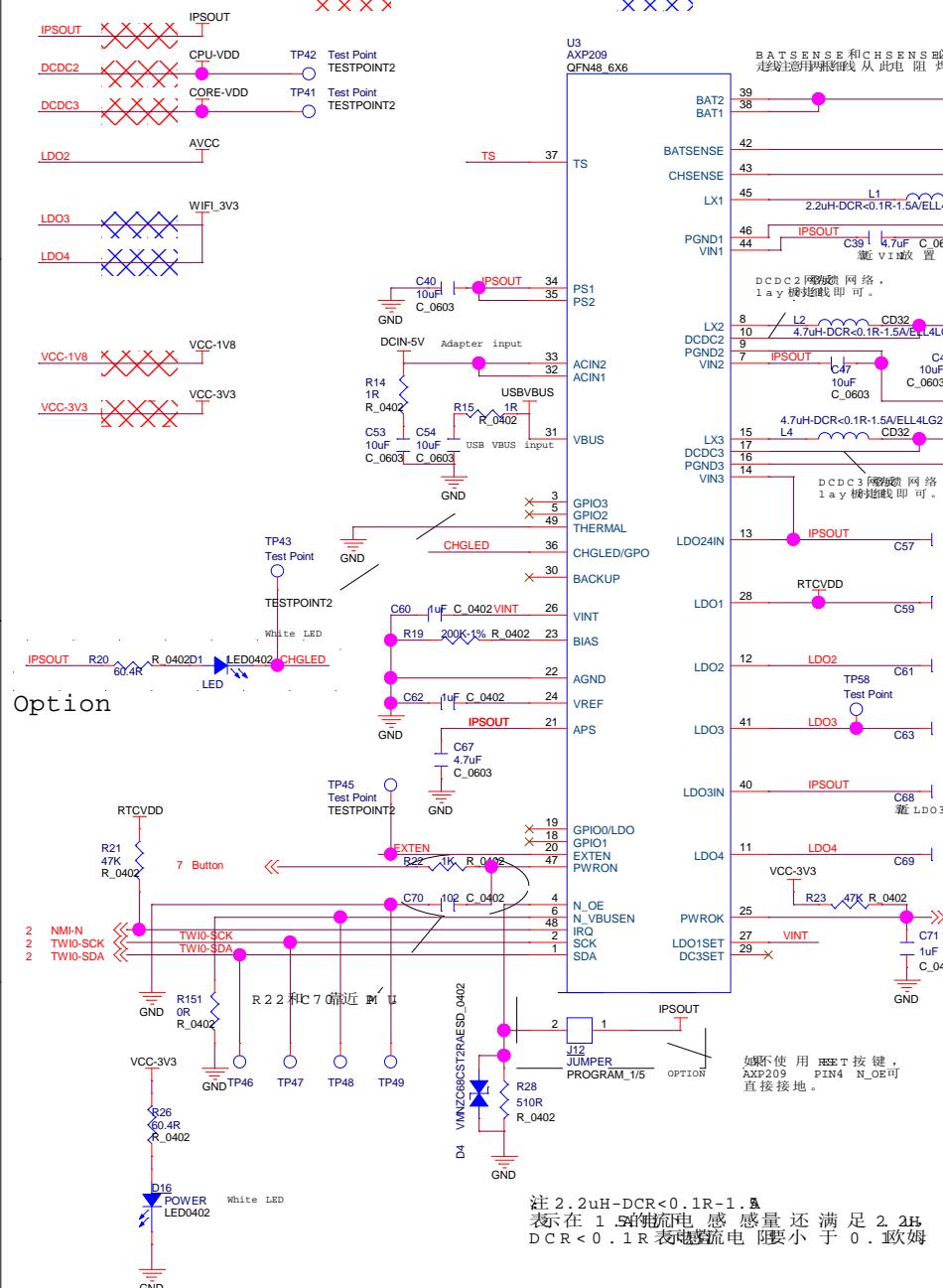
2 2 ND[7:0] NDQS

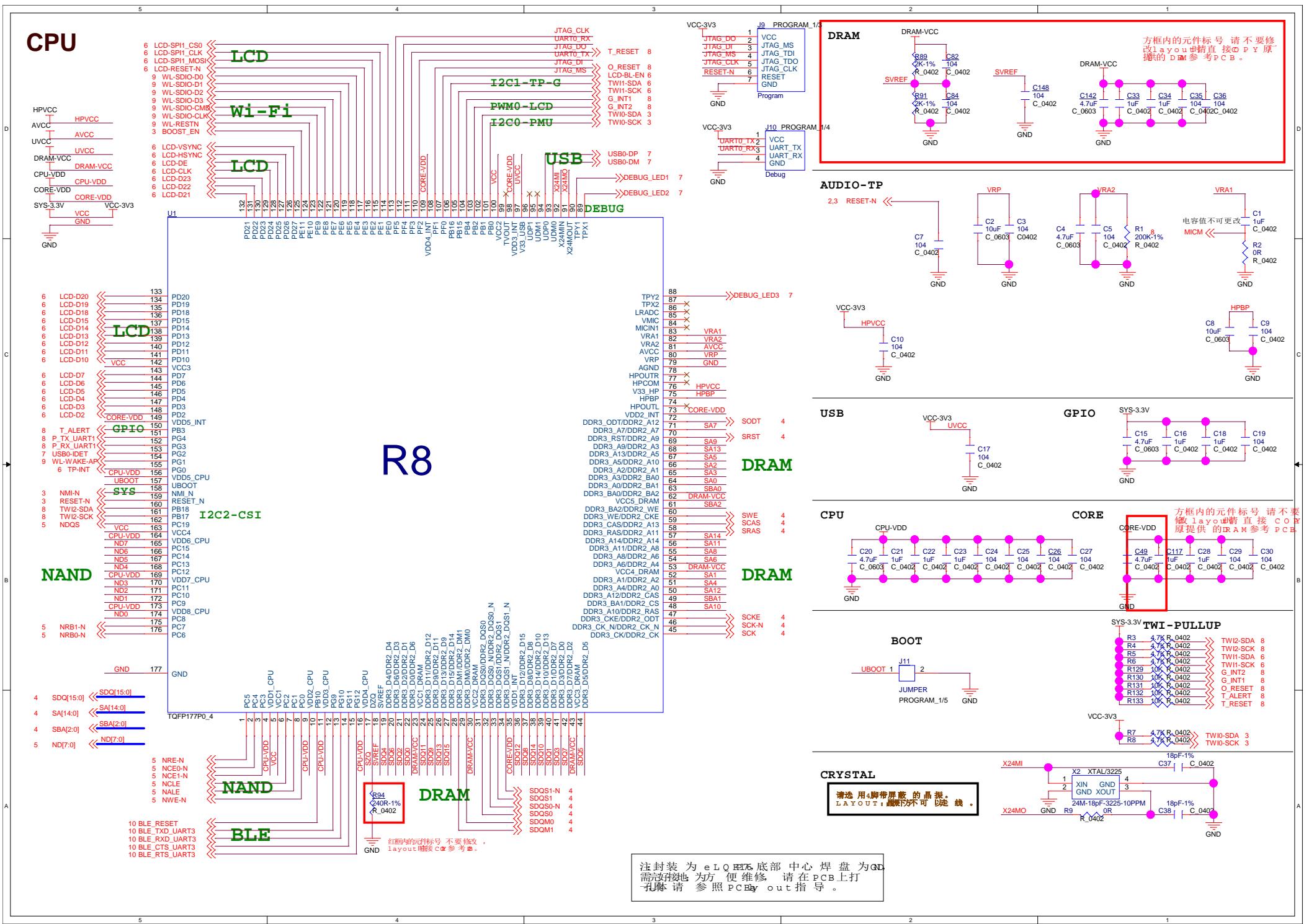
2 2 NRB1-N NRB0-N
2 2 NRE-N NRE-N
2 2 NCE0-N NCE0-N
2 2 NCE1-N NCE1-N
2 2 NCL-E NCL-E
2 2 NALE NALE
2 2 NWE-N NWE-N



POWER

POWER LINE:Width>=80mil POWER LINE:Width>=50mil





COVER

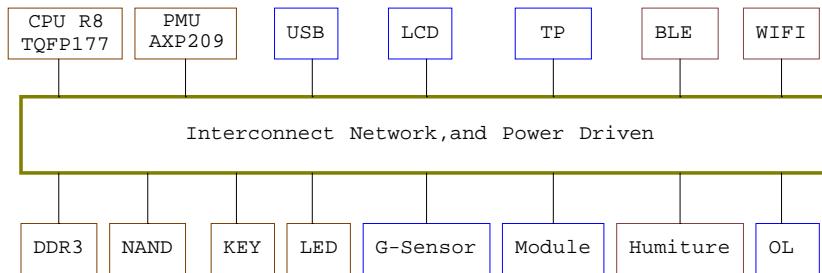
Schematics Index

Bran-Design

- 01 COVER
- 02 CPU
- 03 POWER
- 04 DDR3 16x1
- 05 FLASH
- 06 DISPLAY
- 07 PERIPHERS
- 08 SENSOR
- 09 WI-FI
- Option:
- 10 BLE

特别提醒：
 1: PG0 / PG1 这两个IN脚
 具有 INPIV 功能。
 2: PMU的GPIO0/1/2这三个IN脚
 具有GPIO-OUT功能。
 3: PG10 / PG11 / PG12 这三个IN脚
 的输出可改变。
 4: CSI-PCLK / CSI-MCL这两个IN脚
 具有 INPIV 功能。
 5: CSI-HSYNC具有 INPIV 功能，
 不他用途。

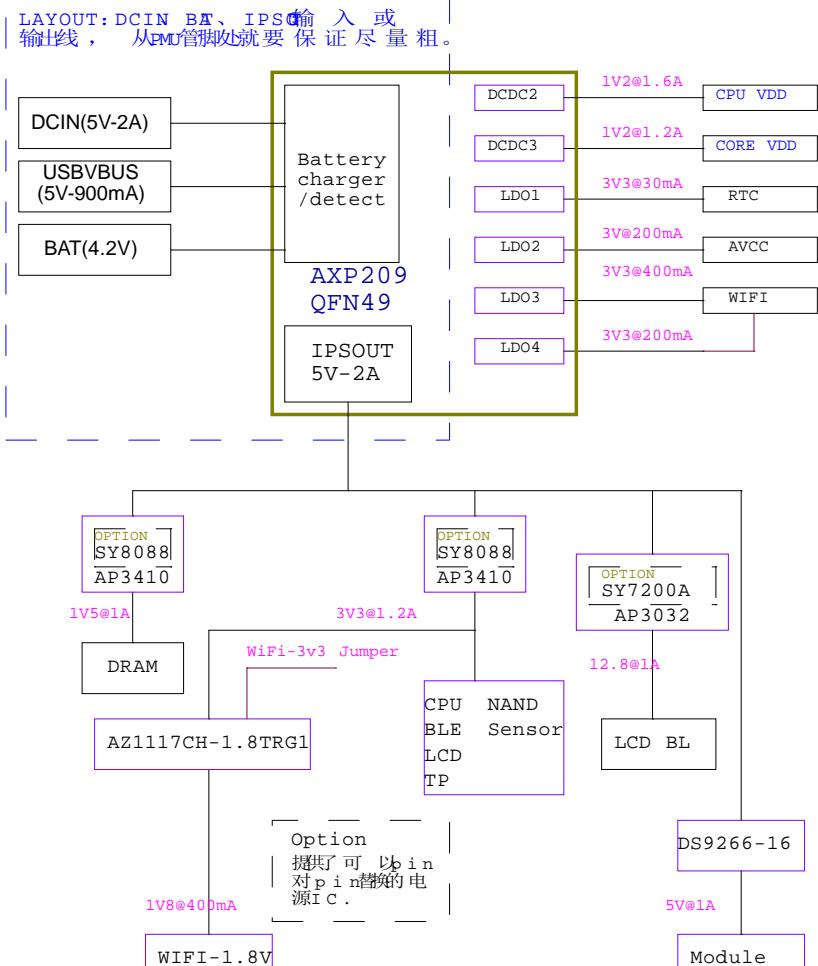
BLOCK



REVISION HISTORY

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Bran Main PCB ASSY	2016/6/19	Violet/Jemmey	Jemmey	

POWER TREE



DDR3 16x1

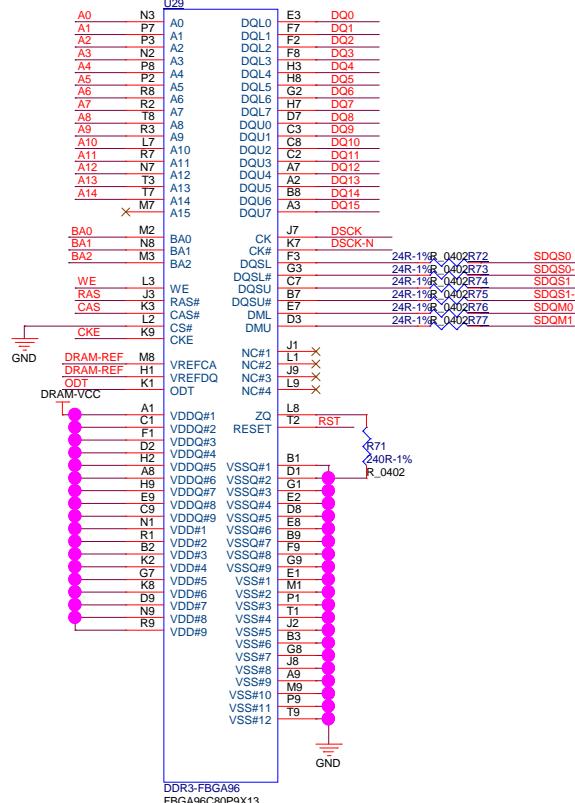
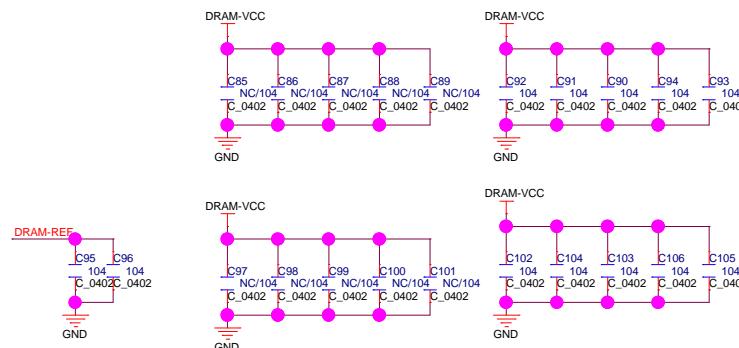
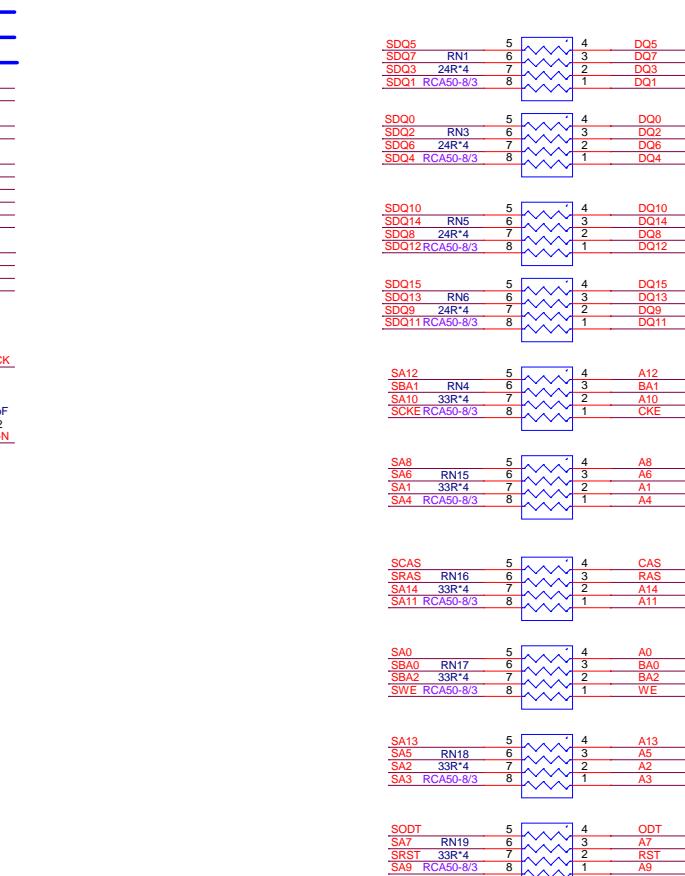
DDR3

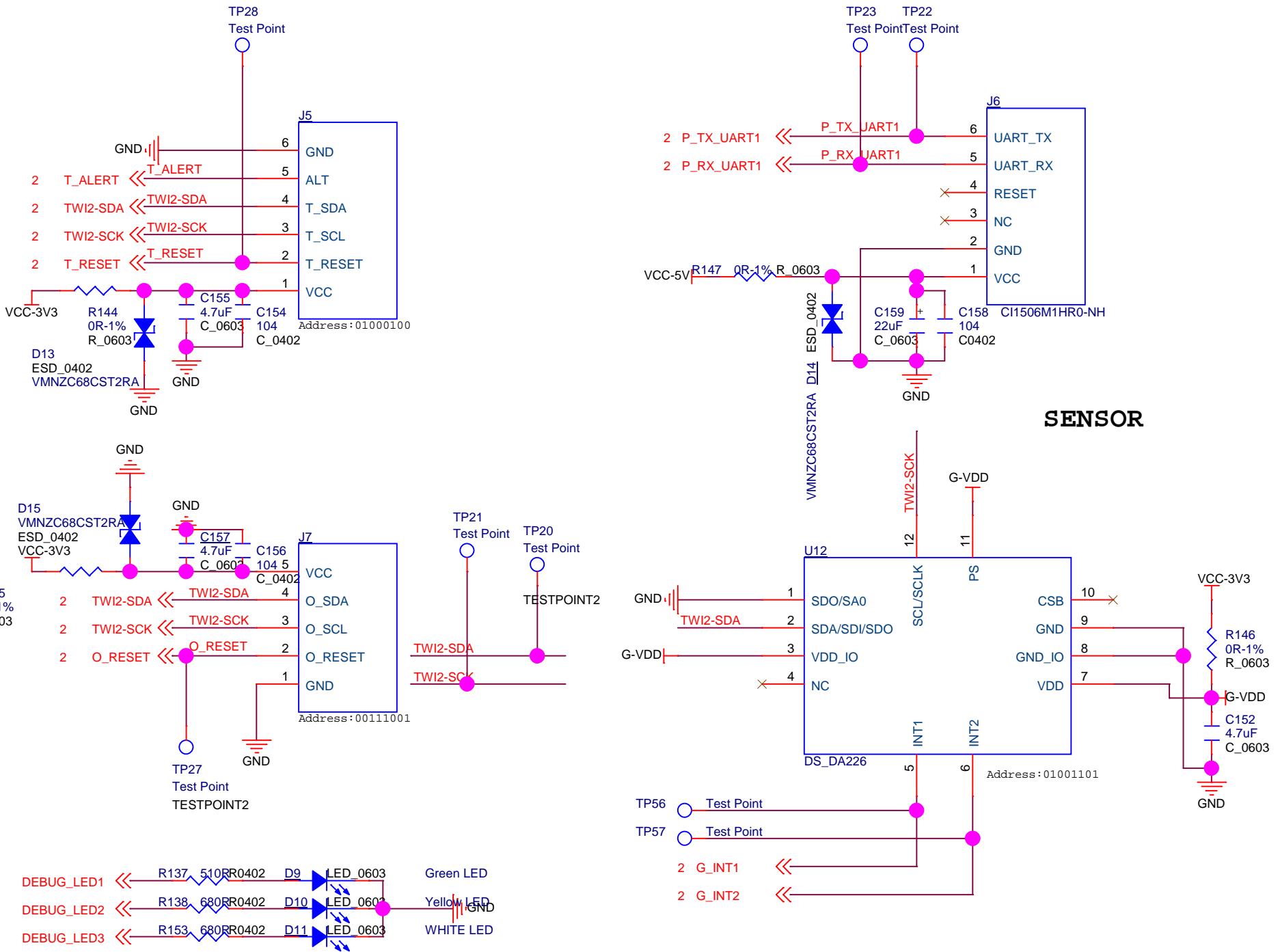
本页的元件标号请不要修改
layout时直接用原厂提供的DRAM参考PCB

2 SDQ[15:0] << SDQ[15:0]
2 SA[14:0] << SA[14:0]
2 SBA[2:0] << SBA[2:0]
2 SRST << SRST
2 SODT << SODT
2 SCK << SCK
2 SCK-N << SCK-N
2 SDQM0 << SDQM0
2 SDQM1 << SDQM1
2 SWE << SWE
2 SRAS << SRAS
2 SCAS << SCAS
2 SCKE << SCKE
2 SDQS0 << SDQS0
2 SDQS0-N << SDQS0-N
2 SDQS1 << SDQS1
2 SDQS1-N << SDQS1-N

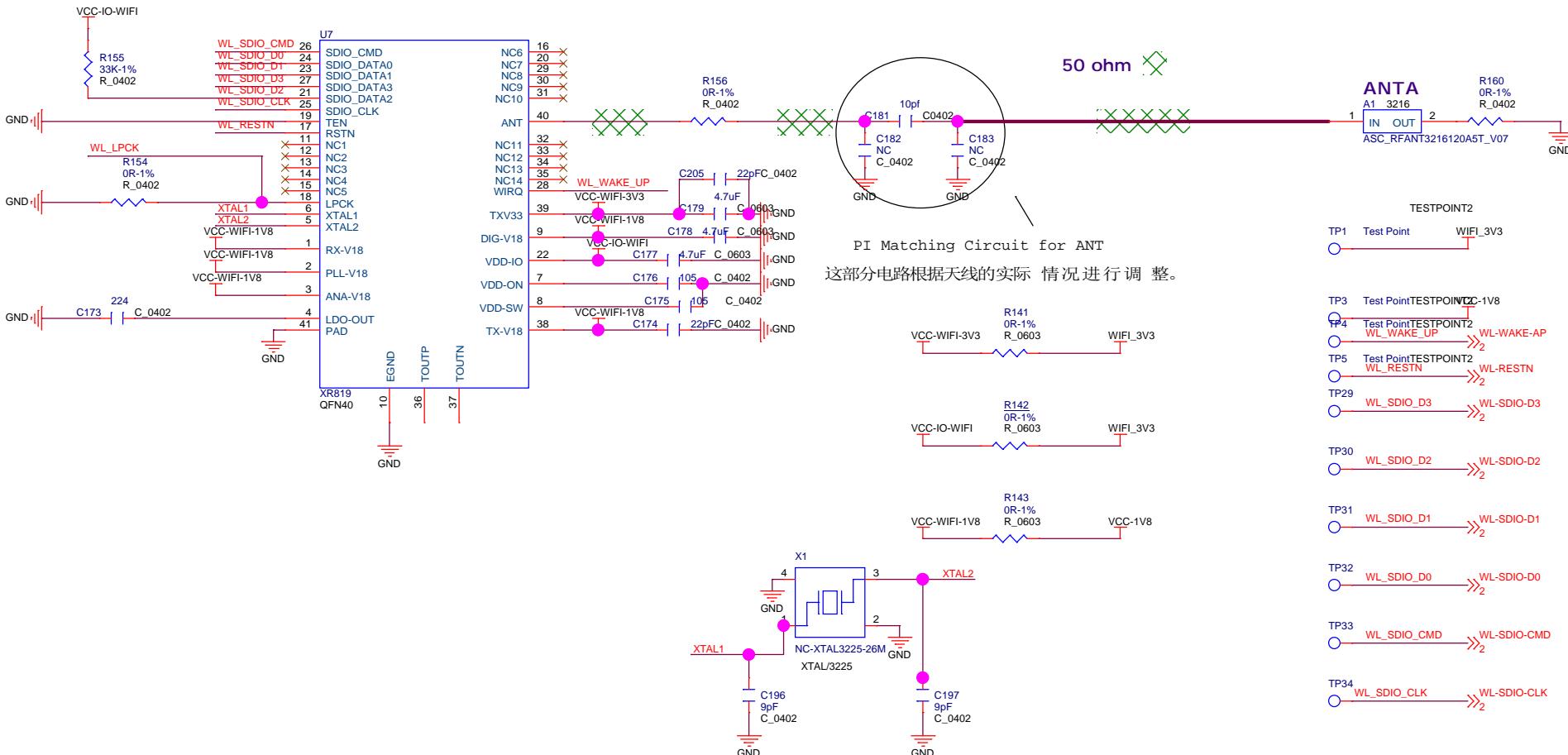
SCK 24R-1% R65 DSCK
R_0402 C109 NC/10pF C_0402
SCK-N 24R-1% R68 DSCK-N
R_0402

DRAM-VCC
R86 2K-1% C81 104
R_0402 C_0402
DRAM-REF
R90 2K-1% C83 104
R_0402 C_0402
GND





Wi-Fi



BLE

