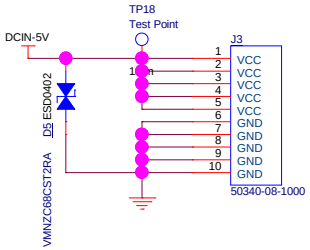
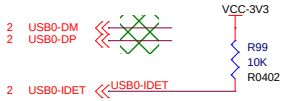
Button

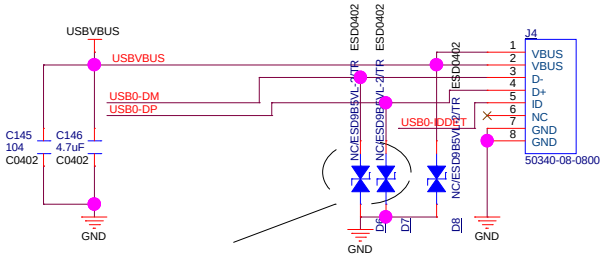
PCB Power Assay





USB-DEVICE

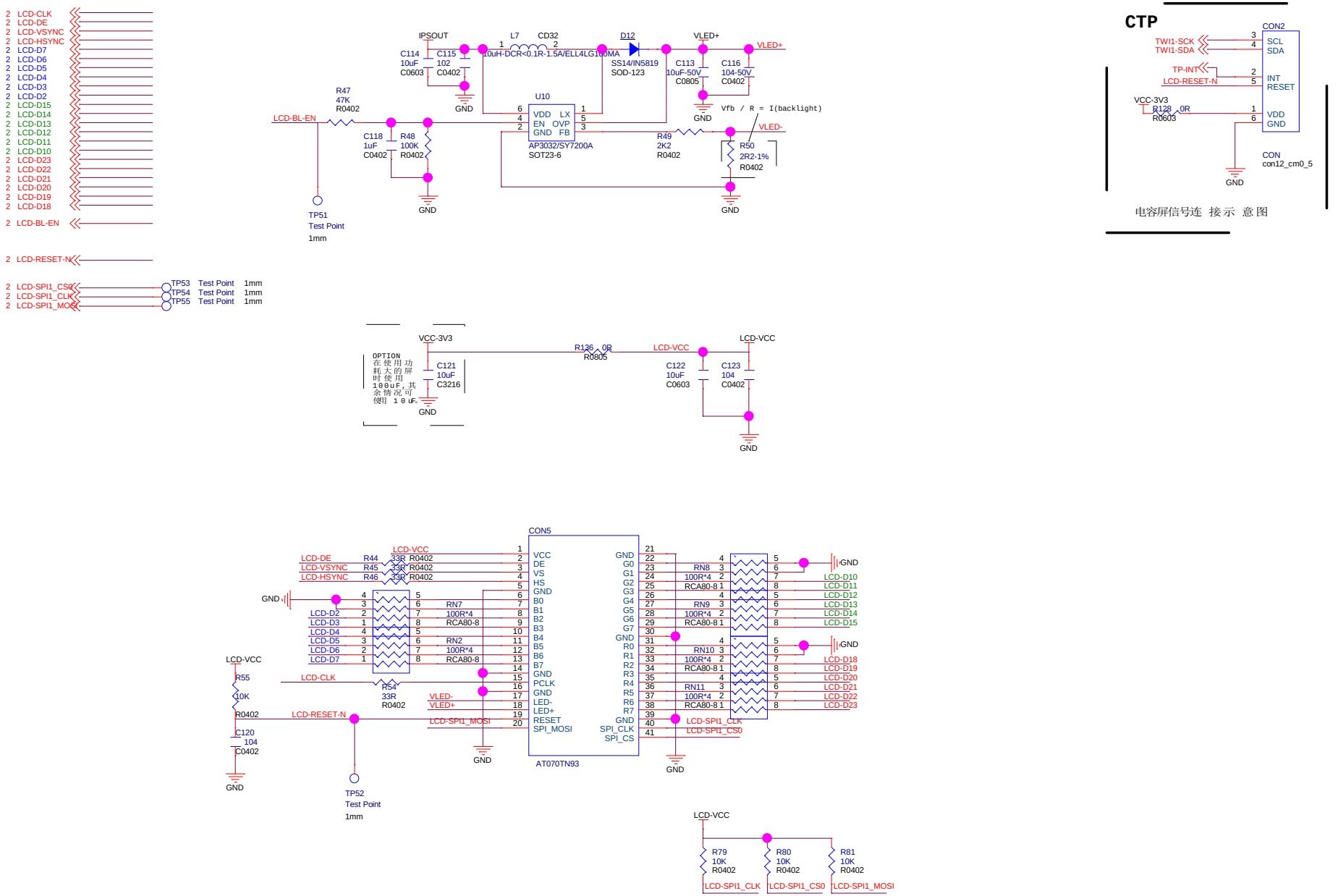
Differential pairs
Z0= 90 ohm



D+/D- 上的 ESD 器件电 容 小 于等于 4 pF(包括了误差)。

DISPLAY

LCD



CTP

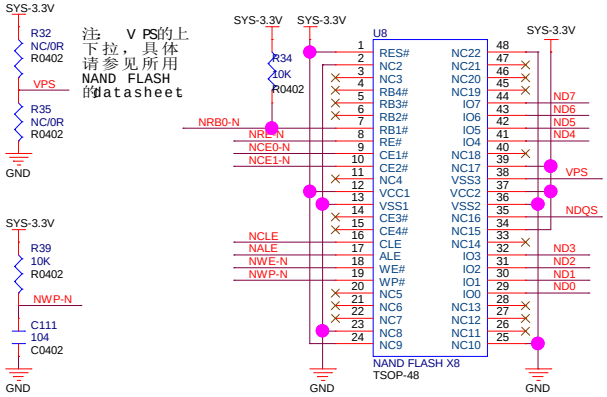
电容屏信号连 接示 意图

FLASH/CARD

2 ND[7:0] — ND[7:0]
2 NDQS — NDQS

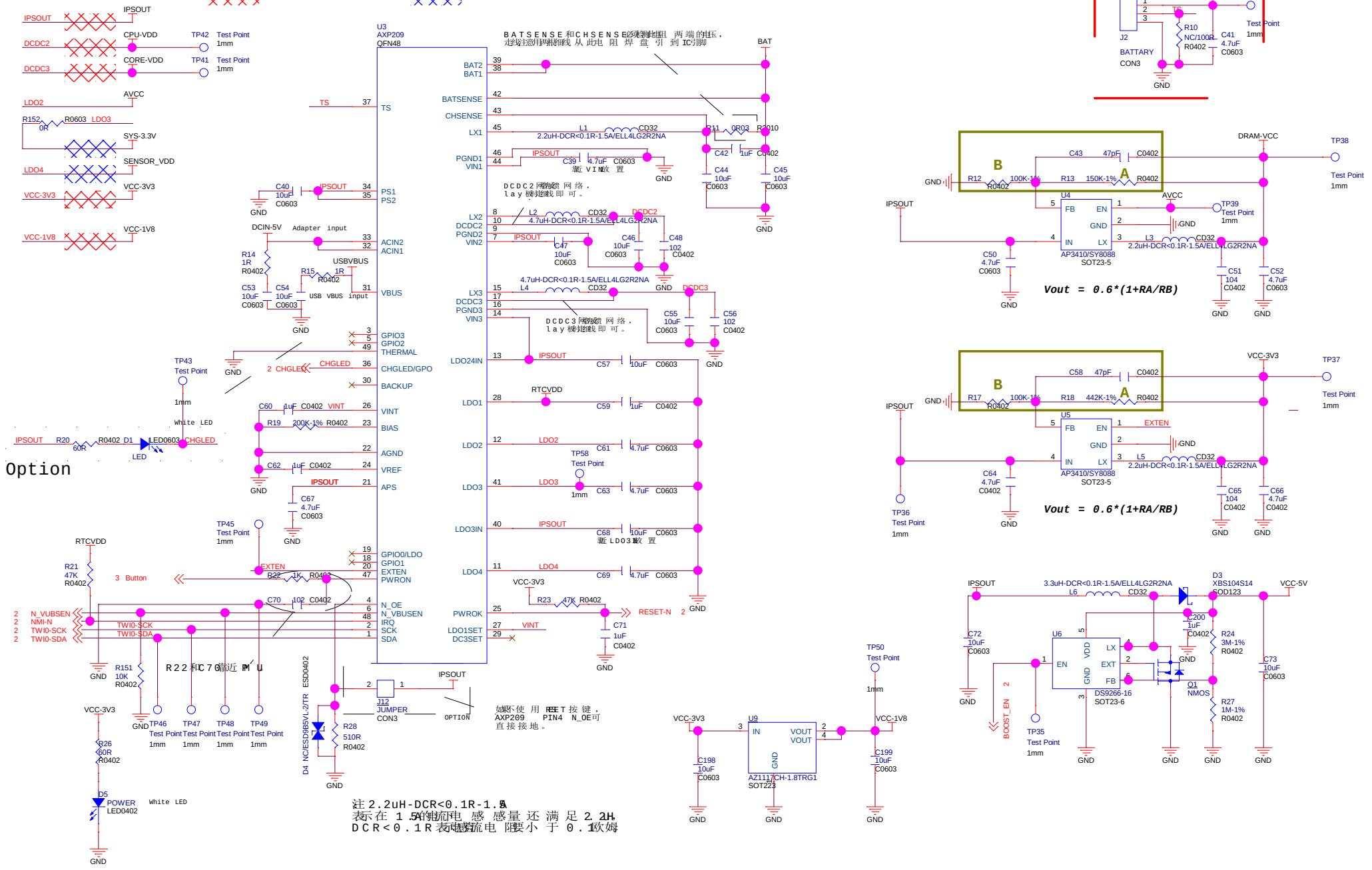
2 NRB0-N — NRB0-N
2 NRE-N — NRE-N
2 NCE0-N — NCE0-N
2 NCE1-N — NCE1-N
2 NCLE — NCLE
2 NALE — NALE
2 NWE-N — NWE-N

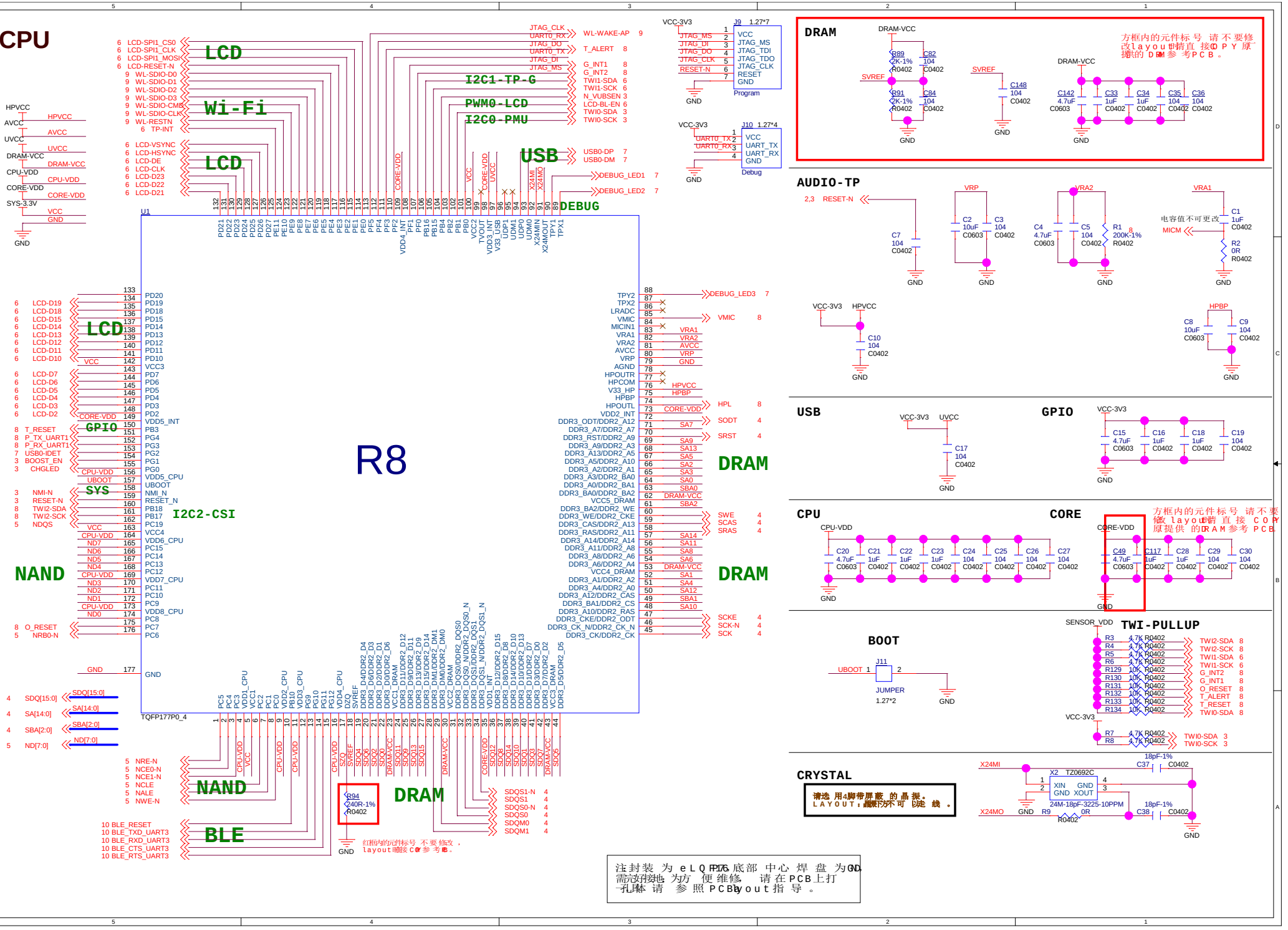
NAND FLASH



POWER

POWER LINE:Width>=80mil POWER LINE:Width>=50mil




CPU
R8
LCD
Wi-Fi
LCD
USB
DEBUG
I2C1-TP-G
PWM0-LCD
I2C0-PMU
LCD
GPIO
SYS
I2C2-CSI
NAND
DRAM
DRAM
NAND
BLE
DRAM
Program
Debug
TQFP177P0_4
DRAM
AUDIO-TP
USB
GPIO
CPU
CORE
BOOT
TWI-PULLUP
CRYSTAL
请选 用4脚带屏蔽 的晶 振。
LAYOUT：晶振下方不 可 以走 线 。
注封装 为 eLQFP176底部 中心 焊 盘 为GND
需完好接地，为方 便维修， 请 在PCB上打
孔具体 请 参 照PCBLayout指 导 。

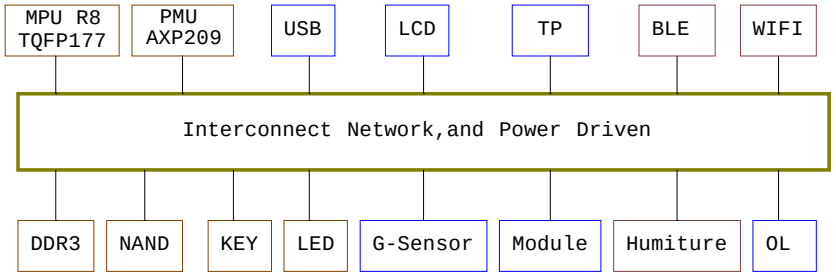
COVER

Schematics Index

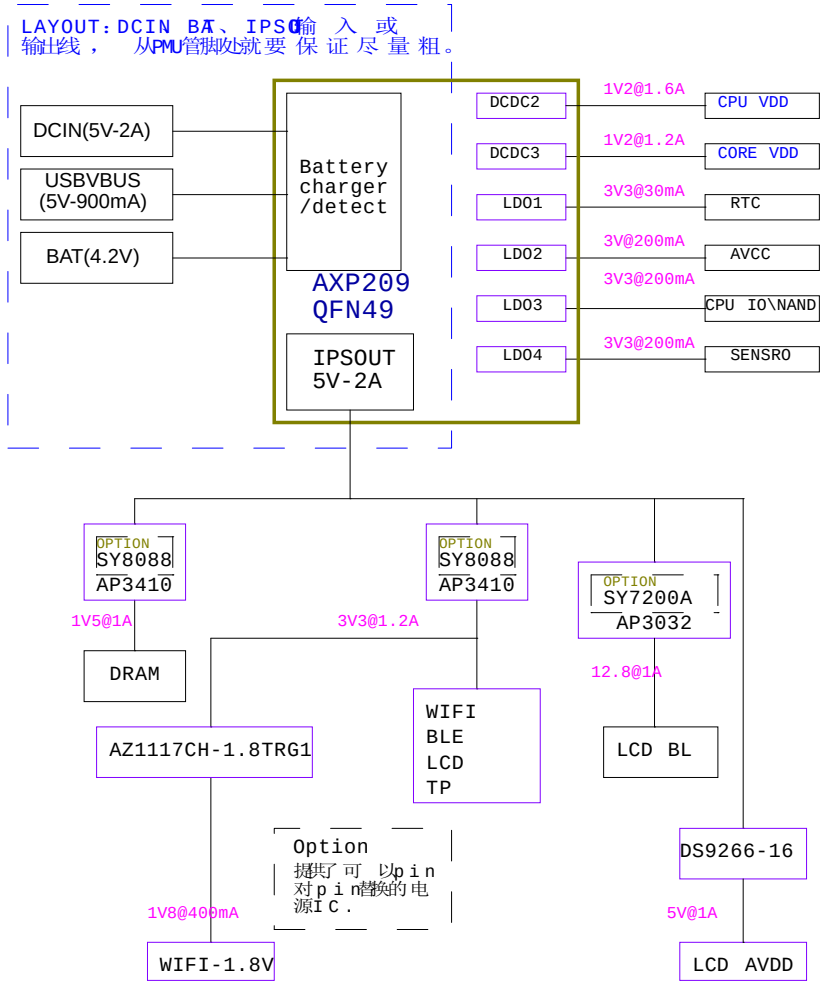
Bran-Design

特别提醒：
1:PG0 / PG1 / PG2这个PIN脚
如果有INPUT功能有 功 能 。
2：PMU的GPIO0/1/2这四个P IN 脚
做GPIO-OUTPUT功能
3:PG10 / PG11 / PG12这个PIN脚
的功能可改变。
4:CSI-PCLK / CSI-MCLK这个P I N 脚
如果有INPUT功能有 功 能 。
5：CSI-HSYNC如果有INPUT专有 功 能 ，
不能他用途 。

BLOCK



POWER TREE



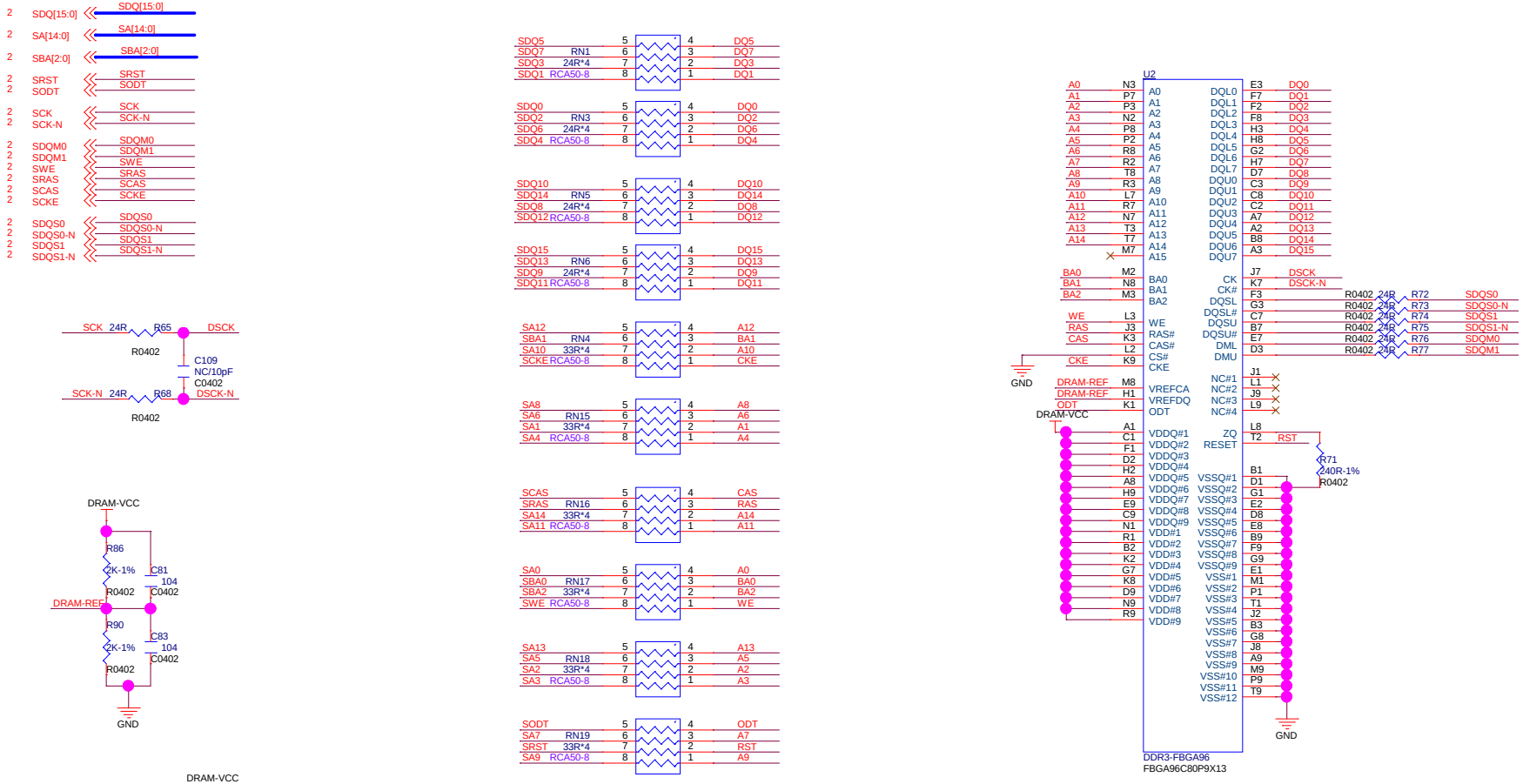
REVISION HISTORY

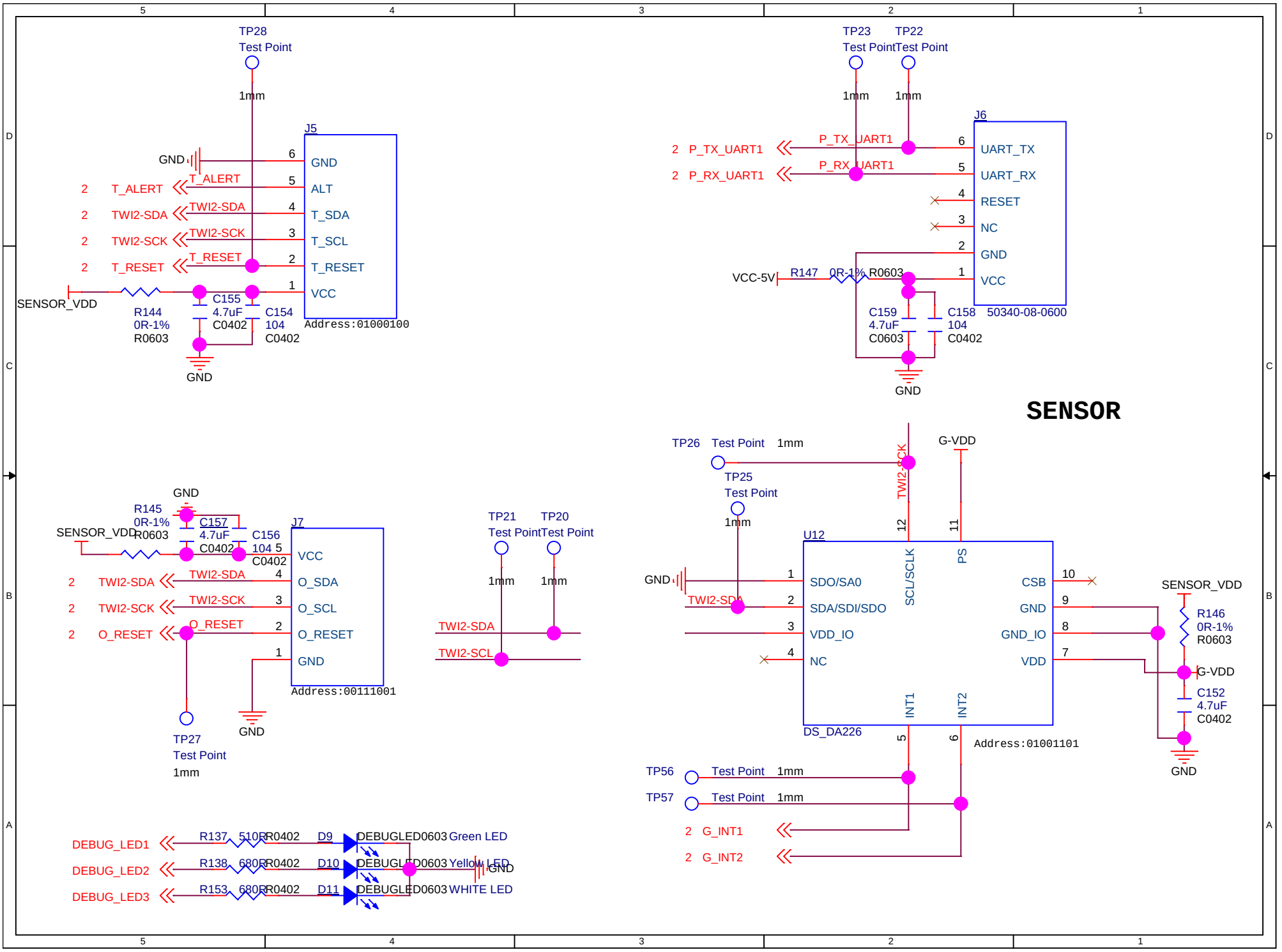
Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Bran Main PCB ASSY	2016/6/2	Violet/Jemmey	Jemmey	

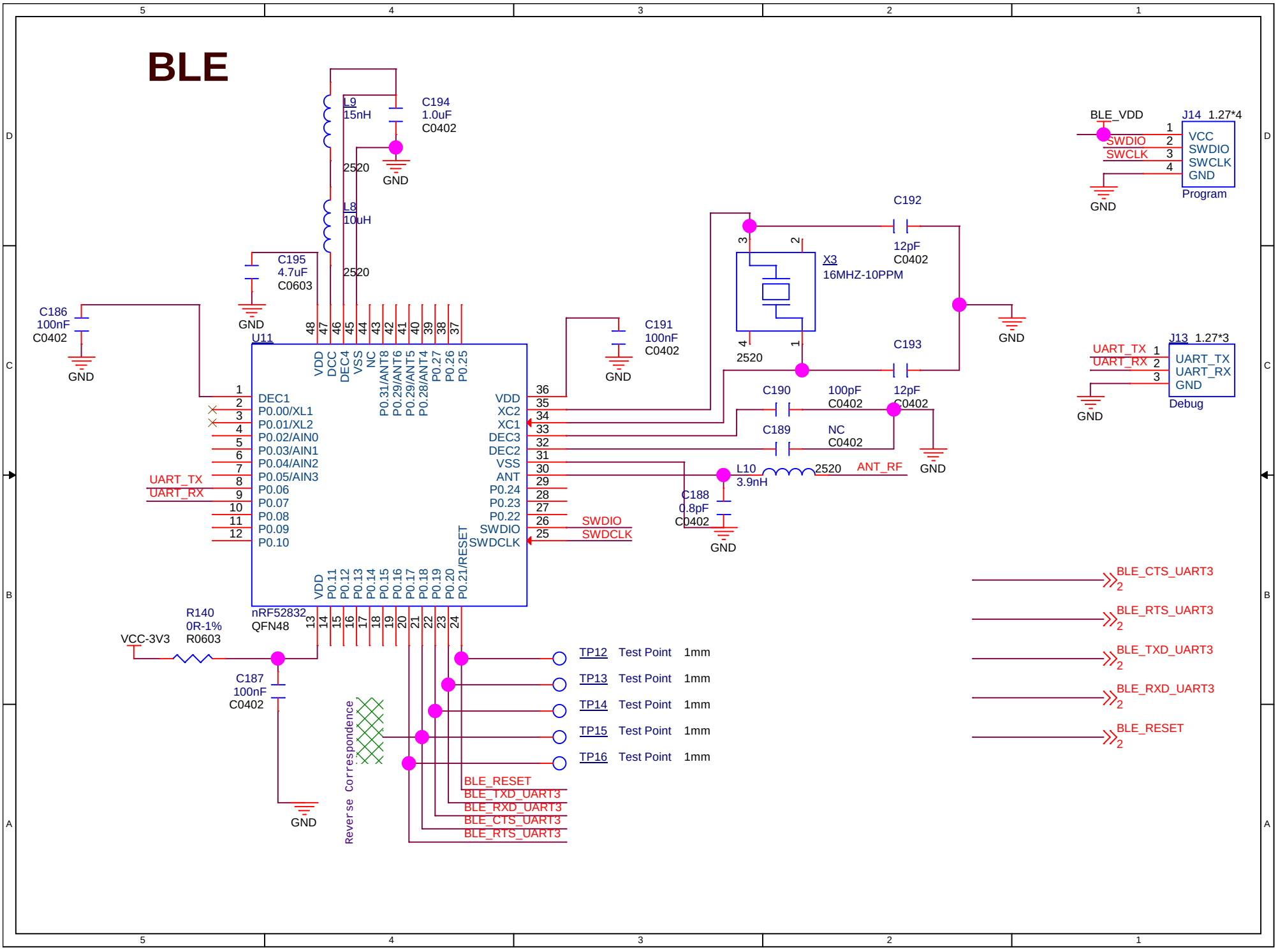
DDR3 16x1

DDR3

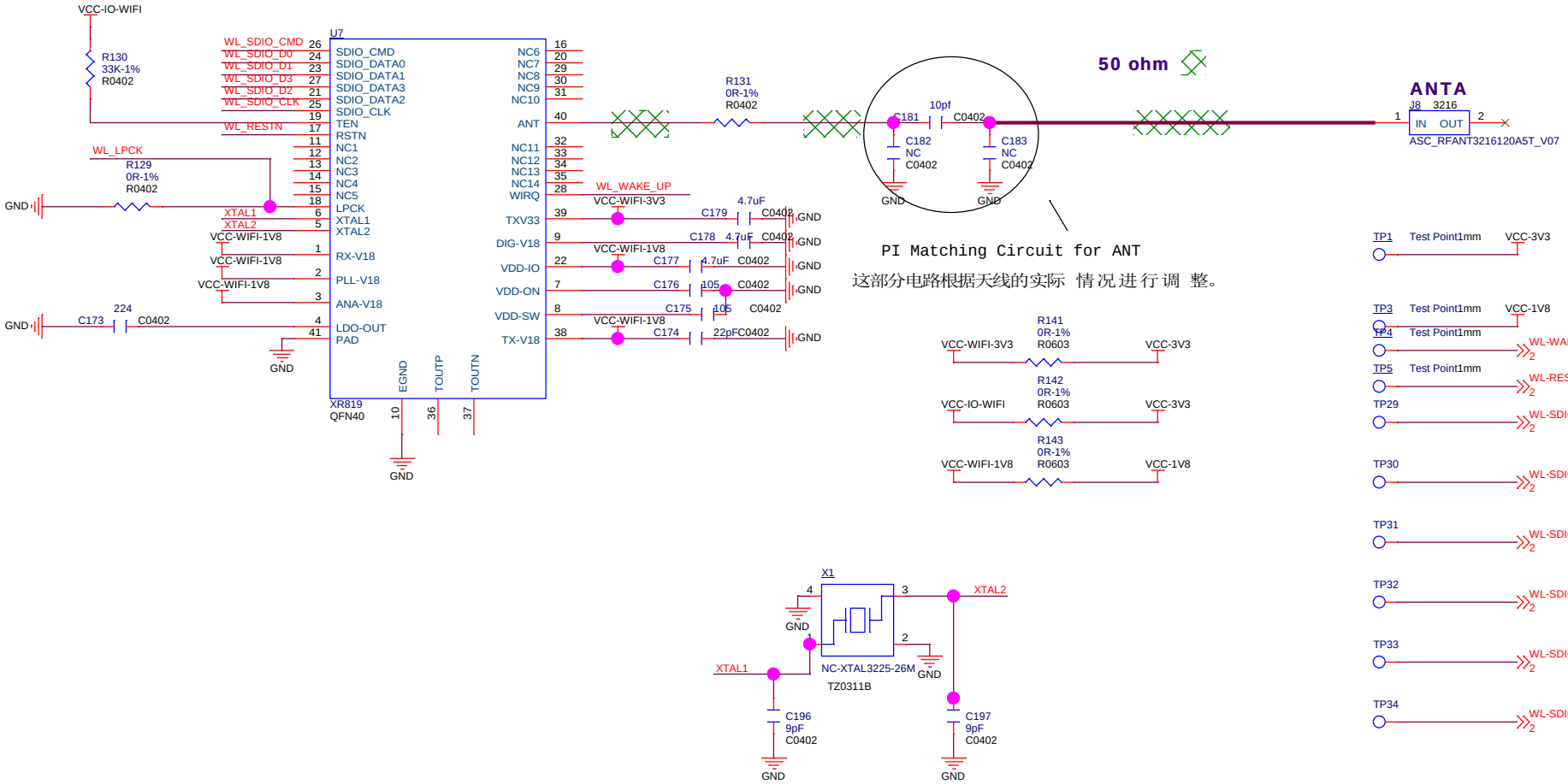
本页的元件标号 请 不 要 修改
layout时直 接 copy 原 厂提 供
的DRAM参考 P C B




SENSOR
TP28
Test Point
1mm
J5
GND
T_ALERT
TWI2-SDA
TWI2-SCK
T_RESET
SENSOR_VDD
R144
0R-1%
R0603
C155
4.7uF
C0402
C154
104
C0402
VCC
T_RESET
T_SCL
T_SDA
ALT
GND
Address:01000100
TP23
TP22
Test Point
Test Point
J6
P_TX_UART1
P_RX_UART1
UART_TX
UART_RX
RESET
NC
GND
VCC
VCC-5V
R147
0R-1%
R0603
C159
4.7uF
C0603
C158
104
C0402
50340-08-0600
TP26
Test Point
TP25
Test Point
TWI2-SCK
G-VDD
U12
SDO/SA0
SDA/SDI/SDO
VDD_IO
NC
SCL/SCLK
PS
CSB
GND
GND_IO
VDD
INT1
INT2
DS_DA226
Address:01001101
SENSOR_VDD
R146
0R-1%
R0603
G-VDD
C152
4.7uF
C0402
TP56
TP57
Test Point
G_INT1
G_INT2
R145
0R-1%
R0603
C157
4.7uF
C0402
C156
104
C0402
J7
VCC
O_SDA
O_SCL
O_RESET
GND
Address:00111001
TP27
Test Point
TP21
TP20
Test Point
Test Point
TWI2-SDA
TWI2-SCL
DEBUG_LED1
DEBUG_LED2
DEBUG_LED3
R137 510R R0402
R138 680R R0402
R153 680R R0402
D9
D10
D11
DEBUGLED0603 Green LED
DEBUGLED0603 Yellow LED
DEBUGLED0603 WHITE LED


BLE
L9
15nH
C194
1.0uF
C0402
2520
GND
L8
10uH
2520
C195
4.7uF
C0603
GND
C186
100nF
C0402
GND
U11
VDD
DCC
DEC4
VSS
NC
P0.31/ANT8
P0.29/ANT6
P0.29/ANT5
P0.28/ANT4
P0.27
P0.26
P0.25
DEC1
P0.00/XL1
P0.01/XL2
P0.02/AIN0
P0.03/AIN1
P0.04/AIN2
P0.05/AIN3
P0.06
P0.07
P0.08
P0.09
P0.10
UART_TX
UART_RX
VDD
XC2
XC1
DEC3
DEC2
VSS
ANT
P0.24
P0.23
P0.22
SWDIO
SWDCLK
P0.21/RESET
VDD
P0.11
P0.12
P0.13
P0.14
P0.15
P0.16
P0.17
P0.18
P0.19
P0.20
nRF52832
QFN48
C191
100nF
C0402
GND
C192
12pF
C0402
X3
16MHZ-10PPM
2520
C193
GND
C190
100pF
C0402
C189
NC
C0402
12pF
C0402
GND
L10
3.9nH
2520
ANT_RF
C188
0.8pF
C0402
GND
SWDIO
SWDCLK
BLE_VDD
J14 1.27*4
SWDIO
SWCLK
VCC
SWDIO
SWCLK
GND
Program
GND
UART_TX
UART_RX
J13 1.27*3
UART_TX
UART_RX
GND
Debug
GND
R140
0R-1%
R0603
VCC-3V3
C187
100nF
C0402
GND
Reverse Correspondence
TP12 Test Point 1mm
TP13 Test Point 1mm
TP14 Test Point 1mm
TP15 Test Point 1mm
TP16 Test Point 1mm
BLE_RESET
BLE_TXD_UART3
BLE_RXD_UART3
BLE_CTS_UART3
BLE_RTS_UART3
BLE_CTS_UART3
BLE_RTS_UART3
BLE_TXD_UART3
BLE_RXD_UART3
BLE_RESET

Wi-Fi



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Size B	Document Number <Doc>	Rev <RevCode>
Date: Friday, June 03, 2016	Sheet 1 of 1	