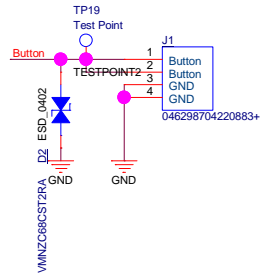
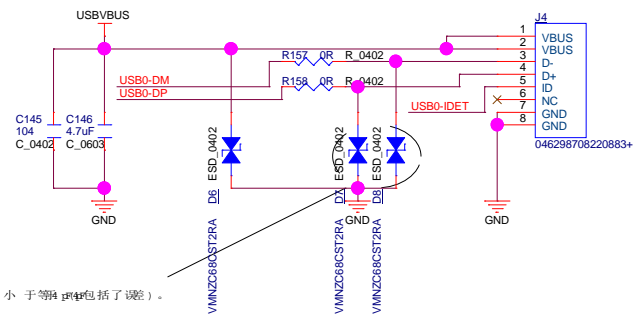


3 Button <<————



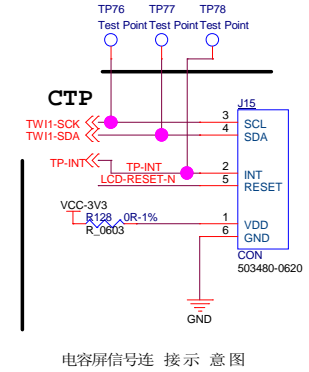
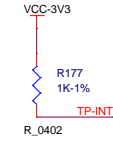
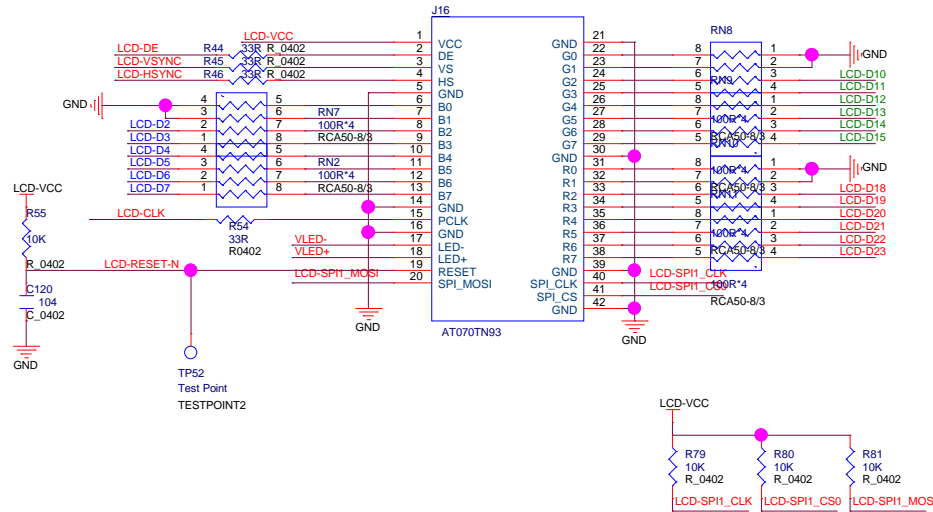
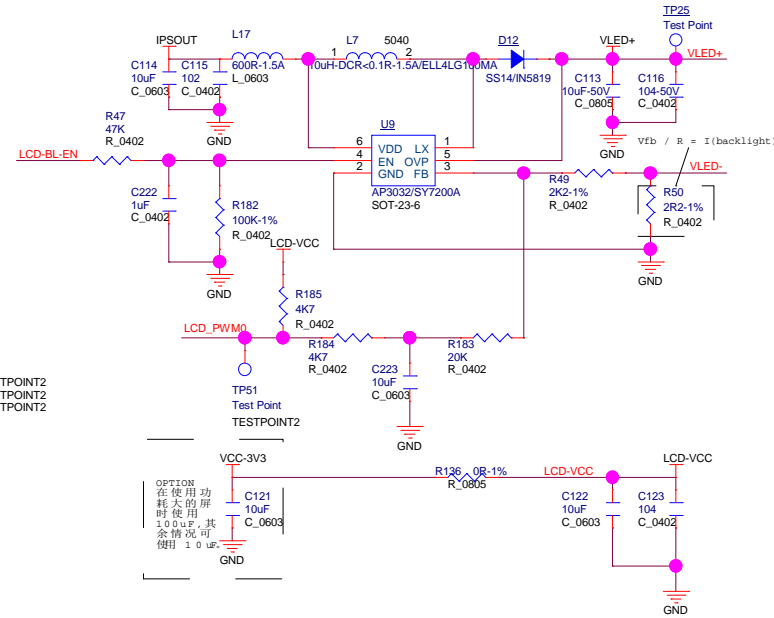
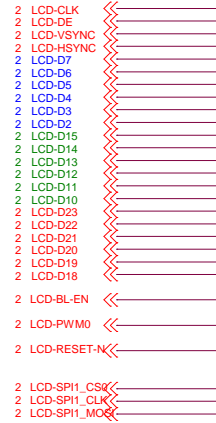
Differential pairs
Z0= 90 ohm



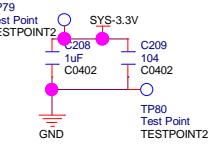
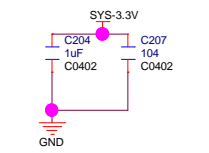
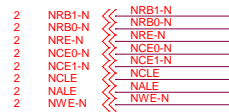
D^+ / D^- 上的ES器件电容小于等于4 pF(包括了误差)。

DISPLAY

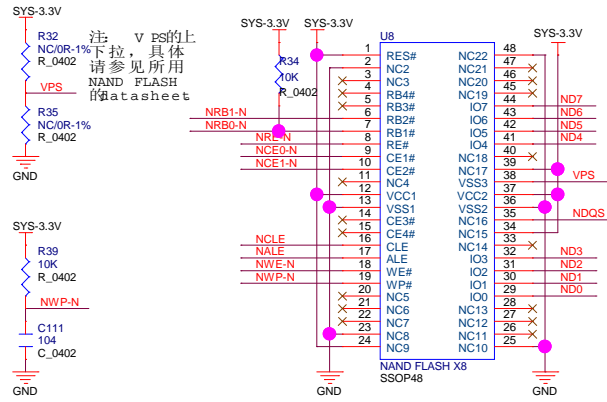
LCD



FLASH/CARD

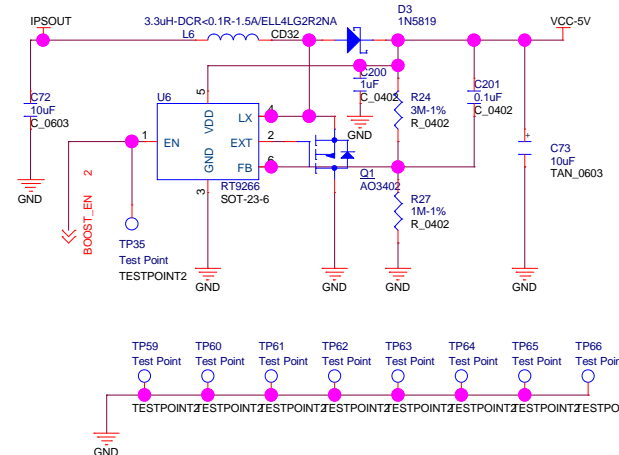
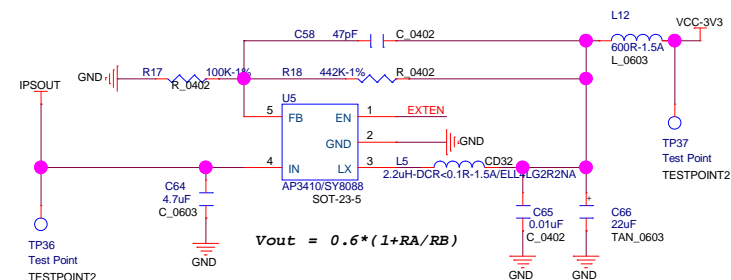
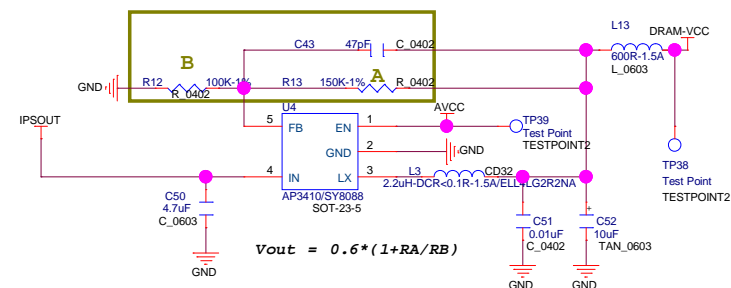
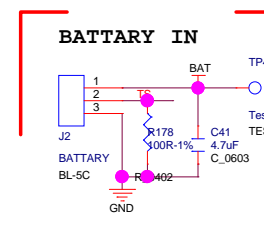
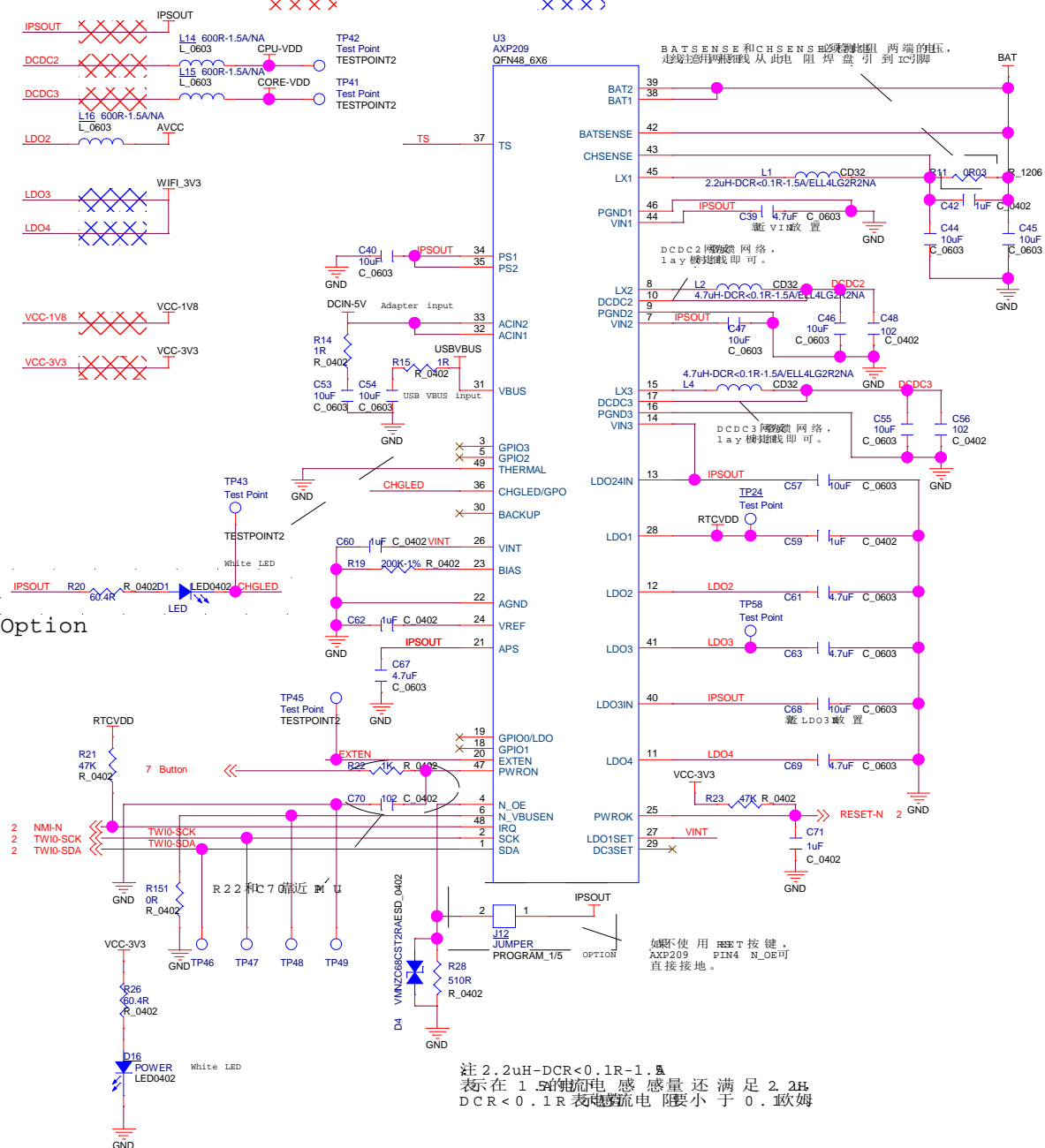


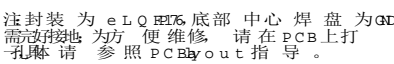
NAND FLASH



POWER

POWER LINE:Width>=80mil POWER LINE:Width>=50mil





COVER

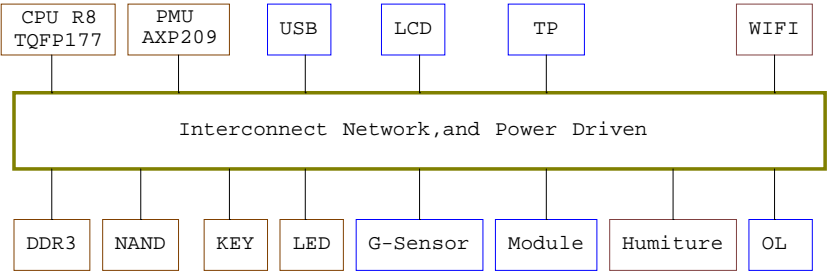
Schematics Index

Bran-Design

- 01 COVER
- 02 CPU
- 03 POWER
- 04 DDR3 16x1
- 05 FLASH
- 06 DISPLAY
- 07 PERIPHERS
- 08 SENSOR
- 09 WI-FI
- Option:
- 10 BLE

特别提醒：
1:PG0 / PG1 / PG这个IN脚
具有INPUT功能。
2:PM的GPIO0/1/2这四个IN脚
做GPIO-OUTPUT功能
3:PG10 / PG11 / PG1这个IN脚
的能可改变。
4:CSI-PCLK / CSI-MCLK这个IN脚
具有INPUT功能。
5:CSI-HSYNC具有INPUT功能，
不能用途。

BLOCK

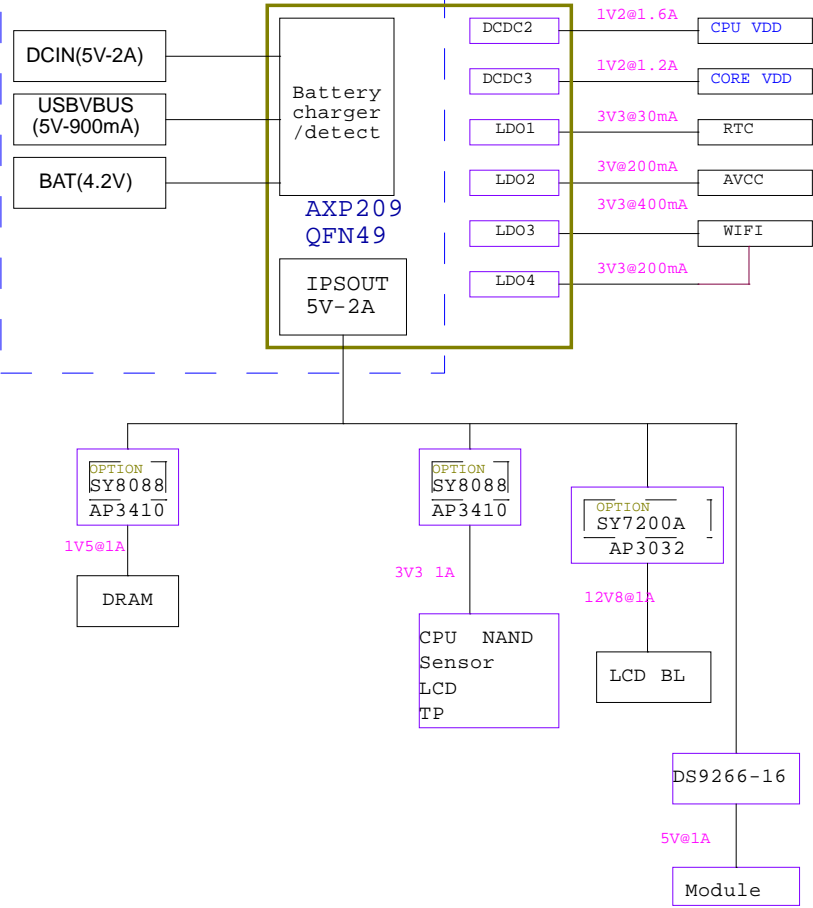


REVISION HISTORY

Revision	Description	Date	Drawn	Checked	Approved
Ver 1.0	Bran Main PCB ASSY	2016/6/19	Violet/Jemmey	Jemmey	
Ver 1.5	Bran Main PCB ASSY	2016/7/31	Jemmey	Jemmey/Violet	
Ver 2.0	Bran Main PCB ASSY	2016/8/11	Jemmey	Jemmey/Violet	

POWER TREE

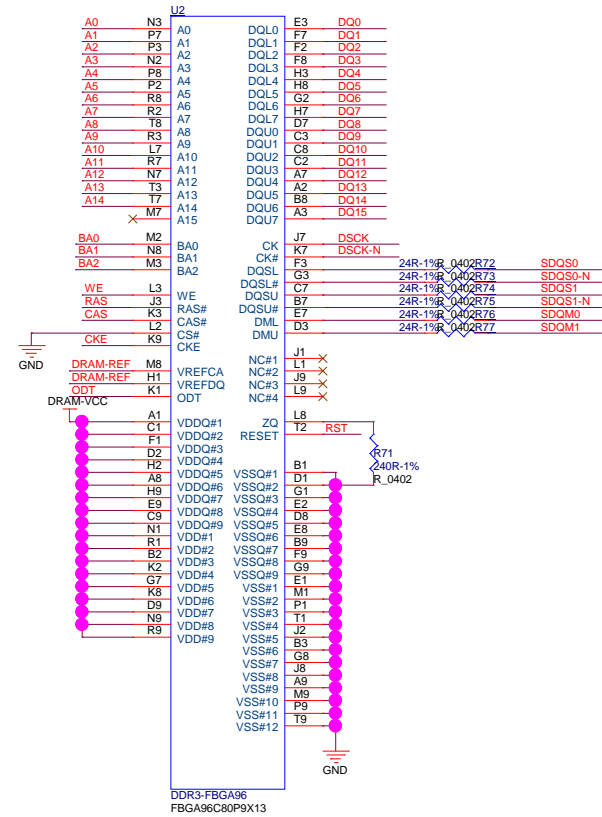
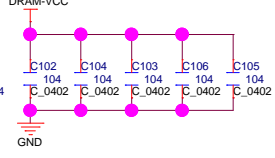
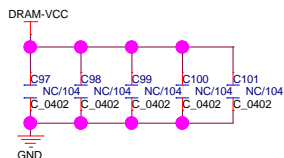
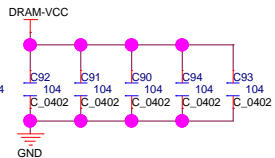
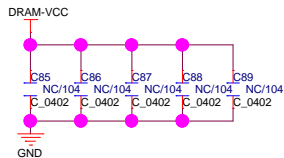
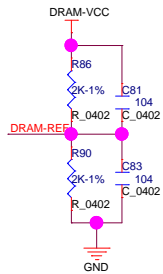
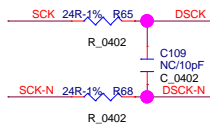
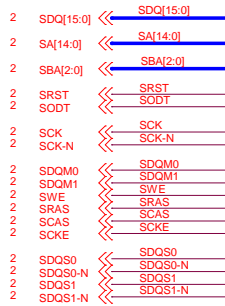
LAYOUT: DCIN BA、IPSC输入或
输出线，从PMU管脚处就要保证尽量粗。

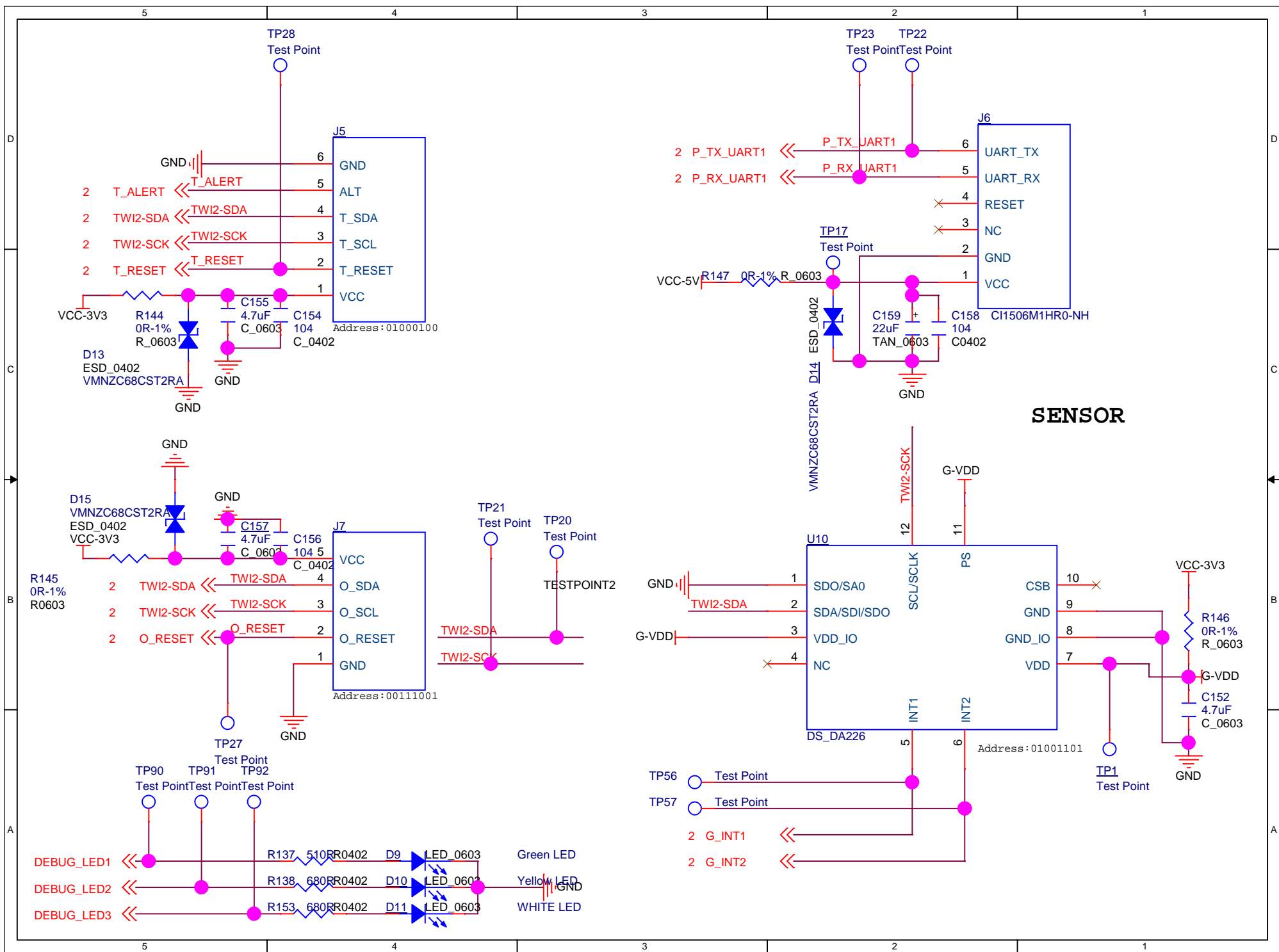


DDR3 16x1

DDR3

本页的元件标号 请 不要 修改
layout 时 直接 在 原理 图 中 提供
的 参考 PCB





Wi-Fi

