UNIVERSIDAD NACIONAL DE CORDOBA
FACULTAD DE CIENCIAS EXACTAS FISICAS Y NATURALES
ELECRONICA DIGITAL I

Grupo Nº 09

Trabajo Práctico Nº 3

CIRCUITOS SECUENCIALES SINCRONOS

Profesor

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Fecha

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OBJETIVOS

Diseñar e implementar una alarma con 4 bits de entrada. Al encenderse la alarma debe iniciarse en estado de “desactivada” y permanecer en el mismo hasta que se ingrese la “secuencia de activación”, la que llevará al estado “activada” (encender un LED amarillo). La alarma puede “desactivarse” con una “secuencia de desactivación”.

Si por alguna razón no se digita el número correcto de la “secuencia de desactivación” y después de digitar la cuarta cifra, se encenderá un LED rojo indicando que esta esta disparada. Este permanecerá encendido hasta que se ingrese la “secuencia de desactivación” correctamente.

DESARROLLO

Todo el sistema contara de 6 bloques, los cuales son:

INGRESO DE DATOS

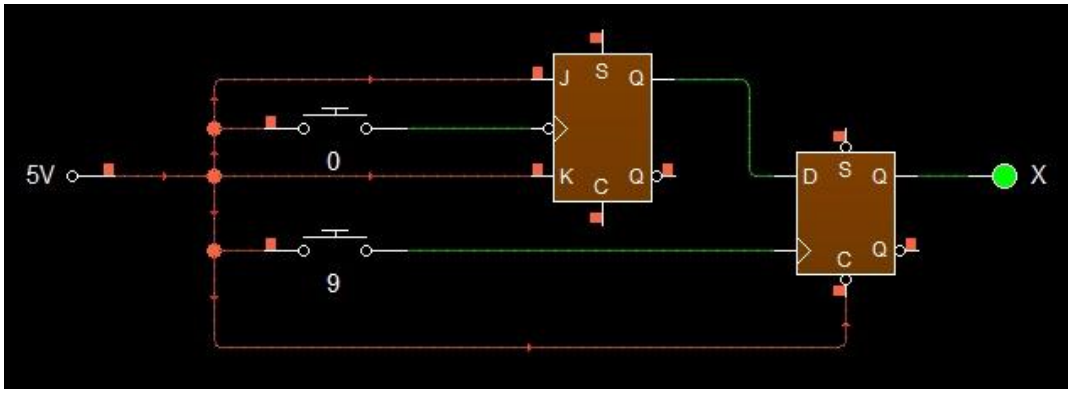
Al ser el grupo Nº 9, nos interesan las combinaciones de activación 0909 y de desactivación 9090.

Dada la consigna del problema y aprovechando la simetría de las secuencias de activación y desactivación, nos surge la duda:

¿Es posible controlar si una secuencia de dos bits 09 o 90 se ingresó correctamente?, En vez de preguntar por cada bit agregando estados al problema, **¿Podemos preguntar de a dos bits, y mandar la respuesta a una única variable X?**

PARA LA SOLOCION NOS VALEMOS DE UNA RELACION ENTRE FLIP-FLOPS DATA Y TOGGLE:

Donde el FF-T es el encargado de poner el alto (“setear”) el dato y el FF-D es encargado de “pasar” el dato.



Cuya tabla de verdad se cumple, en este caso, solo para la combinación 09:

Bit1	Bit2	X
0	**0**	**0**
0	**9**	**1**
9	0	0
9	9	0

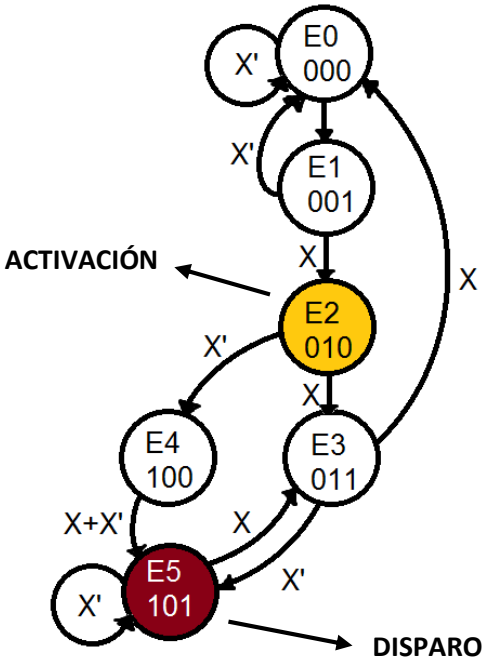
La única combinación de acciones que hará aparecer un alto en la salida es que primero se ponga el dato en alto y luego se pase el dato a la variable X.

Circuito implementable con solo un integrado de 2 Flip-Flops.

Consultando el manual TTL decidimos usar el IC 74LS109 con 2 FF-JK activados por flanco de subida.

MAQUINA DE ESTADOS Y DECODIFICACION

Ahora que sabemos cómo censar el ingreso de datos armamos el diagrama de estados con solo 6 estados:



Armamos la correspondiente tabla según el ciclo de los estados para obtener las expresiones de entrada para los Flip-Flops:

		X	Q0	Q1	Q2	Q0+	Q1+	Q2+	J0	K0	J1	K1	J2	K2
E	**0**	0	0	0	0	0	0	0	**0**	**X**	**0**	**X**	**0**	**X**
E	**1**	0	0	0	1	0	0	0	**0**	**X**	**0**	**X**	**X**	**1**
E	**2**	0	0	1	0	1	0	0	**1**	**X**	**X**	**1**	**0**	**X**
E	**3**	0	0	1	1	1	0	1	**1**	**X**	**X**	**1**	**X**	**0**
E	**4**	0	1	0	0	1	0	1	**X**	**0**	**0**	**X**	**1**	**X**
E	**5**	0	1	0	1	1	0	1	**X**	**0**	**0**	**X**	**X**	**0**
E	**0**	1	0	0	0	0	0	1	**0**	**X**	**0**	**X**	**1**	**X**
E	**1**	1	0	0	1	0	1	0	**0**	**X**	**1**	**X**	**X**	**1**
E	**2**	1	0	1	0	0	1	1	**0**	**X**	**X**	**0**	**1**	**X**
E	**3**	1	0	1	1	0	0	0	**0**	**X**	**X**	**1**	**X**	**1**
E	**4**	1	1	0	0	1	0	1	**X**	**0**	**0**	**X**	**1**	**X**
E	**5**	1	1	0	1	0	1	1	**X**	**1**	**1**	**X**	**X**	**0**

De sus correspondientes mapas de Karnaugh y posterior simplificación por el teorema de DeMorgan se obtienen las siguientes expresiones para los FF-JK:

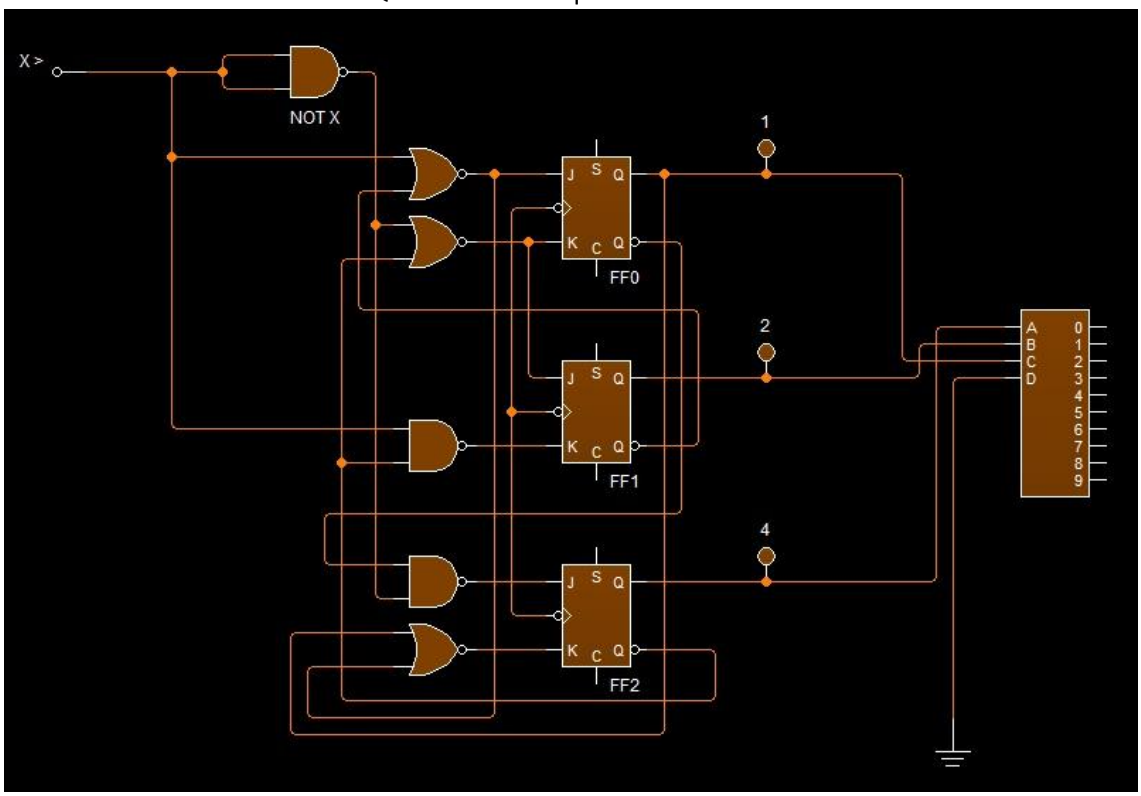
$$J0 = \overline{\overline{Q1} + X} \qquad K0 = \overline{\overline{Q2} + \overline{X}}$$

$$J1 = \overline{\overline{Q2} + \overline{X}} = K0 \qquad K1 = \overline{\overline{Q2}X}$$

$$J2 = \overline{\overline{Q0}\,\overline{X}} \qquad K2 = \overline{\overline{(\overline{Q1} + X)} + Q0} = \overline{J0 + Q0}$$

Además haremos uso de un decodificador para obtener los estados finales.

Quedando la máquina de estados:



Que implementamos con 3 compuertas NOR, 3 NAND, 3 FF-JK y un decodificador 74LS138.

COMBINACIONAL DE SELECCION

La pregunta que sigue ahora es:

Según el estado en el que está la alarma, **¿Qué combinación de números es válida, la de activación o la de desactivación?**

Es decir, según el estado actual, **¿Quién pone el dato el alto y quien lo pasa, la tecla 0 o la 9?**

Debemos hacer un combinacional que, si se está en la secuencia de activación, la tecla 0 "setee" el dato y la 9 lo "pase" a X. Mientras que si se está en la secuencia de desactivación, la tecla 9 "setee" y 0 "pase" el dato a la variable X.

Según el diagrama de estados, la alarma se estará activando en los estados E0 o E1, **y se estará desactivando toda vez que no esté en los estados E0 o E1.**

Así que armamos las siguientes ecuaciones lógicas:

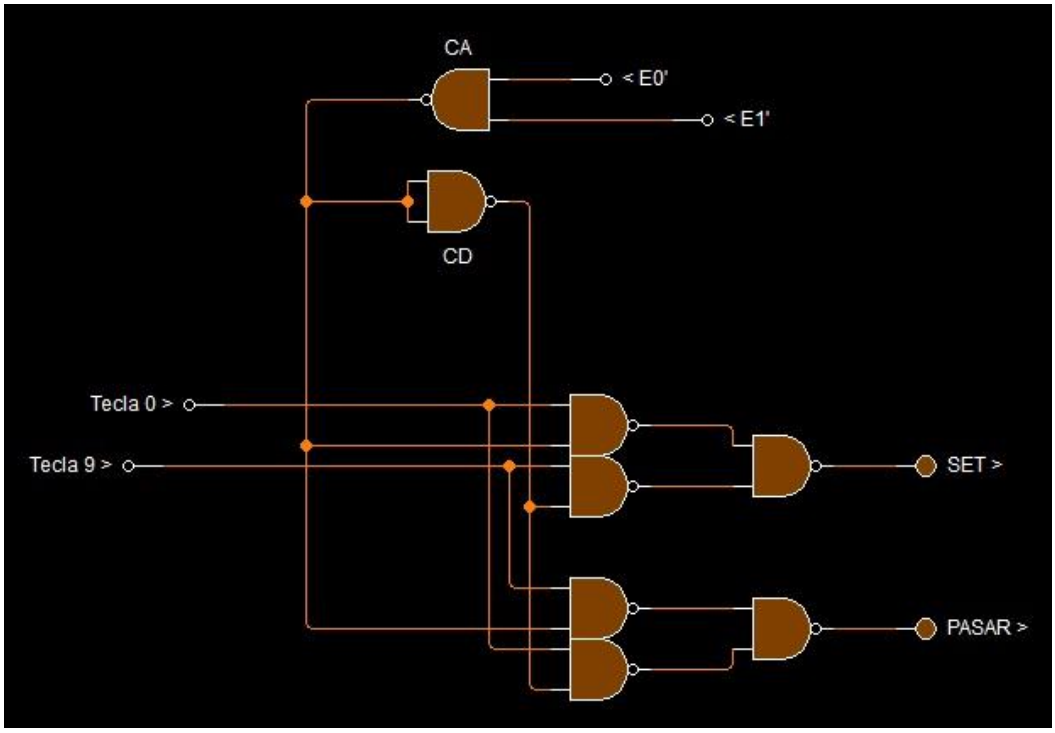
$$\boldsymbol{Condicion\ de\ activacion\ (CA) = E0 + E1 = \overline{\overline{E0}\ \overline{E1}}}$$

$$\boldsymbol{Condicion\ de\ desactivacion\ (CD) = \overline{E0 + E1} = \overline{CA}}$$

$$\boldsymbol{SET = CA\ 0 + CD\ 9 = \overline{(\overline{CA\ 0})\ (\overline{CD\ 9})}}$$

$$\boldsymbol{PASAR = CA\ 9 + CD\ 0 = \overline{(\overline{CA\ 9})(\overline{CD\ 0})}}$$

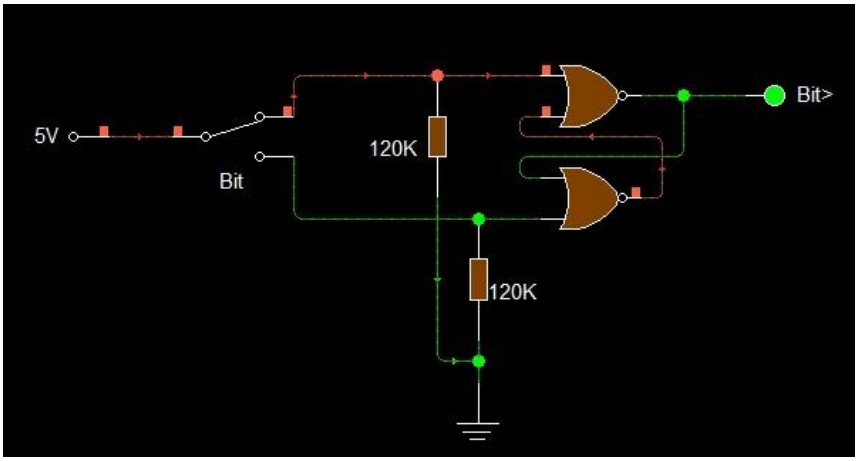
Las que nos dicen que la tecla 0 “seteara” el dato y la 9 lo “pasara” únicamente si estamos en la secuencia de activación de la alarma, en caso contrario se invertirán los roles.



Fácilmente Implementable con 8 compuertas NAND.

ELIMINADOR DE REBOTES

Cada tecla deberá ir con eliminadores de rebote para evitar problemas de sensibilidad. Serán simples Flip-Flops RS hechos con 2 compuertas NOR y resistencias Pull-Down.



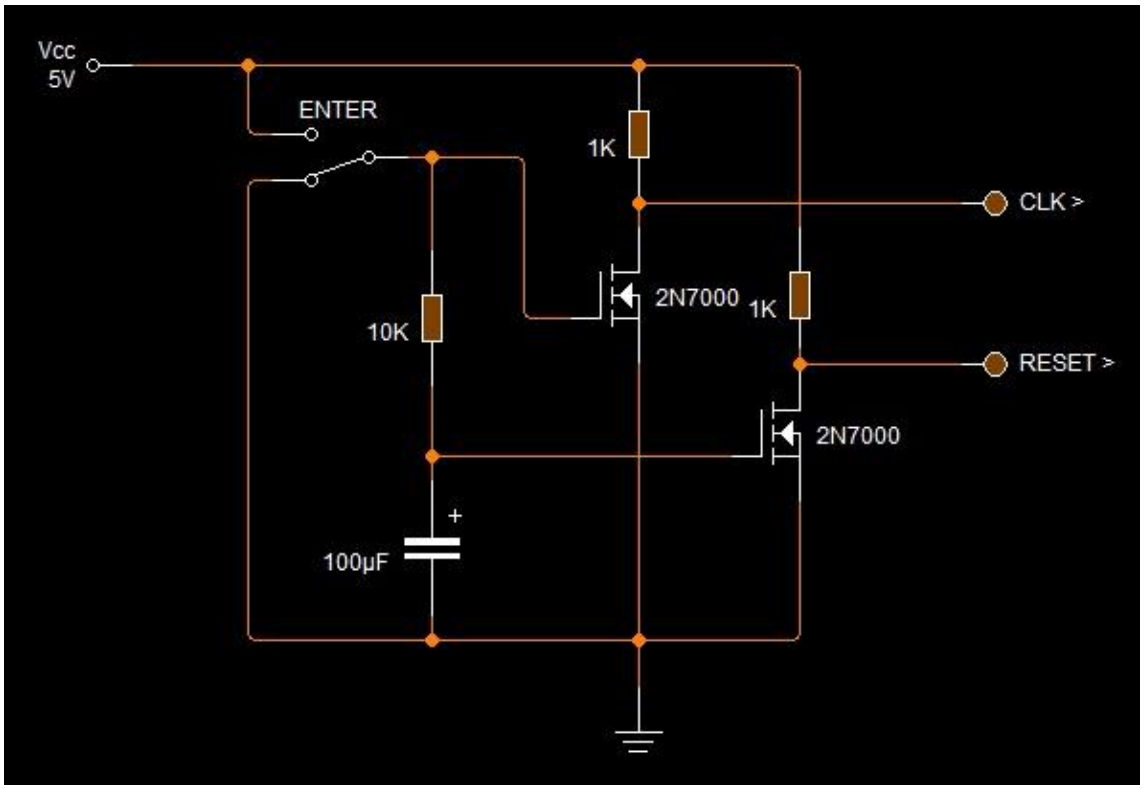
RETARDO CLOCK/RESET

Añadiremos una tecla de entrada de datos que tendrá dos funciones:

1- Mandar un flanco de bajada a los relojes para que avance la máquina de estados.

2- Blanquear los datos guardados en los FF de entrada, para que estén listos para los próximos datos.

Evidentemente debe haber un retardo entre una acción y la otra, puesto que sino la máquina de estados no alcanzaría a leer la variable X y no pasaría nunca de estados.
Para este circuito haremos uso de 2 transistores MOSFET canal N con una VGS (on) = 3V, y un circuito de retardo sencillo para que uno de los transistores se active luego de cierto tiempo.



Donde la llave será un pulsador que si no está oprimido pone en alto el clock y los resets de entrada, luego cuando se pulsa pone inmediatamente en bajo el clock haciendo que el autómata avance y luego de un pequeño tiempo blanquea los datos guardados en los FF de entrada dejándolos listos para la próxima combinación de números. Lo implementaremos con un par de transistores MOSFET 2N7000, unas resistencias y un capacitor electrolítico.

INDICADORES DE SALIDA

Si se ingresa correctamente la secuencia de activación 0909 se encenderá un **LED amarillo** indicando que la alarma esta activada, esto solo podrá pasar si la alarma esta activada y por tanto para apagarla vale la secuencia de desactivación, **ósea si esta activa la condición de desactivación CD.**

Si estando activada se ingresa incorrectamente la secuencia de desactivación 9090 se encenderá un **LED rojo** indicando que la alarma esta disparada, esto podrá ocurrir solo si se llega al estado E5 y no está disparada ya la alarma.

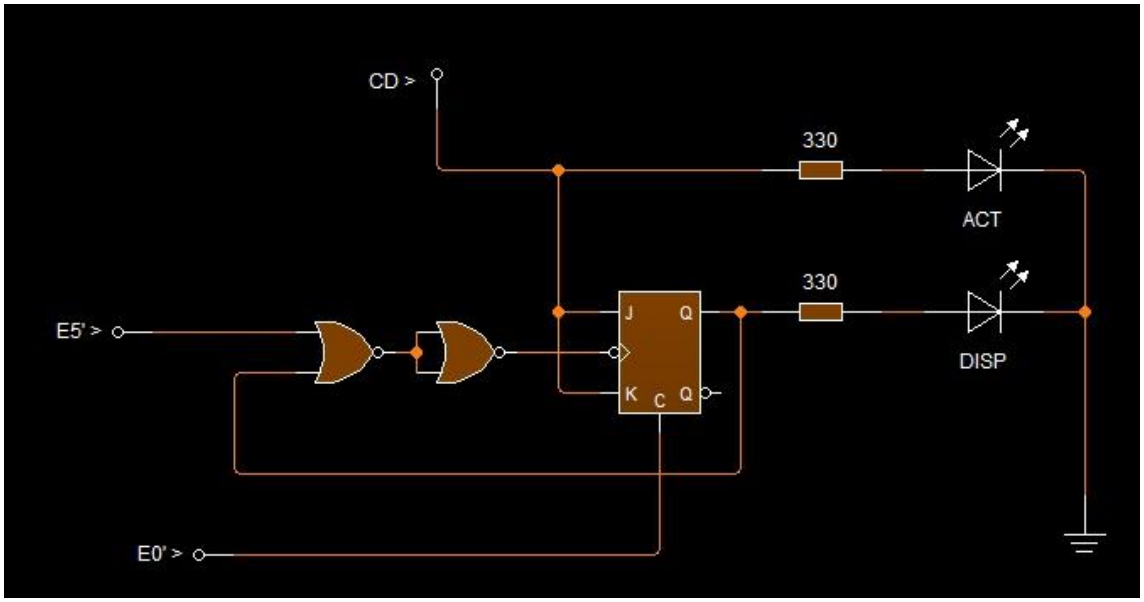
En resumen **el LED amarillo estará prendido si la condición de desactivación está activa y una vez disparada la alarma, la única forma de apagar el LED rojo es desactivándola, ósea llegando al estado E0.**

Por tanto:

$$\boldsymbol{ACT = CD}$$

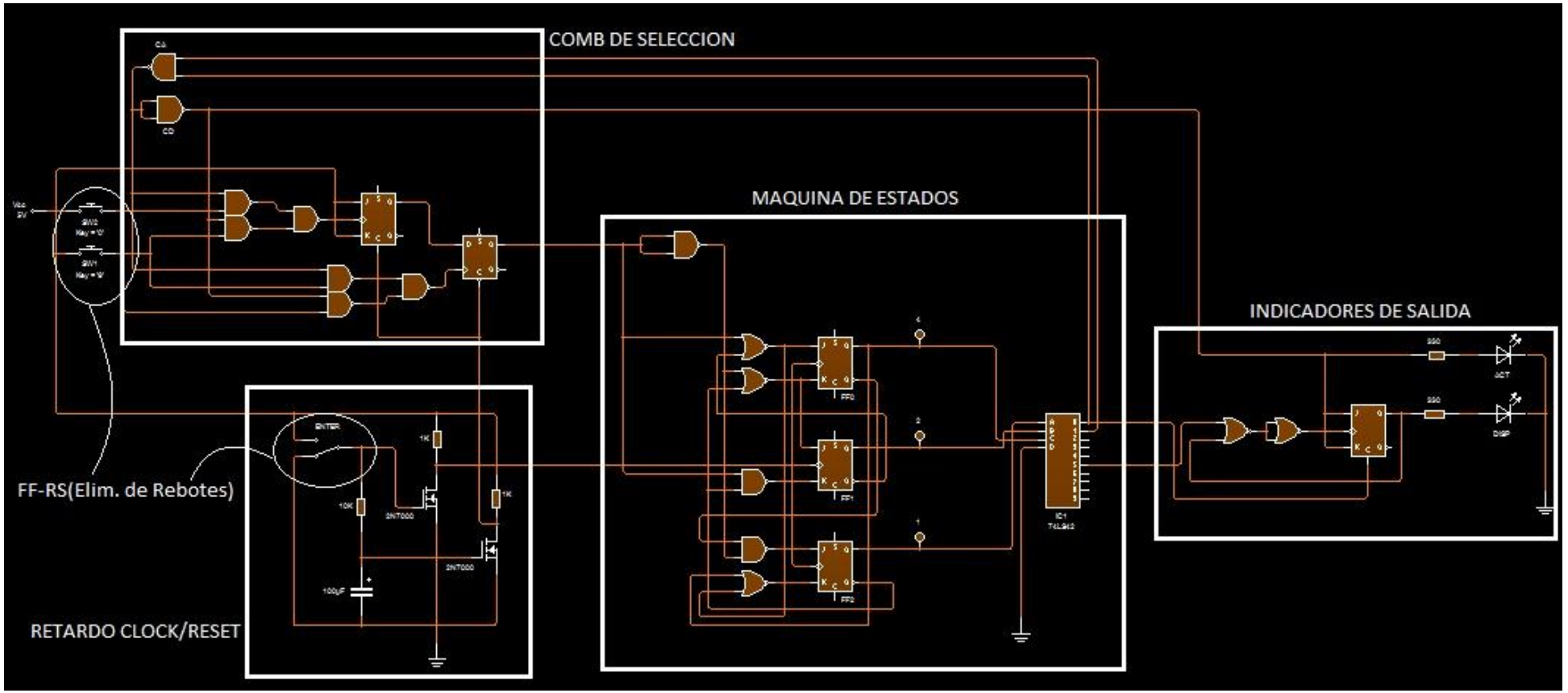
$$\boldsymbol{DISP = E5\,\overline{R} = \overline{\overline{E5} + R}}$$

Debemos utilizar un FF-T para guardar el estado del LED rojo.
Si la alarma se dispara se manda un flanco de bajada al FF haciendo que se encienda el LED rojo, pero esto solo pasa si el LED amarillo esta encendido y además el LED rojo anteriormente no lo estaba.
Una vez disparada si se llega al desactivar la alarma, se pone en cero el Reset del FF apagando el LED rojo, y como ya no vale la condición de activación se apagara también el LED amarillo.



Que implementaremos fácilmente con 2 compuertas NOR, un FF-JK en modo Toggle, LED's y resistencias.

Uniendo los 6 bloques de circuitos descriptos hasta ahora, armamos el diagrama de bloques final del proyecto:


COMB DE SELECCION
MAQUINA DE ESTADOS
INDICADORES DE SALIDA
FF-RS(Elim. de Rebotes)
RETARDO CLOCK/RESET

Consultando el manual TTL decidimos que para los Flip-Flops de las etapas de **INGRESO DE DATOS** y de **INDICADORES DE SALIDA** utilizaremos el 74LS109 provisto de 2 Flip-Flops JK disparados por flanco de reloj positivo.
Para la etapa de **MAQUINA DE ESTADOS Y DECODIFICACION** usaremos el 74LS78 para los Flip-Flops, ya que posee 2 FF JK disparados por flanco descendente con la entrada de reloj compartida, el 74LS138 como decodificador de 3Bit de entrada a 8 salidas, que trabaja en lógica negativa.
Para el circuito **RETARDO CLOCK/RESET** usaremos 2 MOSFET de enriquecimiento 2N7000.
Y utilizaremos los integrados 74LS00 para compuertas NAND y 74LS02 para compuertas NOR.

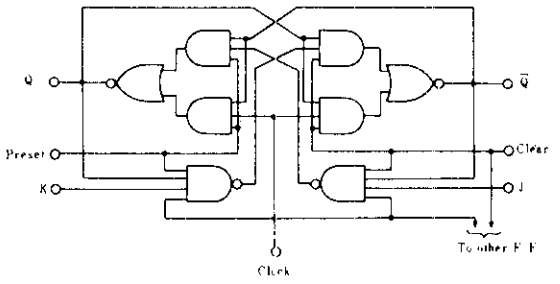
LISTA DE MATERIALES

IC 74LS78 Dual-JK Flip-Flop CLKC	2
IC 74LS109 Dual-JK Flip-Flop	2
IC 74LS138 3 Bit Decoder	1
IC 74ALS00 Quad NAND-2 Input	3
IC 74LS02 Quad NOR-2 Input	3
2N7000 MOSFET canal N	2
Pulsadores SPDT	3
Resistencia 330Ω a ¼ W	2
Resistencia 10K a ¼ W	1
Resistencia 1K a ¼ W	2
Capacitor Electrolítico 100µF/25V	1
LED Rojo	1
LED Amarillo	1

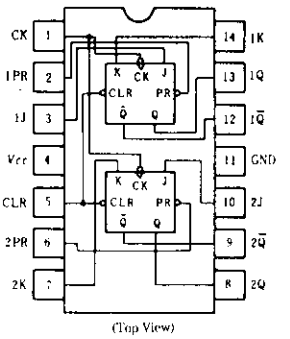
DATASHEETS

HD74LS78A ●Dual J-K Flip-Flops (with Preset, Common Clear, and Common Clock)

■BLOCK DIAGRAM(½)



■PIN ARRANGEMENT



■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Clock frequency		f_{clock}	0	–	30	MHz
Pulse width	Clock High	t_w	20	–	–	ns
	Preset, Clear Low		25	–	–	ns
Setup time	"H" Data	t_{su}	20↓	–	–	ns
	"L" Data		20↓	–	–	ns
Hold time		t_h	0↓	–	–	ns

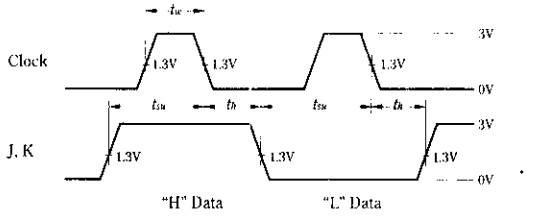
Note) ↓; The arrow indicates the falling edge.

■FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	×	×	Q_0	$\overline{Q}_0$

Notes) H; high level, L; low level, X; irrelevant
↓; transition from high to low level
Q_0; level of Q before the indicated steady-state input conditions were established.
$\overline{Q}_0$; complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.
*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

■TIMING METHOD



■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	–	–	V
		V_{IL}			–	–	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2.7V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=8mA$	–	–	0.5	V
				$I_{OL}=4mA$	–	–	0.4	
Input current	J, K	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	Clear				–	–	120	
	Preset				–	–	60	
	Clock				–	–	160	
	J, K	I_{IL}**	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	Clear				–	–	−1.6	
	Preset				–	–	−0.8	
	Clock				–	–	−1.6	
	J, K	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
	Clear				–	–	0.6	
	Preset				–	–	0.3	
	Clock				–	–	0.8	
Short circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current ***		I_{CC}	$V_{CC}=5.25V$		–	4	6	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* V_{CC} = 5V, Ta = 25°C
** I_{IL} should not be measured when preset and clear inputs are low at same time.
*** With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

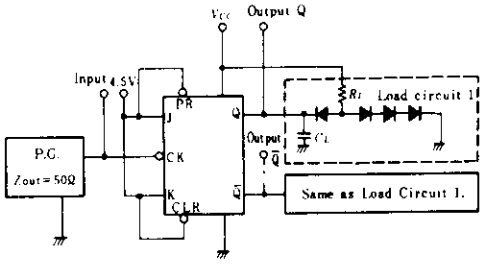
■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			C_L = 15pF, R_L = 2kΩ	30	45		MHz
Propagation delay time	t_{PLH}	Clear Preset Clock	Q, $\bar{Q}$		–	15	20	ns
	t_{PHL}				–	15	20	ns

■TESTING METHOD

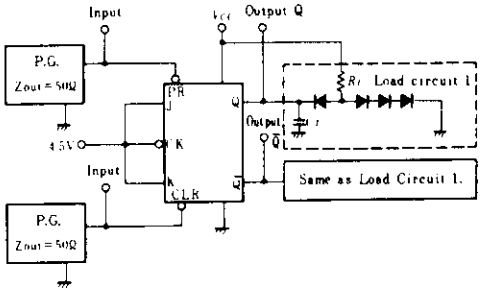
1) Test Circuit

1.1) f_{max}, t_{PLH}, t_{PHL} (Clock→Q,$\bar{Q}$)

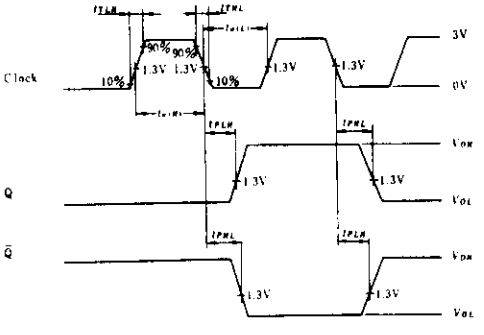


Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

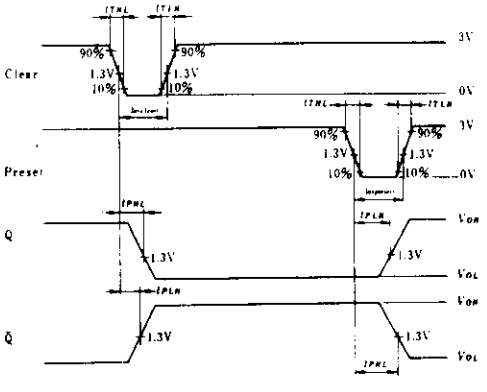
1.2) t_{PHL}, t_{PLH} (Clear, Preset→Q,$\bar{Q}$)



Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

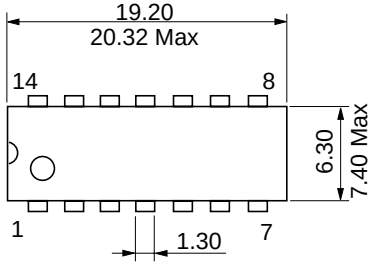


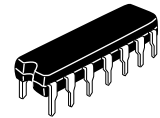
Note) Clock input pulse; t_{TLH}≦15ns, t_{THL}≦6ns, *PRR*=1MHz, duty cycle=50% and: for f_{max}, t_{TLH}=t_{THL}≦2.5ns.

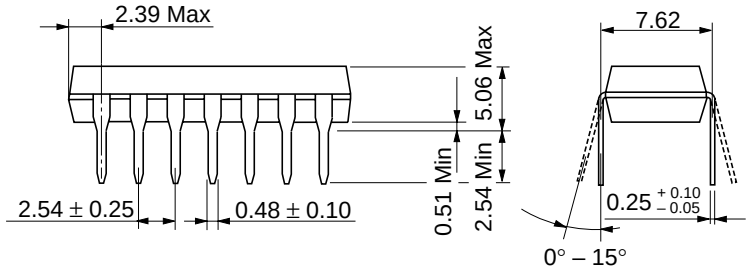


Note) Clear and preset input pulse; t_{TLH}≦15ns, t_{THL}≦6ns, *PRR*=1MHz

Unit: mm

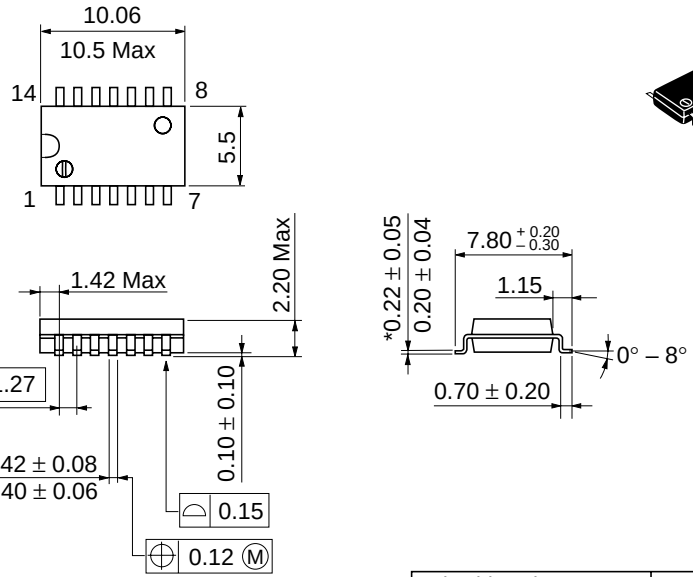


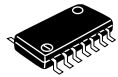




Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm

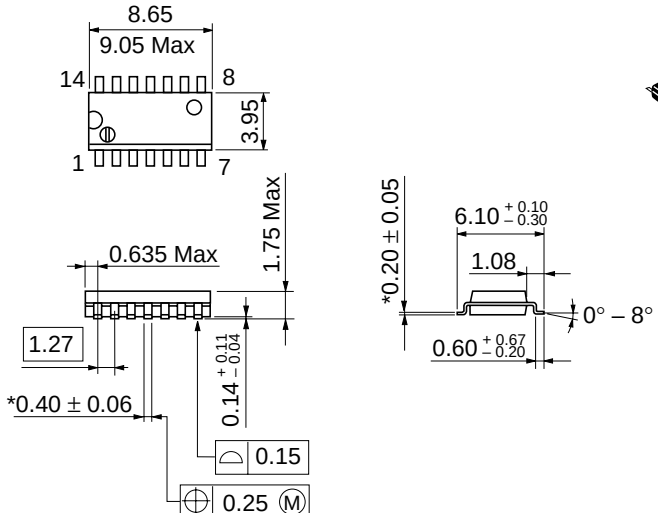




Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

*Pd plating

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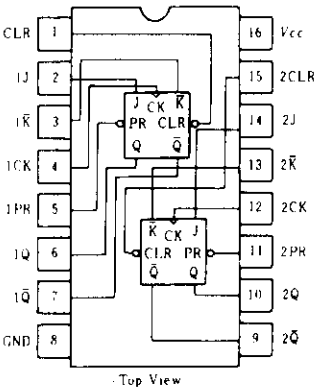
HD74LS109A ●Dual J-$\bar{K}$ Positive-edge-triggered Flip-Flops (with Preset and Clear)

■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Clock frequency		f_{clock}	0	–	25	MHz
Pulse width	Clock High	t_w	25	–	–	ns
	Preset, Clear Low		25	–	–	
Setup time	"H" Data	t_{su}	20↑	–		ns
	"L" Data		20↑	–	–	
Hold time		t_h	5↑	–	–	ns

Note) ↑ ; The arrow indicates the rising edge.

■PIN ARRANGEMENT



Top View

■FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	$\bar{K}$	Q	$\bar{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\bar{Q}_0$
H	H	↑	H	H	H	L
H	H	L	×	×	Q_0	$\bar{Q}_0$

Notes) H; high level, L; low level, X; irrelevant
↑; transition from low to high level
Q_0; level of Q before the indicated steady-state conditions were established.
$\bar{Q}_0$; complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established.
*; This configuration is nonstable, that is, it will not persist where preset and clear inputs return to their inactive (high) level.

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	–	–	V
		V_{IL}			–	–	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=8mA$	–	–	0.5	V
				$I_{OL}=4mA$	–	–	0.4	
Input current	J, $\bar{K}$, CK	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	CLR, PR				–	–	40	
	J, $\bar{K}$, CK	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	-0.4	mA
	CLR, PR				–	–	-0.8	
	J, $\bar{K}$, CK	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
	CLR, PR				–	–	0.2	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		-20	–	-100	mA
Supply current **		I_{CC}	$V_{CC}=5.25V$		–	4	8	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	-1.5	V

* V_{CC}=5V, Ta=25°C
** With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

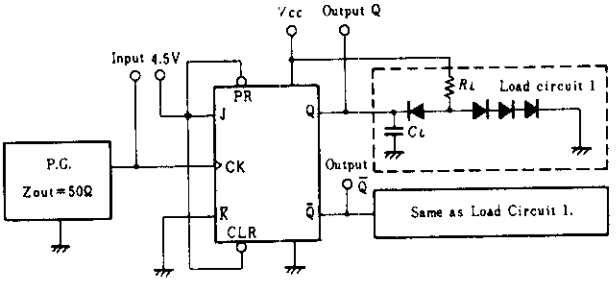
■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			C_L=15pF, R_L=2kΩ	25	33	–	MHz
Propagation delay time	t_{PLH}	Clear Preset Clock	Q, $\overline{Q}$		–	13	25	ns
	t_{PHL}				–	25	40	ns

■TESTING METHOD

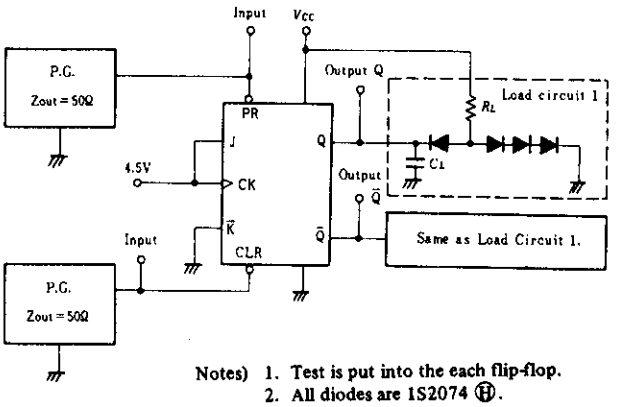
1) Test Circuit

1.1) f_{max}, t_{PLH}, t_{PHL} (Clock→Q,$\overline{Q}$)



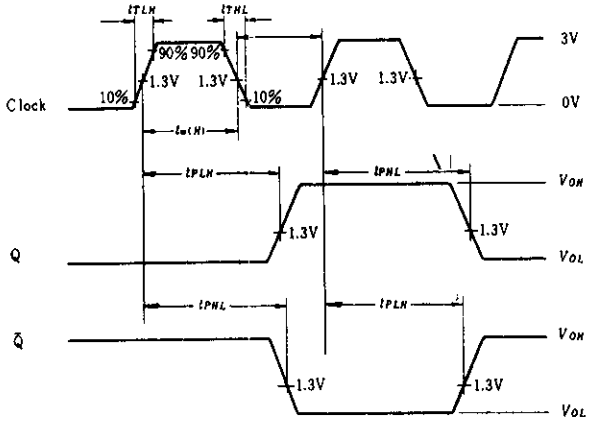
Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

1.2) t_{PHL}, t_{PLH} (Clear, Preset→Q,$\overline{Q}$)

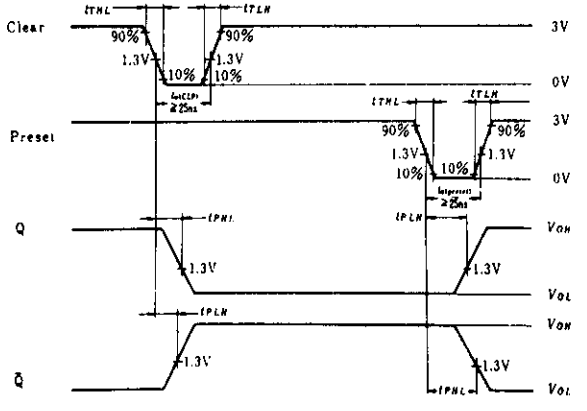


Notes) 1. Test is put into the each flip-flop.
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

Waveform

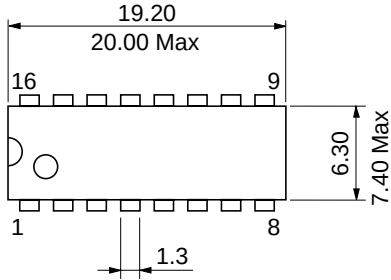


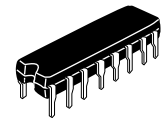
Note) Clock input pulse: t_{TLH}≦15ns, t_{THL}≦6ns, PRR=1MHz, duty cycle=50% and: for f_{max}, t_{TLH}=t_{THL}≦2.5ns.

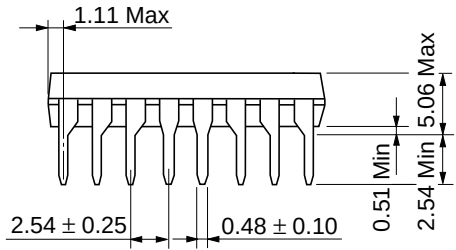


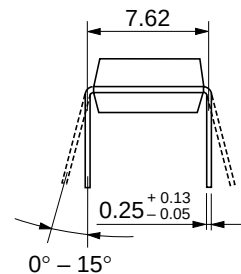
Note) Clear and preset input pulse: t_{TLH}≦15ns, t_{THL}≦6ns, PRR=1MHz.

Unit: mm



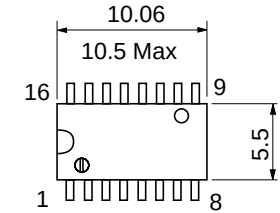


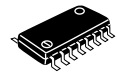


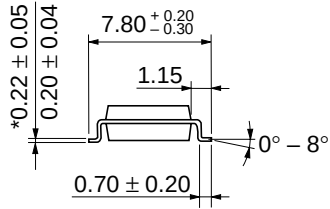


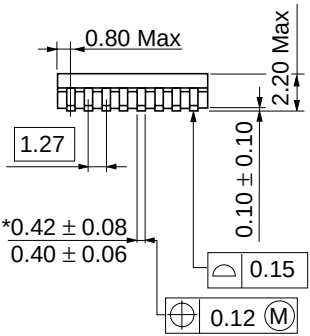
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm





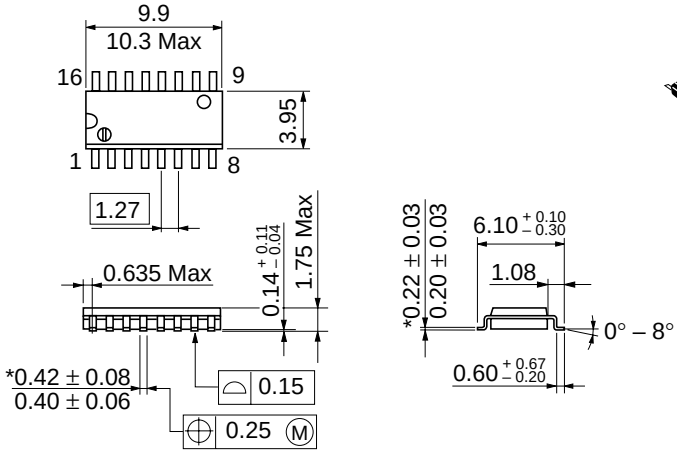




*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm



Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS138 • DM74LS139 Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The DM74LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The DM74LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- DM74LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- DM74LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - DM74LS138 21 ns
  - DM74LS139 21 ns
- Typical power dissipation
  - DM74LS138 32 mW
  - DM74LS139 34 mW

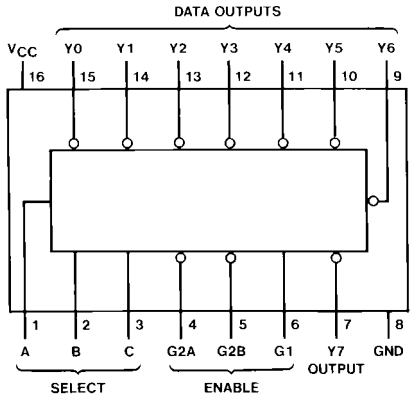
Ordering Code:

Order Number	Package Number	Package Description
DM74LS138M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS138N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74LS139M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS139SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS139N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

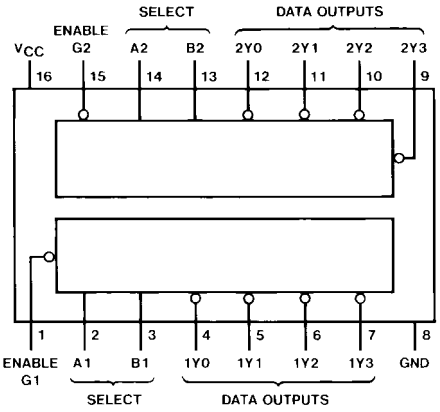
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

DM74LS138



DM74LS139



Function Tables

DM74LS138

Inputs					Outputs							
Enable		Select										
G1	G2 (Note 1)	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

DM74LS139

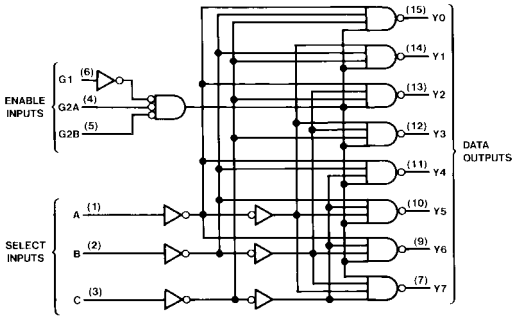
Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Level
L = LOW Level
X = Don't Care

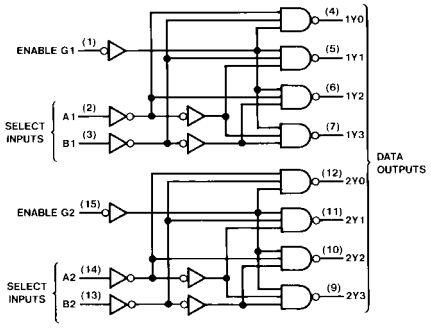
Note 1: G2 = G2A + G2B

Logic Diagrams

DM74LS138



DM74LS139



Absolute Maximum Ratings(Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS138 Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

DM74LS138 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)		6.3	10	mA

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs enabled and OPEN.

DM74LS138 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R_L = 2 kΩ				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output	2		27		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output	3		18		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output	3		27		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output	2		24		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output	3		18		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output	3		28		40	ns

DM74LS139 Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

DM74LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 7)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 8)		6.8	11	mA

Note 6: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second.

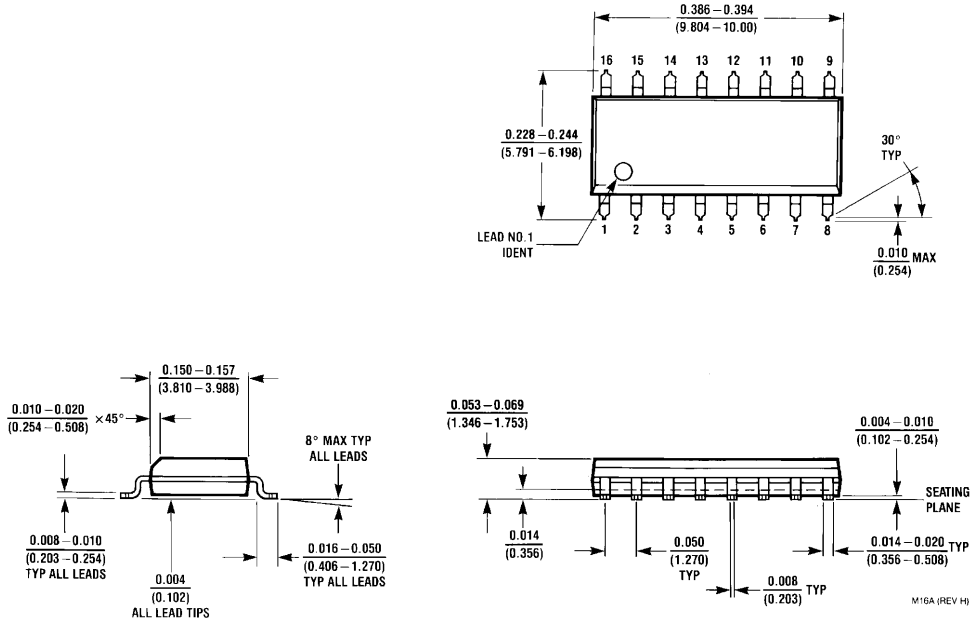
Note 8: I_{CC} is measured with all outputs enabled and OPEN.

DM74LS139 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

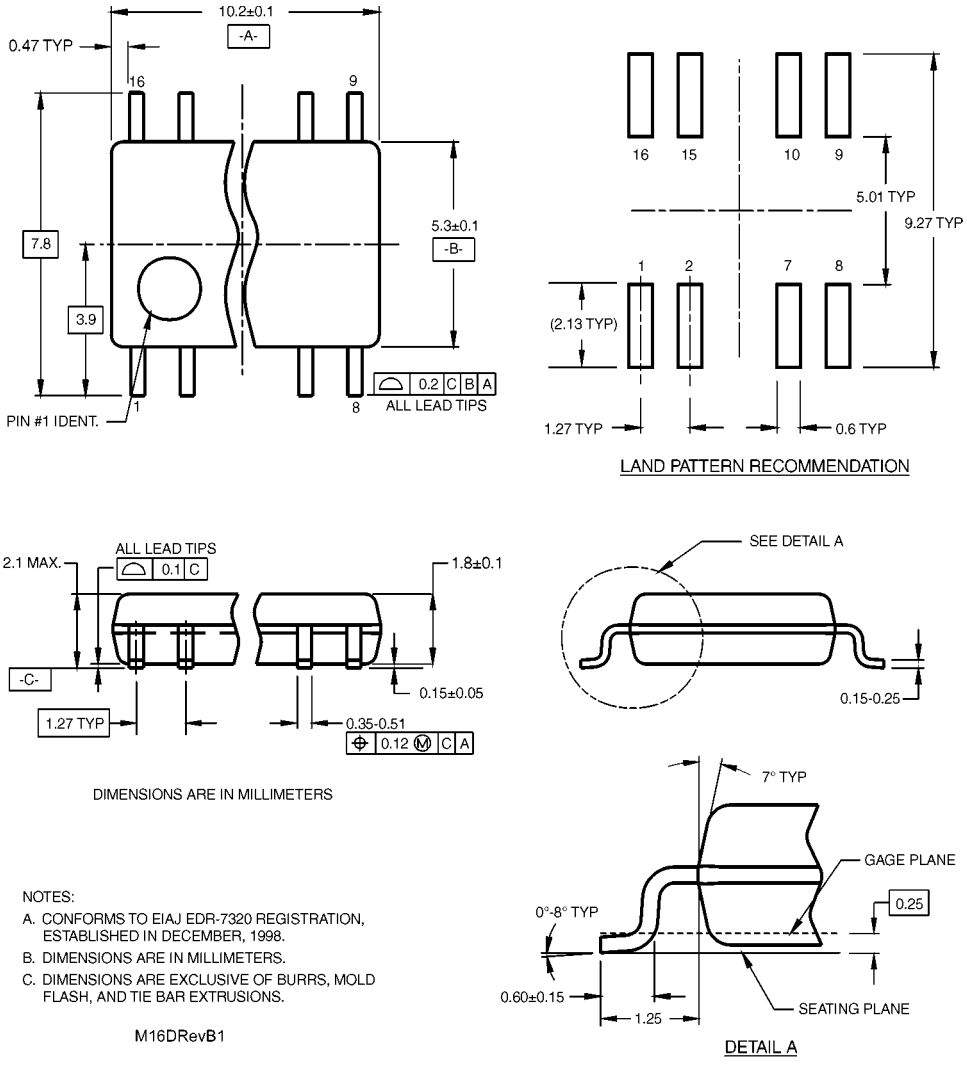
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output		18		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output		27		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output		18		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output		24		40	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

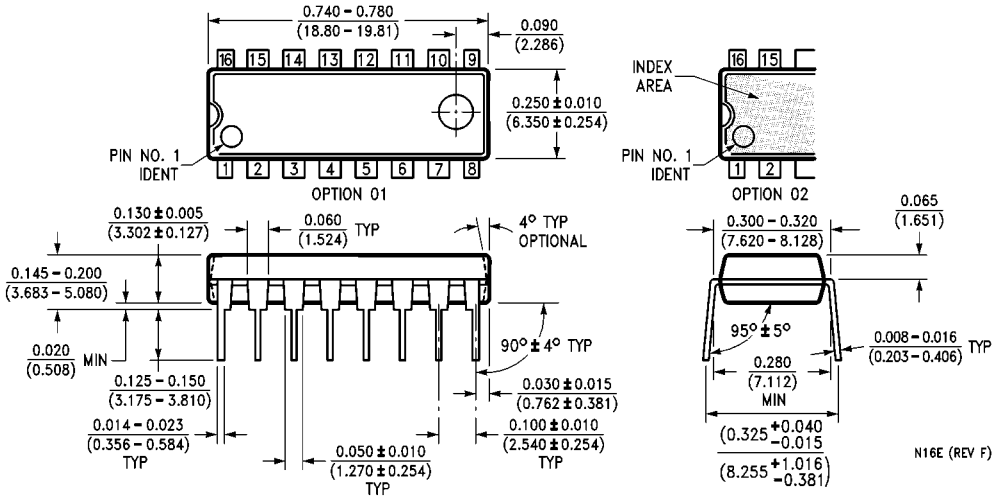
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

FAIRCHILD SEMICONDUCTOR™

September 1986
Revised February 2000

DM74ALS00A
Quad 2-Input NAND Gate

General Description

This device contains four independent gates, each of which performs the logic NAND function.

Features

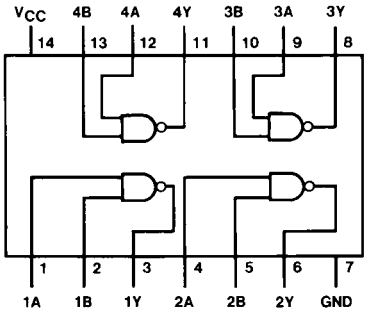
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Ordering Code:

Order Number	Package Number	Package Description
DM74ALS00AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74ALS00ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74ALS00AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	86.5°C/W
M Package	116.0°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

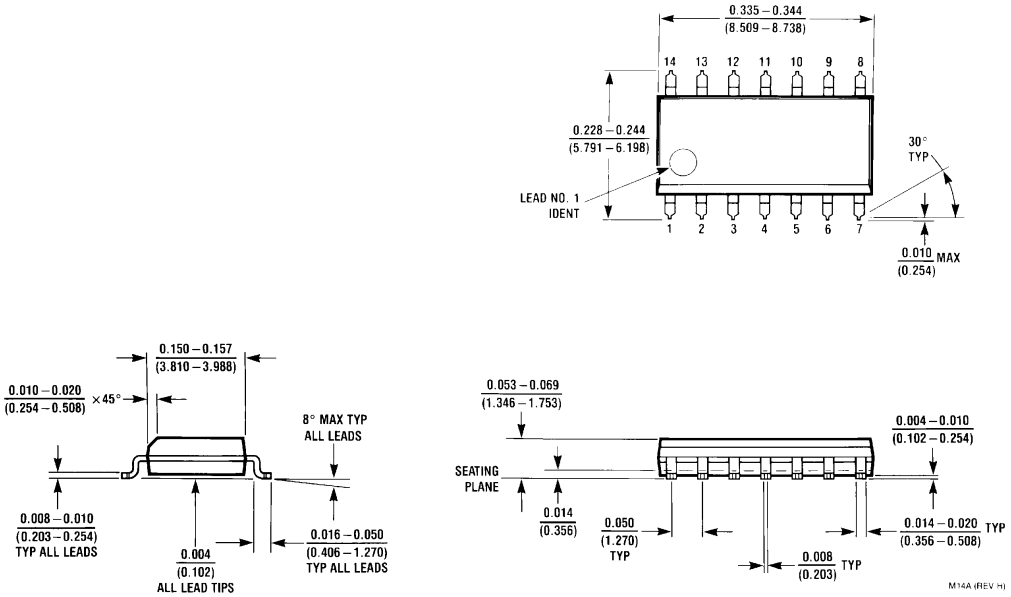
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	LOW Level Output Voltage	V_{CC} = 4.5V	I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	µA
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs HIGH		0.43	0.85	mA
			Outputs LOW		1.62	3	mA

Switching Characteristics

over recommended operating free air temperature range

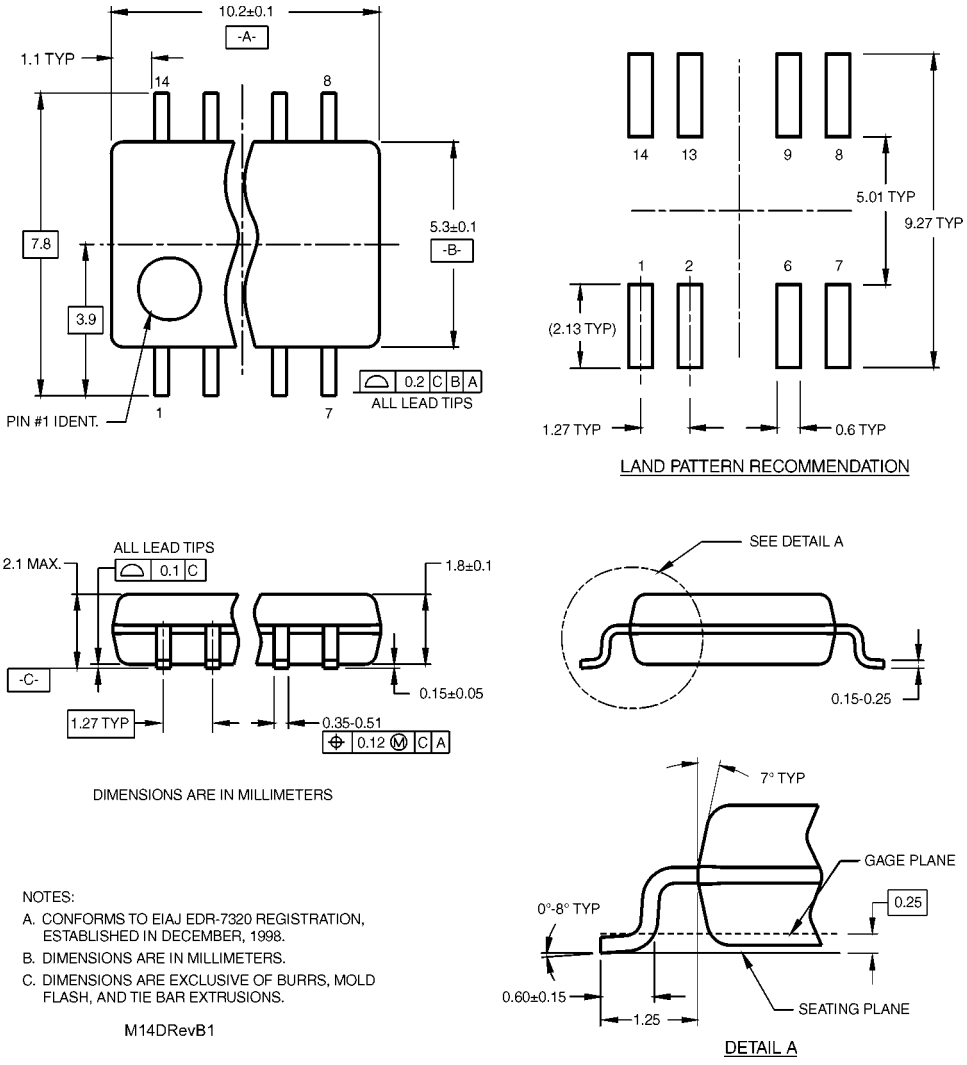
Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	3	11	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		2	8	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

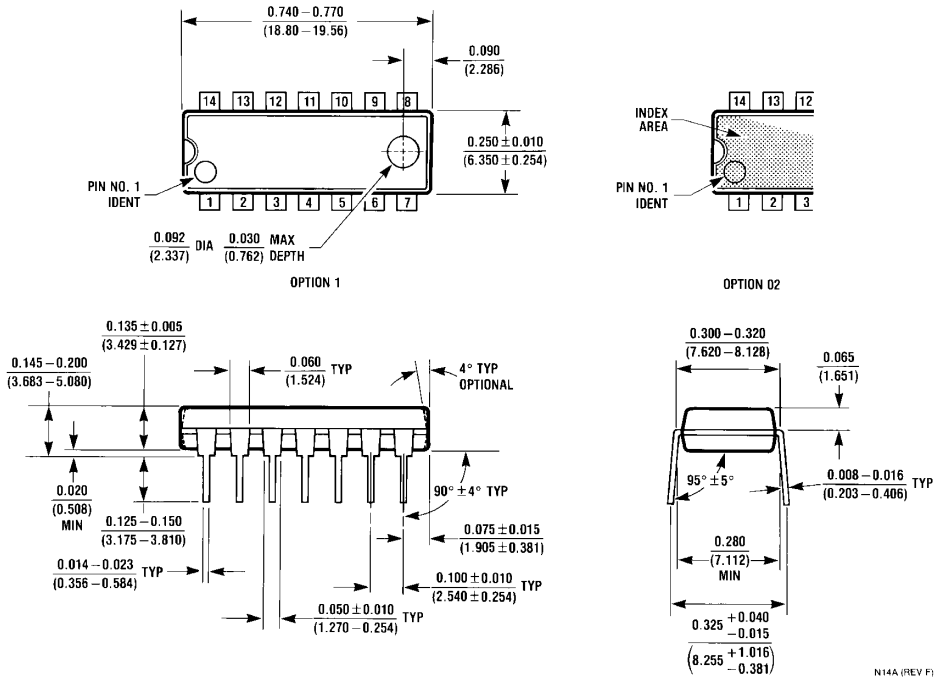
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

FAIRCHILD SEMICONDUCTOR™

May 1986
Revised March 2000

DM74LS02
Quad 2-Input NOR Gate

General Description

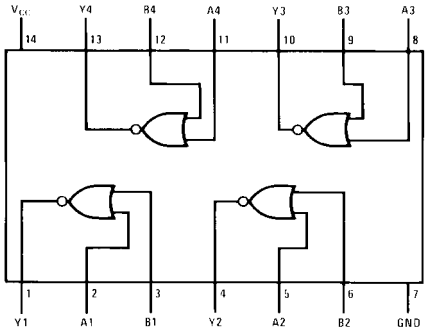
This device contains four independent gates each of which performs the logic NOR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS02M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS02SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS02N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.40	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		1.6	3.2	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		2.8	5.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

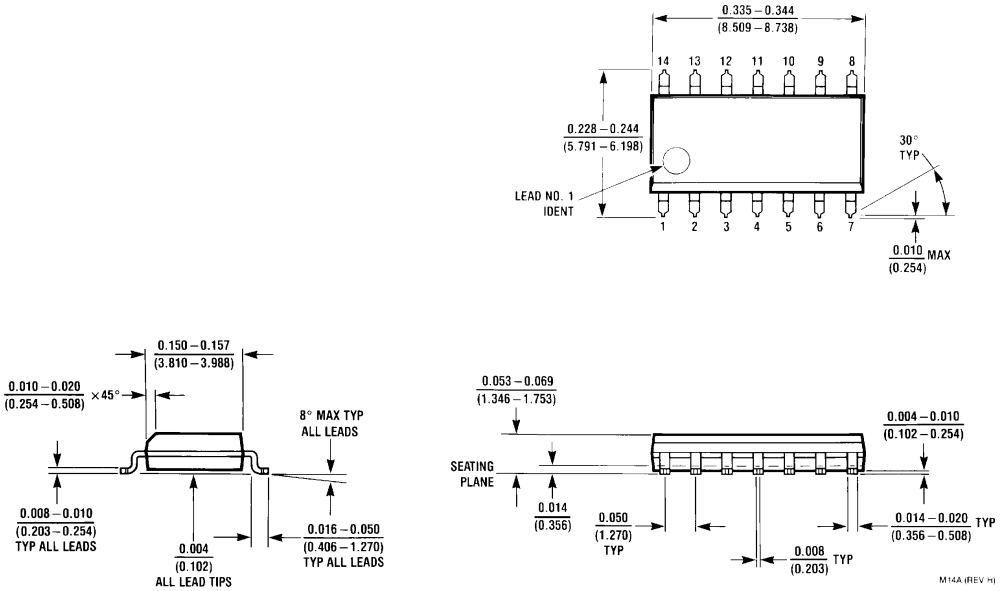
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

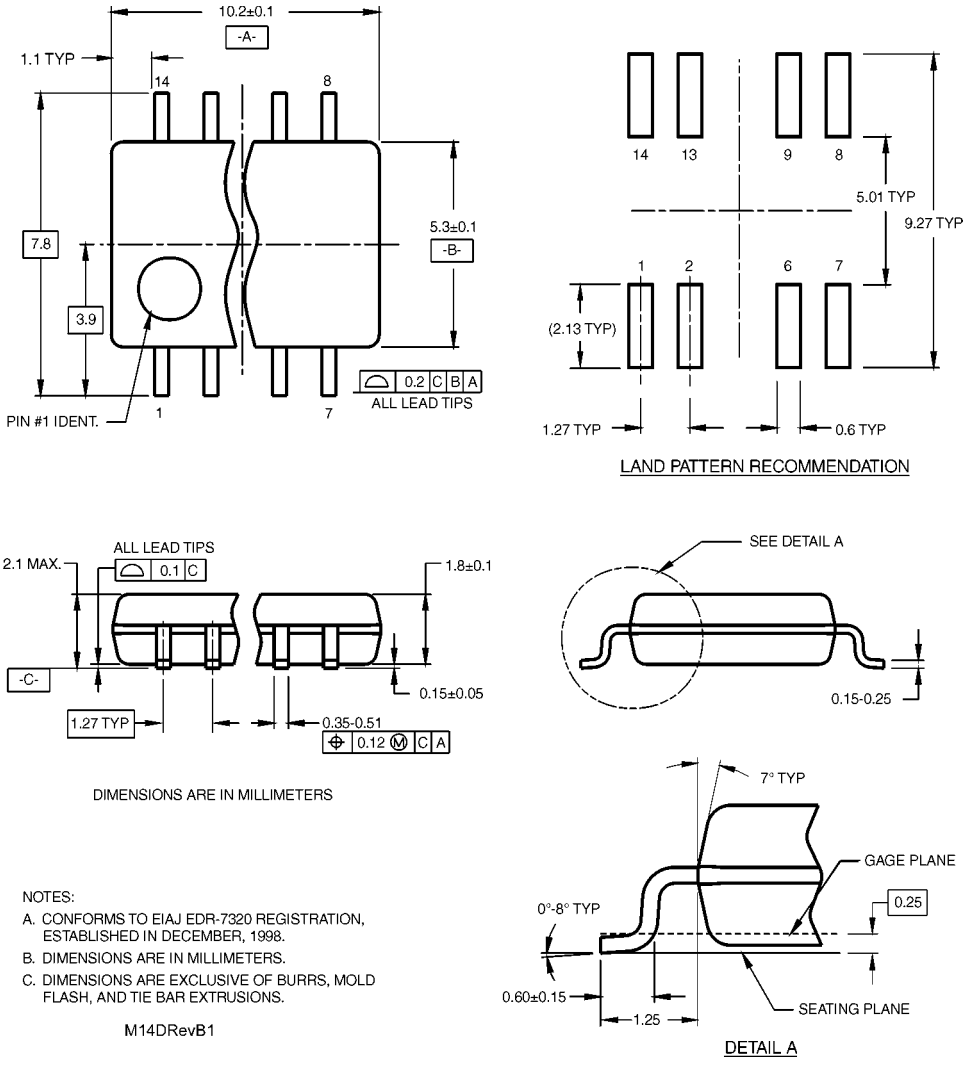
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		13		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		10		15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

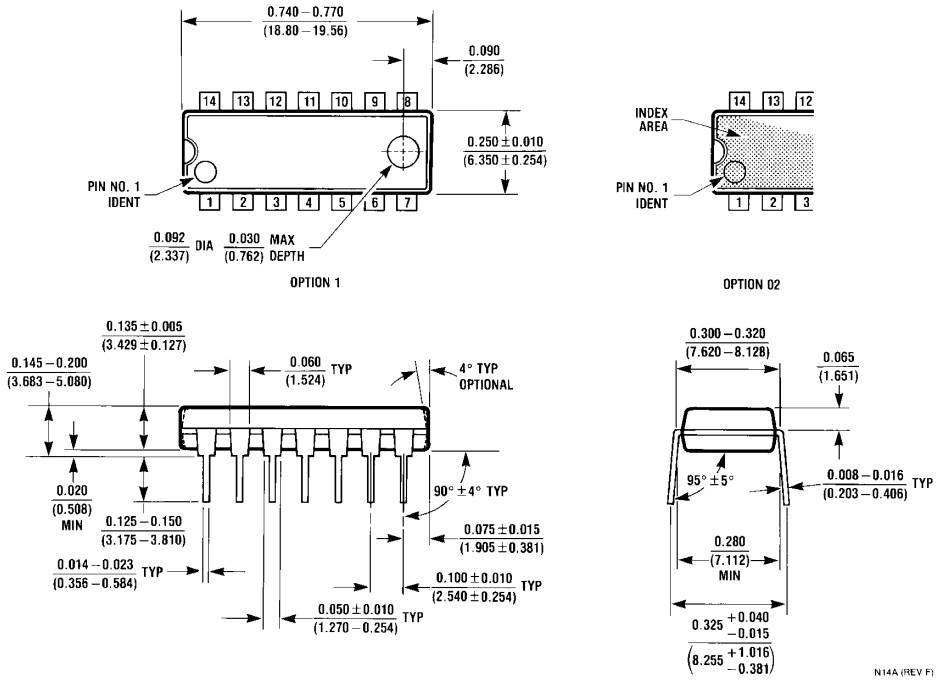
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

FAIRCHILD
SEMICONDUCTOR TM

November 1995

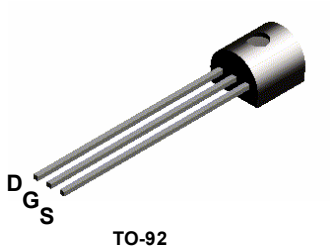
2N7000 / 2N7002 / NDS7002A
N-Channel Enhancement Mode Field Effect Transistor

General Description

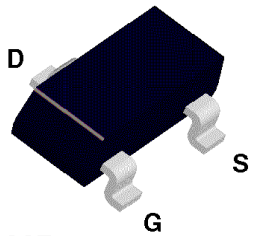
These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 400mA DC and can deliver pulsed currents up to 2A. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

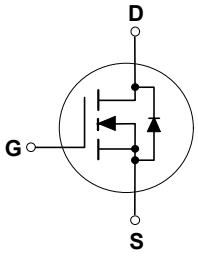
- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.



TO-92



SOT-23



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	2N7000	2N7002	NDS7002A	Units
V_{DSS}	Drain-Source Voltage	60			V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	60			V
V_{GSS}	Gate-Source Voltage - Continuous	±20			V
	- Non Repetitive (tp < 50µs)	±40			
I_D	Maximum Drain Current - Continuous	200	115	280	mA
	- Pulsed	500	800	1500	
P_D	Maximum Power Dissipation	400	200	300	mW
	Derated above 25°C	3.2	1.6	2.4	mW/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150		-65 to 150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300			°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	312.5	625	417	°C/W

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 µA	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	2N7000			1	µA
		T_J=125°C				1	mA
		V_{DS} = 60 V, V_{GS} = 0 V	2N7002 NDS7002A			1	µA
		T_J=125°C				0.5	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 15 V, V_{DS} = 0 V	2N7000			10	nA
		V_{GS} = 20 V, V_{DS} = 0 V	2N7002 NDS7002A			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -15 V, V_{DS} = 0 V	2N7000			-10	nA
		V_{GS} = -20 V, V_{DS} = 0 V	2N7002 NDS7002A			-100	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	2N7000	0.8	2.1	3	V
		V_{DS} = V_{GS}, I_D = 250 µA	2N7002 NDS7002A	1	2.1	2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 500 mA	2N7000		1.2	5	Ω
		T_J =125°C			1.9	9	
		V_{GS} = 4.5 V, I_D = 75 mA			1.8	5.3	
		V_{GS} = 10 V, I_D = 500 mA	2N7002		1.2	7.5	
		T_J =100°C			1.7	13.5	
		V_{GS} = 5.0 V, I_D = 50 mA			1.7	7.5	
		T_J =100C			2.4	13.5	
		V_{GS} = 10 V, I_D = 500 mA	NDS7002A		1.2	2	
		T_J =125°C			2	3.5	
		V_{GS} = 5.0 V, I_D = 50 mA			1.7	3	
		T_J =125°C			2.8	5	
$V_{DS(ON)}$	Drain-Source On-Voltage	V_{GS} = 10 V, I_D = 500 mA	2N7000		0.6	2.5	V
		V_{GS} = 4.5 V, I_D = 75 mA			0.14	0.4	
		V_{GS} = 10 V, I_D = 500mA	2N7002		0.6	3.75	
		V_{GS} = 5.0 V, I_D = 50 mA			0.09	1.5	
		V_{GS} = 10 V, I_D = 500mA	NDS7002A		0.6	1	
		V_{GS} = 5.0 V, I_D = 50 mA			0.09	0.15	

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
ON CHARACTERISTICS Continued (Note 1)							
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 10 V	2N7000	75	600		mA
		V_{GS} = 10 V, $V_{DS} \geq 2\ V_{DS(on)}$	2N7002	500	2700		
		V_{GS} = 10 V, $V_{DS} \geq 2\ V_{DS(on)}$	NDS7002A	500	2700		
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 200 mA	2N7000	100	320		mS
		$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA	2N7002	80	320		
		$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA	NDS7002A	80	320		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	All		20	50	pF
C_{oss}	Output Capacitance		All		11	25	pF
C_{rss}	Reverse Transfer Capacitance		All		4	5	pF
t_{on}	Turn-On Time	V_{DD} = 15 V, R_L = 25 Ω, I_D = 500 mA, V_{GS} = 10 V, R_{GEN} = 25	2N7000			10	ns
		V_{DD} = 30 V, R_L = 150 Ω, I_D = 200 mA, V_{GS} = 10 V, R_{GEN} = 25 Ω	2N700 NDS7002A			20	
t_{off}	Turn-Off Time	V_{DD} = 15 V, R_L = 25 Ω, I_D = 500 mA, V_{GS} = 10 V, R_{GEN} = 25	2N7000			10	ns
		V_{DD} = 30 V, R_L = 150 Ω, I_D = 200 mA, V_{GS} = 10 V, R_{GEN} = 25 Ω	2N700 NDS7002A			20	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		2N7002			115	mA
			NDS7002A			280	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		2N7002			0.8	A
			NDS7002A			1.5	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 115 mA (Note 1)	2N7002		0.88	1.5	V
		V_{GS} = 0 V, I_S = 400 mA (Note 1)	NDS7002A		0.88	1.2	

Note:
1. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

2N7000 / 2N7002 / NDS7002A

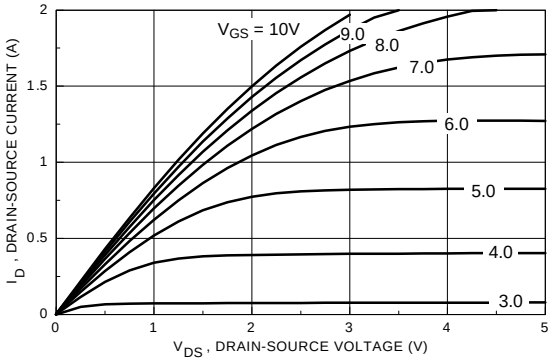


Figure 1. On-Region Characteristics

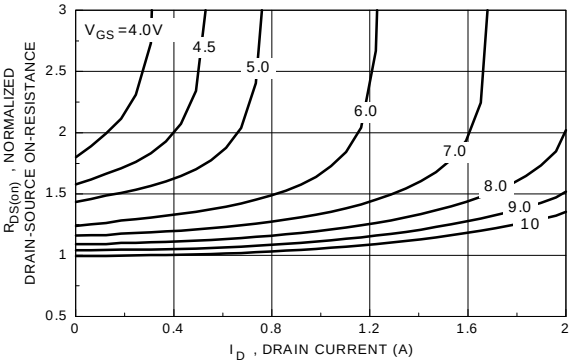


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

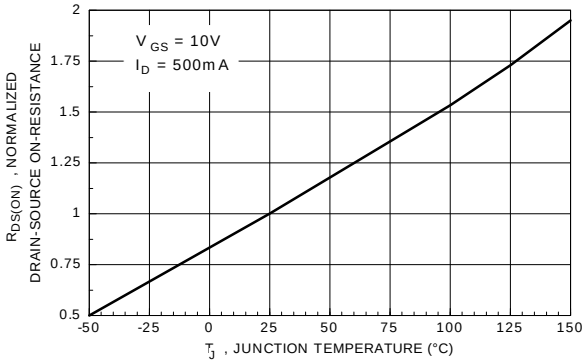


Figure 3. On-Resistance Variation with Temperature

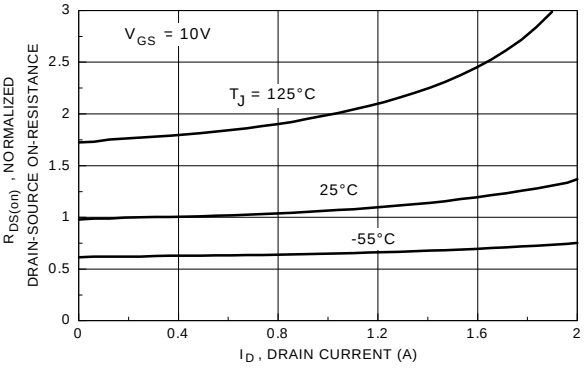


Figure 4. On-Resistance Variation with Drain Current and Temperature

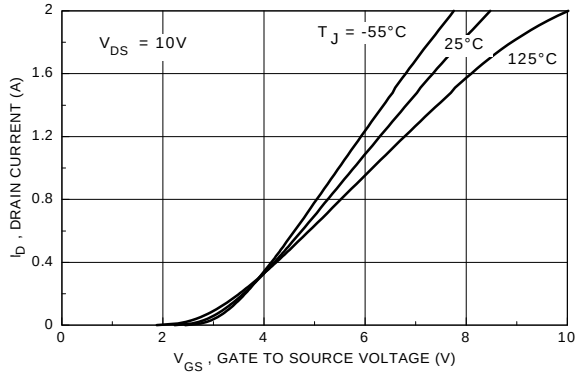


Figure 5. Transfer Characteristics

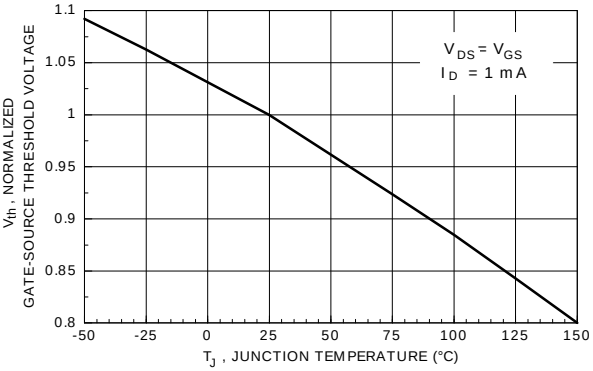


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

2N7000 / 2N7002 /NDS7002A

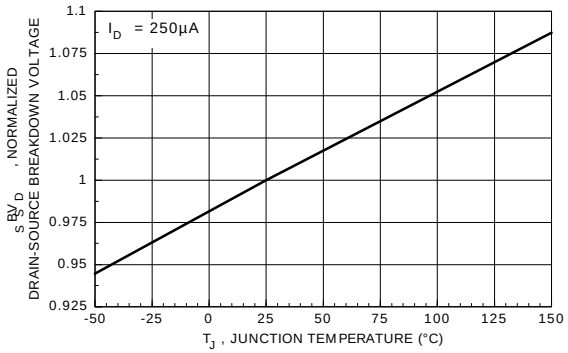


Figure 7. Breakdown Voltage Variation with Temperature

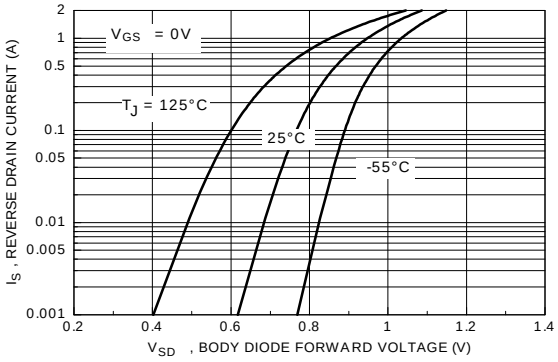


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

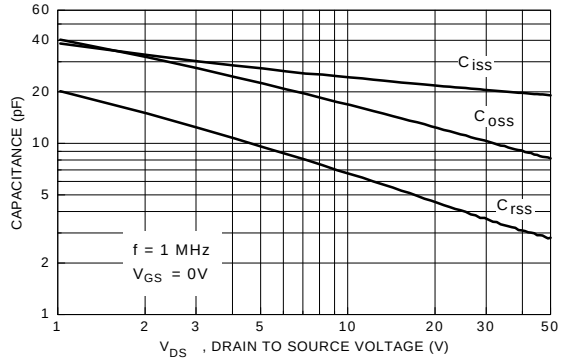


Figure 9. Capacitance Characteristics

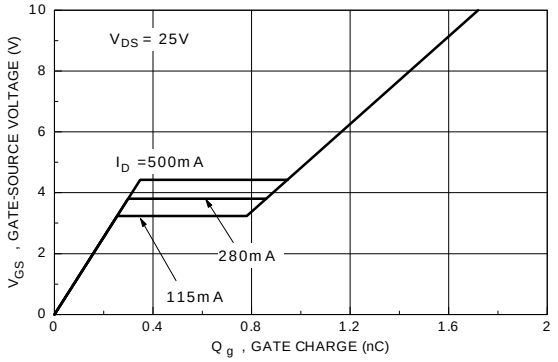


Figure 10. Gate Charge Characteristics

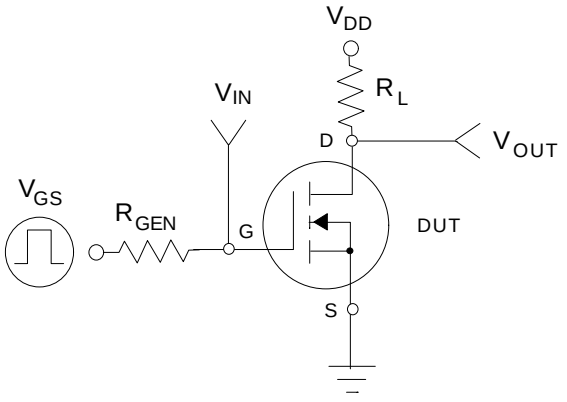


Figure 11. Switching Test Circuit

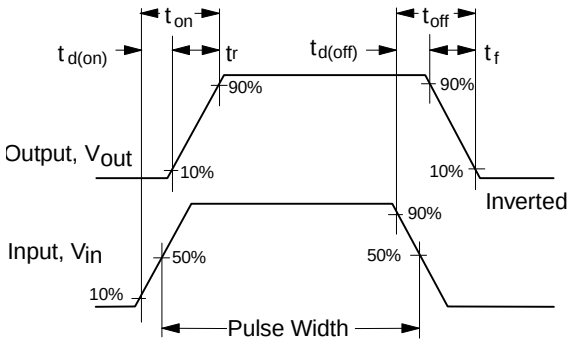


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

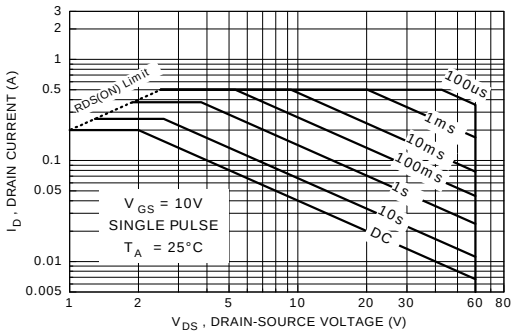


Figure 13. 2N7000 Maximum Safe Operating Area

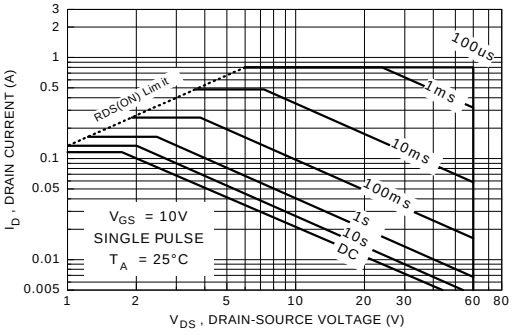


Figure 14. 2N7002 Maximum Safe Operating Area

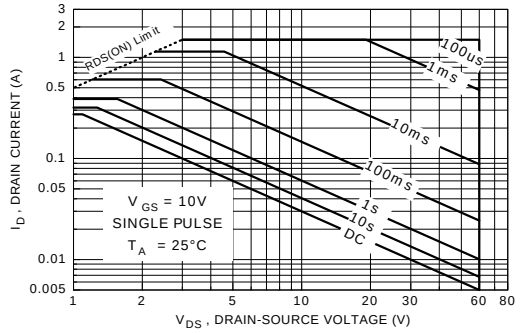


Figure 15. NDS7000A Maximum Safe Operating Area

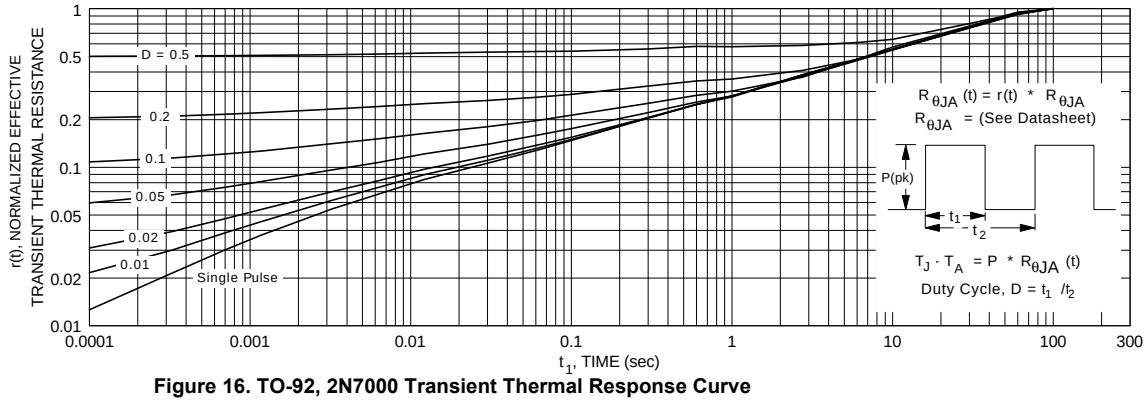


Figure 16. TO-92, 2N7000 Transient Thermal Response Curve

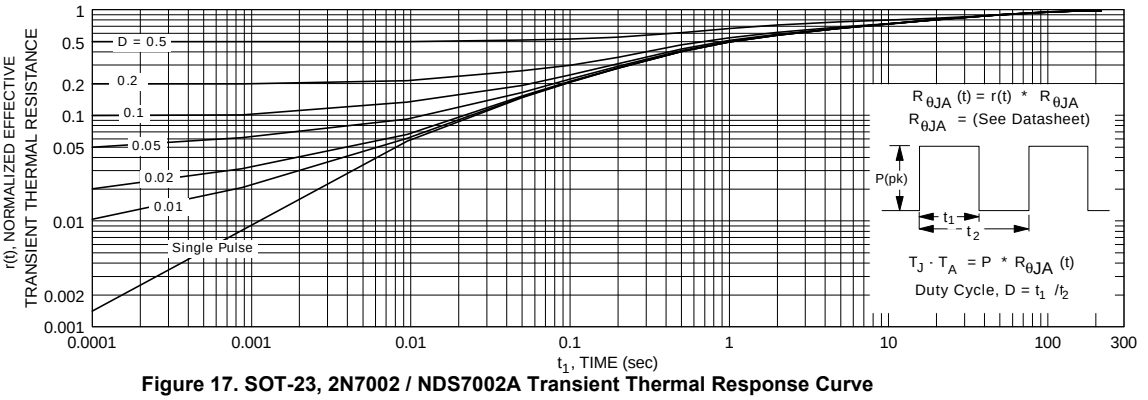


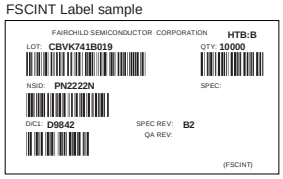
Figure 17. SOT-23, 2N7002 / NDS7002A Transient Thermal Response Curve

TO-92 Tape and Reel Data and Package Dimensions

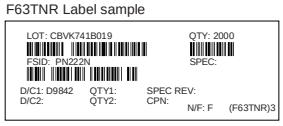
FAIRCHILD SEMICONDUCTOR™

TO-92 Packaging
Configuration: Figure 1.0

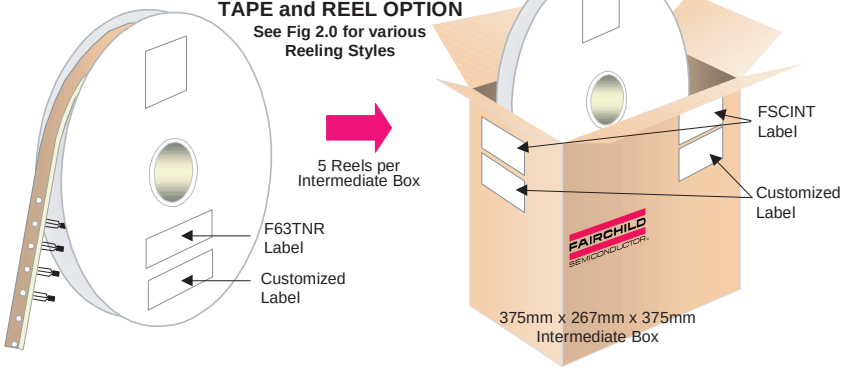
FSCINT Label sample



F63TNR Label sample



TAPE and REEL OPTION
See Fig 2.0 for various Reeling Styles

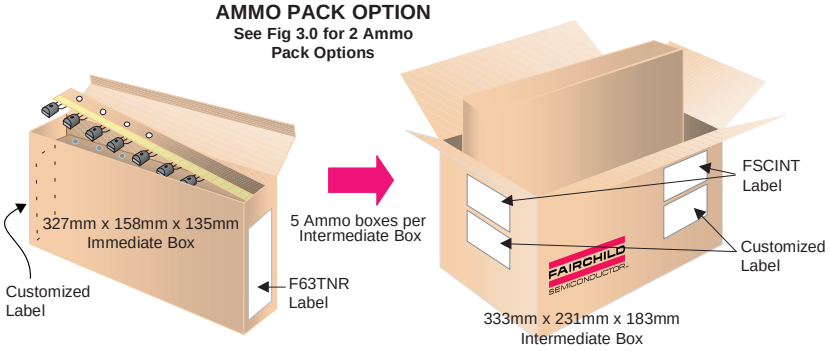


TO-92 TNR/AMMO PACKING INFROMATION

Packing	Style	Quantity	EOL code
Reel	A	2,000	D26Z
	E	2,000	D27Z
Ammo	M	2,000	D74Z
	P	2,000	D75Z

Unit weight = 0.22 gm
Reel weight with components = 1.04 kg
Ammo weight with components = 1.02 kg
Max quantity per intermediate box = 10,000 units

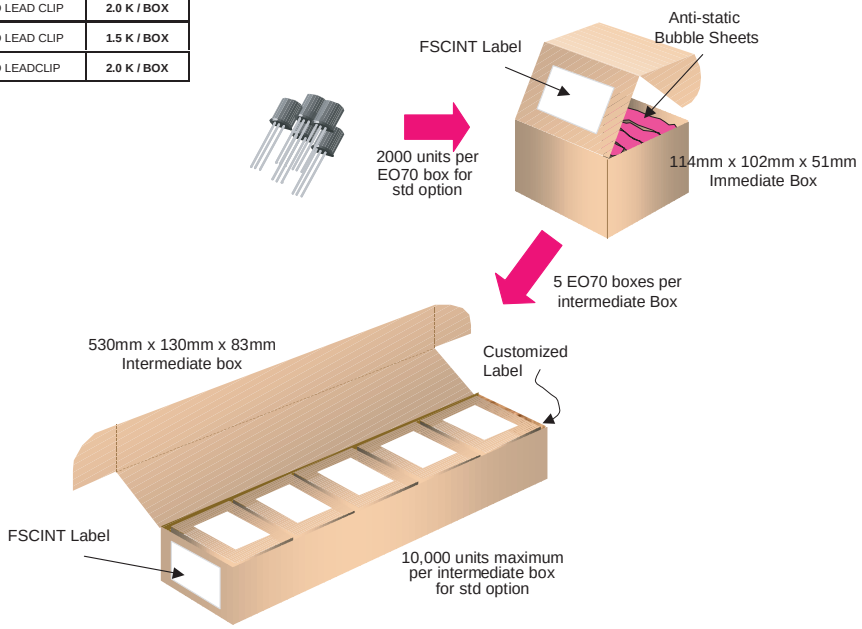
AMMO PACK OPTION
See Fig 3.0 for 2 Ammo Pack Options



(TO-92) BULK PACKING INFORMATION

EOL CODE	DESCRIPTION	LEADCLIP DIMENSION	QUANTITY
J18Z	TO-18 OPTION STD	NO LEAD CLIP	2.0 K / BOX
J05Z	TO-5 OPTION STD	NO LEAD CLIP	1.5 K / BOX
NO EOL CODE	TO-92 STANDARD STRAIGHT	NO LEADCLIP	2.0 K / BOX

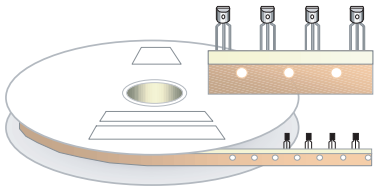
BULK OPTION
See Bulk Packing Information table



TO-92 Tape and Reel Data and Package Dimensions, continued

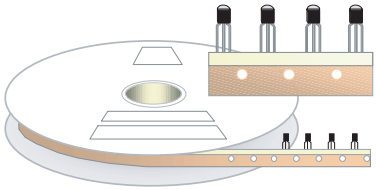
TO-92 Reeling Style
Configuration: Figure 2.0

Machine Option “A” (H)



Style “A”, D26Z, D70Z (s/h)

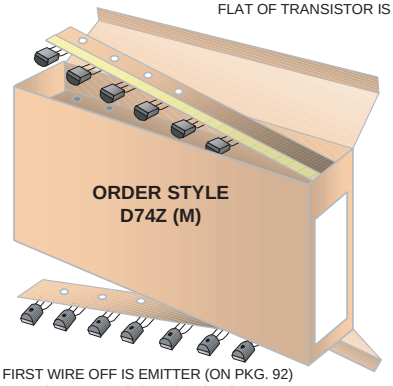
Machine Option “E” (J)



Style “E”, D27Z, D71Z (s/h)

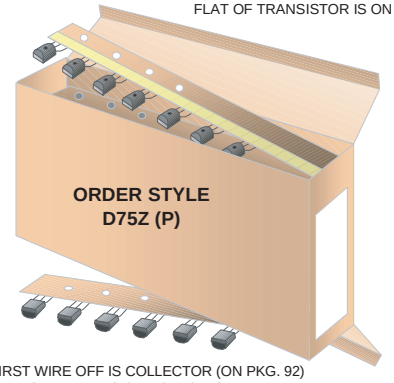
TO-92 Radial Ammo Packaging
Configuration: Figure 3.0

FIRST WIRE OFF IS COLLECTOR
ADHESIVE TAPE IS ON THE TOP SIDE
FLAT OF TRANSISTOR IS ON TOP



FIRST WIRE OFF IS EMITTER (ON PKG. 92)
ADHESIVE TAPE IS ON BOTTOM SIDE
FLAT OF TRANSISTOR IS ON BOTTOM

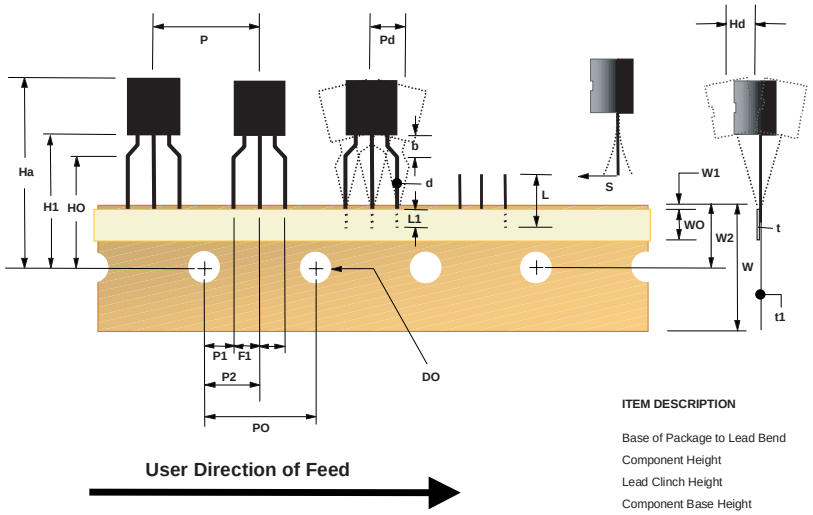
FIRST WIRE OFF IS EMITTER
ADHESIVE TAPE IS ON THE TOP SIDE
FLAT OF TRANSISTOR IS ON BOTTOM



FIRST WIRE OFF IS COLLECTOR (ON PKG. 92)
ADHESIVE TAPE IS ON BOTTOM SIDE
FLAT OF TRANSISTOR IS ON TOP

TO-92 Tape and Reel Data and Package Dimensions, continued

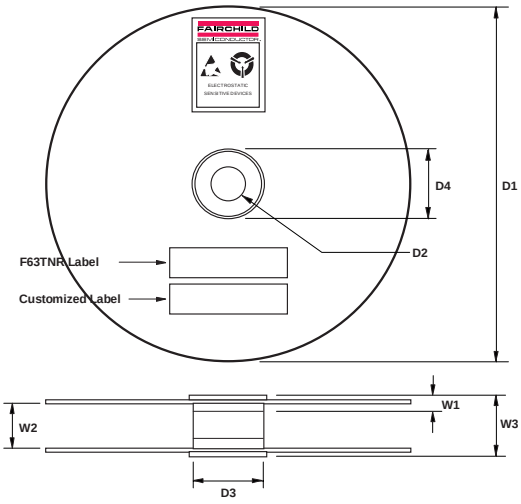
TO-92 Tape and Reel Taping
Dimension Configuration: Figure 4.0



ITEM DESCRIPTION	SYMBOL	DIMENSION
Base of Package to Lead Bend	b	0.098 (max)
Component Height	Ha	0.928 (+/- 0.025)
Lead Clinch Height	HO	0.630 (+/- 0.020)
Component Base Height	H1	0.748 (+/- 0.020)
Component Alignment (side/side)	Pd	0.040 (max)
Component Alignment (front/back)	Hd	0.031 (max)
Component Pitch	P	0.500 (+/- 0.020)
Feed Hole Pitch	PO	0.500 (+/- 0.008)
Hole Center to First Lead	P1	0.150 (+0.009, -0.010)
Hole Center to Component Center	P2	0.247 (+/- 0.007)
Lead Spread	F1/F2	0.104 (+/- 0 .010)
Lead Thickness	d	0.018 (+0.002, -0.003)
Cut Lead Length	L	0.429 (max)
Taped Lead Length	L1	0.209 (+0.051, -0.052)
Taped Lead Thickness	t	0.032 (+/- 0.006)
Carrier Tape Thickness	t1	0.021 (+/- 0.006)
Carrier Tape Width	W	0.708 (+0.020, -0.019)
Hold - down Tape Width	WO	0.236 (+/- 0.012)
Hold - down Tape position	W1	0.035 (max)
Feed Hole Position	W2	0.360 (+/- 0.025)
Sprocket Hole Diameter	DO	0.157 (+0.008, -0.007)
Lead Spring Out	S	0.004 (max)

Note : All dimensions are in inches.

TO-92 Reel
Configuration: Figure 5.0

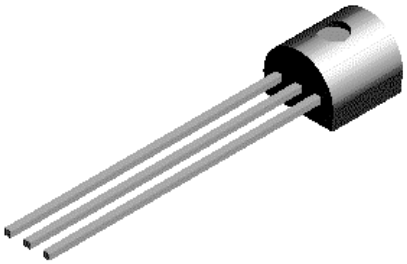


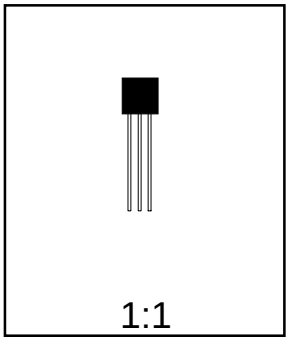
ITEM DESCRIPTION	SYSMBOL	MINIMUM	MAXIMUM
Reel Diameter	D1	13.975	14.025
Arbor Hole Diameter (Standard)	D2	1.160	1.200
(Small Hole)	D2	0.650	0.700
Core Diameter	D3	3.100	3.300
Hub Recess Inner Diameter	D4	2.700	3.100
Hub Recess Depth	W1	0.370	0.570
Flange to Flange Inner Width	W2	1.630	1.690
Hub to Hub Center Width	W3		2.090

Note: All dimensions are inches

TO-92 Tape and Reel Data and Package Dimensions

TO-92 (FS PKG Code 92, 94, 96)





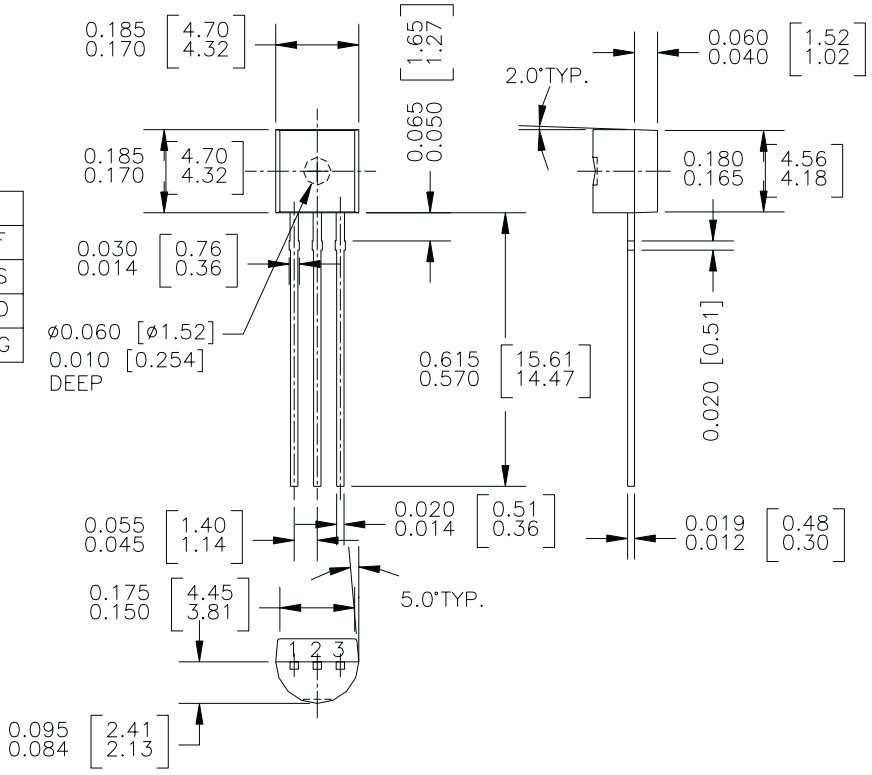
Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.1977

TO−92 (92,94,96)

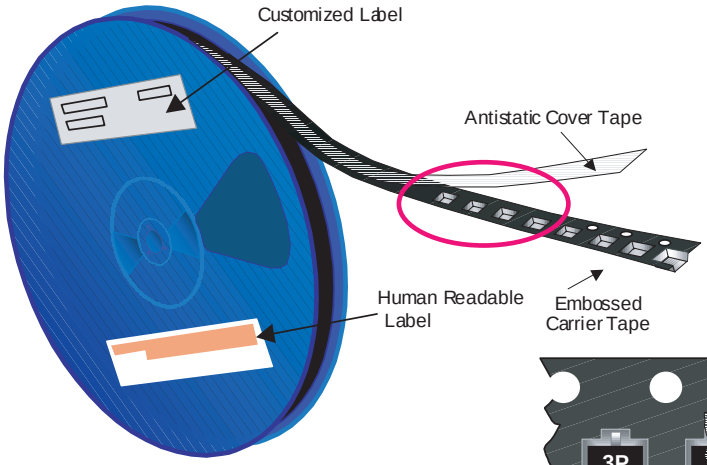
PIN	92		94		96	
	B	F	B	F	B	F
1	E	D	E	D	B	S
2	B	S	C	G	E	D
3	C	G	B	S	C	G



SOT-23 Tape and Reel Data and Package Dimensions

FAIRCHILD SEMICONDUCTOR™

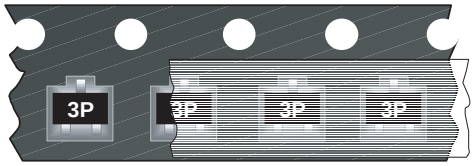
SOT-23 Packaging Configuration: Figure 10



Packaging Description:

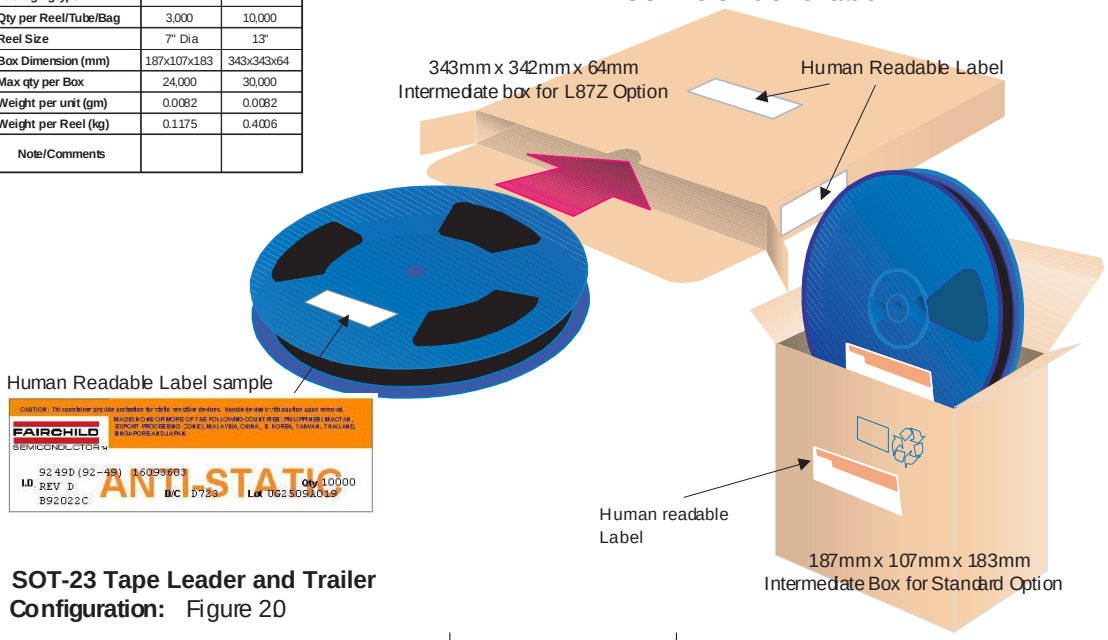
SOT-23 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 177cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 10,000 units per 13" or 330cm diameter reel. This and some other options are described in the Packaging Information table.

These full reels are individually labeled and placed inside a standard intermediate made of recyclable corrugated brown paper with a Fairchild logo printing. One pizza box contains eight reels maximum. And these intermediate boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

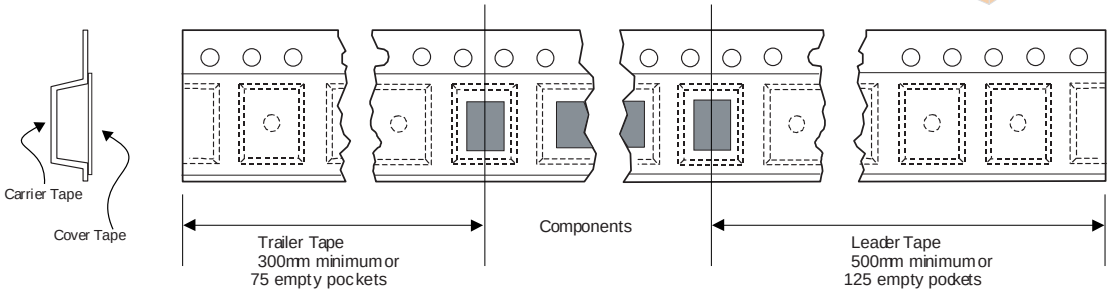


SOT-23 Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	187x107x183	343x343x64
Max qty per Box	24,000	30,000
Weight per unit (gm)	0.0082	0.0082
Weight per Reel (kg)	0.1175	0.4006
Note/Comments		

SOT-23 Unit Orientation

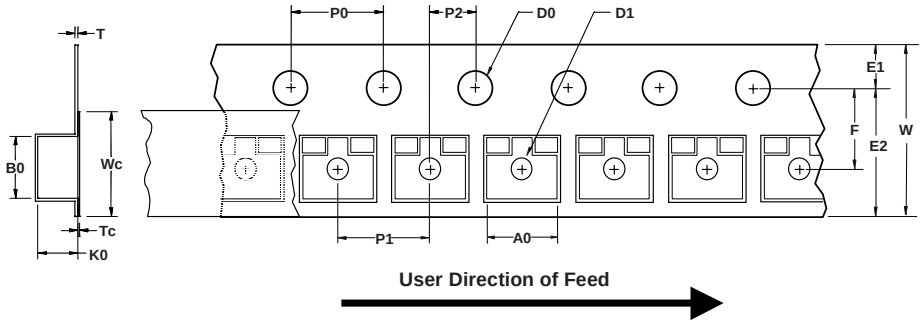


SOT-23 Tape Leader and Trailer Configuration: Figure 20



SOT-23 Tape and Reel Data and Package Dimensions, continued

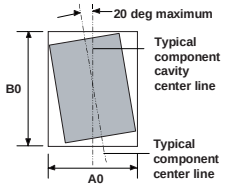
SOT-23 Embossed Carrier Tape
Configuration: Figure 3.0



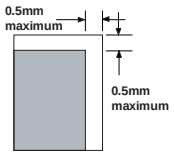
Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SOT-23 (8mm)	3.15 +/-0.10	2.77 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.30 +/-0.10	0.228 +/-0.013	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Sketch A (Side or Front Sectional View)
Component Rotation

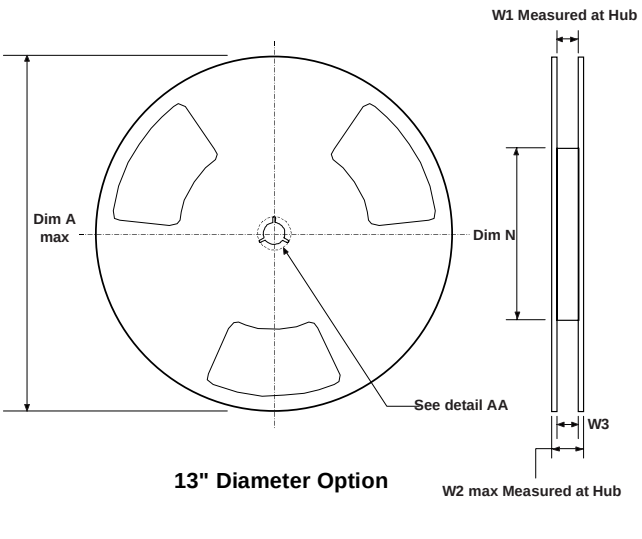


Sketch B (Top View)
Component Rotation

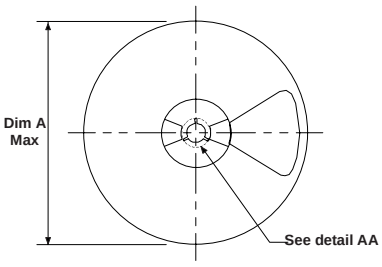


Sketch C (Top View)
Component lateral movement

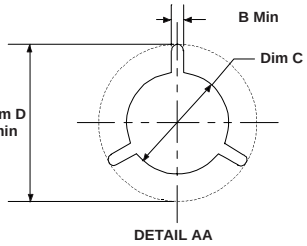
SOT-23 Reel Configuration: Figure 4.0



13" Diameter Option



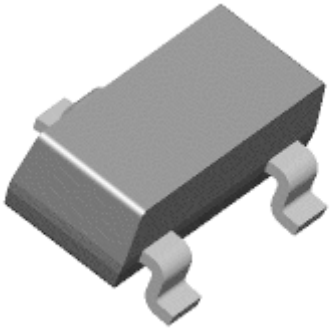
7" Diameter Option

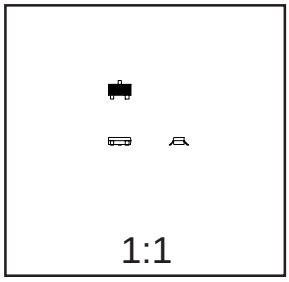


Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9

SOT-23 Tape and Reel Data and Package Dimensions, continued

SOT-23 (FS PKG Code 49)

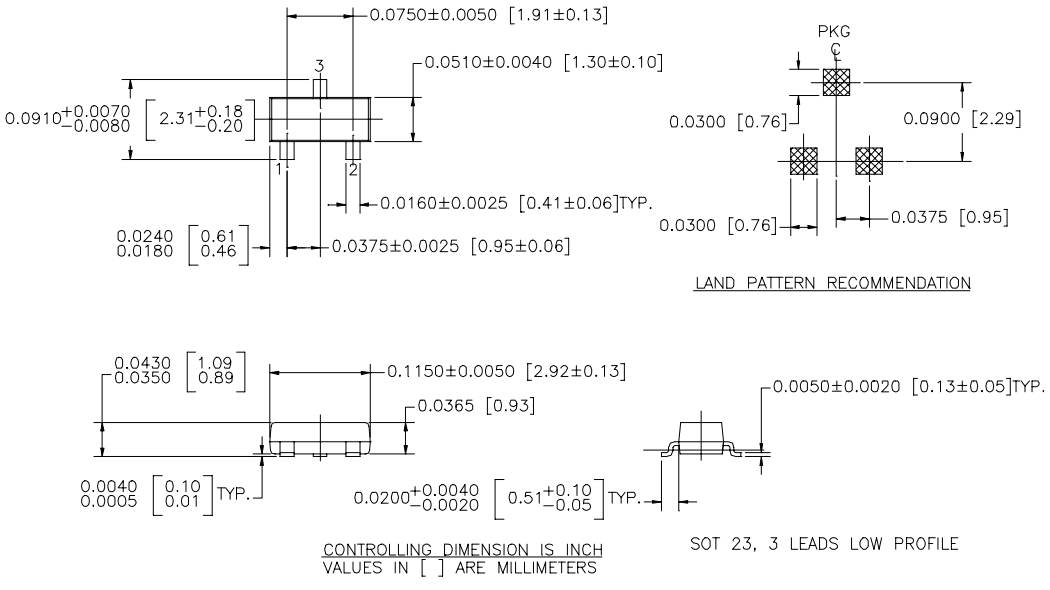




Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0082



NOTE : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH 150 MICROINCHES / 3.81 MICROMETERS MINIMUM TIN / LEAD (SOLDER) ON ALLOY 42
2. REFERENCE JEDEC REGISTRATION TO−236, VARIATION AB, ISSUE G, DATED JUL 1993

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