

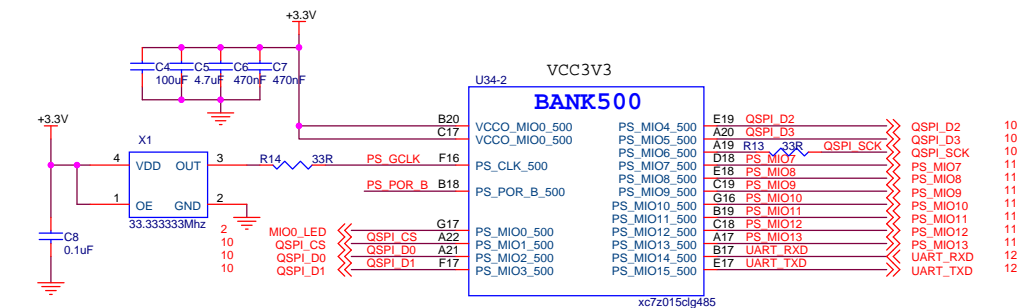
BOOT OPTION

PS MIO8
QSPI D0
QSPI D1
QSPI SCK
PS MIO7

SW1
SW DIP-2

QSPI D3
QSPI D2

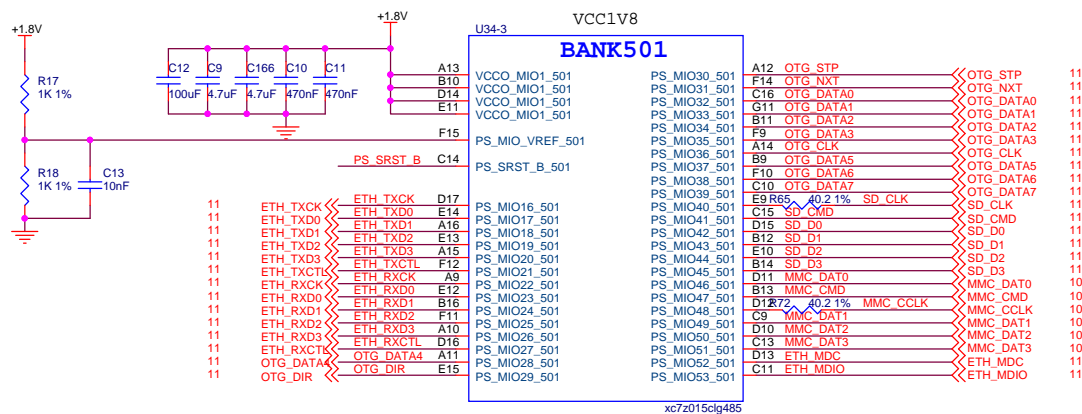
Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

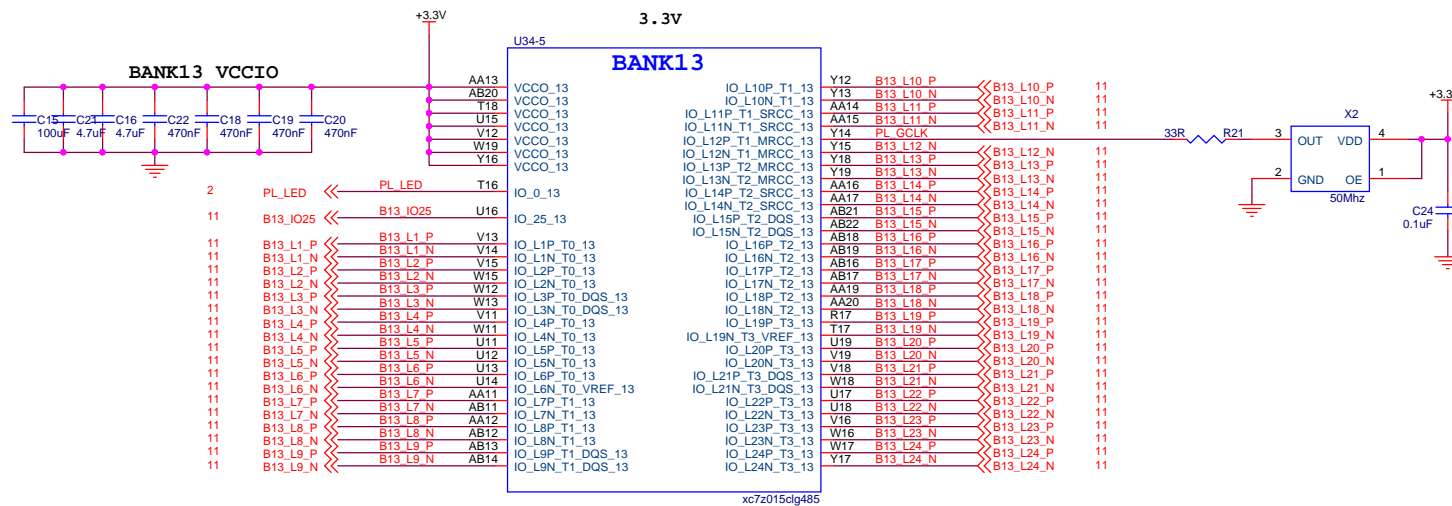


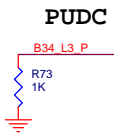
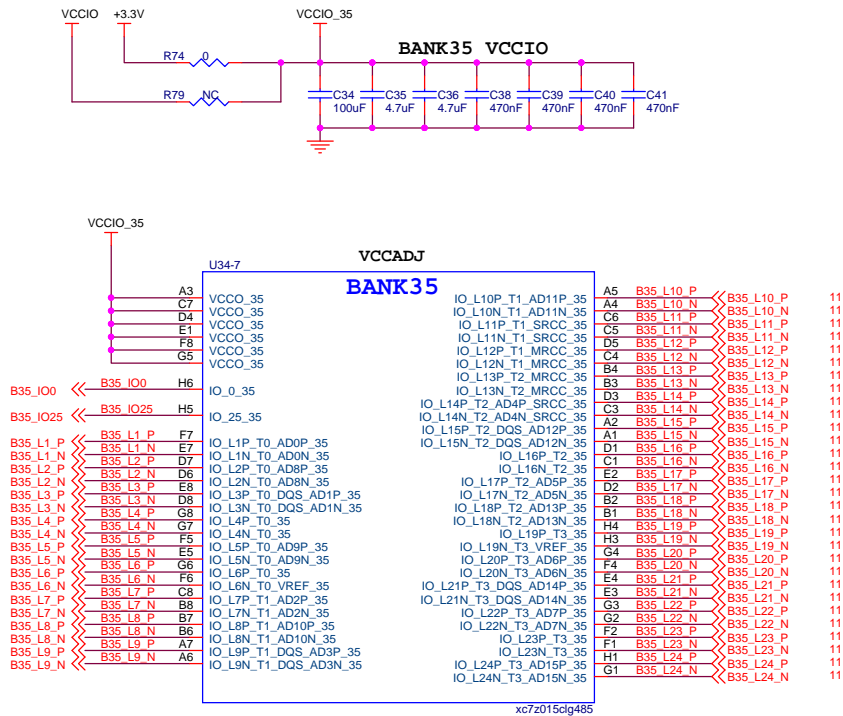
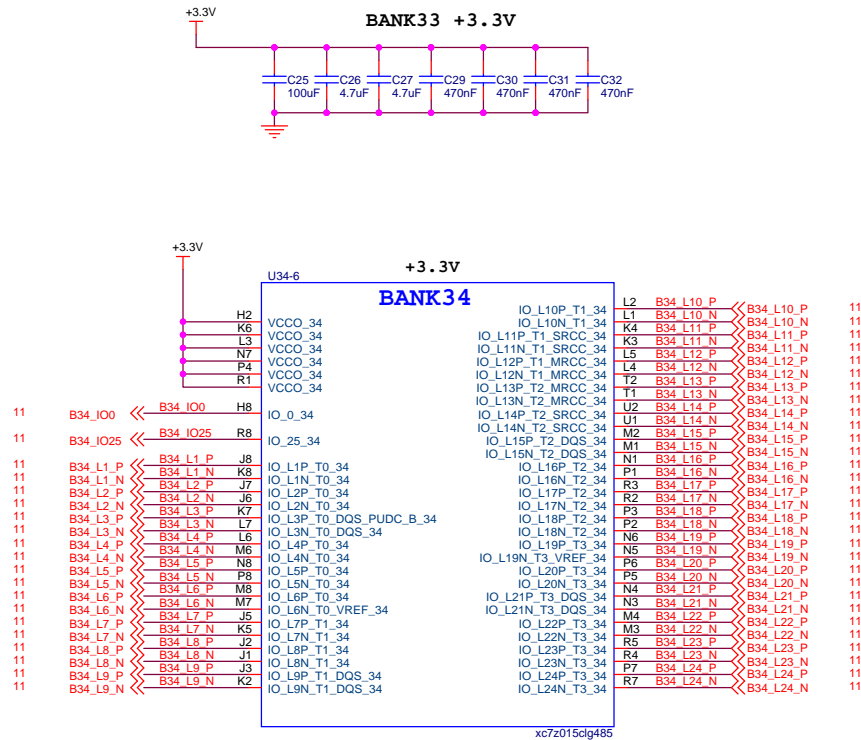
POWER ON RESET

The diagram illustrates a Power On Reset (POR) circuit. The central component is the TCM811TERCTR chip (U3). Its pins are configured as follows:

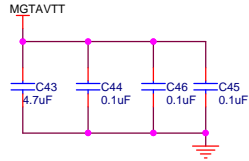
- Pin 1 (#MR):** Connected to ground.
- Pin 2 (VDD):** Connected to a +3.3V supply through a 0.1uF capacitor (C14).
- Pin 3 (#RESET):** Connected to a push-button switch labeled KEY1.
- Pin 4 (GND):** Connected to ground.
- Pin 5 (#RESET):** Connected to a +3.3V supply through a 4.7K resistor (R19) and to the output signal PS_POR_B.



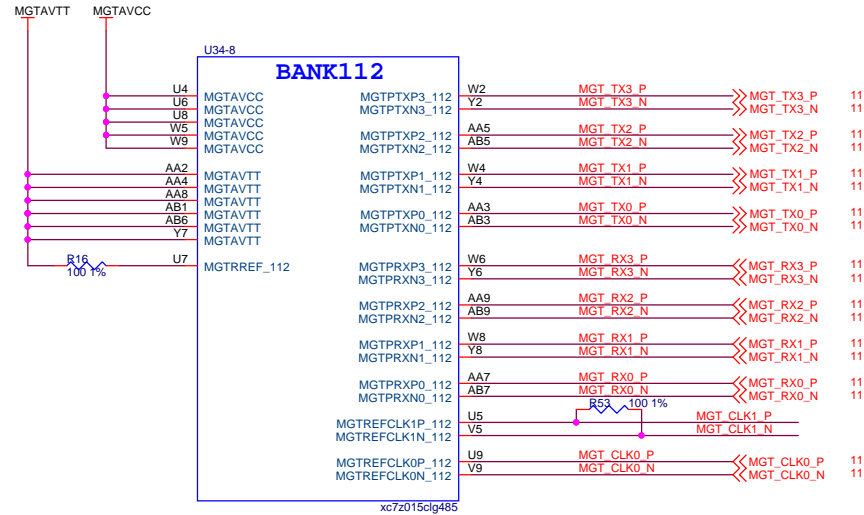
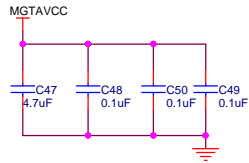




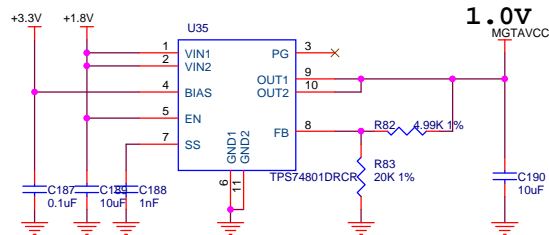
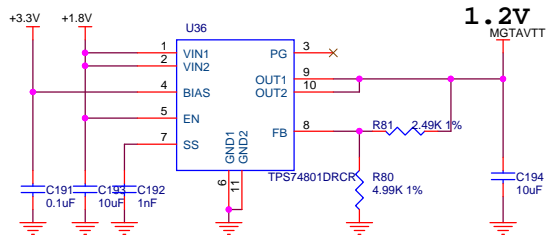
MGTAVTT 4.7uF(1) 0.1uF(2)



MGTAVCC 4.7uF(1) 0.1uF(2)

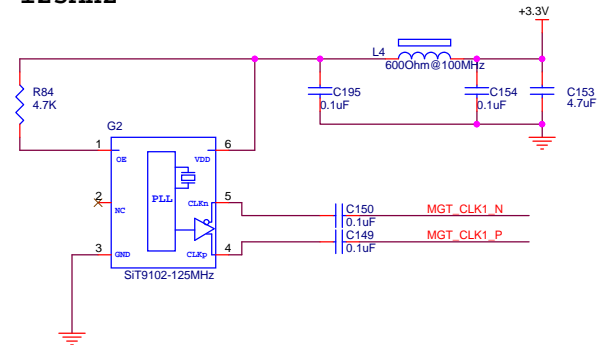


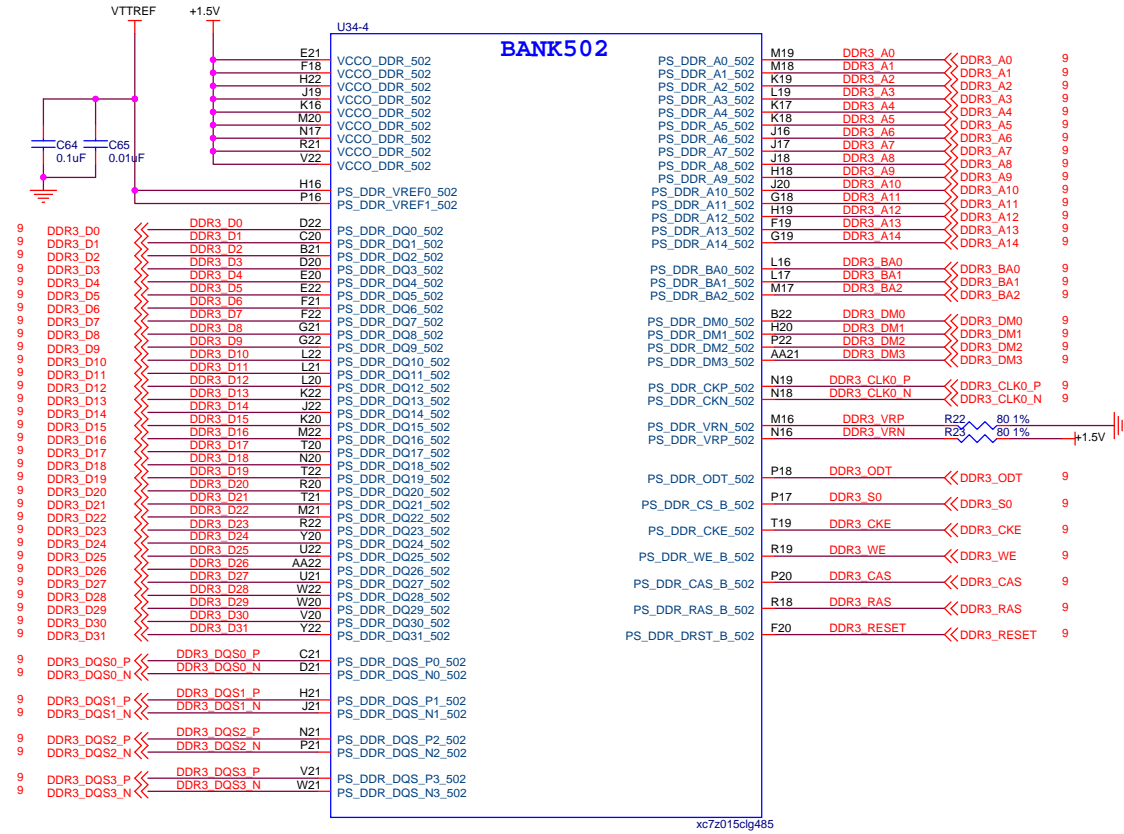
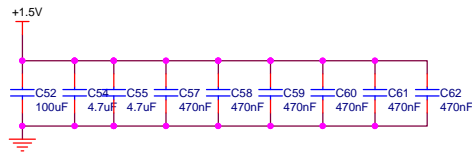
POWER ON: VCCINT(1.0V)->VMGTAVCC(1.0V)->VMGTAVTT(1.2V)

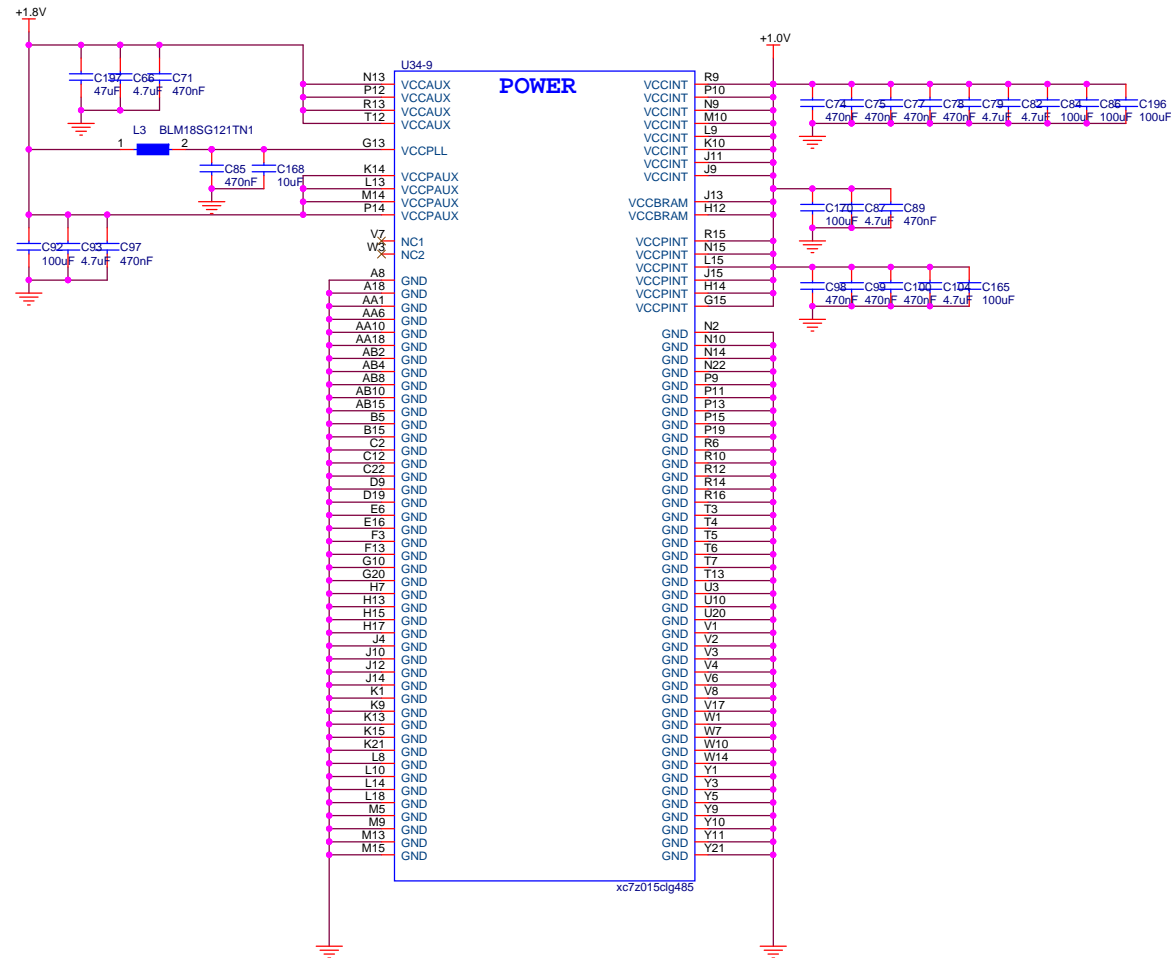


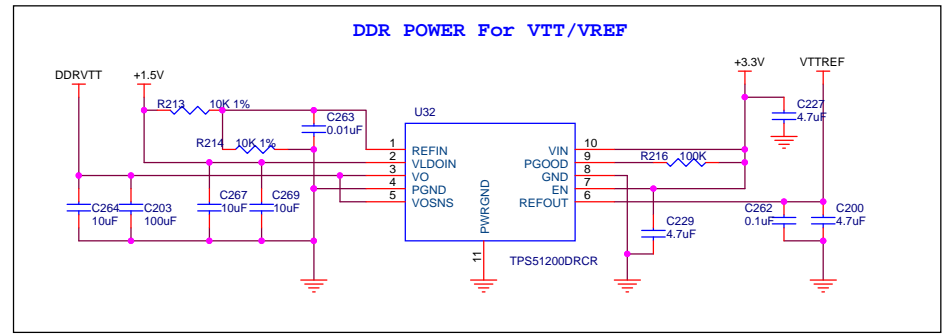
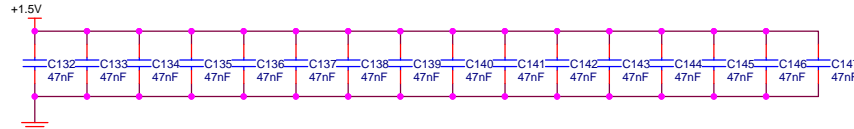
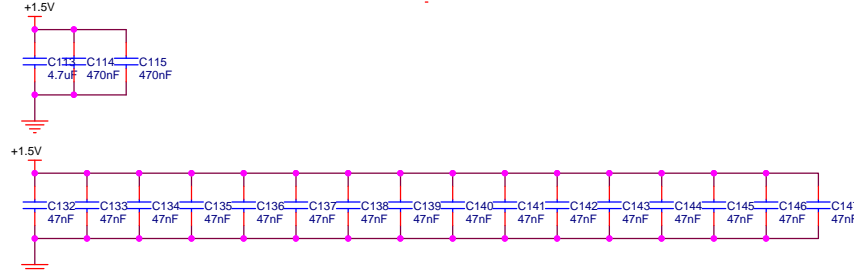
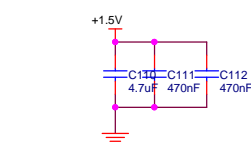
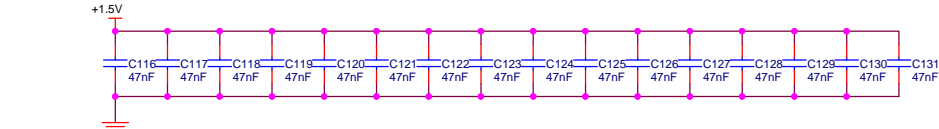
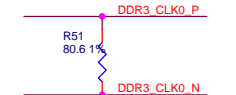
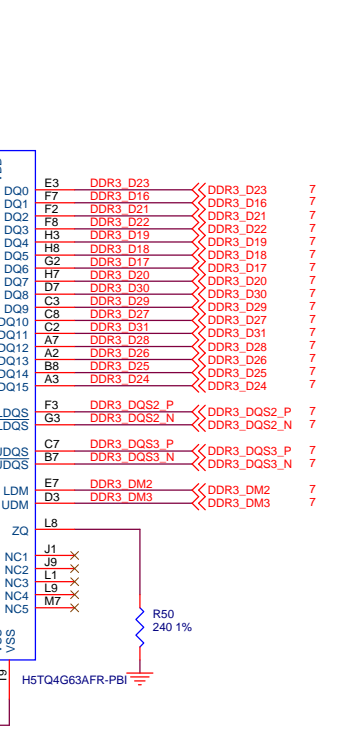
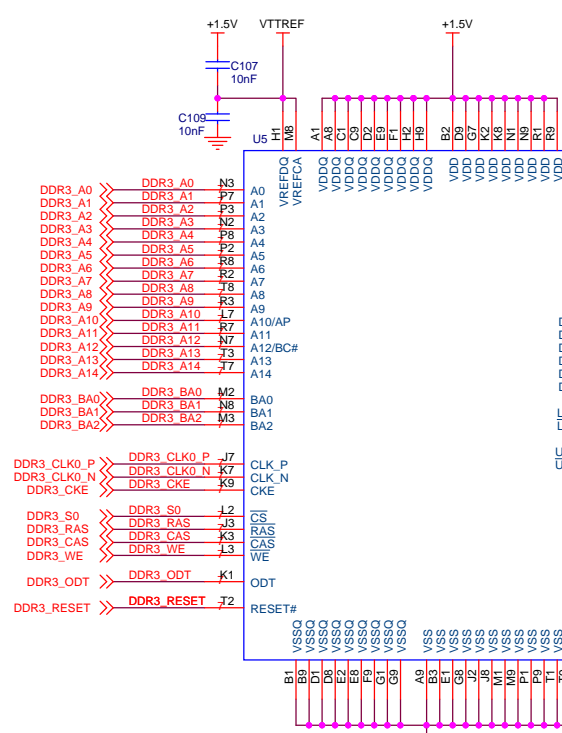
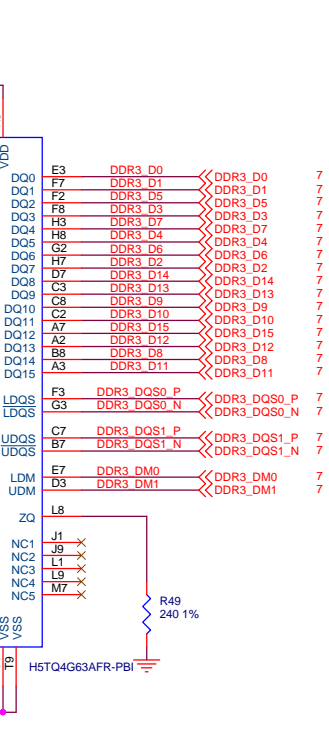
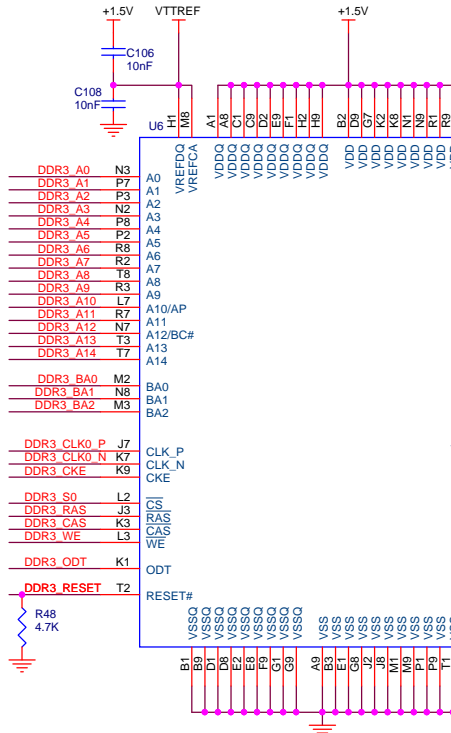
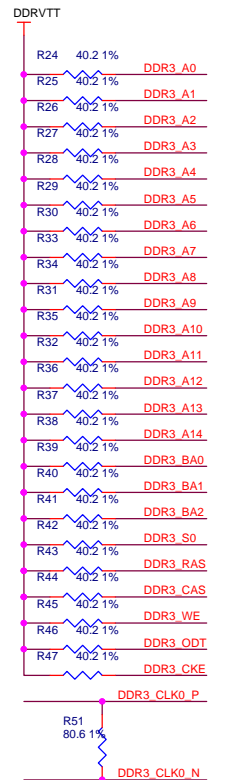
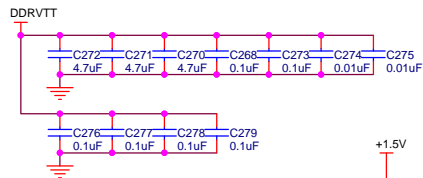
GTP CLOCK

125MHz

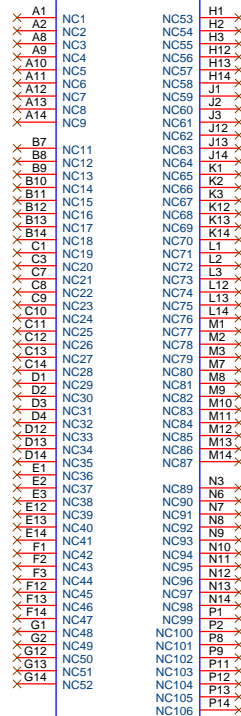
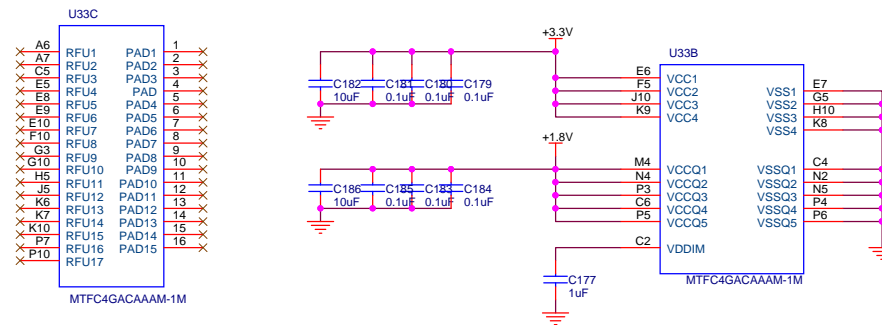







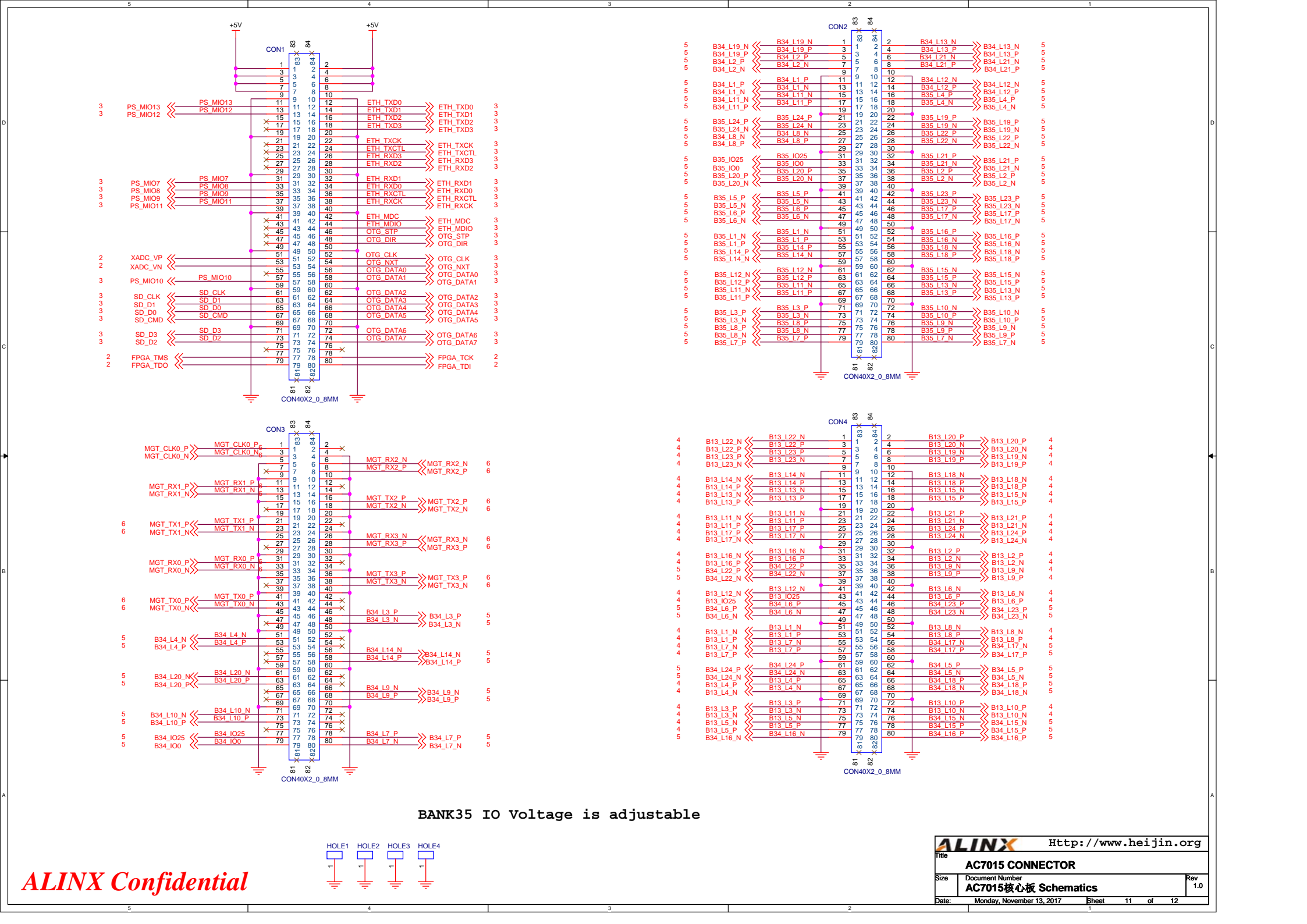
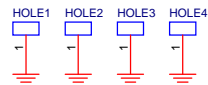


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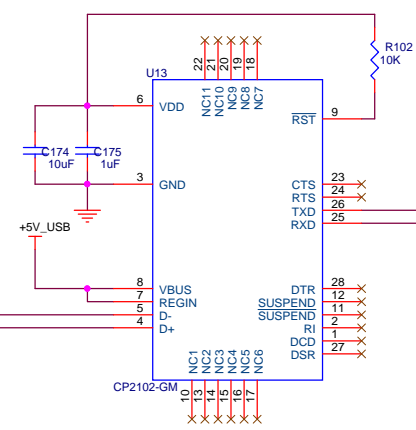
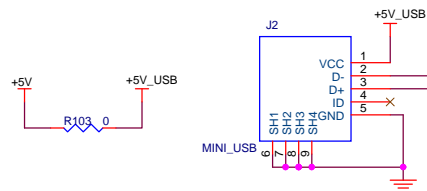


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BANK35 IO Voltage is adjustable



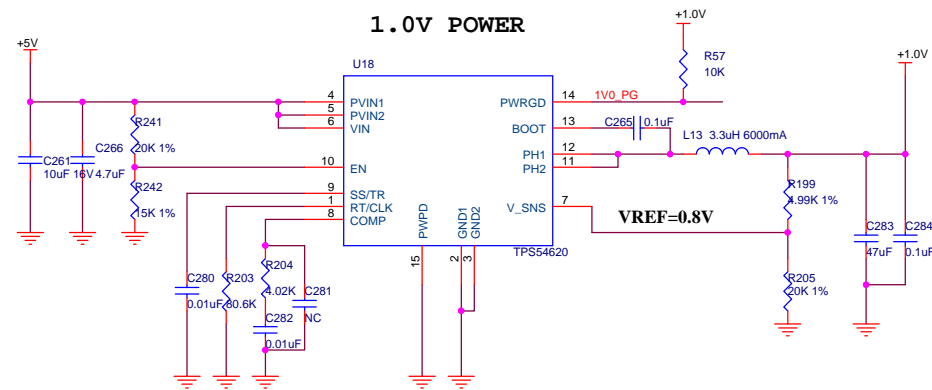
USB Uart



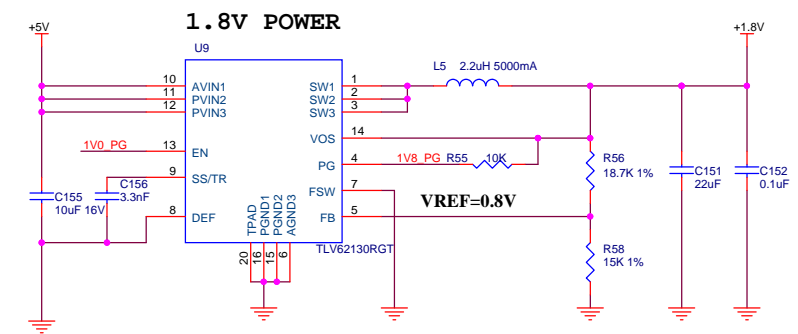
Power On Sequence:

1.0V -> 1.8V -> 1.5 V/3.3V -> VCCIO

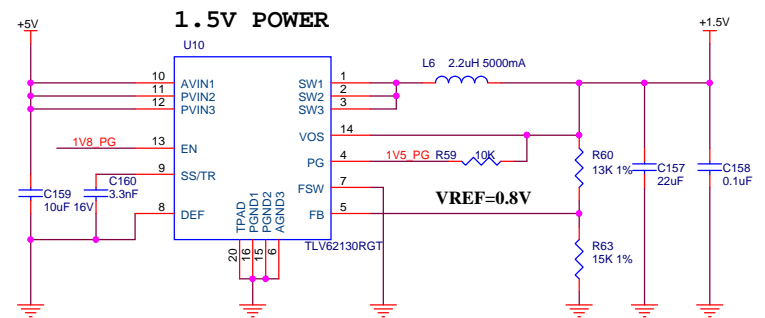
1.0V POWER



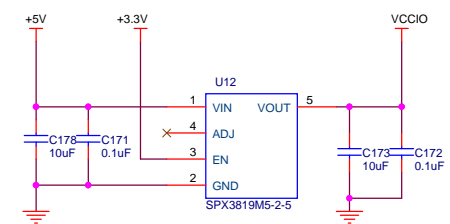
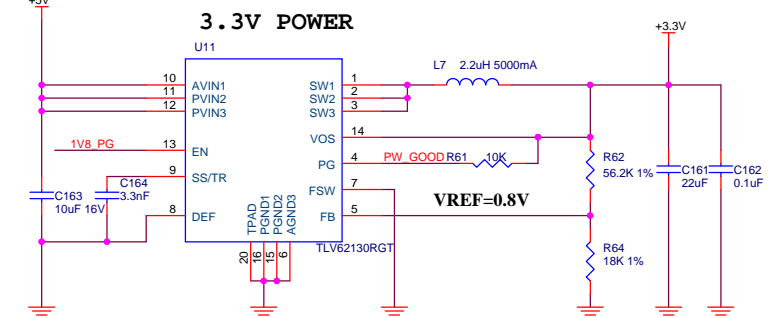
1.8V POWER



1.5V POWER



3.3V POWER



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