ALINX FPGA BOARD

AX7015

User Manual

ALINX

Revsion History:

Revision	Description
1.0	First Release

Development Environment:
Vivado 2017.4 is from Xilinx website
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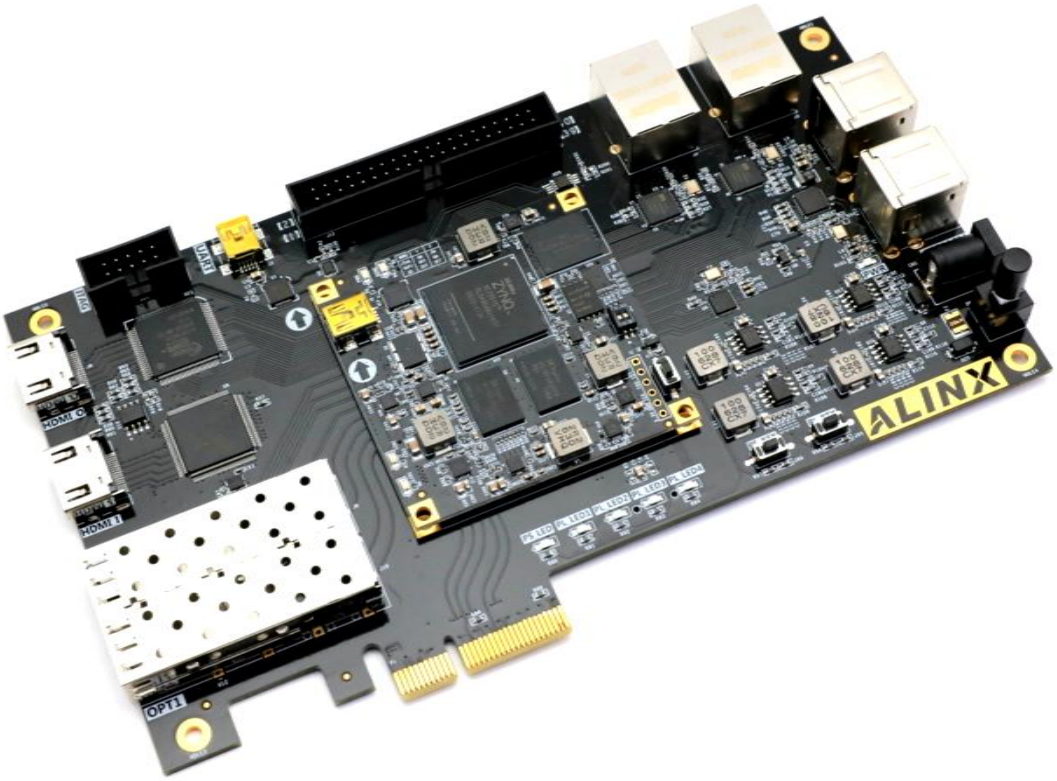
Contents

The AX7015 FPGA Development Board uses the core board and the expansion board mode, to facilitate the user's secondary development and utilization of the core board. The core board uses XILINX Zynq7000 series XC7Z015, which uses the ARM+FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. In addition, the core board contains 1GB DDR3 SDRAM, an 8GB eMMC memory and a 256Mb QSPI FLASH.
In the expansion board design, we have expanded the user's rich peripheral interfaces, such as 1 PCIE X2 interface, 2 optical interfaces, 2 Gigabit Ethernet interfaces, 4 USB2.0 HOST interfaces, 1 HDMI input interface, 1 HDMI output interface, 1 UART serial interface, 1 SD card interface, a 40-pin expansion interface, etc., to meet the user's various high-speed data exchange, data storage, video transmission processing and industrial control requirements. I believe that such a product is very suitable for ZYNQ development students, engineers and other groups.



Overview

The entire structure of the development board is designed using the core board + expansion board model. High-speed board-to-board connector connections are used between the core board and the expansion board.
The core board is mainly composed of the smallest system of ZYNQ7015 + 2 DDR3 + eMMC + QSPI FLASH and assumes the high-speed data processing and storage functions of the ZYNQ system. The data width between the ZYNQ7015 and the two DDR3s is 32 bits, and the capacity of two DDR3 chips Up to 1GB. The 8GB eMMC FLASH memory chip and the 256Mb QSPI FLASH are used to statically store the ZYNQ operating system, file system, and user data. Users can select different boot modes through the DIP switch on the core board. ZYNQ7015 uses Xilinx zynq7000 series chip, model XC7Z015-2CLG485I. ZYNQ7015 can be divided into processor system part Processor System (PS) and programmable logic part Programmable Logic (PL).
The Expansion Board expands the rich peripheral interfaces for the core board, including one PCIE X2 interface, two optical interfaces, two Gigabit Ethernet interfaces, four USB2.0 HOST interfaces, one HDMI input interface, and one HDMI output interface. , 1 UART serial interface, 1 SD card interface, 1 40-pin expansion interface and some key LED.
The following figure shows the structure of the entire development system:

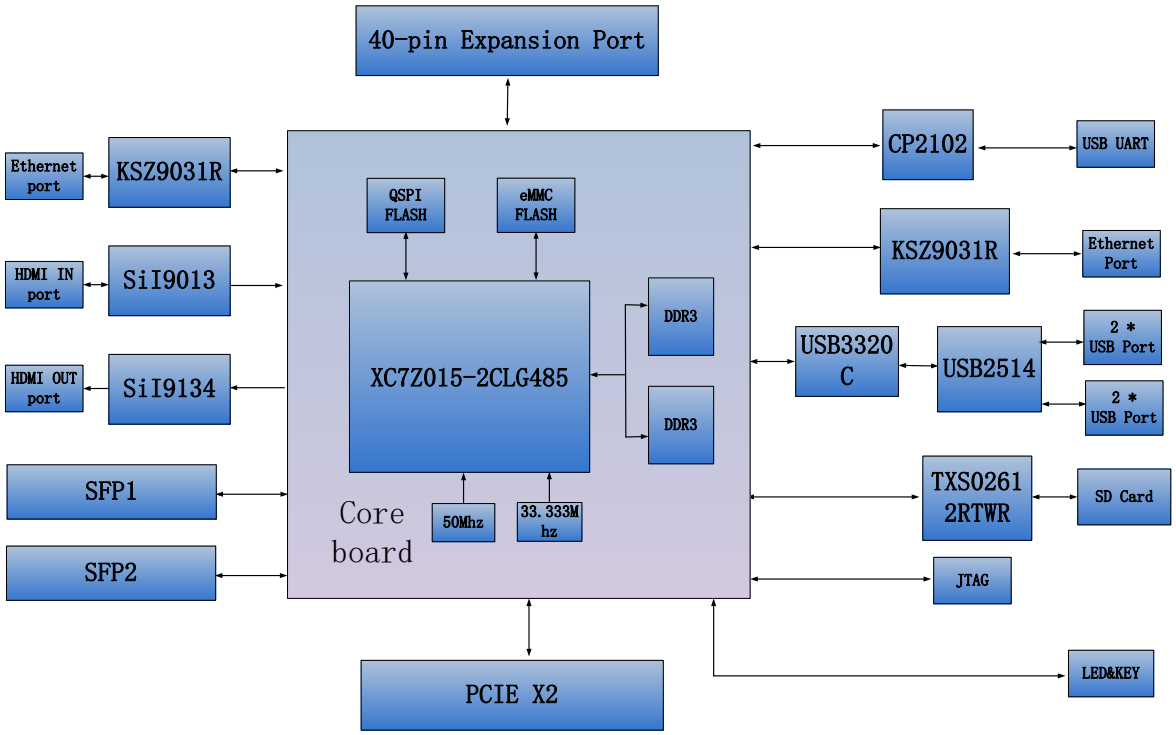


Figure1-1

From Figure 1-1, we can see the interfaces and functions that our development platform.

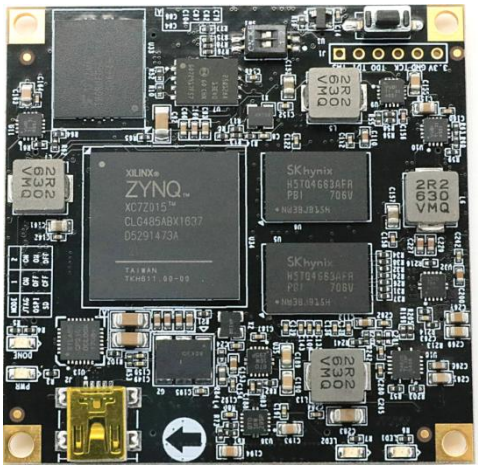
- XILINX XC7Z015-2CLG485I
- 1GB DDR3

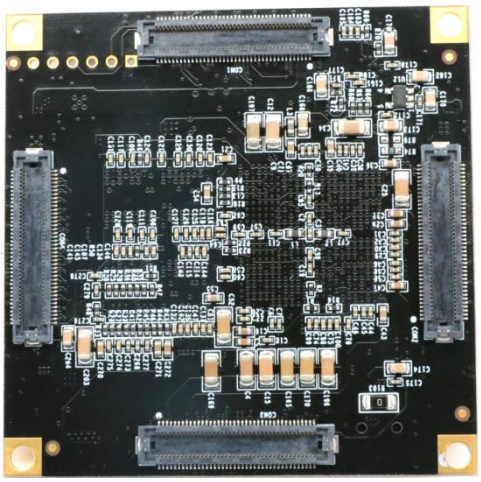
  - 8GB eMMC FLASH
  - 256Mbit QSPI FLASH
- PL side 50MHz active crystal and 125M differential crystal, PS side 33.33MHz active crystal
- Support PCI Express 2.0 standard, provide standard PCIE X2 high-speed data transmission interface, single channel communication rate up to 5GBaud.
- The 2 high-speed transceiver of ZYNQ's GTP transceiver is connected to the transmission and reception of two optical modules to implement two high-speed optical fiber communication interfaces. Each optical fiber data communication receives and transmits at up to 6.25 Gb/s.
- 2 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices. The network interface chip uses Micrel's KSZ9031 industrial grade GPHY chip. One Ethernet is connected to the PS side of the ZYNQ chip, and one Ethernet is connected to the PL side of the ZYNQ chip.
- 1 HDMI video output interface, we have chosen Silion Image's SIL9134 HDMI encoding chip, supports up to 1080P@60Hz output, supports 3D output.
- 1 HDMI video input interface, we have chosen Silion Image's SIL9013 HDMI decoding chip, supports up to 1080P@60Hz input, supports different formats of data input.
- 4 USB HOST interface through the USB Hub chip to connect external USB slave devices such as mouse, keyboard, U disk, etc. The USB interface uses a flat USB interface (USB Type A).
- 2 Uart to USB interface for communication with the computer for user debugging. One way is on the core board, the core board is used for independent work, and one is on the bottom board. The whole board is used for debugging. The serial chip adopts USB-UAR chip of Silicon Labs CP2102GM, USB interface adopts MINI USB interface.
  - 1 Micro SD card slot for storing operating system images and file systems.
- 1 40-pin 2.54mm pitch expansion port that can be connected to various modules of black gold (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port includes one 5V power supply, two 3.3V power supplies, three grounds, and 34 IO ports.
- 1 10-pin 2.54mm standard JTAG port for downloading and debugging of FPGA programs. The user can debug and download the ZYNQ system through the XILINX Downloader.
- 10 LEDs, 4 on the core board and 6 on the bottom board. 1 power indicator on the core board; 1 DONE configuration indicator; 1 user indicators. There is 1 power indicator and 5 user indicators on the backplane.
  - 3 buttons, 1 reset button on the core board, 2 user buttons on the bottom board.

Core Board

1. Overview

The core board (AC7015) is based on the XC7Z015-2CLG485I from Xilinx ZYNQ7000 series. Zynq's PS side integrates two ARM CortexTM-A9 processors, an AMBA® interconnect, internal memory, external memory interfaces, and peripherals. The FPGA inside ZYNQ chip contains rich programmable logic unit, DSP and internal RAM.
This core board uses two SK Hynix H5TQ4G63AFR-PBI DDR3 chips, each with a DDR capacity of 4 Gbits; two DDR chips combined into a 32-bit data bus width, and a read/write data clock between ZYNQ and DDR3. The data frequency up to 1066Mhz; This configuration can meet the system's high bandwidth data processing needs.
In order to connect to the backplane, the four board-to-board connectors of this core board extend the PS-side USB interface, Gigabit Ethernet interface, SD card interface and other remaining MIO interfaces; it also extends the 4 pairs of high-speed ZYNQ Transceiver GTP interface; and almost all IO ports (84) of BANK13, BAN34, and BANK35 on the PL side, where the IO level of BANK35 can be modified by replacing the LDO chip on the core board to meet the user's need for a level interface. Claim. For users who need a lot of IO, this core board will be a good choice. And the IO connection part, ZYNQ chip to interface between the wiring to do the same length and differential processing, and the core board size is only 60 * 60 (mm), for secondary development, is very suitable.





2. ZYNQ

The development board uses Xilinx Zynq 7000 series chip, model XC7Z015-2CLG485I. The chip's PS side integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces, and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO and so on. The PS can operate independently and start on power-up or reset. The overall

block diagram of the ZYNQ7000 chip is shown in Figure 2-1

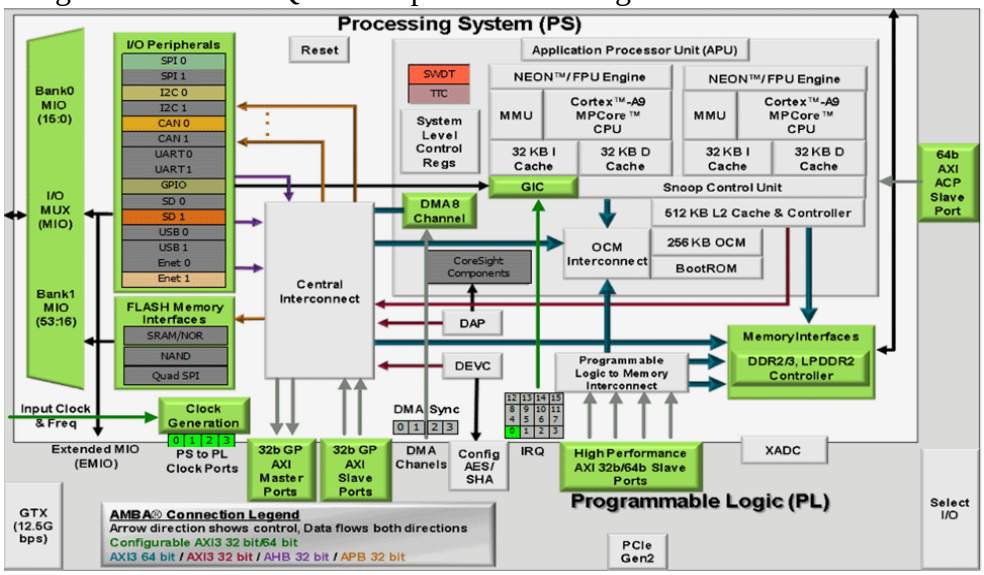


Figure 2-1

The main parameters of the PS system part are as follows:
- Application processor based on ARM dual-core CortexA9, ARM-v7 architecture up to 766MHz
- 32KB Level 1 instruction and data cache per CPU, 512KB Level 2 cache shared by 2 CPUs
- On-chip boot ROM and 256KB on-chip RAM
- External memory interface supporting 16/32 bit DDR2 and DDR3 interfaces
- Two Gigabit LAN Support: Divergent-Aggregate DMA, GMII, RGMII, SGMII Interfaces
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD card, SDIO, MMC compatible controllers
- 2 SPIs, 2 UARTs, 2 I2C interfaces
- 4 sets of 32bit GPIO, 54 (32+22) as PS system IO, 64 connects to PL
- High-bandwidth connection within PS and PS to PL

The main parameters of the PL logic section are as follows:
Logical unit Logic Cells: 74K
Lookup Table LUTs: 46,200
Flip-flops: 92,400
Multiplier 18x25MACCs:160
Block RAM: 3.3Mb;
4-way high-speed GTP transceiver supporting PCIE Gen2 X4
2 AD converters for on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS
The XC7Z015-2CLG485I chip has a speed grade of -2, an industrial grade, and is packaged as a BGA484 with a pin pitch of 0.8mm. The specific chip model definition for the ZYNQ7000 series is shown in Figure 2-2.

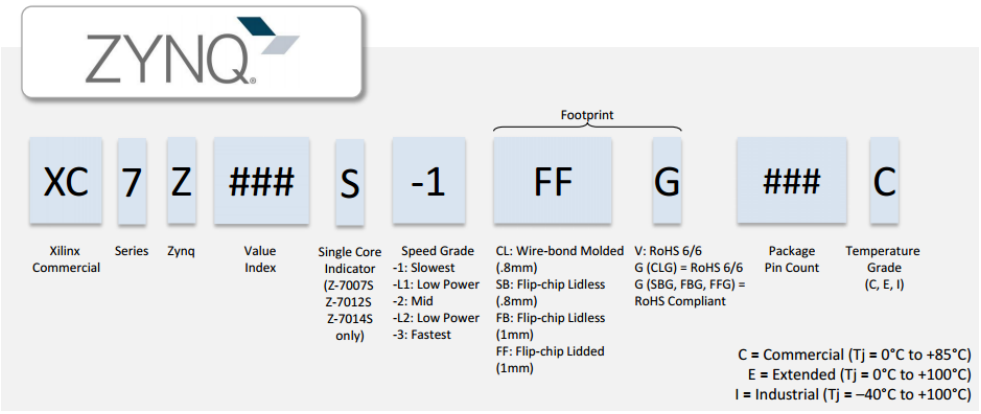


Figure 2-2

Figure 2-3 shows the physical map of the XC7Z015 chip used in the development board.

Figure 2-3

3. DDR3

The AC7015 core board is equipped with two SK Hynix DDR3 SDRAM chips (1GB in total), model number H5TQ4G63AFR-PBI. The bus width of DDR3 SDRAM is 32 bits in total. The maximum operating speed of DDR3 SDRAM is up to 533MHz (data rate 1066Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 502 of the ZYNQ processing system (PS). The specific configuration of DDR3 SDRAM is shown in Table 3-1.

Position	Model	Capacity	Factory
U5,U6	H5TQ4G63AFR-PBI	256M Byte*16bit	SKHynix

Table 3-1

The hardware design of DDR3 needs to strictly consider the signal integrity. We have fully considered the matching resistor/termination resistance, trace impedance control, and the length of the trace during the circuit design and PCB design to ensure the high-speed and stable operation of DDR3.

The hardware connection of DDR3 DRAM is shown in Figure 3-1.

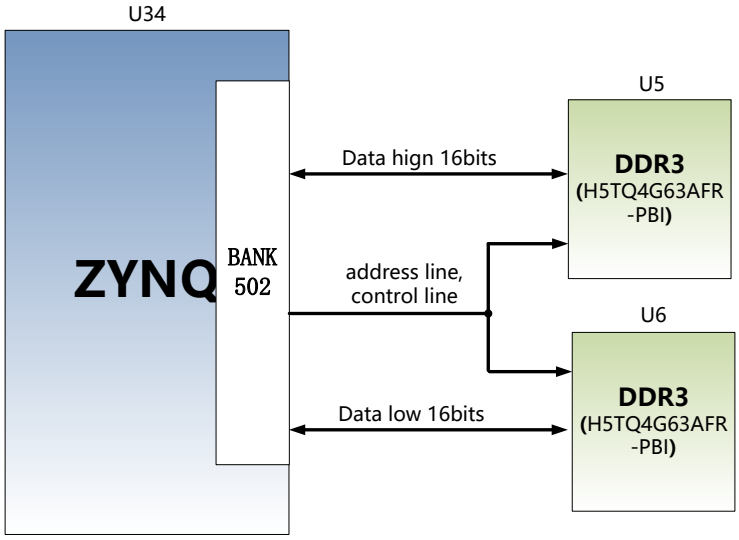


Figure 3-1

DDR3 DRAM Pin Assignment:

Signal Name	Pin Name	Pin Number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C21
DDR3_DQS0_N	PS_DDR_DQS_N0_502	D21
DDR3_DQS1_P	PS_DDR_DQS_P1_502	H21
DDR3_DQS1_N	PS_DDR_DQS_N1_502	J21
DDR3_DQS2_P	PS_DDR_DQS_P2_502	N21
DDR3_DQS2_N	PS_DDR_DQS_N2_502	P21
DDR3_DQS3_P	PS_DDR_DQS_P3_502	V21
DDR3_DQS4_N	PS_DDR_DQS_N3_502	W21
DDR3_D0	PS_DDR_DQ0_502	D22
DDR3_D1	PS_DDR_DQ1_502	C20
DDR3_D2	PS_DDR_DQ2_502	B21
DDR3_D3	PS_DDR_DQ3_502	D20
DDR3_D4	PS_DDR_DQ4_502	E20
DDR3_D5	PS_DDR_DQ5_502	E22
DDR3_D6	PS_DDR_DQ6_502	F21
DDR3_D7	PS_DDR_DQ7_502	F22
DDR3_D8	PS_DDR_DQ8_502	G21
DDR3_D9	PS_DDR_DQ9_502	G22
DDR3_D10	PS_DDR_DQ10_502	L22
DDR3_D11	PS_DDR_DQ11_502	L21
DDR3_D12	PS_DDR_DQ12_502	L20
DDR3_D13	PS_DDR_DQ13_502	K22
DDR3_D14	PS_DDR_DQ14_502	J22

DDR3_D15	PS_DDR_DQ15_502	K20
DDR3_D16	PS_DDR_DQ16_502	M22
DDR3_D17	PS_DDR_DQ17_502	T20
DDR3_D18	PS_DDR_DQ18_502	N20
DDR3_D19	PS_DDR_DQ19_502	T22
DDR3_D20	PS_DDR_DQ20_502	R20
DDR3_D21	PS_DDR_DQ21_502	T21
DDR3_D22	PS_DDR_DQ22_502	M21
DDR3_D23	PS_DDR_DQ23_502	R22
DDR3_D24	PS_DDR_DQ24_502	Y20
DDR3_D25	PS_DDR_DQ25_502	U22
DDR3_D26	PS_DDR_DQ26_502	AA22
DDR3_D27	PS_DDR_DQ27_502	U21
DDR3_D28	PS_DDR_DQ28_502	W22
DDR3_D29	PS_DDR_DQ29_502	W20
DDR3_D30	PS_DDR_DQ30_502	V20
DDR3_D31	PS_DDR_DQ31_502	Y22
DDR3_DM0	PS_DDR_DM0_502	B22
DDR3_DM1	PS_DDR_DM1_502	H20
DDR3_DM2	PS_DDR_DM2_502	P22
DDR3_DM3	PS_DDR_DM3_502	AA21
DDR3_A0	PS_DDR_A0_502	M19
DDR3_A1	PS_DDR_A1_502	M18
DDR3_A2	PS_DDR_A2_502	K19
DDR3_A3	PS_DDR_A3_502	L19
DDR3_A4	PS_DDR_A4_502	K17
DDR3_A5	PS_DDR_A5_502	K18
DDR3_A6	PS_DDR_A6_502	J16
DDR3_A7	PS_DDR_A7_502	J17
DDR3_A8	PS_DDR_A8_502	J18
DDR3_A9	PS_DDR_A9_502	H18
DDR3_A10	PS_DDR_A10_502	J20
DDR3_A11	PS_DDR_A11_502	G18
DDR3_A12	PS_DDR_A12_502	H19
DDR3_A13	PS_DDR_A13_502	F19
DDR3_A14	PS_DDR_A14_502	G19
DDR3_BA0	PS_DDR_BA0_502	L16
DDR3_BA1	PS_DDR_BA1_502	L17
DDR3_BA2	PS_DDR_BA2_502	M17
DDR3_S0	PS_DDR_CS_B_502	P17

DDR3_RAS	PS_DDR_RAS_B_502	R18
DDR3_CAS	PS_DDR_CAS_B_502	P20
DDR3_WE	PS_DDR_WE_B_502	R19
DDR3_ODT	PS_DDR_ODT_502	P18
DDR3_RESET	PS_DDR_DRST_B_502	F20
DDR3_CLK0_P	PS_DDR_CKP_502	N19
DDR3_CLK0_N	PS_DDR_CKN_502	N18
DDR3_CKE	PS_DDR_CKE_502	T19

4. QSPI Flash

The core board has a 256MBit Quad-SPI FLASH chip, model W25Q256FVEI, which uses a 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, in use, it can be used as the boot device of the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific model and related parameters of QSPI FLASH are shown in Table 4-1.

Position	Model	Capacity	Factory
U7	W25Q256FVEI	32M Byte	Winbond

Table 4-1

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 2-4-1 shows the QSPI Flash in the schematic.

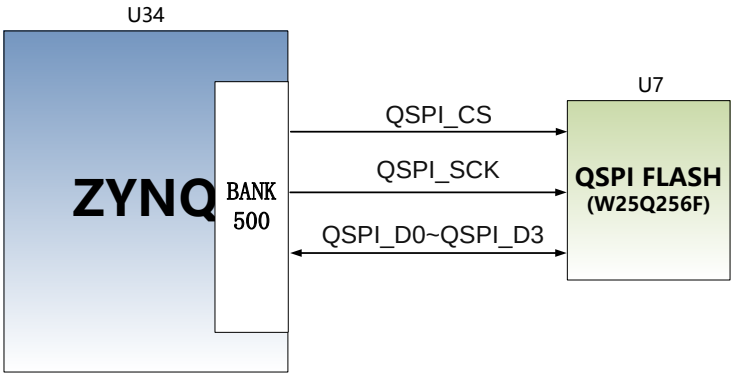


Figure 4-1

Pin Assignment:

Signal Name	Pin Name	Pin Number
QSPI_SCK	PS_MIO6_500	A19
QSPI_CS	PS_MIO1_500	A22
QSPI_D0	PS_MIO2_500	A21
QSPI_D1	PS_MIO3_500	F17
QSPI_D2	PS_MIO4_500	E19

QSPI_D3	PS_MIO5_500	A20

5. eMMC Flash

The core board have a large-capacity 8GB eMMC FLASH chip, model THGBMFG6C1LBAIL, which supports the HS-MMC interface of the JEDEC e-MMC V5.0 standard, and the level supports 1.8V or 3.3V. The data width of eMMC FLASH and ZYNQ connections is 4 bits. Due to the large capacity and non-volatile nature of eMMC FLASH, it can be used as a large-capacity storage device in the ZYNQ system, such as storing ARM applications, system files, and other user data files. The specific models and related parameters of eMMC FLASH are shown in Table 5-1.

eMMC Pin Assignment:

Position	Model	Capacity	Factory
U33	THGBMFG6C1LBAIL	8G Byte	TOSHIBA

Table 5-1

The eMMC FLASH is connected to the GPIO port of the BANK501 of the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the SD interface. Figure 5-1 shows the eMMC Flash in the schematic.

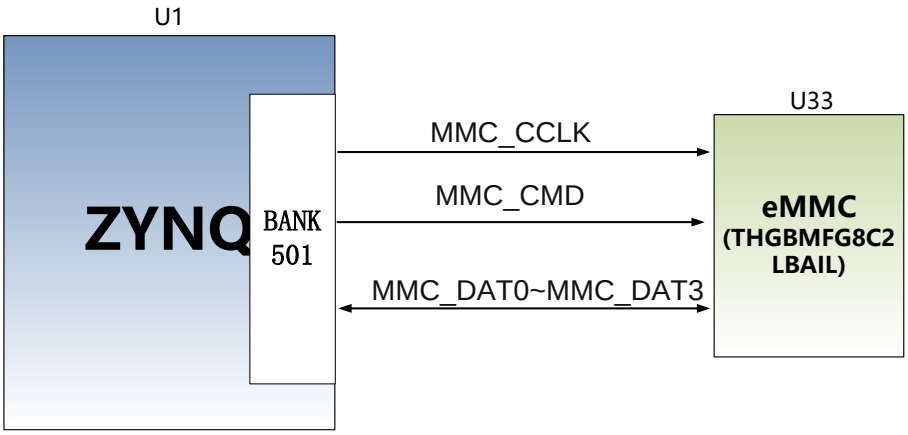


Figure 5-1

Pin Assignment:

Signal Name	Pin Name	Pin Number
MMC_CCLK	PS_MIO48_501	D12
MMC_CMD	PS_MIO47_501	B13
MMC_D0	PS_MIO46_501	D11
MMC_D1	PS_MIO49_501	C9
MMC_D2	PS_MIO50_501	D10
MMC_D3	PS_MIO51_501	C13

6. Clock source

The AC7015 core board provides active clocks for the PS system and the PL logic sections, respectively, so that the PS system and the PL logic can work independently.

PS system clock source

The ZYNQ chip provides a 33.333 MHz clock input to the PS section through the X1 crystal on the development board. The input of the clock is connected to the pins of PS_CLK_500 of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 6-1:

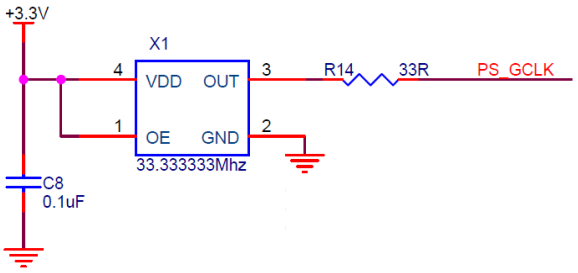


Figure 6-1

Clock pin assignment:

Signal Name	Pin
PS_GCLK	F16

PL system clock source

The AC7015 core board provides a single-ended 50MHz PL system clock source with 3.3V supply. The crystal output is connected to the global clock (MRCC) of the FPGA BANK13, which can be used to drive the user logic within the FPGA. The schematic of this clock source is shown in Figure 6-3.

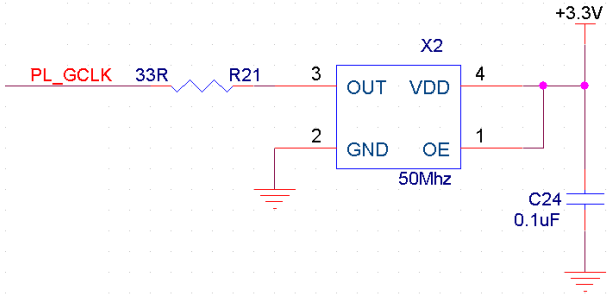


Figure 6-3

PL Clock pin assignment:

Signal Name	Pin
PL_GCLK	Y14

7. USB to Uart

For the AC7015 core board to work and debug separately, we have a Uart to USB interface for the core board. Used for power supply and debugging of the core board.

The conversion chip adopts the USB-UAR chip of Silicon Labs CP2102GM. The USB interface adopts the MINI USB interface. It can connect it to the USB port of the upper PC for independent power supply and serial port data communication using a USB cable.
A schematic diagram of USB Uart circuit design is shown in Figure 7-1.

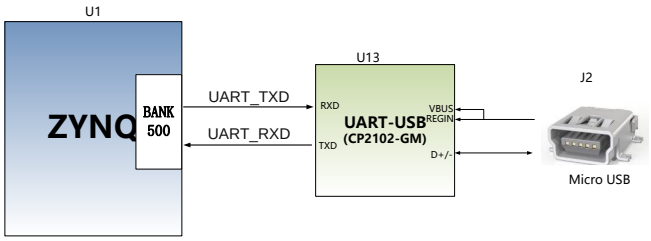


Figure7-1

Uart Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
UART_RXD	PS_MIO14_500	B17	Uart data output
UART_TXD	PS_MIO15_500	E17	Uart data input

8. LED

The AC7015 core board has four red LEDs, one of which is a power indicator (PWR), one is a configuration LED (DONE), and two are user LED (LED1~LED2). When the core board is powered up, the power indicator lights up; when the FPGA is configured, the configuration LED lights up. Two user LED lights One is connected to the MIO of the PS. One is connected to the IO of the PL. The user can control the light on and off through the program. When the voltage of the IO connected to the user LED lamp is high, the user LED light goes out when the connection is made. When the IO voltage is low, the user LED will be lit. The schematic diagram of the LED lamp hardware connection is shown in Figure 8-1.

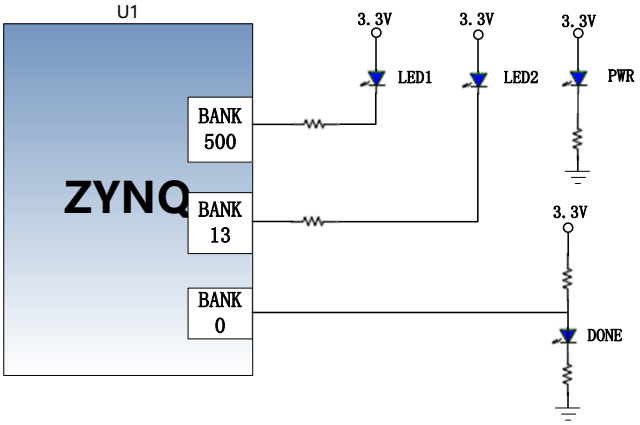


Figure 8-1

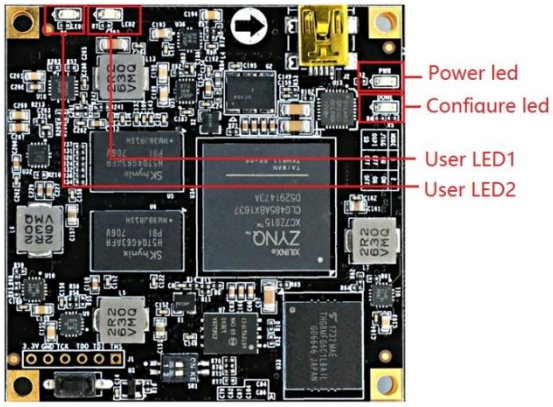


Figure 8-2

LED Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
MIO0_LED	PS_MIO0_500	G17	User LED1
PL_LED	IO_0_13	T16	User LED2

9. Reset Key

There is a reset button RESET and circuit on the core board of AC7015. The reset signal is connected to the PS reset pin of ZYNQ chip. Users can use this reset button to reset the ZYNQ system. Pressing the reset button will reset the chip to generate a low level reset signal to the ZYNQ chip. A schematic diagram of the reset button and reset chip connection is shown in Figure 9-1.

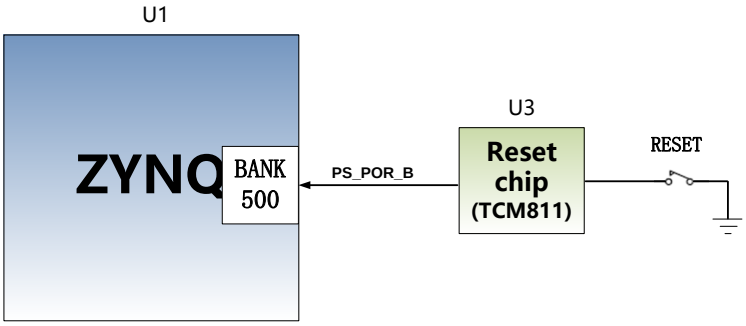


Figure 9-1

Reset Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PS_POR_B	PS_POR_B_500	B18	Reset Key

10. JTAG

On the AC7015 core board, we also reserved JTAG test socket J1 for JTAG download and debugging of the core board. Figure 10-1 is the schematic part of the JTAG port, which relates to TMS, TDI, TDO, and TCK. , GND, +3.3V These six signals.

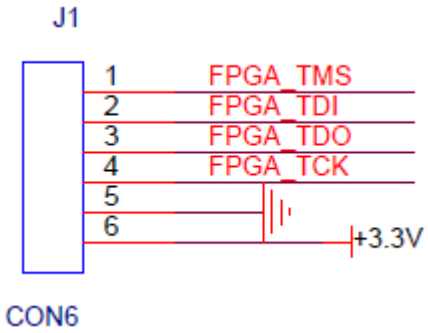


Figure 10-1

The JTAG interface J1 on the core board uses a 6-pin 2.54mm pitch single-row test hole. If the user needs JTAG connection debugging on the core board, it needs to weld 6-pin single row pins.

11. Start configuration

A 2-bit code switch SW1 is used on the AC7015 core board to configure the boot mode of the ZYNQ system. The AC7015 system development platform supports three startup modes. The three boot modes are JTAG debug mode, QSPI FLASH and SD

card boot mode. After the chip is powered on, the XC7Z015 detects the level of the responding MIO (MIO5 and MIO4) to determine which boot mode. Users can select different boot modes through the DIP switch SW1 on the core board. The SW1 startup mode is configured as shown in Table 11-1.

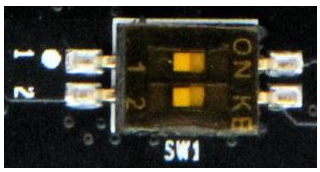
SW1	Position（1，2）	MIO5,MIO4 Level	Startup mode
	ON、ON	0、0	JTAG
	OFF、OFF	1、1	SD Card
	OFF、ON	1、0	QSPI FLASH

Table 11-1

12. Power

The power supply voltage of the AC7015 core board is DC5V. When it is used alone, power is supplied through the Mini USB interface. When the board is connected to the chassis, power is supplied through the chassis. Be careful not to supply power to the Mini USB and the chassis at the same time to avoid damage. The power supply design on the board is shown in Figure 12-1.

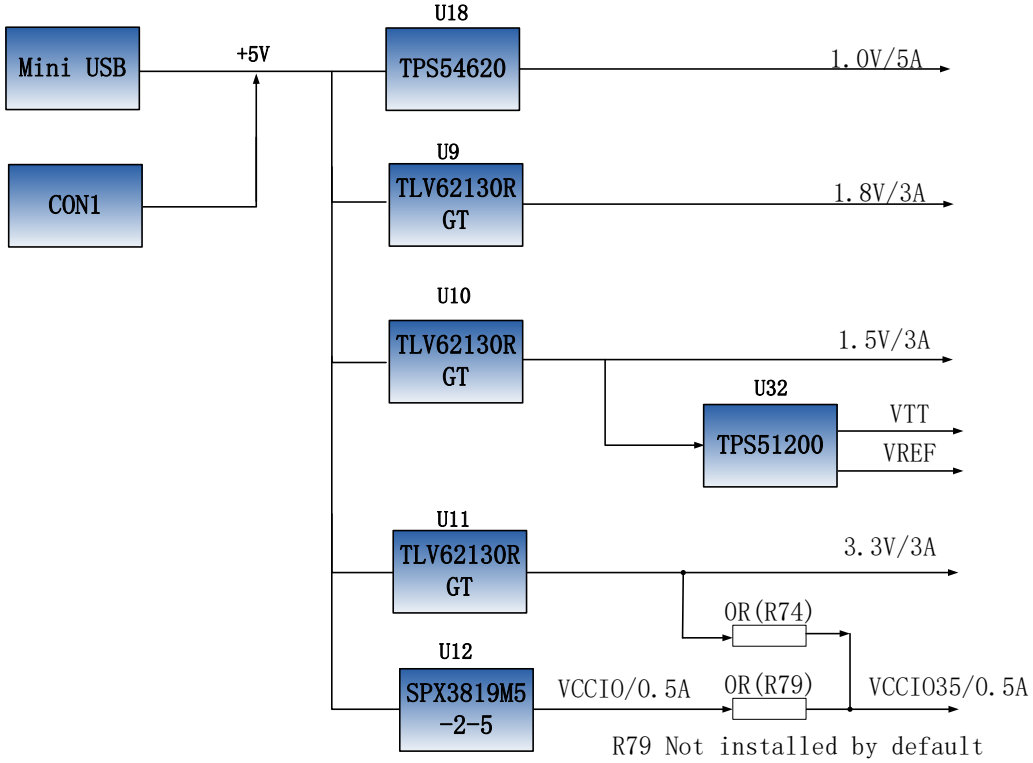


Figure 12-1

The development board is powered by +5V, and converted to +1.0V, +1.8V, +1.5V, +3.3V four-way power supply via four DC/DC power supply chips TPS54620 and TLV62130RGT. The +1.0V output current can be as high as 5A, and the other 3 The

power supply current is 3A. In addition, the VCCIO 2.5V power supply is generated by a LDO SPX3819M5-2-5. The VCCIO 2.5V power supply is mainly the BANK power reserved for the BANK35 of the FPGA. The user can select the BANK35 power supply through two 0-ohm resistors (R74, R79). R74 is installed on the default development board. The resistor of R79 is not installed, so the power supply of BANK35 is +3.3V. The user can replace the resistor so that the NK input and output of the BANK35 is a 2.5V voltage standard. 1.5V generates the VTT and VREF voltages required for DDR3 through TI's TPS51200. The functions of each power distribution are shown in the following table:

Power	Function
+1.0V	ZYNQ PS and PL section core voltage
+1.8V	ZYNQ PS and PL partial auxiliary voltage, BANK501 IO voltage, eMMC
+3.3V	ZYNQ Bank0,Bank500，Bank13，Bank34 的 VCCIO, QSIP FLASH, Clock
+1.5V	DDR3, ZYNQ Bank501
VREF, VTT（+0.75V）	DDR3
VCCIO(+2.5V)	Reserved for ZYNQ Bank35

Because the power supply of the ZYNQ FPGA has the order of power on, we have designed according to the power requirements of the chip in the circuit design, and the power supply is +1.0V->+1.8V->(+1.5 V, +3.3V, VCCIO) The circuit design of the chip ensures the normal operation of the chip.
The power circuit of the AC7015 core board is shown in Figure 12-2 below.

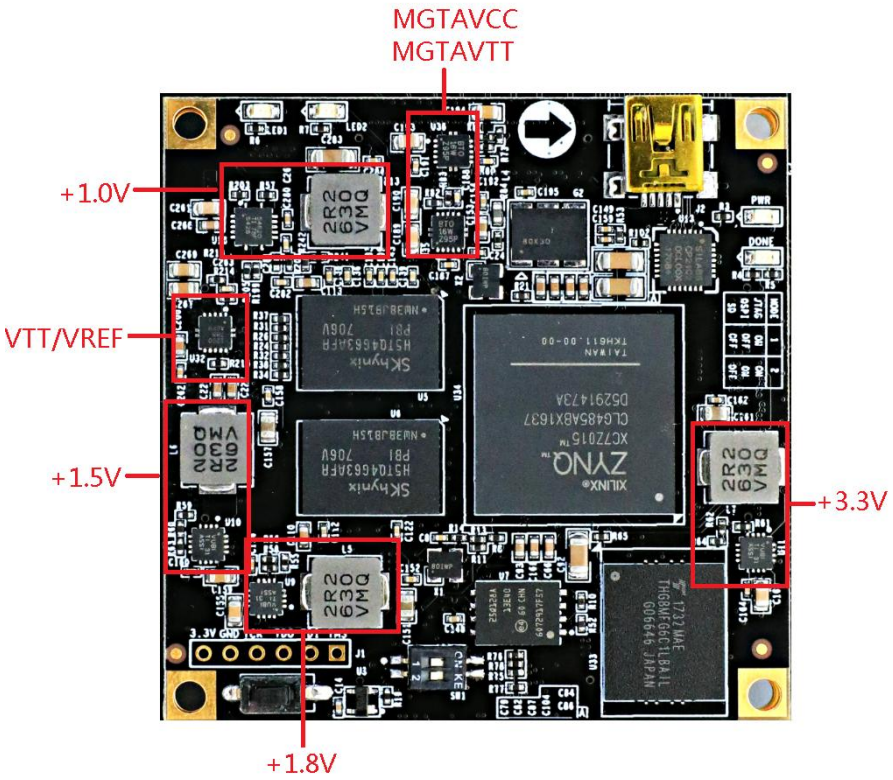
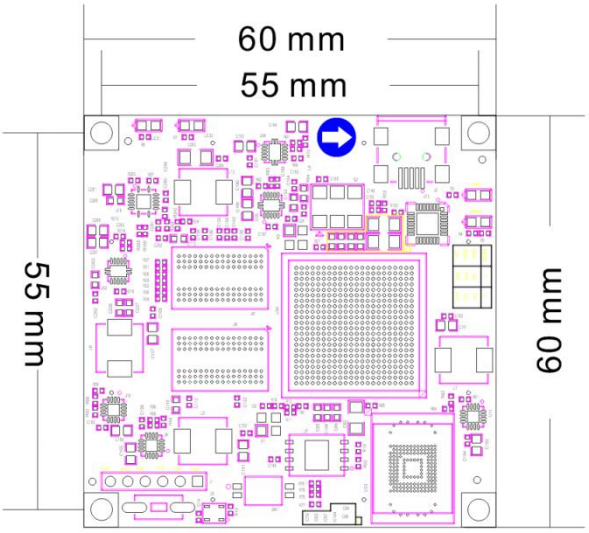


Figure 12-2

13. Structure



Expanding Board

1. Overview

Through the introduction of the previous function, we can understand the function of the expansion board part

1 PCIEx2 interface
2 fiber interface
2 10/100M/1000M Ethernet RJ-45 interface
1 HDMI video output interface
1 HDMI video input connector
4 USB HOST interface
1 USB Uart communication interface
1 SD card interface
2 40-pin expansion port
JTAG debugging interface
2 independent keys
5 user LED lights

2. Ethernet

There are two Gigabit Ethernet interfaces on the AX7015 Expanding board. One Ethernet interface is connected to the PS system, and the other Ethernet interface is connected to the logical IO interface of the PL. The Gigabit Ethernet interface connected to the PL side needs to be called by program to IP mount on the AXI bus system of ZYNQ.
The Ethernet chip uses KSZ9031RNX Ethernet PHY chip to provide users with network communication services. The Ethernet PHY chip on the PS side is connected to the GPIO interface of the BANK501 on the PS side of ZYNQ. The PL Ethernet PHY chip is connected to the BANK35 IO. The KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate and communicates with the Zynq7000 system's MAC layer through the RGMII interface. The KSZ9031RNX supports MDI/MDX adaptation, various speed adaptations, Master/Slave adaptation, and MDIO bus support for PHY register management.When the KSZ9031RNX is powered on, it detects certain IO levels to determine its own operating mode. Table 2-2-1 describes the default settings after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 011
CLK125_EN	Enable 125Mhz clock output selection	Enable
LED_MODE	LED light mode configuration	Single LED light mode
MODE0~MODE3	Link adaptation and full duplex configuration	10/100/1000 adaptive, compatible with full-duplex, half-duplex

Table 2-2-1

When the network is connected to Gigabit Ethernet, the data of ZYNQ and PHY chip KSZ9031RNX is transmitted through the RGMII bus when the data is transmitted, and the transfer clock is 125Mhz. The data is sampled at the rising edge and falling sample of the clock.

When the network is connected to Fast Ethernet, data transmission between the ZYNQ and PHY chip KSZ9031RNX is performed through the RMII bus and the transmission clock is 25 MHz. Data is sampled on the rising edge and falling samples of the clock.

Figure 2-2-1 shows the connection of a 1-channel Ethernet PHY chip on the ZYNQ PS side:

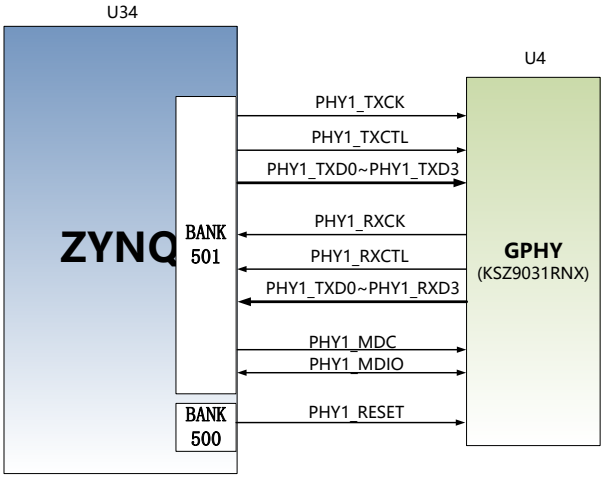


Figure 2-2-1

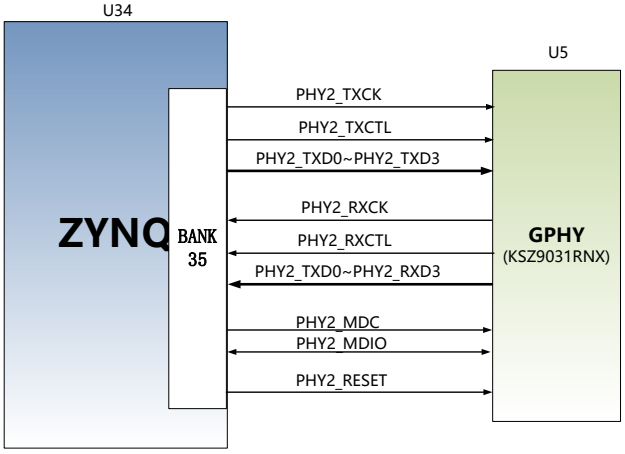


Figure 2-2-2

PS Ethernet Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY1_TXCK	PS_MIO16_501	D17	RGMII Send clock
PHY1_TXD0	PS_MIO17_501	E14	Send data bit 0
PHY1_TXD1	PS_MIO18_501	A16	Send data bit1
PHY1_TXD2	PS_MIO19_501	E13	Send data bit2
PHY1_TXD3	PS_MIO20_501	A15	Send data bit3
PHY1_TXCTL	PS_MIO21_501	F12	Send enable signal
PHY1_RXCK	PS_MIO22_501	A9	RGMII Receive clock

PHY1_RXD0	PS_MIO23_501	E12	Receive data Bit0
PHY1_RXD1	PS_MIO24_501	B16	Receive data Bit1
PHY1_RXD2	PS_MIO25_501	F11	Receive data Bit2
PHY1_RXD3	PS_MIO26_501	A10	Receive data Bit3
PHY1_RXCTL	PS_MIO27_501	D16	Receive data valid signal
PHY1_MDC	PS_MIO52_501	D13	MDIO Management clock
PHY1_MDIO	PS_MIO53_501	C11	MDIO Management clock
PHY1_RESET	PS_MIO7	D18	Reset

PL Ethernet Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY2_TXCK	B35_L16_P	D1	RGMII Send clock
PHY2_TXD0	B35_L23_P	F2	Send data bit 0
PHY2_TXD1	B35_L23_N	F1	Send data bit1
PHY2_TXD2	B35_L17_P	E2	Send data bit2
PHY2_TXD3	B35_L17_N	D2	Send data bit3
PHY2_TXCTL	B35_L16_N	C1	Send enable signal
PHY2_RXCK	B35_L13_P	B4	RGMII Receive clock
PHY2_RXD0	B35_L15_P	A2	Receive data Bit0
PHY2_RXD1	B35_L15_N	A1	Receive data Bit1
PHY2_RXD2	B35_L18_P	B2	Receive data Bit2
PHY2_RXD3	B35_L18_N	B1	Receive data Bit3
PHY2_RXCTL	B35_L13_N	B3	Receive data valid signal
PHY2_MDC	B35_L7_P	C8	MDIO Management clock
PHY2_MDIO	B35_L7_P	B8	MDIO Management clock
PHY2_RESET	B35_L8_P	B7	Reset

3. USB2.0 Host

There are four USB2.0 HOST interfaces on the AX7015 Expanding Board. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI standard interface, and then expands out of four USB HOSTs through a USB HUB chip USB2514. ZYNQ's USB bus interface is connected to the USB3320C-EZK transceiver to enable high-speed USB 2.0 Host mode data communication. The data and control signals of the USB3320C USB are connected to the IO port of the BANK501 on the PS side of the ZYNQ chip. The USB differential signal (DP/DM) is connected to the USB2514 chip to expand the four USB ports. Two 24MHz crystal oscillators provide the system clock for the USB3320C and USB2514 chips,

respectively.
The Expanding Board provides users with four USB HOST interfaces. The USB interface is a USB Type A interface , which allows users to simultaneously connect different USB Slave peripherals (such as USB mouse and USB keyboard). In addition, the backplane also provides +5V power for each USB interface.
Figure 2-3-1 shows the connection between the ZYNQ processor, the USB3320C-EZK chip and the USB2514 chip.

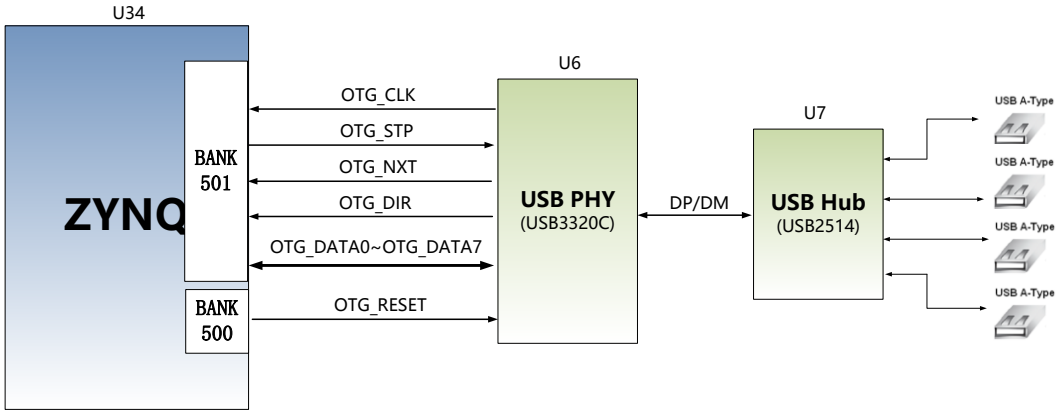


Figure 2-3-1

USB2.0 Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
OTG_DATA4	PS_MIO28_501	A11	USB data bit4
OTG_DIR	PS_MIO29_501	E15	USB data direction signal
OTG_STP	PS_MIO30_501	A12	USB stop signal
OTG_NXT	PS_MIO31_501	F14	USB next data signal
OTG_DATA0	PS_MIO32_501	C16	USB data bit0
OTG_DATA1	PS_MIO33_501	G11	USB data bit1
OTG_DATA2	PS_MIO34_501	B11	USB data bit2
OTG_DATA3	PS_MIO35_501	F9	USB data bit3
OTG_CLK	PS_MIO36_501	A14	USB clock signal
OTG_DATA5	PS_MIO37_501	B9	USB data bit5
OTG_DATA6	PS_MIO38_501	F10	USB data bit6
OTG_DATA7	PS_MIO39_501	C10	USB data bit7
OTG_RESETN	PS_MIO8_500	E18	USB reset signal

4. HDMI OUT

The HDMI output interface uses Silion Image's SIL9134 HDMI (DVI) encoding chip, which supports up to 1080P@60Hz output and supports 3D output.
Among them, SIL9134's video digital interface, audio digital interface and I2C

configuration interface are connected with BANK34/35 IO of ZYNQ7000 PL part. ZYNQ7000 system performs initialization and control operation of SIL9134 through I2C pin. The hardware connection between the SIL9134 chip and the ZYNQ7000 is shown in Figure 2-4-1.

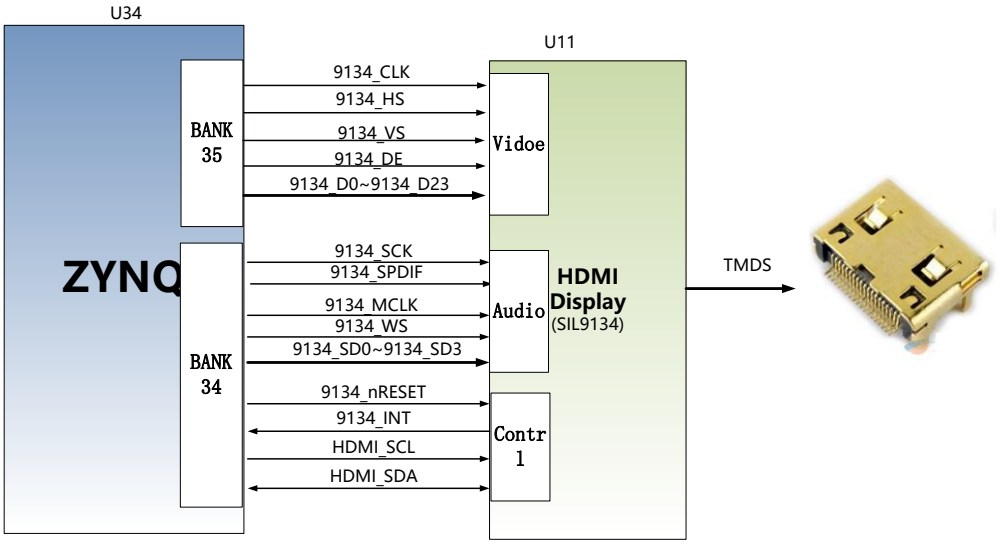


Figure 2-4-1

HDMI out Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
9134_CLK	B35_L24_P	H1	clock
9134_HS	B35_L21_P	E4	line synchronization
9134_VS	B35_L21_N	E3	column synchronization
9134_DE	B35_L22_N	G2	Signal valid
9134_D[0]	B35_L22_P	G3	Data0
9134_D[1]	B35_L19_N	H3	Data 1
9134_D[2]	B35_L19_P	H4	Data 2
9134_D[3]	B35_L4_N	G7	Data 3
9134_D[4]	B35_L4_P	G8	Data 4
9134_D[5]	B35_L24_N	G1	Data 5
9134_D[6]	B35_IO25	H5	Data 6
9134_D[7]	B35_IO0	H6	Data 7
9134_D[8]	B35_L20_P	G4	Data 8
9134_D[9]	B35_L20_N	F4	Data 9
9134_D[10]	B35_L5_P	F5	Data 10
9134_D[11]	B35_L5_N	E5	Data 11
9134_D[12]	B35_L6_P	G6	Data 12
9134_D[13]	B35_L6_N	F6	Data 13
9134_D[14]	B35_L1_N	E7	Data 14

9134_D[15]	B35_L1_P	F7	Data 15
9134_D[16]	B35_L14_P	D3	Data 16
9134_D[17]	B35_L14_N	C3	Data 17
9134_D[18]	B35_L12_N	C4	Data 18
9134_D[19]	B35_L12_P	D5	Data 19
9134_D[20]	B35_L11_N	C5	Data 20
9134_D[21]	B35_L11_P	C6	Data 21
9134_D[22]	B35_L3_P	E8	Data 22
9134_D[23]	B35_L3_N	D8	Data 23
9134_SCK	B34_L2_N	J6	Audio Interface I2S Clock
9134_SPDIF	B34_L21_N	N3	Audio S/PDIF input
9134_MCLK	B34_L21_P	N4	Audio input master clock
9134_WS	B34_L2_P	J7	Audio interface I2S word selection
9134_SD0	B34_L19_N	N5	Audio Interface I2S Data0
9134_SD1	B34_L19_P	N6	Audio Interface I2S Data1
9134_SD2	B34_L13_N	T1	Audio Interface I2S Data2
9134_SD3	B34_L13_P	T2	Audio Interface I2S Data3
9134_nRESET	B34_L12_N	L4	Reset signal
9134_INT	B34_L12_P	L5	Interrupt signal
HDMI_SCL	B34_L1_P	J8	IIC control clock
HDMI _SDA	B34_L1_N	K8	IIC Control data

5. HDMI IN

The HDMI input interface uses Silion Image's SIL9013 HDMI decoding chip, which supports up to 1080P@60Hz input and supports data output in different formats. ; Among them, the IIC configuration interface of SIL9013 is also connected with the IO of BANK13 of FPGA. ZYNQ initializes and controls SIL9013 through the programming of I2C bus. The hardware connection of HDMI input interface is shown in Figure 2-5-1.

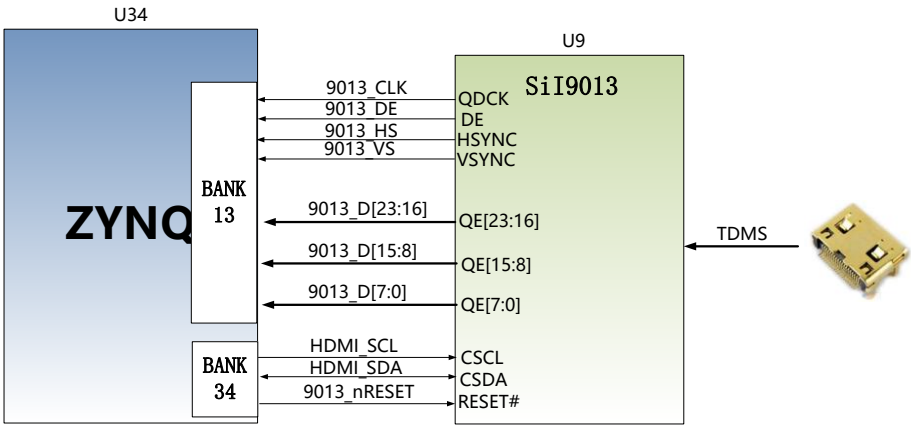


Figure 2-5-1

HDMI in Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
9013_nRESET	B34_L16_N	P1	Reset signal
9013_CLK	B13_L14_P	AA16	clock
9013_HS	B13_L20_P	U19	line synchronization
9013_VS	B13_L22_N	U18	column synchronization
9013_DE	B13_L20_N	V19	Signal valid
9013_D[0]	B13_L22_P	U17	Data0
9013_D[1]	B13_L23_P	V16	Data 1
9013_D[2]	B13_L23_N	W16	Data 2
9013_D[3]	B13_L14_N	AA17	Data 3
9013_D[4]	B13_L13_N	Y19	Data 4
9013_D[5]	B13_L13_P	Y18	Data 5
9013_D[6]	B13_L11_N	AA15	Data 6
9013_D[7]	B13_L11_P	AA14	Data 7
9013_D[8]	B13_L17_P	AB16	Data 8
9013_D[9]	B13_L17_N	AB17	Data 9
9013_D[10]	B13_L16_N	AB19	Data 10
9013_D[11]	B13_L16_P	AB18	Data 11
9013_D[12]	B13_L12_N	Y15	Data 12
9013_D[13]	B13_IO25	U16	Data 13
9013_D[14]	B13_L1_N	V14	Data 14
9013_D[15]	B13_L1_P	V13	Data 15
9013_D[16]	B13_L7_N	AB11	Data 16
9013_D[17]	B13_L7_P	AA11	Data 17
9013_D[18]	B13_L4_P	V11	Data 18
9013_D[19]	B13_L4_N	W11	Data 19
9013_D[20]	B13_L3_P	W12	Data 20
9013_D[21]	B13_L3_N	W13	Data 21
9013_D[22]	B13_L5_N	U12	Data 22
9013_D[23]	B13_L5_P	U11	Data 23
HDMI_SCL	B34_L1_P	J8	IIC control clock
HDMI _SDA	B34_L1_N	K8	IIC control data

6. Optical

The AX7015 expansion board has two optical interfaces. Users can purchase optical modules (1.25G /2.5G/10G optical modules on the market) to insert optical fiber data into the two optical interfaces. The 2-way fiber interfaces are connected to the 2-way RX/TX of the ZYNQ GTP transceiver. The TX signals and the RX signals are

connected to the ZYNQ and the optical module through a DC-blocking capacitor in a differential signal manner. Each TX transmission and RX reception data rate is as high as 6.125Gb/s. The reference clock for the GTP transceiver is provided by the 125M differential crystal on the core board.
The schematic diagram of FPGA and fiber design is shown in Figure 2-6-1.

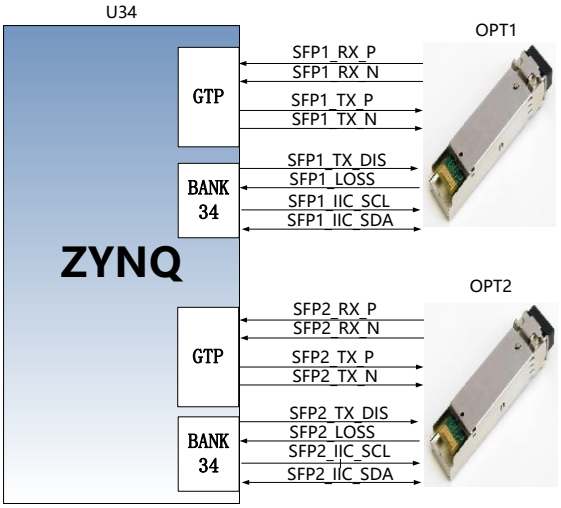


Figure 2-6-1

First SFP pin Assignment:

Signal Name	Pin Number	Explain
SFP1_TX_P	W2	SFP data transmission Positive
SFP1_TX_N	Y2	SFP data transmission Negative
SFP1_RX_P	W6	SFP data reception Positive
SFP1_RX_P	Y6	SFP data reception Negative
SFP1_TX_DIS	U1	SFP Launch prohibition, high efficiency
SFP1_LOSS	U2	SFP Receive LOSS signal, high means no light signal received
SFP1_IIC_SCL	K7	SFP DDMI IIC clock
SFP1_IIC_SDA	L7	SFP DDMI IIC data

Second SFP pin Assignment:

Signal Name	Pin Number	Explain
SFP2_TX_P	AA5	SFP data transmission Positive
SFP2_TX_N	AB5	SFP data transmission Negative
SFP2_RX_P	AA9	SFP data reception Positive
SFP2_RX_P	AB9	SFP data reception Negative
SFP2_TX_DIS	K2	SFP Launch prohibition, high efficiency
SFP2_LOSS	K5	SFP Receive LOSS signal, high means no light signal received

SFP2_IIC_SCL	J5	SFP DDMI IIC clock
SFP2_IIC_SDA	J3	SFP DDMI IIC data

7. PCIE

The AX7015 expansion board provides an industrial-grade high-speed data transmission PCIe x2 interface. The external dimensions of the PCIE card comply with the standard PCIe card electrical specifications and can be used directly on the PCIe slot of an ordinary desktop PC.
The transmit and receive signals of the PCIe interface are directly connected with the GTP transceiver of the FPGA. The two channels of the TX signal and the RX signal are connected to the FPGA in a differential signal mode, and the single channel communication rate can reach up to 5 Gbit bandwidth. The PCIe reference clock is provided by the computer's PCIe slot to the development board. The reference clock frequency is 100Mhz.
The PCIe interface of the development board is designed as shown in Figure 2-7-1 below. The TX transmit signal and the reference clock CLK signal are connected in AC-coupled mode.

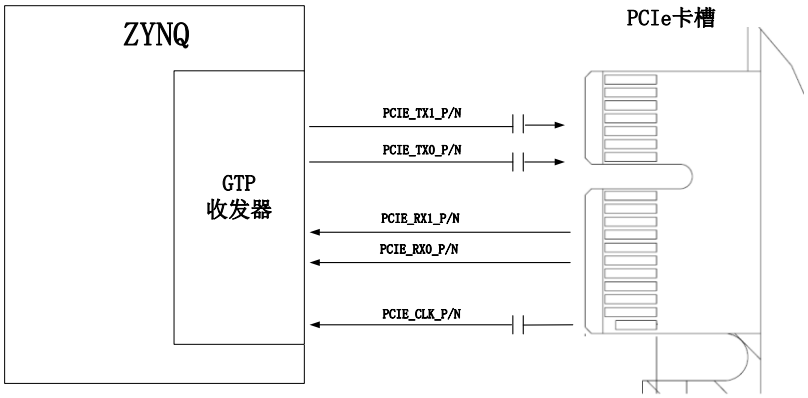


Figure 2-7-1

PCIE pin Assignment:

Signal Name	Pin Number	Explain
PCIE_RX0_P	W8	PCIE Channel 0 data reception Positive
PCIE_RX0_N	Y8	PCIE Channel 0 data reception Negative
PCIE_RX1_P	AA7	PCIE Channel 1 data reception Positive
PCIE_RX1_N	AB7	PCIE Channel 1 data reception Negative
PCIE_TX0_P	W4	PCIE Channel 0 data send Positive
PCIE_TX0_N	Y4	PCIE Channel 0 data send Negative
PCIE_TX1_P	AA3	PCIE Channel 1 data send Positive
PCIE_TX1_N	AB3	PCIE Channel 1 data send Negative
PCIE_CLK_P	U9	PCIE clock Positive
PCIE_CLK_N	V9	PCIE clock Negative

8. USB to Uart

AX7015 is also equipped with a serial interface on the backplane for overall debugging of the ZYNQ7000 system. The conversion chip uses a USB-UAR chip from Silicon Labs CP2102GM. The USB interface uses a MINI USB interface, which can be connected to the USB of the PC using a USB cable. The port performs separate power supply and serial data communication for the core board.
A schematic diagram of USB Uart circuit design is shown in Figure 2-8-1 below:

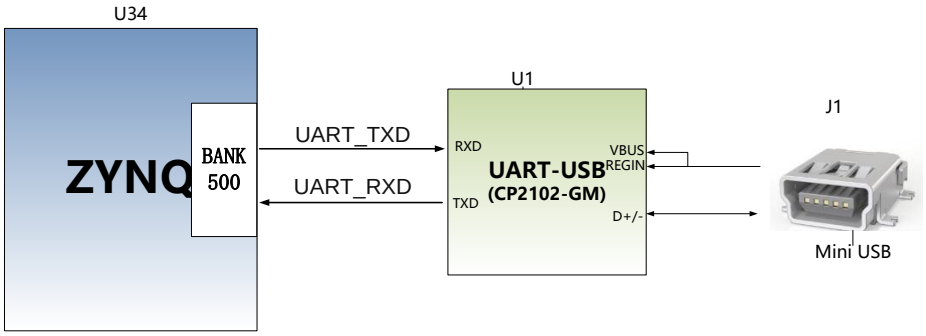


Figure 2-8-1

Uart Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
UART_RXD	PS_MIO13_500	A17	Uart data input
UART_TXD	PS_MIO12_500	C18	Uart data output

9. SD Card slot

The AX7015 Expanding Board incorporates a Micro SD card interface to provide user access to SD card memory, BOOT programs for storing ZYNQ chips, Linux operating system kernels, file systems, and other user data files.
The SDIO signal is connected to the IO signal of the PSNKNK501 of the ZYNQ. Since the VCCMIO of the BANK is set to 1.8V, the data level of the SD card is 3.3V, and we connect here through the TXS02612 level converter. The schematic of the Zynq7000 PS and SD card connector is shown in Figure 2-9-1.

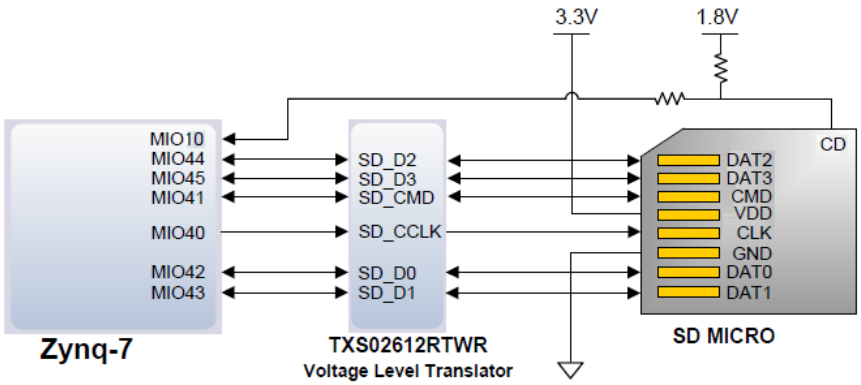


Figure 2-9-1

SD Card slot Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
SD_CLK	PS_MIO40	E9	SD clock signal
SD_CMD	PS_MIO41	C15	SD command signal
SD_D0	PS_MIO42	D15	SD data0
SD_D1	PS_MIO43	B12	SD data1
SD_D2	PS_MIO44	E10	SD data2
SD_D3	PS_MIO45	B14	SD data3
SD_CD	PS_MIO10	G16	SD card insert signal

10. JTAG

The AX7015 expansion board reserves a JTAG interface for downloading FPGA programs or firmware to FLASH. In order to damage the FPGA chip caused by hot swapping, we added a protection diode on the JTAG signal to ensure that the voltage of the signal is within the acceptable range of the FPGA and avoid the damage of the FPGA.

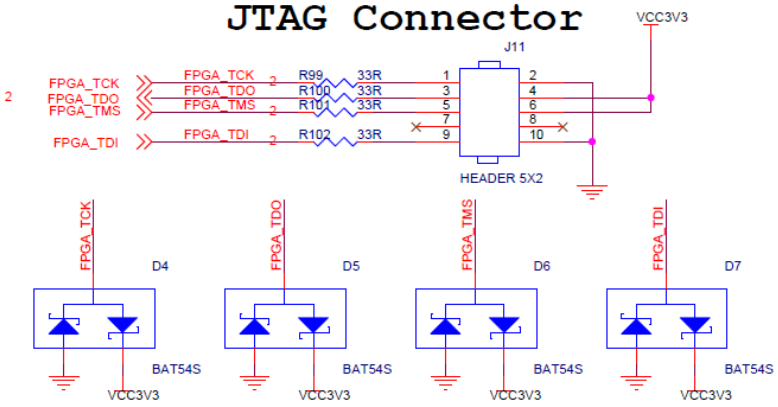


Figure 2-10-1

Note: Users connect the PC and JTAG interface through the USB downloader provided by us to perform ZYNQ system debugging. Do not hot-plug the JTAG line when plugging or unplugging.

11. User LED

The AX7015 expansion board has six red LEDs, one of which is the power indicator (PWR) and five of which are user LEDs. When the expansion board power supply, the power indicator will light; 5 user LED lights one is connected to the MIO of the PS, and the other four are connected to the PL IO, the user can control the light and off through the program, when connected to the user LED lights When the IO voltage is high, the user LED turns off, and when the connected IO voltage is low, the user LED is lit. The schematic diagram of the LED lamp hardware connection is shown in Figure 2-11-1:

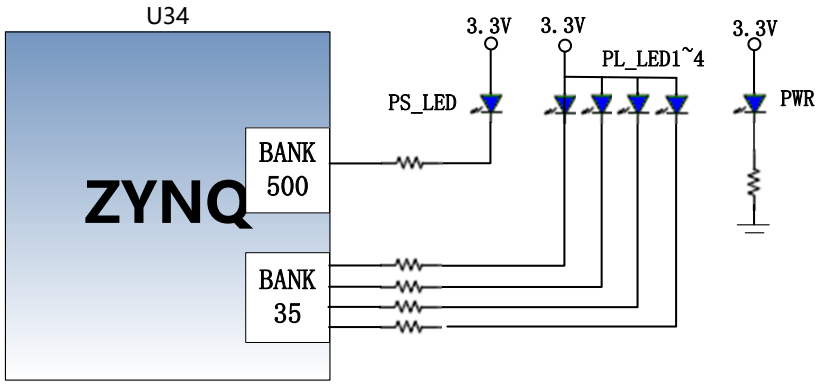


Figure 2-11-1

User LED Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PS_LED	PS_MIO9_500	C19	PS LED
PL_LED1	B35_L10_P	A5	PL LED1
PL_LED2	B35_L9_P	A7	PL LED2
PL_LED3	B35_L9_N	A6	PL LED3
PL_LED4	B35_L7_N	B8	PL LED4

12. User KEY

The AX7015 expansion board has two user buttons PS KEY and PL KEY. The PS KEY is connected to the MIO pin of the ZYNQ chip PS, and the PL KEY is connected to the IO pin of the ZYNQ chip PL. When the button is pressed, the signal is low and the ZYNQ chip detects a low level to determine whether the button is pressed. A schematic diagram of a user's key connection is shown in Figure 2-12-1:

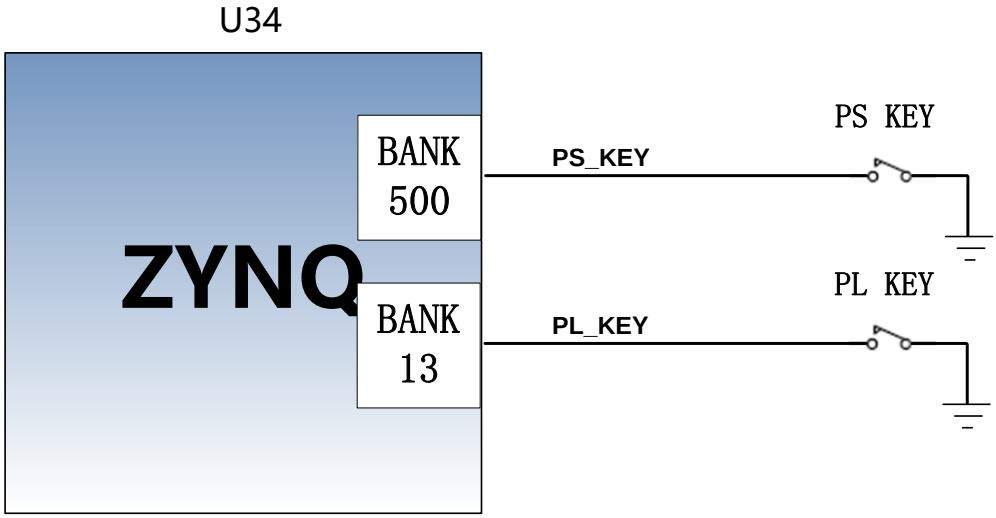


Figure 2-12-1

User Key Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PS_KEY	PS_MIO11_500	B19	PS KEY

PL_KEY	B13_L8_N	AB12	PL KEY

13. Expansion

The AX7015 expansion board has reserved a 40-pin expansion port J12 with a 2.54mm standard spacing for connecting the black gold modules or the user's own external circuit design. The expansion port has 40 signals, among which, 5V power supply has 1 channel, 3.3 V power 2 way, 3 way, IO port 34 way. Never directly connect IO directly to 5V devices to avoid burning the ZYNQ7000 chip. If you want to connect 5V equipment, you need to connect the level conversion chip.
The circuit of the expansion port (J12) is shown in Figure 2-13-1.

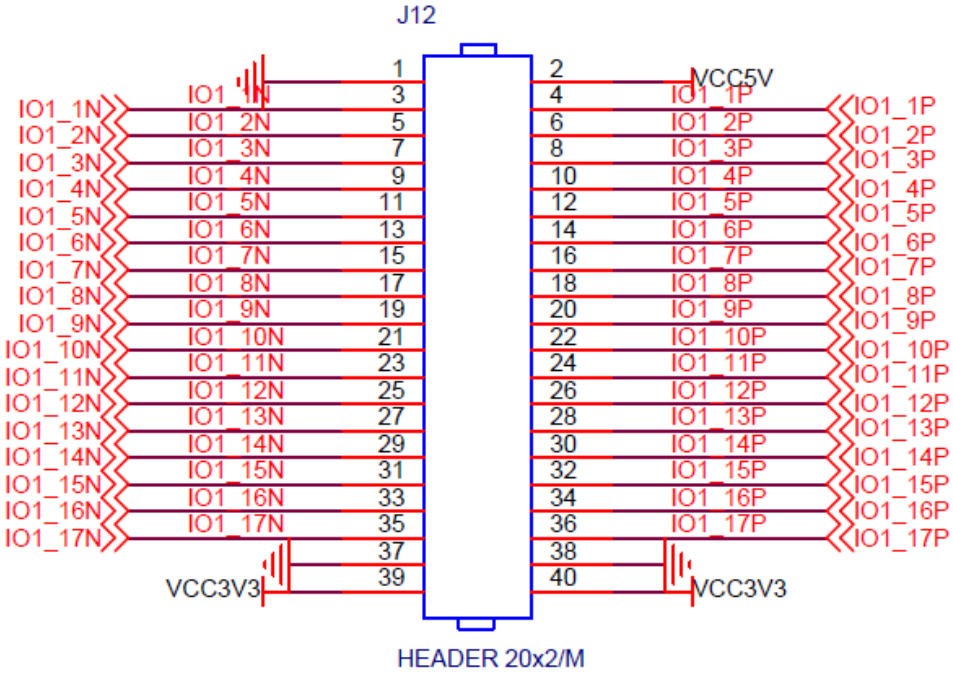


Figure 2-13-1

Pin Assignment:

Pin	Signal Name	Pin Name	Pin Number
1	GND	2	+5V（Input）
3	M1	4	M2
5	Y13	6	Y12
7	P2	8	P3
9	R7	10	P7
11	P8	12	N8
13	R2	14	R3
15	R4	16	R5
17	M7	18	M8
19	M3	20	M4
21	U14	22	U13

23	AB14	24	AB13
25	W15	26	V15
27	Y17	28	W17
29	W18	30	V18
31	AB22	32	AB21
33	AA20	34	AA19
35	T17	36	R17
37	GND	38	GND
39	+3.3V（Output）	40	+3.3V（Output）

14. Power

The power input voltage of the development board is DC12V, and the board can be powered through the PCIE slot or an external +12V power supply. When using an external power supply, please use the power supply that comes with the development board. Do not use other power supplies to avoid damaging the development board.
The base plate is converted to +5V, +1.2V, +3.3V and 1.8V four-way power supplies via one-way DC/DC power supply chip MP2303 and three-way DC/DC power supply chip MP1482. Because the +5V power supply powers the core board through the inter-board connector, the DCDC power supply has a current output of 3A and the other three power supply current outputs are 2A.
The power supply on the expansion is shown in Figure 2-14-1.

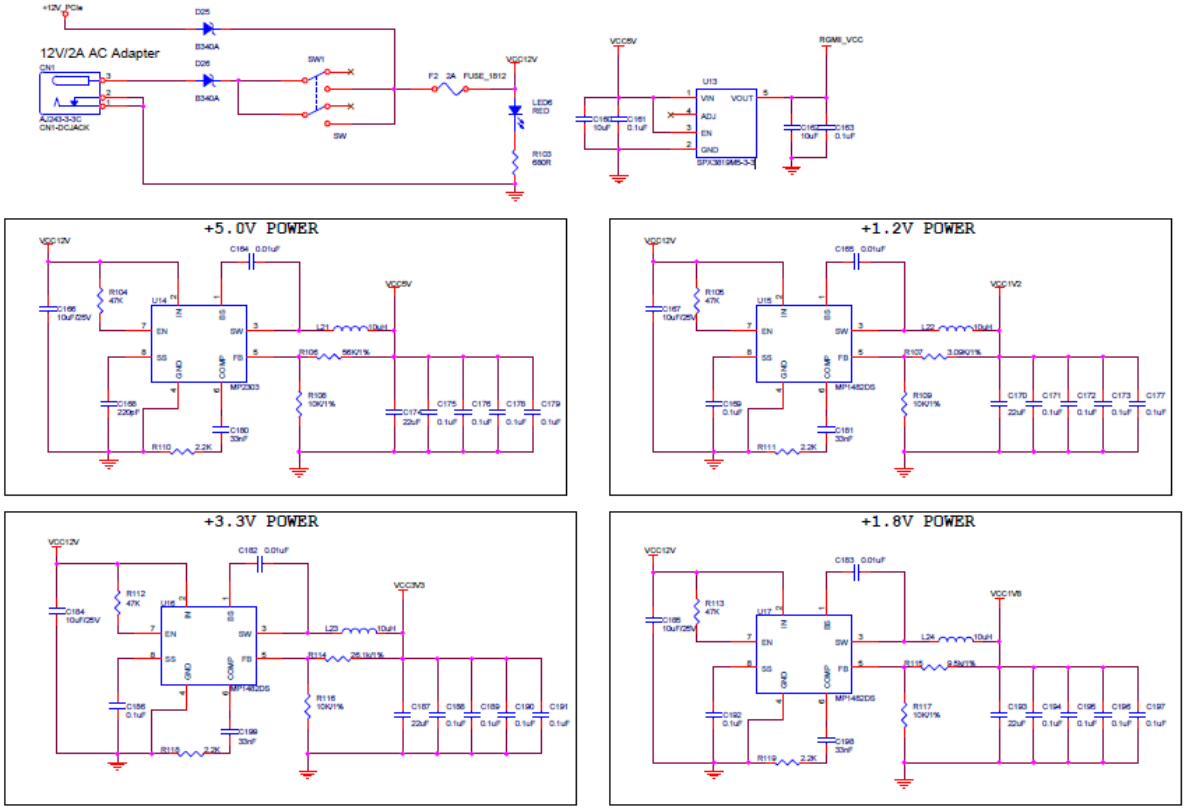


Figure 2-14-1

15. Structure