

BOOT OPTION

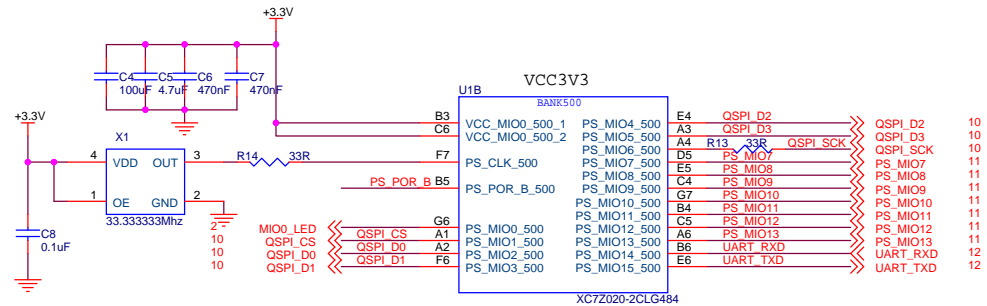
The diagram illustrates the boot option circuit. A +3.3V supply is connected to a network of resistors (R9, R8, R10, R11, R12) that pull up the MIO pins (PS_MIO8, GSPI_D0, GSPI_D1, GSPI_SCK, PS_MIO7). Another section shows a SW1 switch connected to a network of resistors (R75, R76, R77, R78) that pull up the MIO pins (QSPI_D3, QSPI_D2).

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MIO[8] = 1 ----MIO bank1 voltage=1.8V
MIO[2] = 0 ----cascaded JTAG
MIO[3] = 0 ----JTAG/NAND/Quad-SPI/SD
MIO[6] = 0 ----PLL used
MIO[7] = 0 ----MIO bank0 voltage=3.3V

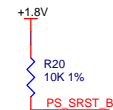
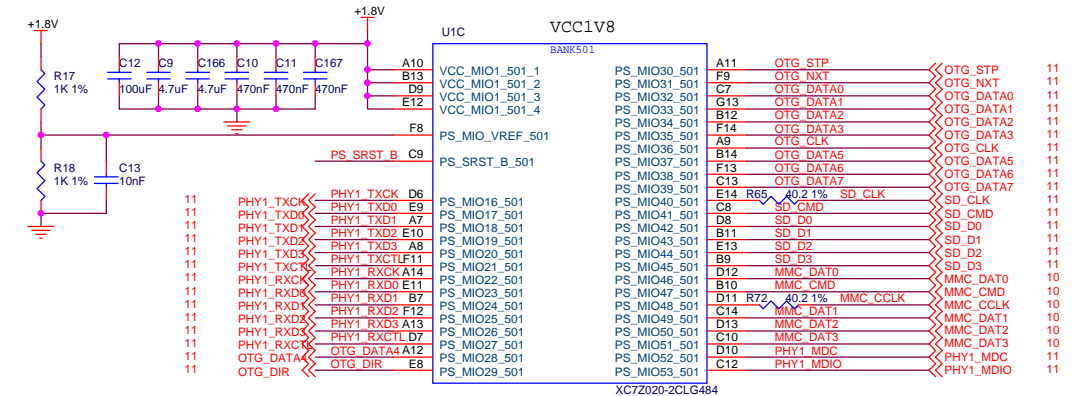
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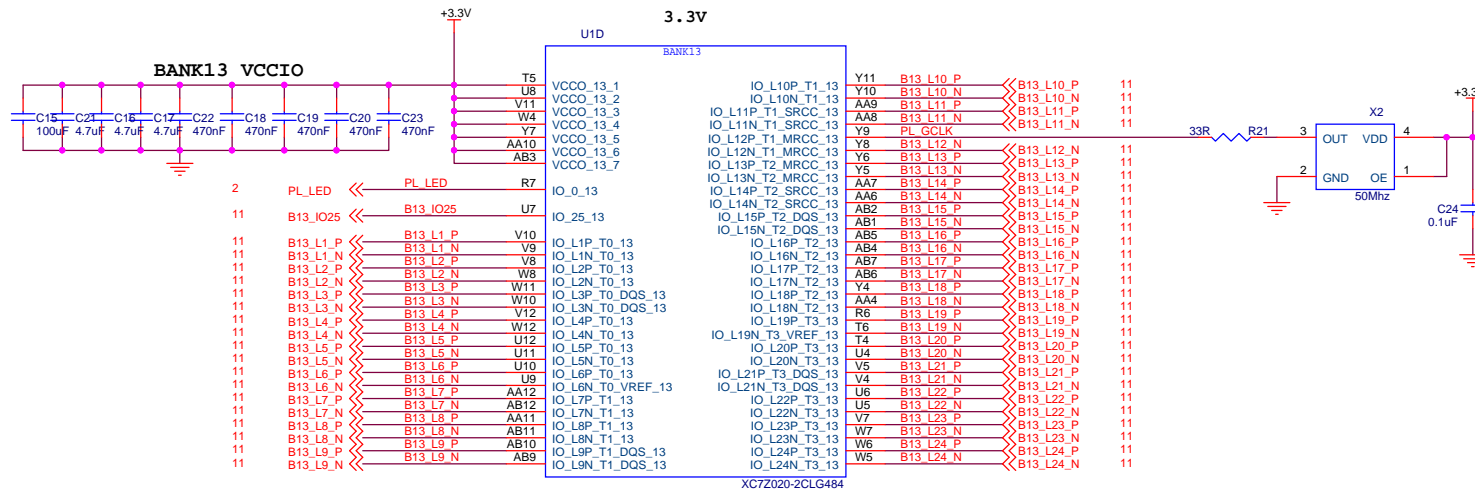
Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

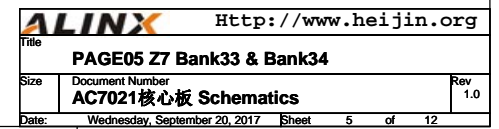
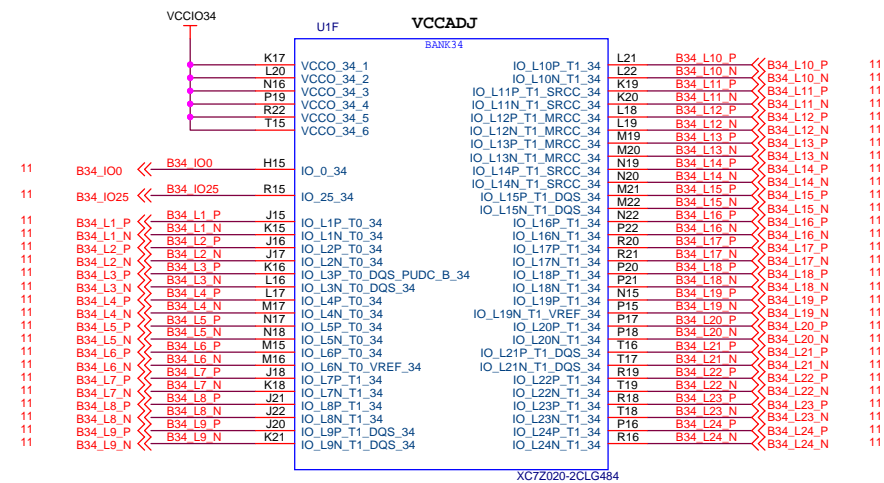
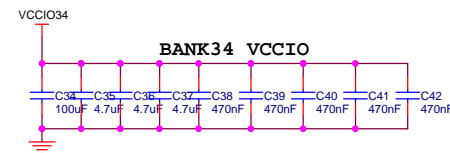


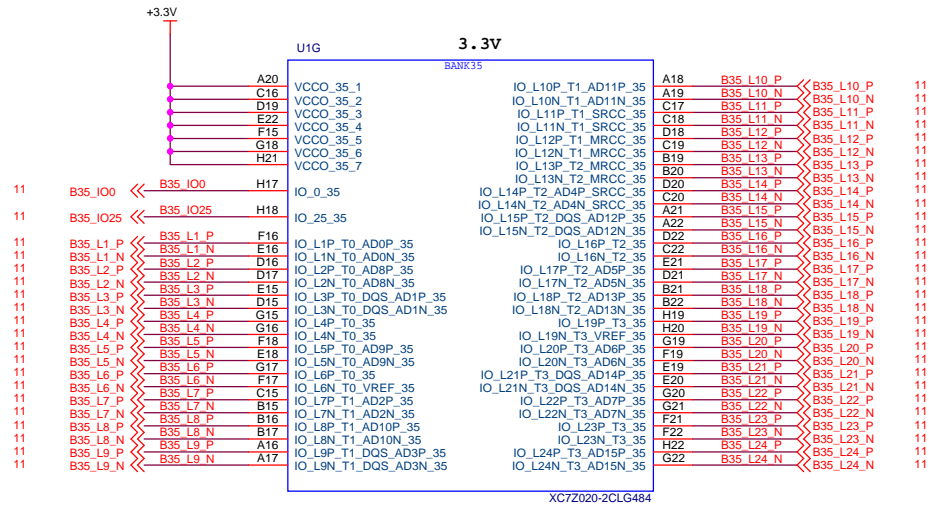
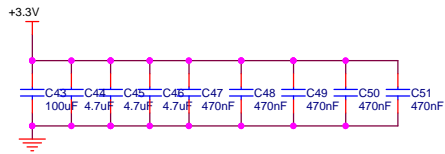
POWER ON RESET

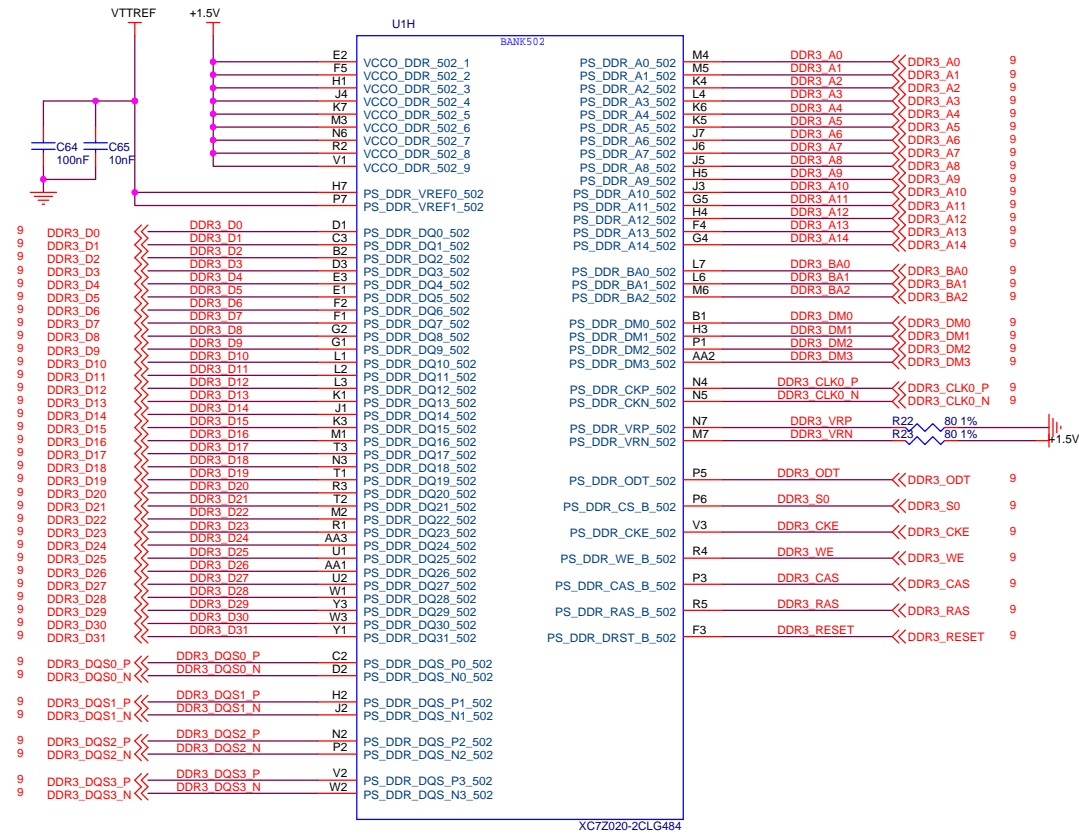
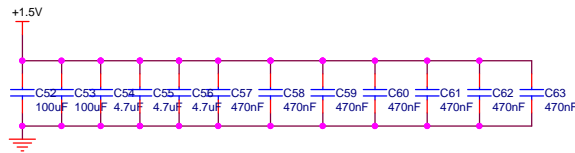
The diagram illustrates a Power On Reset (POR) circuit using the TCM811TERCTR chip. The chip is connected to a +3.3V supply through a 4.7K resistor (R19) and a 0.1uF capacitor (C14). The chip's #MIR pin (3) is connected to a push-button (KEY1) labeled 'POR RST'. The chip's VDD pin (4) is connected to the +3.3V supply. The chip's GND pin (1) is connected to ground. The chip's #RESET pin (2) is connected to the output of the push-button. The chip is labeled 'TCM811TERCTR'.

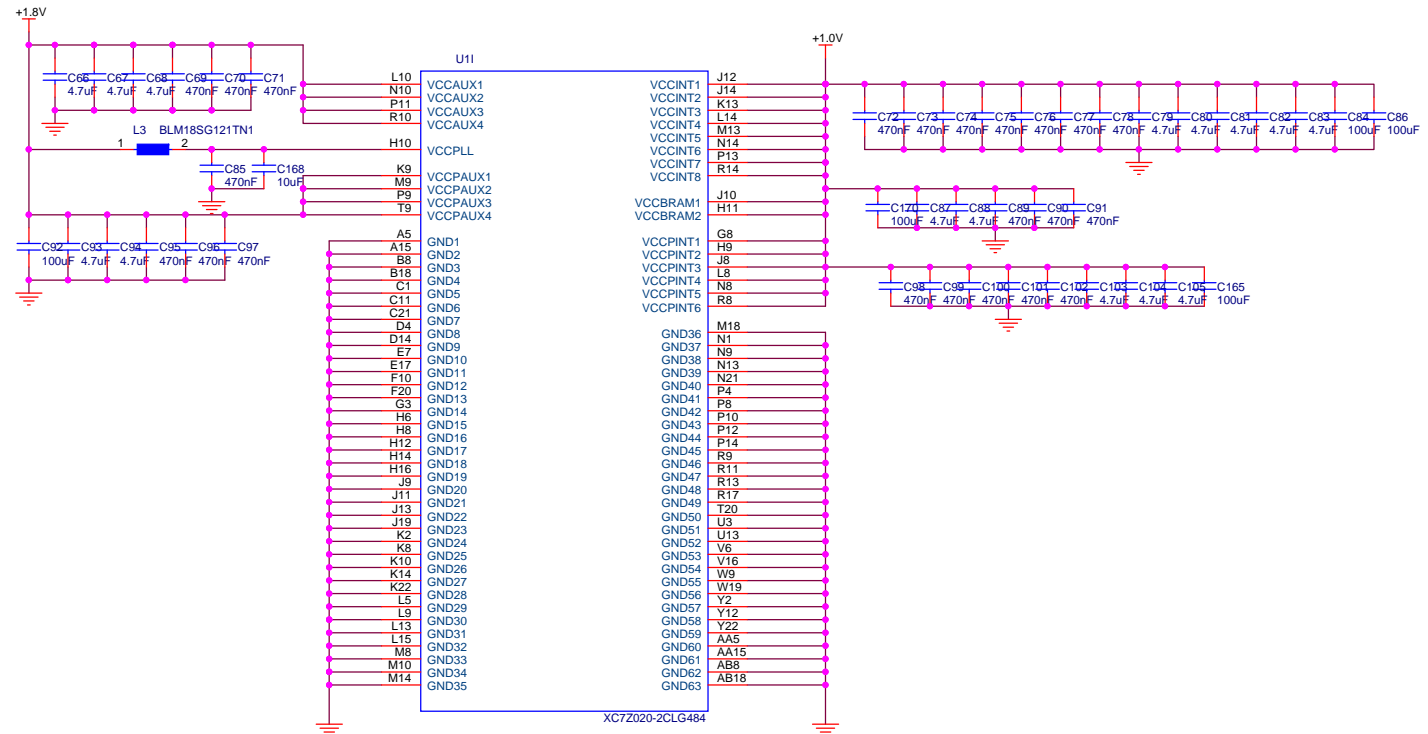


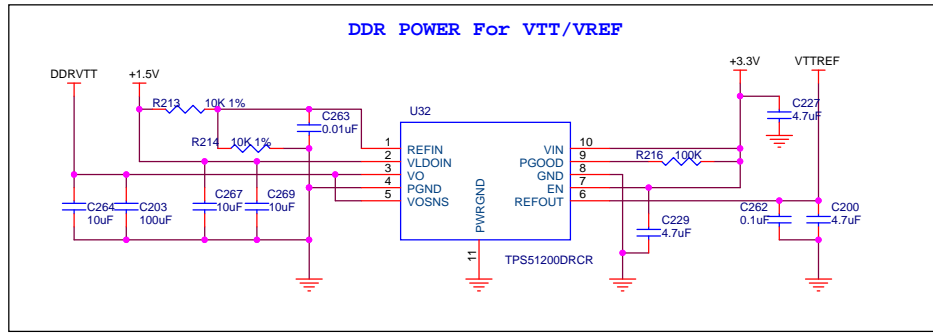
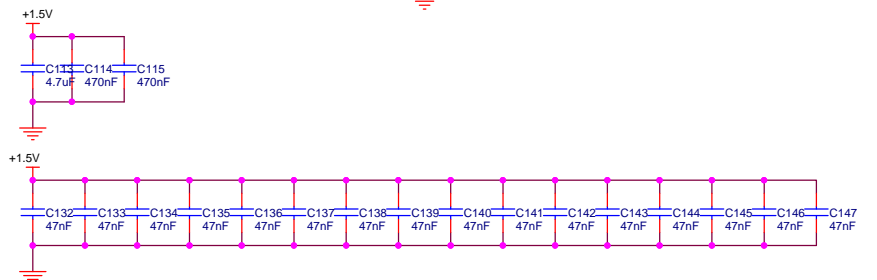
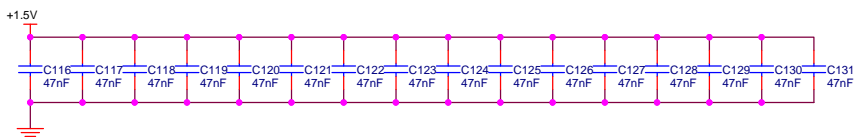
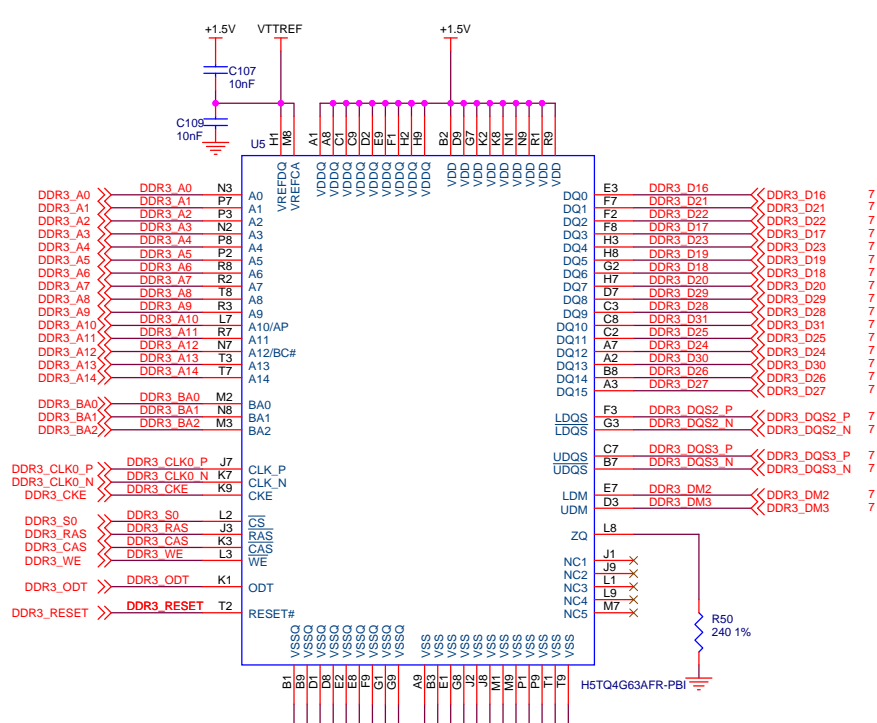
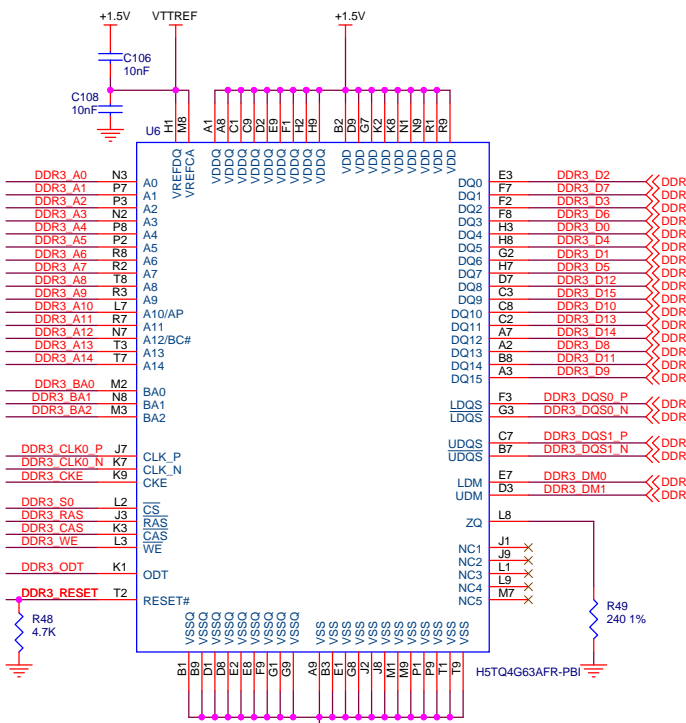
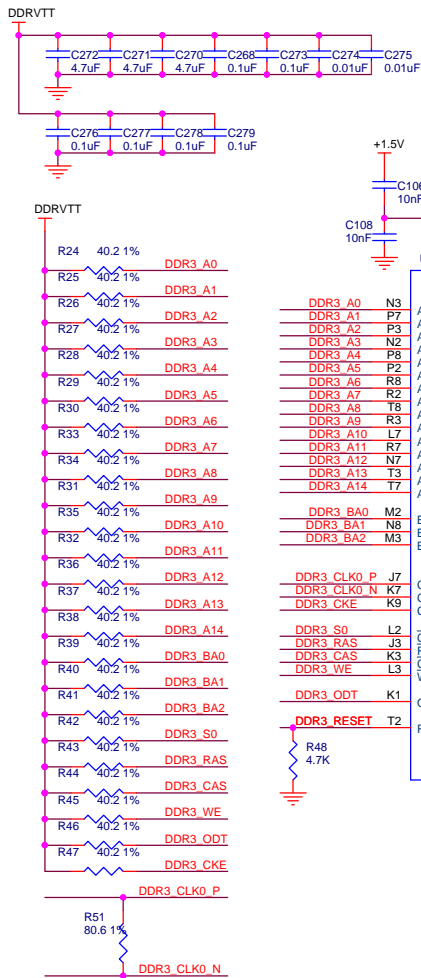




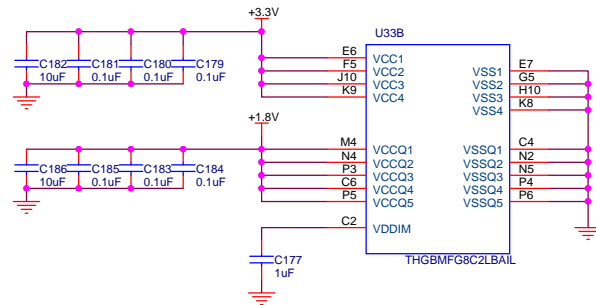
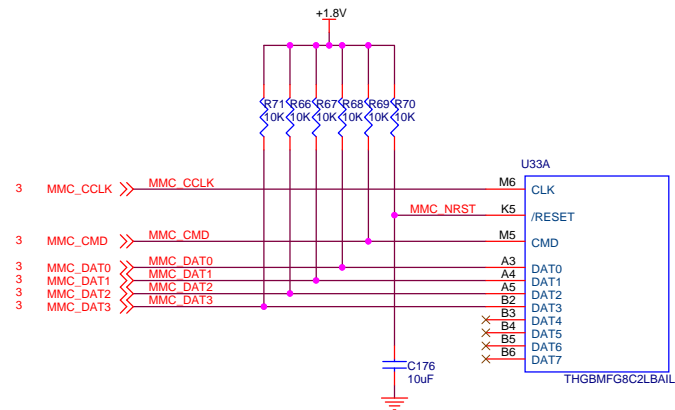
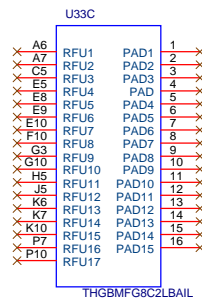
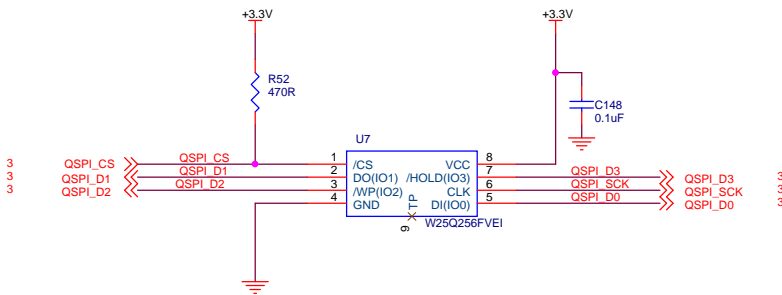
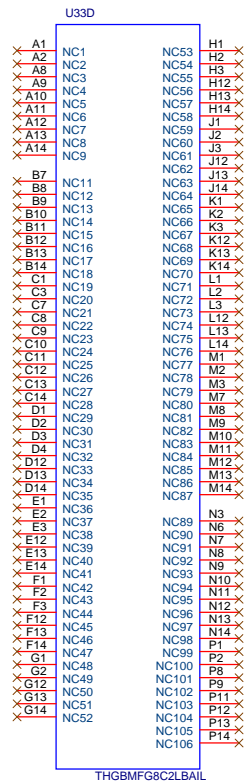








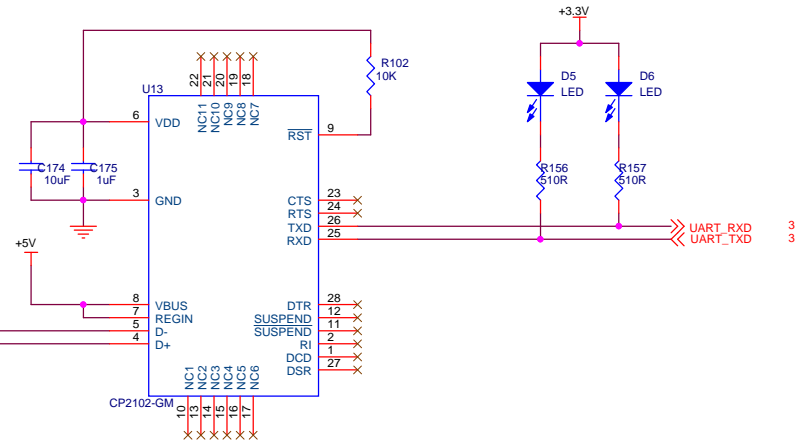
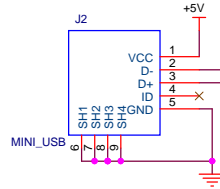
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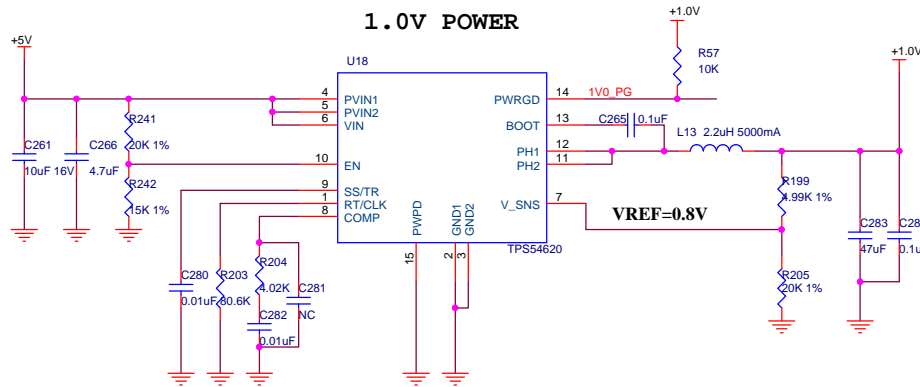
Power On Sequence:

1.0V -> 1.8V -> 1.5V -> 3.3V -> VCCIO

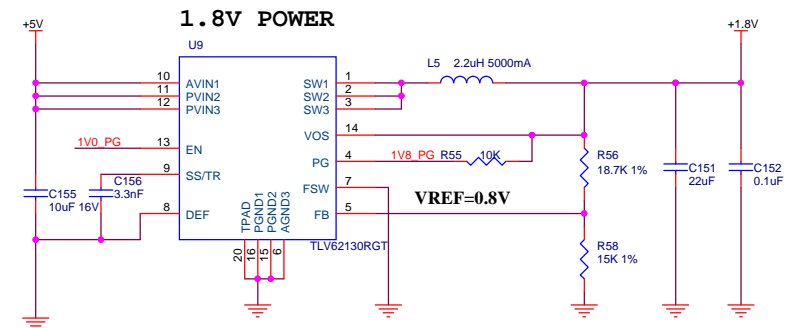
USB Uart



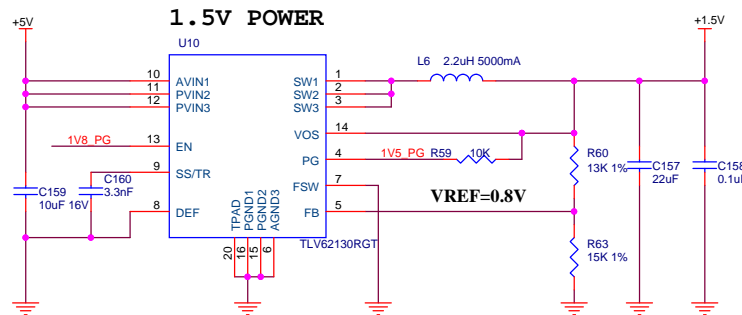
1.0V POWER



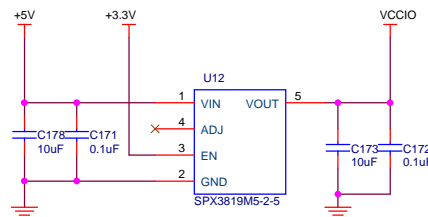
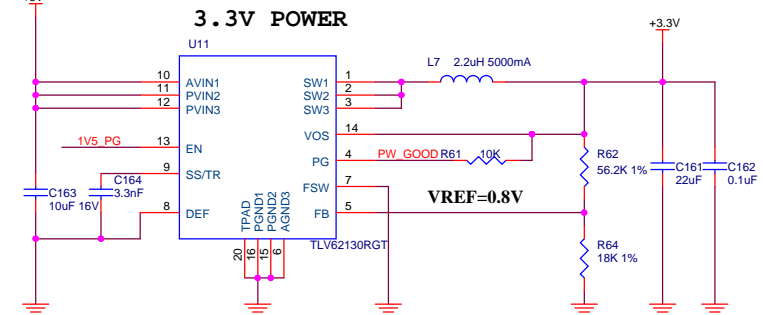
1.8V POWER



1.5V POWER



3.3V POWER



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