ALINX FPGA BOARD

AX7021

User Manual

ALINX

Revsion History:

Revision	Description
1.0	First Release

Development Environment:
Vivado 2017.4 is from Xilinx website
https://www.xilinx.com

Official website:
Http://www.alinx.com.cn

E-mail:
avic@alinx.com.cn

Tel:
+86-021-67676997

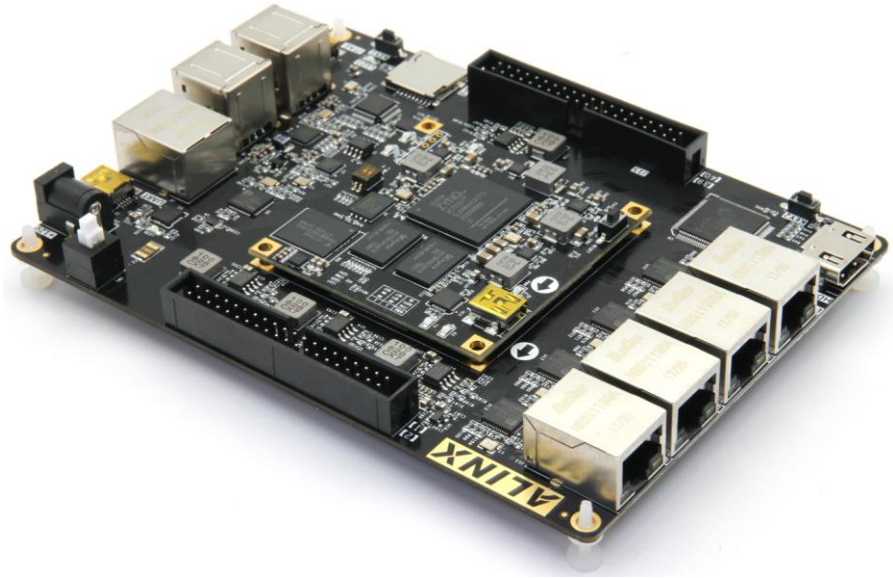
WeChat public number：
ALINX-HEIJIN

Contents

Overview

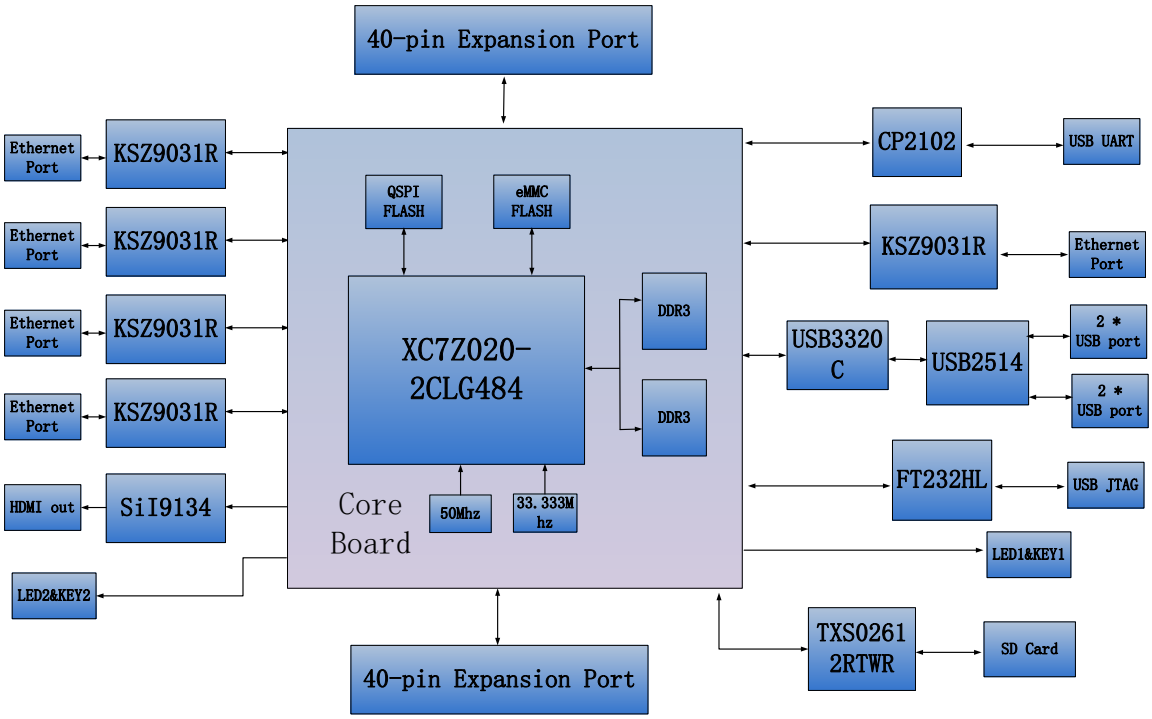
The AX7021 development platform uses core board and expansion board mode,to facilitate the user's secondary development and utilization of the core board. The core board uses the solution of the XILINX Zynq7000 SOC chip, which uses the ARM+FPGA SOC technology to integrate the dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. In addition, the core board contains two 1GB high-speed DDR3 SDRAM chips, a 32GB eMMC memory chip, and a 256Mb QSPI FLASH chip.

In the design of the expansion board, we have expanded the rich peripheral interfaces for users, such as 5 Gigabit Ethernet interfaces, 4 USB2.0 HOST interfaces, 1 HDMI output interface, Uart communication interface, SD card socket, 40-pin expansion interface and many more. It meets various needs of users, such as Ethernet high-speed data exchange, data storage, video transmission processing, is a "professional" ZYNQ development platform. Pre-verification and post-application of data processing are possible for high-speed Ethernet data transmission and exchange. I believe that such a product is very suitable for ZYNQ development students, engineers and other groups.



The development board uses the core board + expansion board model. High-speed board-to-board connector connections are used between the core board and the expansion board.

The structure of the entire development board is shown below:



The interfaces and functions that our development platform can contain are as follows:

- XILINX XC7Z020-2CLG484I
- 1GB DDR3
- 32GB eMMC FLASH
- 256Mbit QSPI FLASH
- PL side 50MHz active crystal, PS side 33.33MHz active crystal
- 5 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices. The network interface chip uses the KSZ9031 industrial-grade GPHY chip from Micrel, one Ethernet is connected to the PS side of the ZYNQ chip, and four Ethernet is connected to the PL side of the ZYNQ chip.
- 1 HDMI output interface, we have chosen Silion Image's SIL9134 HDMI encoding chip, supports up to 1080P@60Hz output, supports 3D output.
- 2 Uart to USB interface for communication with the computer for user debugging. One is on the core board, the core board is used independently for work, and the other one is on the expansion board. The whole board is used for debugging. The serial chip adopts USB-UAR chip of Silicon Labs CP2102GM, USB interface adopts MINI USB interface.
- 1 Micro SD card slot for storing operating system images and file systems.
- 2 40-pin 2.54mm pitch expansion ports that can be connected to various black gold modules (binocular cameras, TFT LCD screens, high-speed AD modules, etc.). The expansion port includes one 5V power supply, two 3.3V power supplies, three grounds, and 34 IO ports.
- 1 JTAG debug interface, using the MINI USB interface, users can debug and download the ZYNQ system through the USB cable and the onboard JTAG circuit.
- 9 LEDs, 6 on the core board and 3 on the bottom board. One power indicator on the core board; one DONE configuration indicator; two user indicators and two serial port transceiver indicators. There is one power indicator and two user indicators on the expansion board.
- 3 buttons, 1 reset button on the core board, 2 user buttons on the bottom board.

Core Board

1. Overview

The core board (AC7021) is based on the XC7Z020-2CLG484I from Xilinx's ZYNQ7000 series. Zynq's PS system integrates two ARM CortexTM-A9 processors, an AMBA® interconnect, internal memory, external memory interfaces, and peripherals. The FPGA inside ZYNQ chip contains rich programmable logic unit, DSP and internal RAM.

This core board uses two SK Hynix H5TQ4G63AFR-PBI DDR3 chips, each with a DDR capacity of 4 Gbits; two DDR chips combined into a 32-bit data bus width, and a read/write data clock between ZYNQ and DDR3. The frequency up to 533Mhz; This configuration can meet the system's high bandwidth data processing needs.

In order to connect to the expansion board, the four board-to-board connectors of this core board extend the PS-side USB interface, Gigabit Ethernet interface, SD card interface and other remaining MIO ports. And almost all the IO ports (198) of the BANK13, BANK33, BAN34, and BANK35 on the PL side, where the IO levels of the BANK33 and BANK34 can be modified by replacing the LDO chip on the core board to meet the user's requirement that the level interface is not used. . For users who need a lot of IO, this core board will be a good choice. And the IO connection part, ZYNQ chip to interface between the wiring to do the same length and differential processing, and the core board size is only 60 * 60 (mm), for secondary development, is very suitable.

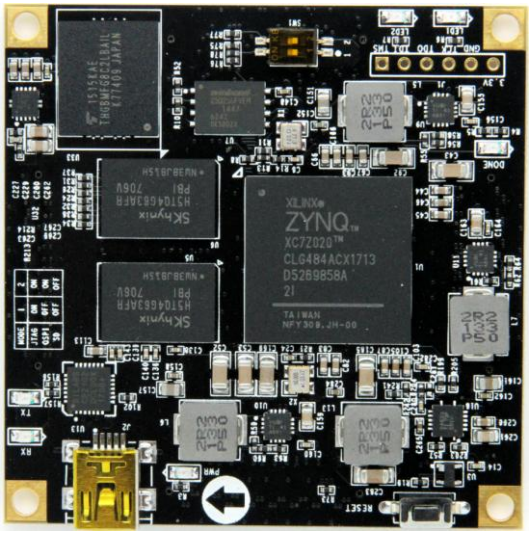


Figure 1-1

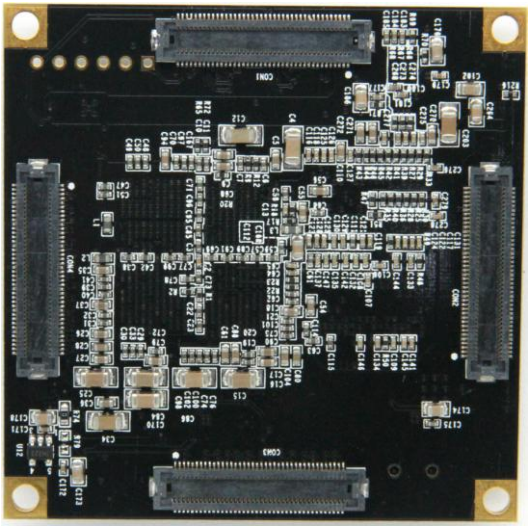


Figure 1-2

2. ZYNQ

The development board uses Xilinx's Zynq 7000 series chip, model XC7Z020-2CLG484I. The chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces, and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO and

so on. The PS can operate independently and start on power-up or reset. The overall block diagram of the ZYNQ7000 chip is shown in Figure 2-1

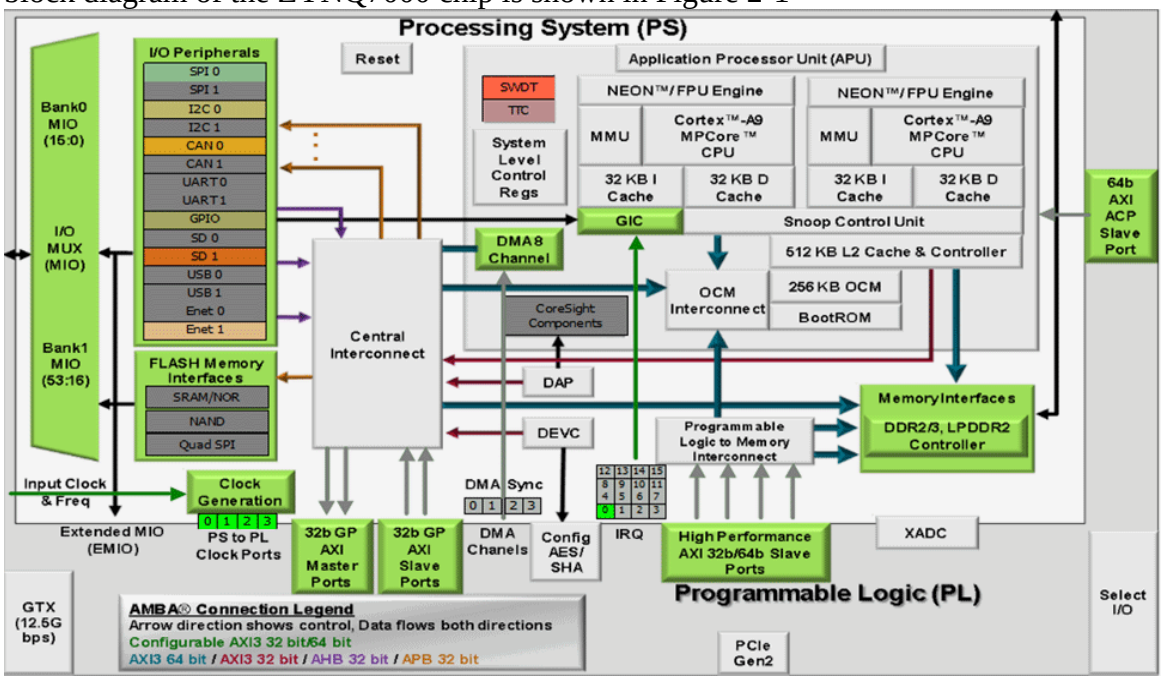


Figure 2-1

The main parameters of the PS system part are as follows:
- ARM-v7 architecture up to 1GHz based on ARM dual-core CortexA9 application processor
- 32KB Level 1 instruction and data cache per CPU, 512KB Level 2 cache shared by 2 CPUs
- On-chip boot ROM and 256KB on-chip RAM
- External memory interface supporting 16/32 bit DDR2, DDR3 interface
- Two Gigabit LAN Support: Divergent-Aggregate DMA, GMII, RGMII, SGMII Interfaces
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD Cards, SDIO, MMC Compatible Controllers
- 2 SPIs, 2 UARTs, 2 I2C Interfaces
- 4 sets of 32bit GPIO, 54 (32+22) as PS system IO, 64 connects to PL
- High bandwidth connections within PS and PS to PL

The main parameters of the PL logic section are as follows:
- Logic Cells: 85K;
- Lookup Table LUTs: 53,200
- Flip-flops: 106,400
- Multiplier 18x25MACCs:220;
- Block RAM: 4.9Mb;
- Two AD converters that can measure on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS

The XC7Z020-2CLG484I chip has a speed grade of -2, an industrial grade, and is packaged as a BGA484 with a pin pitch of 0.8mm. The specific chip model definition for the ZYNQ7000 series is shown in Figure 2-2.

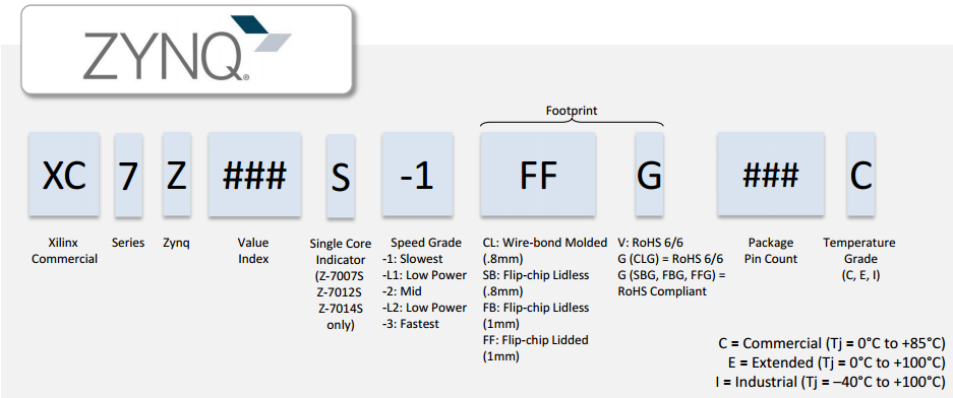


Figure 2-2

Figure 2-3 shows the physical map of the XC7Z020 chip used in the development board.

Figure 2-3

3. DDR3 DRAM

The AC7021 core board is equipped with two SK Hynix DDR3 SDRAM chips (1GB in total), model number H5TQ4G63AFR-PBI. The bus width of DDR3 SDRAM is 32 bits in total. The maximum operating speed of DDR3 SDRAM is up to 533MHz (data rate 1066Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 502 of the ZYNQ processing system (PS). The specific configuration of DDR3 SDRAM is shown in Table 3-1.

Position	Model	Capacity	Factory
U5,U6	H5TQ4G63AFR-PBI	256M Byte*16bit	SKHynix

Table 3-1

The hardware design of DDR3 needs to strictly consider the signal integrity. We have

fully considered the matching resistor/termination resistance, trace impedance control, and the length of the trace during the circuit design and PCB design to ensure the high-speed and stable operation of DDR3.
The hardware connection of DDR3 DRAM is shown in Figure 3-1.

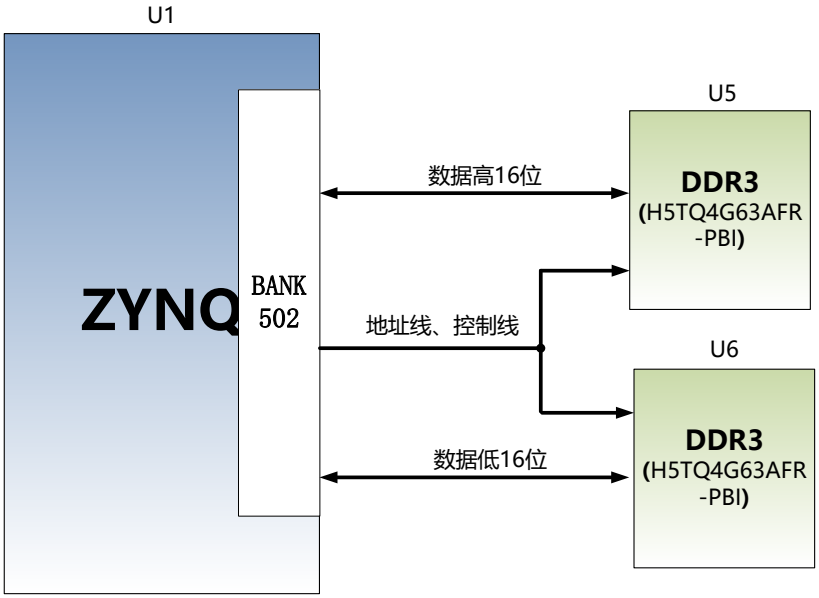


Figure 3-1

DDR3 DRAM Pin Assignment:

Signal Name	Pin Name	Pin Number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C2
DDR3_DQS0_N	PS_DDR_DQS_N0_502	D2
DDR3_DQS1_P	PS_DDR_DQS_P1_502	H2
DDR3_DQS1_N	PS_DDR_DQS_N1_502	J2
DDR3_DQS2_P	PS_DDR_DQS_P2_502	N2
DDR3_DQS2_N	PS_DDR_DQS_N2_502	P2
DDR3_DQS3_P	PS_DDR_DQS_P3_502	V2
DDR3_DQS4_N	PS_DDR_DQS_N3_502	W2
DDR3_D0	PS_DDR_DQ0_502	D1
DDR3_D1	PS_DDR_DQ1_502	C3
DDR3_D2	PS_DDR_DQ2_502	B2
DDR3_D3	PS_DDR_DQ3_502	D3
DDR3_D4	PS_DDR_DQ4_502	E3
DDR3_D5	PS_DDR_DQ5_502	E1
DDR3_D6	PS_DDR_DQ6_502	F2
DDR3_D7	PS_DDR_DQ7_502	F1
DDR3_D8	PS_DDR_DQ8_502	G2
DDR3_D9	PS_DDR_DQ9_502	G1
DDR3_D10	PS_DDR_DQ10_502	L1

DDR3_D11	PS_DDR_DQ11_502	L2
DDR3_D12	PS_DDR_DQ12_502	L3
DDR3_D13	PS_DDR_DQ13_502	K1
DDR3_D14	PS_DDR_DQ14_502	J1
DDR3_D15	PS_DDR_DQ15_502	K3
DDR3_D16	PS_DDR_DQ16_502	M1
DDR3_D17	PS_DDR_DQ17_502	T3
DDR3_D18	PS_DDR_DQ18_502	N3
DDR3_D19	PS_DDR_DQ19_502	T1
DDR3_D20	PS_DDR_DQ20_502	R3
DDR3_D21	PS_DDR_DQ21_502	T2
DDR3_D22	PS_DDR_DQ22_502	M2
DDR3_D23	PS_DDR_DQ23_502	R1
DDR3_D24	PS_DDR_DQ24_502	AA3
DDR3_D25	PS_DDR_DQ25_502	U1
DDR3_D26	PS_DDR_DQ26_502	AA1
DDR3_D27	PS_DDR_DQ27_502	U2
DDR3_D28	PS_DDR_DQ28_502	W1
DDR3_D29	PS_DDR_DQ29_502	Y3
DDR3_D30	PS_DDR_DQ30_502	W3
DDR3_D31	PS_DDR_DQ31_502	Y1
DDR3_DM0	PS_DDR_DM0_502	B1
DDR3_DM1	PS_DDR_DM1_502	H3
DDR3_DM2	PS_DDR_DM2_502	P1
DDR3_DM3	PS_DDR_DM3_502	AA2
DDR3_A0	PS_DDR_A0_502	M4
DDR3_A1	PS_DDR_A1_502	M5
DDR3_A2	PS_DDR_A2_502	K4
DDR3_A3	PS_DDR_A3_502	L4
DDR3_A4	PS_DDR_A4_502	K6
DDR3_A5	PS_DDR_A5_502	K5
DDR3_A6	PS_DDR_A6_502	J7
DDR3_A7	PS_DDR_A7_502	J6
DDR3_A8	PS_DDR_A8_502	J5
DDR3_A9	PS_DDR_A9_502	H5
DDR3_A10	PS_DDR_A10_502	J3
DDR3_A11	PS_DDR_A11_502	G5
DDR3_A12	PS_DDR_A12_502	H4
DDR3_A13	PS_DDR_A13_502	F4
DDR3_A14	PS_DDR_A14_502	G4

DDR3_BA0	PS_DDR_BA0_502	L7
DDR3_BA1	PS_DDR_BA1_502	L6
DDR3_BA2	PS_DDR_BA2_502	M6
DDR3_S0	PS_DDR_CS_B_502	P6
DDR3_RAS	PS_DDR_RAS_B_502	R5
DDR3_CAS	PS_DDR_CAS_B_502	P3
DDR3_WE	PS_DDR_WE_B_502	R4
DDR3_ODT	PS_DDR_ODT_502	P5
DDR3_RESET	PS_DDR_DRST_B_502	F3
DDR3_CLK0_P	PS_DDR_CKP_502	N4
DDR3_CLK0_N	PS_DDR_CKN_502	N5
DDR3_CKE	PS_DDR_CKE_502	V3

4. QSPI Flash

The core board has a 256MBit Quad-SPI FLASH chip, model W25Q256FVEI, which uses a 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, in use, it can be used as the boot device of the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific model and related parameters of QSPI FLASH are shown in Table 4-1.

Position	Model	Capacity	Factory
U7	W25Q256FVEI	32M Byte	Winbond

Table 4-1

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 2-4-1 shows the QSPI Flash in the schematic.

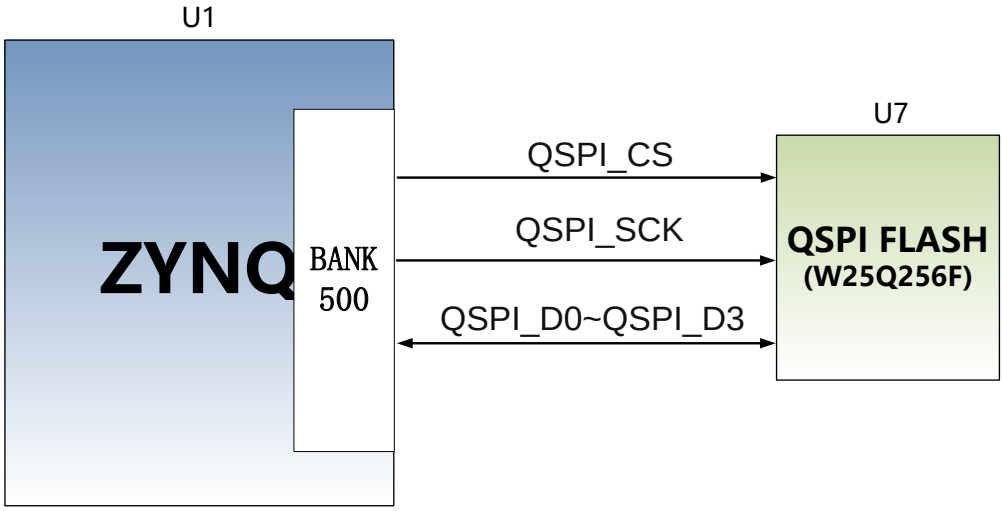


Figure 4-1

Pin Assignment:

Signal Name	Pin Name	Pin Number
QSPI_SCK	PS_MIO6_500	A4
QSPI_CS	PS_MIO1_500	A1
QSPI_D0	PS_MIO2_500	A2
QSPI_D1	PS_MIO3_500	F6
QSPI_D2	PS_MIO4_500	E4
QSPI_D3	PS_MIO5_500	A3

5. eMMC Flash

The core board have a large-capacity 32GB eMMC FLASH chip, model THGBMFG8C2LBAIL, which supports the HS-MMC interface of the JEDEC e-MMC V5.0 standard, and the level supports 1.8V or 3.3V. The data width of eMMC FLASH and ZYNQ connections is 4 bits. Due to the large capacity and non-volatile nature of eMMC FLASH, it can be used as a large-capacity storage device in the ZYNQ system, such as storing ARM applications, system files, and other user data files. The specific models and related parameters of eMMC FLASH are shown in Table 5-1.

eMMC Pin Assignment:

Position	**Model**	**Capacity**	**Factory**
U33	THGBMFG8C2LBAIL	32G Byte	TOSHIBA

Table 5-1

The eMMC FLASH is connected to the GPIO port of the BANK501 of the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the SD interface. Figure 5-1 shows the eMMC Flash in the schematic.

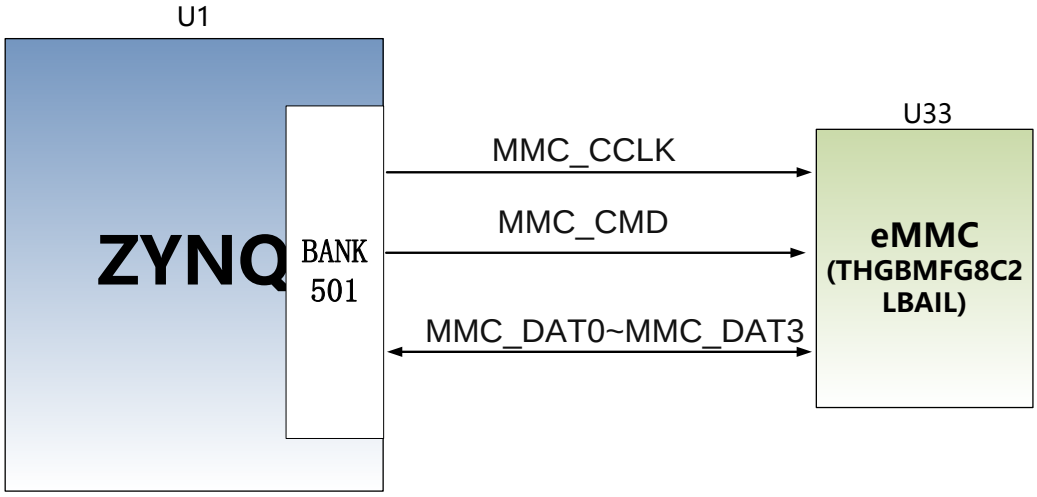


Figure 5-1

Pin Assignment:

Signal Name	Pin Name	Pin Number
MMC_CCLK	PS_MIO48_501	D11

MMC_CMD	PS_MIO47_501	B10
MMC_D0	PS_MIO46_501	D12
MMC_D1	PS_MIO49_501	C14
MMC_D2	PS_MIO50_501	D13
MMC_D3	PS_MIO51_501	C10

6. Clock source

The AC7021 core board provides active clocks for the PS system and the PL logic sections, respectively, so that the PS system and the PL logic can work independently.

PS system clock source

The ZYNQ chip provides a 33.333 MHz clock input to the PS section through the X1 crystal on the development board. The input of the clock is connected to the pins of PS_CLK_500 of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 6-1:

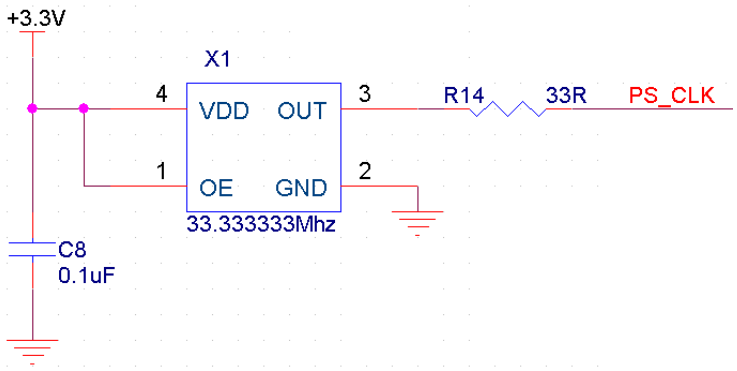


Figure 6-1

PS Clock pin assignment:

Signal Name	Pin
PS_CLK_500	F7

PL system clock source

The AC7021 core board provides a single-ended 50MHz PL system clock source with 3.3V supply. The crystal output is connected to the global clock (MRCC) of the FPGA BANK13, which can be used to drive the user logic within the FPGA. The schematic of this clock source is shown in Figure 6-2.

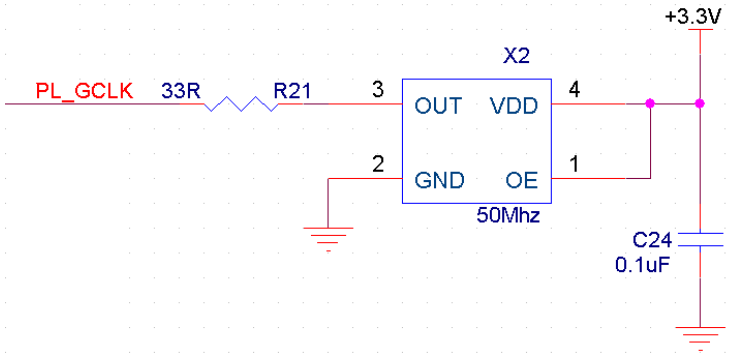


Figure 6-2

PL Clock pin assignment:

Signal Name	Pin
PL_GCLK	Y9

7. USB to UART

For the AC7021 core board to work and debug separately, we have a Uart to USB interface for the core board. Used for power supply and debugging of the core board. The conversion chip adopts the USB-UAR chip of Silicon Labs CP2102GM. The USB interface adopts the MINI USB interface. It can connect it to the USB port of the upper PC for independent power supply and serial port data communication using a USB cable. A schematic diagram of USB Uart circuit design is shown in Figure 7-1.

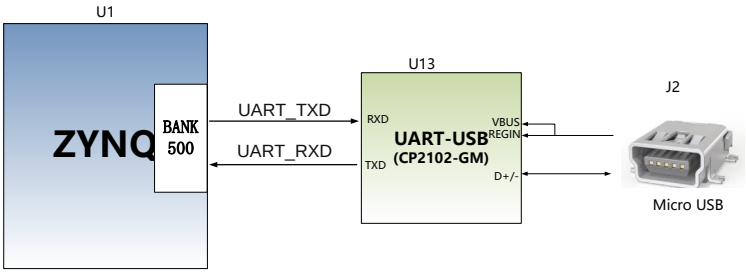


Figure7-1

Uart Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
UART_RXD	PS_MIO14_500	B6	Uart data output
UART_TXD	PS_MIO15_500	E6	Uart data input

8. LED

The AC7021 core board has four red LEDs, one of which is a power indicator (PWR), one is a configuration LED (DONE), and two are user LED (LED1~LED2). When the core board is powered up, the power indicator lights up; when the FPGA is configured, the configuration LED lights up. Two user LED lights One is connected to the MIO of the PS. One is connected to the IO of the PL. The user can control the light on and off

through the program. When the voltage of the IO connected to the user LED lamp is high, the user LED light goes out when the connection is made. When the IO voltage is low, the user LED will be lit. The schematic diagram of the LED lamp hardware connection is shown in Figure 8-1.

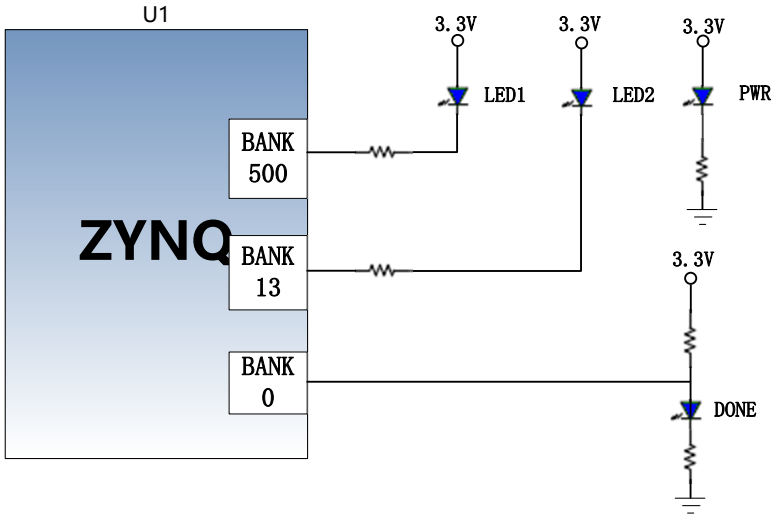


Figure 8-1

LED Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
MIO0_LED	PS_MIO0_500	G6	User LED1
PL_LED	IO_0_13	R7	User LED2

9. Reset Key

There is a reset button RESET and circuit on the core board of AC7021. The reset signal is connected to the PS reset pin of ZYNQ chip. Users can use this reset button to reset the ZYNQ system. Pressing the reset button will reset the chip to generate a low level reset signal to the ZYNQ chip. A schematic diagram of the reset button and reset chip connection is shown in Figure 9-1.

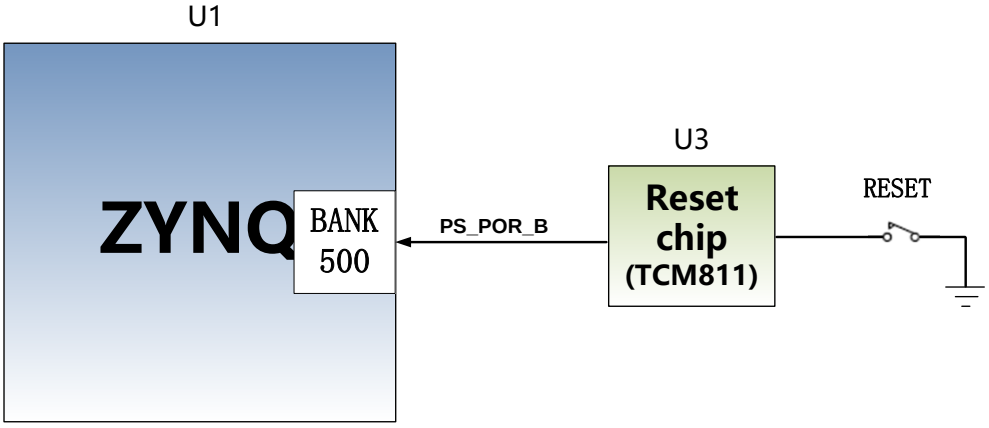


Figure 9-1

Reset Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain

PS_POR_B	PS_POR_B_500	B5	Reset Key

10. JTAG

On the AC7021 core board, we also reserved JTAG test socket J1 for JTAG download and debugging of the core board. Figure 10-1 is the schematic part of the JTAG port, which relates to TMS, TDI, TDO, and TCK. , GND, +3.3V These six signals.

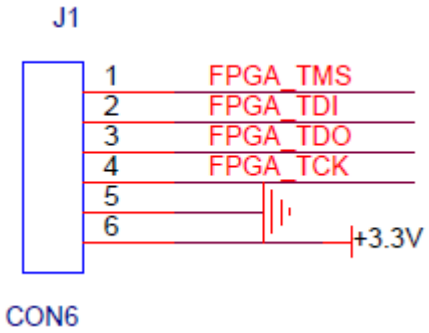


Figure 10-1

The JTAG interface J1 on the core board uses a 6-pin 2.54mm pitch single-row test hole. If the user needs JTAG connection debugging on the core board, it needs to weld 6-pin single row pins.

11. Start configuration

A 2-bit code switch SW1 is used on the AC7021 core board to configure the boot mode of the ZYNQ system. The AC7021 system development platform supports three startup modes. The three boot modes are JTAG debug mode, QSPI FLASH and SD card boot mode. After the chip is powered on, the XC7Z020 detects the level of the responding MIO (MIO5 and MIO4) to determine which boot mode. Users can select different boot modes through the DIP switch SW1 on the core board. The SW1 startup mode is configured as shown in Table 11-1.

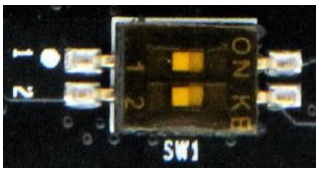
SW1	Position（1，2）	MIO5,MIO4 Level	Startup mode
	ON、ON	0、0	JTAG
	OFF、OFF	1、1	SD Card
	OFF、ON	1、0	QSPI FLASH

Table 11-1

12. Power

The power supply voltage of the AC7021 core board is DC5V. When it is used alone, power is supplied through the Mini USB interface. When the board is connected to the chassis, power is supplied through the expansion board. Please be careful not to supply power to the Mini USB and the chassis at the same time to avoid damage. The power supply design on the board is shown in Figure 12-1.

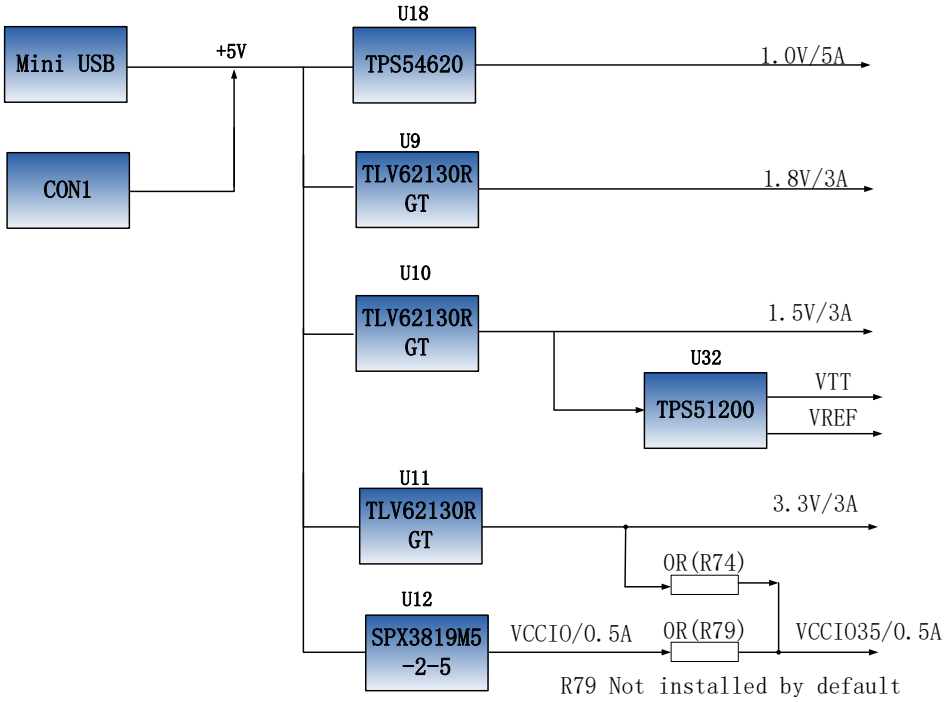


Figure 12-1

The development board is powered by +5V, and converted to +1.0V, +1.8V, +1.5V, +3.3V four-way power supply via four-way DC/DC power supply chips TPS54620 and TLV62130RGT. The +1.0V output current can be as high as 5A, and the other 3 Road power is 3A. The VCCIO 2.5V power supply is generated by one LDO SPX3819M5-2-5. The VCCIO 2.5V power supply can be selected as BANK33 and BANK34 BANK power supplies for the FPGA. The user can select BANK33 and BANK34 with two 0 ohm resistors (R74, R79). Power supply. The default development board R74 is installed, R79's resistance is not installed, so the BANK33, BANK34 power supply is +3.3V. The user can replace the resistor so that the BANK33, 34's IO output voltage is 2.5V. 1.5V generates the VTT and VREF voltages required for DDR3 through TI's TPS51200. The functions of each power distribution are shown in the following table 12-1:

Power	Function
+1.0V	**ZYNQ PS and PL section core voltage**
+1.8V	**ZYNQ PS and PL partial auxiliary voltage, BANK501 IO voltage, eMMC**
+3.3V	**ZYNQ Bank0,Bank500，Bank13，Bank34 的 VCCIO, QSIP FLASH, Clock**
+1.5V	**DDR3, ZYNQ Bank501**
VREF, VTT（+0.75V）	**DDR3**
VCCIO(+2.5V)	**Reserved for ZYNQ Bank33,Bank 34**

Table 12-1

Because the power supply of the ZYNQ FPGA has the order of power on, we have designed according to the power requirements of the chip in the circuit design, and the power supply is +1.0V->+1.8V->(+1.5 V, +3.3V, VCCIO) The circuit design of the chip

ensures the normal operation of the chip.
The power circuit of the AC7021 core board is shown in Figure 12-2 below.

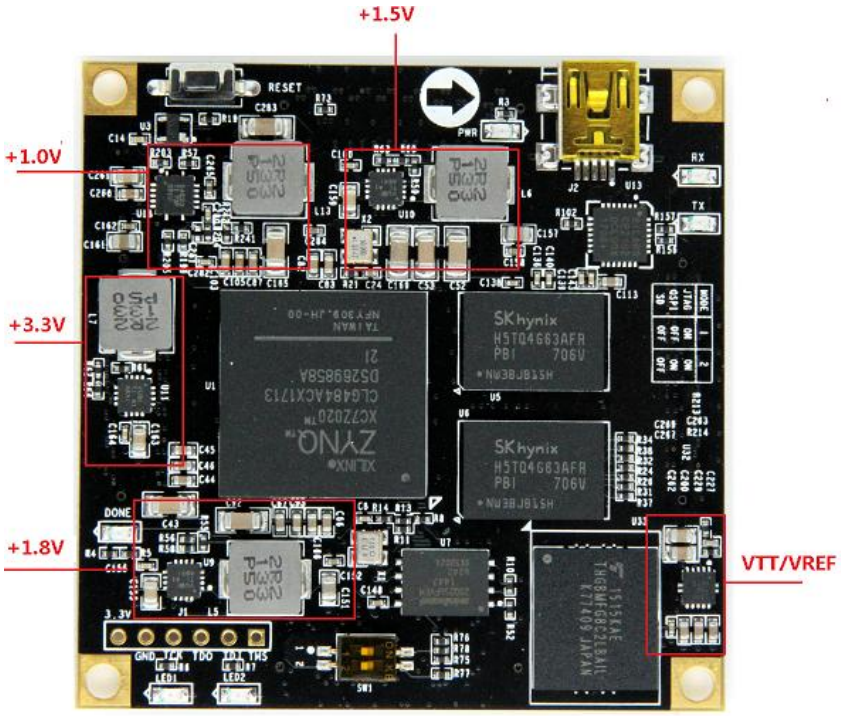
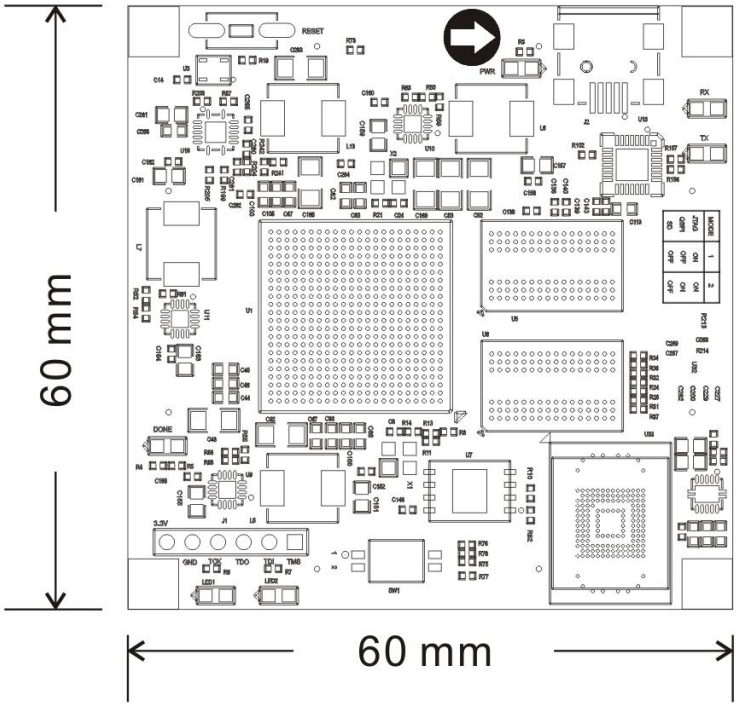


Figure 12-2

13. Structure



Expansion Board

1. Overview

Expansion board function

- 5 10/100M/1000M Ethernet RJ-45 Interface
- 1 HDMI output display interface
- 4 USB HOST interface
- 1 USB Uart Communication Interface
- 1 SD card interface
- 2 40-pin expansion port
- JTAG debugging interface
- 2 independent keys
- 2 user LED lights

2. Ethernet

There are five Gigabit Ethernet interfaces on the AX7021 expansion board. One Ethernet interface is connected to the PS system and the other four Ethernet interfaces are connected to the logical IO port of the PL. The 4 Gigabit Ethernet interface connected to the PL side needs to be called by program to IP mount on the AXI bus system of ZYNQ. The Ethernet chip uses Micrel's KSZ9031RNX Ethernet PHY chip to provide users with network communication services. The Ethernet PHY chip on the PS side is connected to the GPIO interface of the BANK501 on the PS side of ZYNQ. The Ethernet PHY chip on the PL side is connected to the IOs of BANK33 and BANK34. The KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate and communicates with the Zynq7000 system's MAC layer through the RGMII interface. The KSZ9031RNX supports MDI/MDX adaptation, various speed adaptations, Master/Slave adaptation, and MDIO bus support for PHY register management.
When the KSZ9031RNX is powered on, it detects certain IO levels to determine its own operating mode. Table 2-2-1 describes the default settings after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 011
CLK125_EN	Enable 125Mhz clock output selection	Enable
LED_MODE	LED light mode configuration	Single LED light mode
MODE0~MODE3	Link adaptation and full duplex configuration	10/100/1000 adaptive, compatible with full-duplex, half-duplex

Table 2-2-1

When the network is connected to Gigabit Ethernet, the data of ZYNQ and PHY chip

KSZ9031RNX is transmitted through the RGMII bus when the data is transmitted, and the transfer clock is 125Mhz. The data is sampled at the rising edge and falling sample of the clock.
When the network is connected to Fast Ethernet, data transmission between the ZYNQ and PHY chip KSZ9031RNX is performed through the RMII bus and the transmission clock is 25 MHz. Data is sampled on the rising edge and falling samples of the clock.
Figure 2-2-1 shows the connection of a 1-channel Ethernet PHY chip on the ZYNQ PS side:

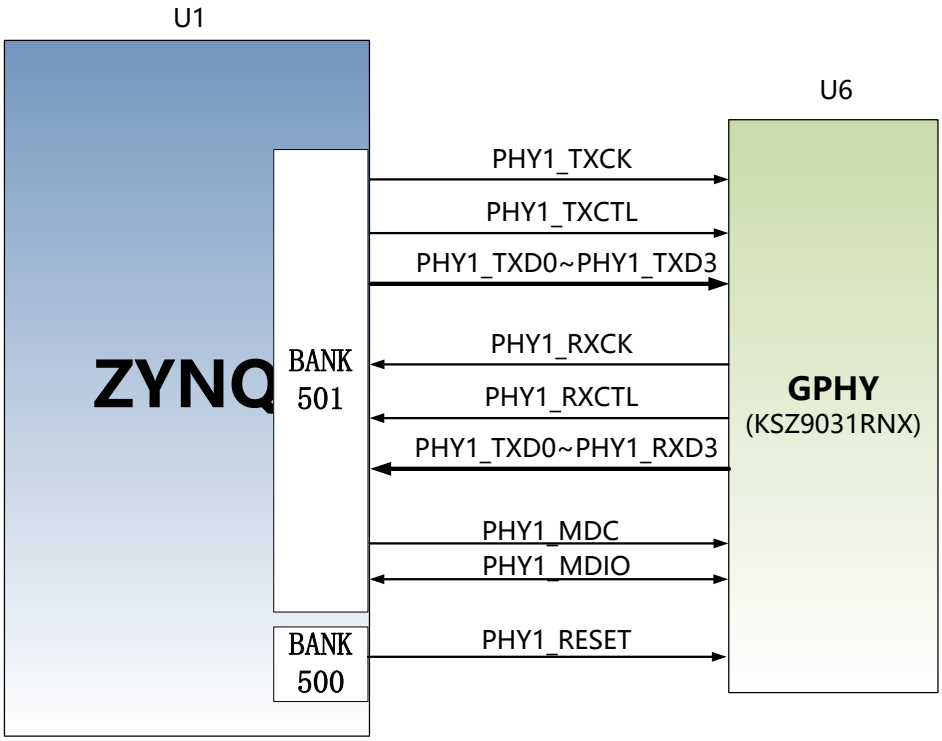


Figure 2-2-1

Figure 2-2-2 shows the connection of the four-node Ethernet PHY chip on the ZYNQ PL side:

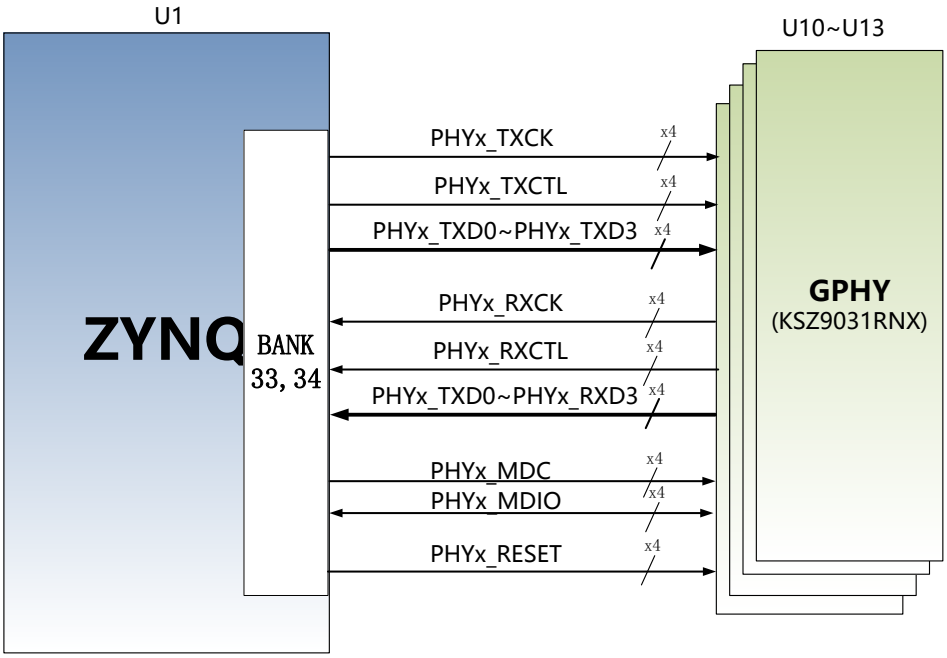


Figure 2-2-2

ETH0(PS) Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY1_TXCK	PS_MIO16_501	D6	RGMII Send clock
PHY1_TXD0	PS_MIO17_501	E9	Send data bit 0
PHY1_TXD1	PS_MIO18_501	A7	Send data bit1
PHY1_TXD2	PS_MIO19_501	E10	Send data bit2
PHY1_TXD3	PS_MIO20_501	A8	Send data bit3
PHY1_TXCTL	PS_MIO21_501	F11	Send enable signal
PHY1_RXCK	PS_MIO22_501	A14	RGMII Receive clock
PHY1_RXD0	PS_MIO23_501	E11	Receive data Bit0
PHY1_RXD1	PS_MIO24_501	B7	Receive data Bit1
PHY1_RXD2	PS_MIO25_501	F12	Receive data Bit2
PHY1_RXD3	PS_MIO26_501	A13	Receive data Bit3
PHY1_RXCTL	PS_MIO27_501	D7	Receive data valid signal
PHY1_MDC	PS_MIO52_501	D10	MDIO Management clock
PHY1_MDIO	PS_MIO53_501	C12	MDIO Management clock

ETH1(PL) Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY2_TXCK	B34_L17_N	R21	RGMII Send clock

PHY2_TXD0	B34_L5_P	N17	Send data bit 0
PHY2_TXD1	B34_L5_N	N18	Send data bit1
PHY2_TXD2	B34_L14_P	N19	Send data bit2
PHY2_TXD3	B34_L14_N	N20	Send data bit3
PHY2_TXCTL	B34_L17_P	R20	Send enable signal
PHY2_RXCK	B34_L11_P	K19	RGMII Receive clock
PHY2_RXD0	B34_L7_P	J18	Receive data Bit0
PHY2_RXD1	B34_L7_N	K18	Receive data Bit1
PHY2_RXD2	B34_L1_P	J15	Receive data Bit2
PHY2_RXD3	B34_L1_N	K15	Receive data Bit3
PHY2_RXCTL	B34_L11_N	K20	Receive data valid signal
PHY2_MDC	B34_L2_N	J17	MDIO Management clock
PHY2_MDIO	B34_L2_P	J16	MDIO Management data

ETH2(PL) Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY3_TXCK	B34_L3_P	K16	RGMII Send clock
PHY3_TXD0	B34_L12_P	L18	Send data bit 0
PHY3_TXD1	B34_L10_N	L22	Send data bit1
PHY3_TXD2	B34_L10_P	L21	Send data bit2
PHY3_TXD3	B34_L3_N	L16	Send data bit3
PHY3_TXCTL	B34_L15_N	M22	Send enable signal
PHY3_RXCK	B34_L13_P	M19	RGMII Receive clock
PHY3_RXD0	B34_L20_N	P18	Receive data Bit0
PHY3_RXD1	B34_L16_N	P22	Receive data Bit1
PHY3_RXD2	B34_L16_P	N22	Receive data Bit2
PHY3_RXD3	B34_L15_P	M21	Receive data Bit3
PHY3_RXCTL	B34_L20_P	P17	Receive data valid signal
PHY3_MDC	B34_L13_N	M20	MDIO Management clock
PHY3_MDIO	B34_L21_N	T17	MDIO Management data

ETH3(PL) Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY4_TXCK	B33_L17_P	AA17	RGMII Send clock
PHY4_TXD0	B33_L6_P	V18	Send data bit 0

PHY4_TXD1	B33_L16_P	U17	Send data bit1
PHY4_TXD2	B33_L16_N	V17	Send data bit2
PHY4_TXD3	B33_L17_N	AB17	Send data bit3
PHY4_TXCTL	B33_L7_P	AA22	Send enable signal
PHY4_RXCK	B33_L14_P	W16	RGMII Receive clock
PHY4_RXD0	B33_L15_N	U16	Receive data Bit0
PHY4_RXD1	B33_L19_P	V14	Receive data Bit1
PHY4_RXD2	B33_L19_N	V15	Receive data Bit2
PHY4_RXD3	B33_L7_N	AB22	Receive data Bit3
PHY4_RXCTL	B33_L15_P	U15	Receive data valid signal
PHY4_MDC	B33_L14_N	Y16	MDIO Management clock
PHY4_MDIO	B33_L22_P	Y14	MDIO Management data

ETH4(PL) Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PHY5_TXCK	B33_L24_N	AB15	RGMII Send clock
PHY5_TXD0	B33_L20_P	V13	Send data bit 0
PHY5_TXD1	B33_L20_N	W13	Send data bit1
PHY5_TXD2	B33_L23_P	Y13	Send data bit2
PHY5_TXD3	B33_L23_N	AA13	Send data bit3
PHY5_TXCTL	B33_L24_P	AB14	Send enable signal
PHY5_RXCK	B33_L13_P	W17	RGMII Receive clock
PHY5_RXD0	B33_L18_N	AB16	Receive data Bit0
PHY5_RXD1	B33_L18_P	AA16	Receive data Bit1
PHY5_RXD2	B33_L21_N	Y15	Receive data Bit2
PHY5_RXD3	B33_L21_P	W15	Receive data Bit3
PHY5_RXCTL	B33_L13_N	W18	Receive data valid signal
PHY5_MDC	B33_L12_P	Y18	MDIO Management clock
PHY5_MDIO	B33_L12_N	AA18	MDIO Management data

3. USB2.0 Host

There are four USB2.0 HOST interfaces on the AX7021 expansion board. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI

standard interface, and then expands out of four USB channels through a USB HUB chip USB2514. HOST interface. ZYNQ's USB bus interface is connected to the USB3320C-EZK transceiver to enable high-speed USB 2.0 Host mode data communication. The data and control signals of the USB3320C USB are connected to the IO port of the BANK501 on the PS side of the ZYNQ chip. The USB differential signal (DP/DM) is connected to the USB2514 chip to expand the four USB ports. Two 24MHz crystal oscillators provide the system clock for the USB3320C and USB2514 chips, respectively.

The USB interface is a flat USB interface (USB Type A), which allows users to simultaneously connect different USB Slave peripherals (such as USB mouse and USB keyboard). In addition, the expansion board also provides +5V power for each USB interface.

Figure 2-3-1 shows the connection between the ZYNQ processor, the USB3320C-EZK chip and the USB2514 chip.

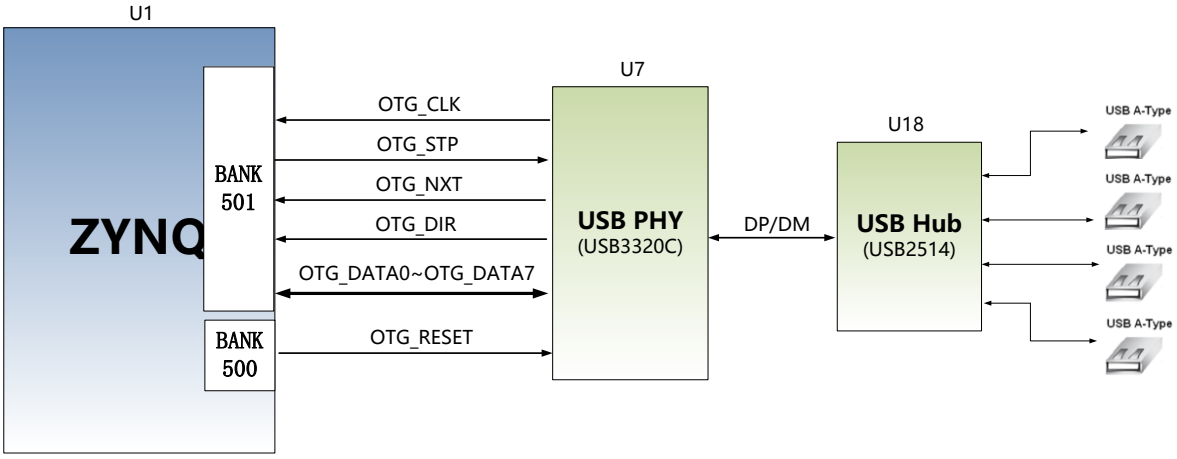


Figure2-3-1

USB2.0 Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
OTG_DATA4	PS_MIO28_501	A12	USB data bit4
OTG_DIR	PS_MIO29_501	E8	USB data direction signal
OTG_STP	PS_MIO30_501	A11	USB stop signal
OTG_NXT	PS_MIO31_501	F9	USB next data signal
OTG_DATA0	PS_MIO32_501	C7	USB data bit0
OTG_DATA1	PS_MIO33_501	G13	USB data bit1
OTG_DATA2	PS_MIO34_501	B12	USB data bit2
OTG_DATA3	PS_MIO35_501	F14	USB data bit3
OTG_CLK	PS_MIO36_501	A9	USB clock signal
OTG_DATA5	PS_MIO37_501	B14	USB data bit5
OTG_DATA6	PS_MIO38_501	F13	USB data bit6
OTG_DATA7	PS_MIO39_501	C13	USB data bit7
OTG_RESETN	PS_MIO8_500	E5	USB reset signal

4. HDMI OUT

The HDMI output interface uses Silion Image's SIL9134 HDMI (DVI) encoding chip, which supports up to 1080P@60Hz output and supports 3D output.
Among them, the SIL9134's video digital interface, audio digital interface and I2C configuration interface are connected to the BANK35 IO of the ZYNQ7000 PL. The ZYNQ7000 system uses the I2C pin to initialize and control the SIL9134. The hardware connection between the SIL9134 chip and the ZYNQ7000 is shown in Figure 2-4-1.

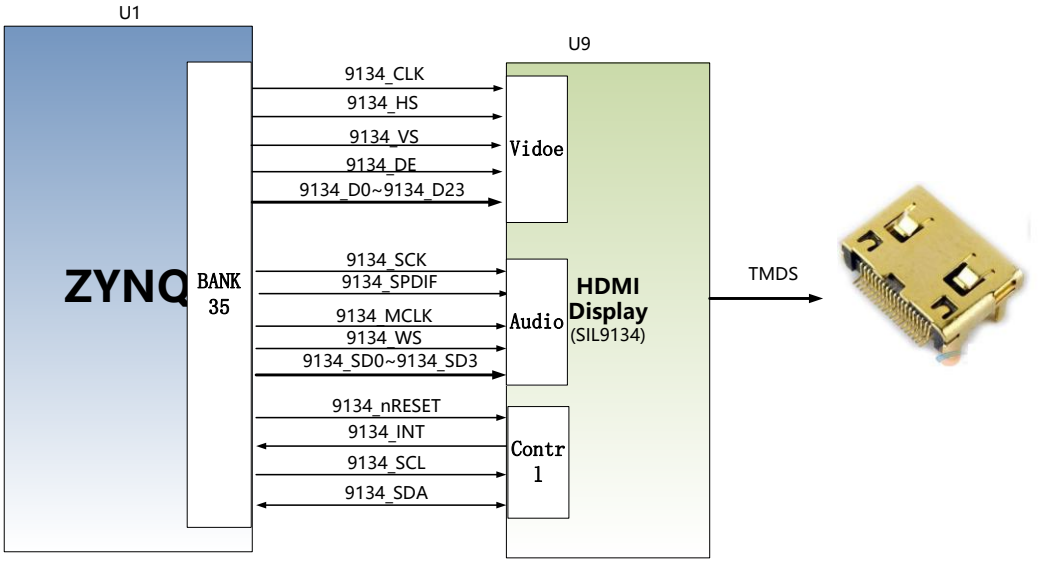


Figure3-4-1

HDMI out Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
9134_CLK	B35_L4_N	G16	clock
9134_HS	B35_L21_P	E19	line synchronization
9134_VS	B35_L1_P	F16	column synchronization
9134_DE	B35_L21_N	E20	Signal valid
9134_D[0]	B35_L24_P	H22	Data0
9134_D[1]	B35_L24_N	G22	Data 1
9134_D[2]	B35_L6_P	G17	Data 2
9134_D[3]	B35_L6_N	F17	Data 3
9134_D[4]	B35_L4_P	G15	Data 4
9134_D[5]	B35_L3_N	D15	Data 5
9134_D[6]	B35_L3_P	E15	Data 6
9134_D[7]	B35_L5_P	F18	Data 7
9134_D[8]	B35_L5_N	E18	Data 8
9134_D[9]	B35_IO0	H17	Data 9
9134_D[10]	B35_IO25	H18	Data 10
9134_D[11]	B35_L19_P	H19	Data 11

9134_D[12]	B35_L19_N	H20	Data 12
9134_D[13]	B35_L20_P	G19	Data 13
9134_D[14]	B35_L20_N	F19	Data 14
9134_D[15]	B35_L22_P	G20	Data 15
9134_D[16]	B35_L22_N	G21	Data 16
9134_D[17]	B35_L23_P	F21	Data 17
9134_D[18]	B35_L23_N	F22	Data 18
9134_D[19]	B35_L17_P	E21	Data 19
9134_D[20]	B35_L17_N	D21	Data 20
9134_D[21]	B35_L16_P	D22	Data 21
9134_D[22]	B35_L16_N	C22	Data 22
9134_D[23]	B35_L18_P	B21	Data 23
9134_SCK	B35_L13_P	B19	Audio Interface I2S Clock
9134_SPDIF	B35_L1_N	E16	Audio S/PDIF input
9134_MCLK	B35_L2_P	D16	Audio input master clock
9134_WS	B35_L14_N	C20	Audio interface I2S word selection
9134_SD0	B35_L14_P	D20	Audio Interface I2S Data0
9134_SD1	B35_L12_P	D18	Audio Interface I2S Data1
9134_SD2	B35_L12_N	C19	Audio Interface I2S Data2
9134_SD3	B35_L2_N	D17	Audio Interface I2S Data3
9134_nRESET	B35_L11_P	C17	Reset signal
9134_INT	B35_L13_N	B20	Interrupt signal
9134_SCL	B35_L18_N	B22	IIC control clock
9134_SDA	B35_L15_N	A22	IIC Control data

5. USB to UART

The AX7021 expansion board also has a serial port interface for debugging of the ZYNQ7000 system. The conversion chip uses a USB-UAR chip from Silicon Labs CP2102GM. The USB interface uses a MINI USB interface, which can be connected to the PC using a USB cable. The USB port provides separate power supply and serial data communication for the core board.
The USB Uart circuit design diagram is shown in Figure 2-5-1.:

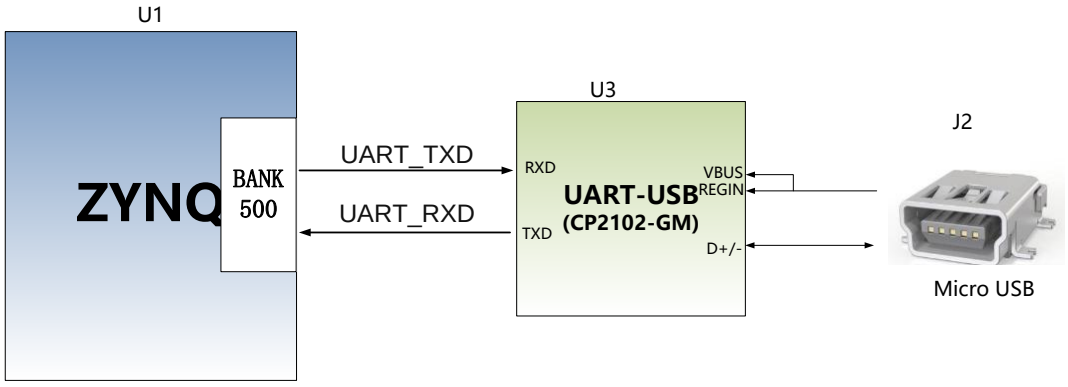


Figure 2-5-1

Uart Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
UART_RXD	PS_MIO13_500	A6	Uart data input
UART_TXD	PS_MIO12_500	C5	Uart data output

6. SD Card Slot

The AX7021 expansion board contains a Micro SD card interface to provide user access to SD card memory, BOOT programs for storing ZYNQ chips, Linux operating system kernels, file systems, and other user data files.

The SDIO signal is connected to the IO signal of the PSNKNK501 of the ZYNQ. Since the VCCMIO of the BANK is set to 1.8V, the data level of the SD card is 3.3V, and we connect here through the TXS02612 level converter. Figure 2-6-1 shows the schematic of the Zynq7000 PS and SD card connectors.

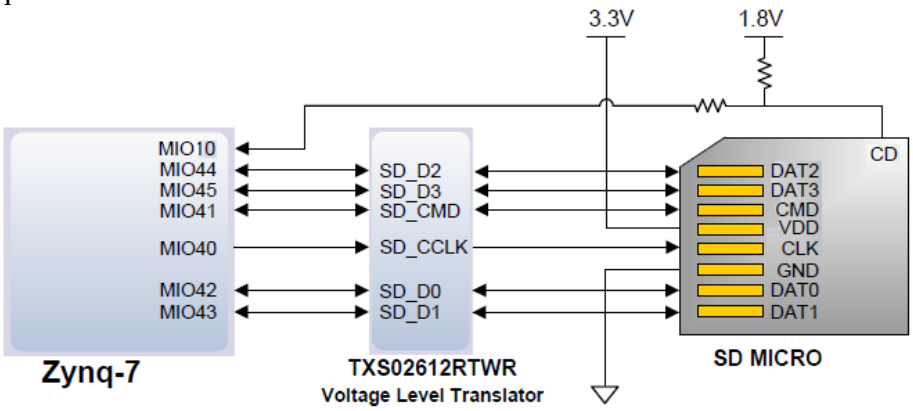


Figure 2-6-1

Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
SD_CLK	PS_MIO40	E14	SD clock signal
SD_CMD	PS_MIO41	C8	SD command signal
SD_D0	PS_MIO42	D8	SD data0
SD_D1	PS_MIO43	B11	SD data1
SD_D2	PS_MIO44	E13	SD data2

SD_D3	PS_MIO45	B9	SD data3
SD_CD	PS_MIO10	G7	SD card insert signal

7. JTAG

The AX7021 has integrated JTAG download debug circuitry, so users do not need to purchase additional Xilinx downloaders. As long as a USB cable can be ZYNQ development and debugging. In the development board through a FTDI USB bridge chip FT232HL PC USB and ZYNQ JTAG debug signals TCK, TDO, TMS, TDI for data communication. Figure 2-7-1 shows the schematic part of the JTAG port on the development board:

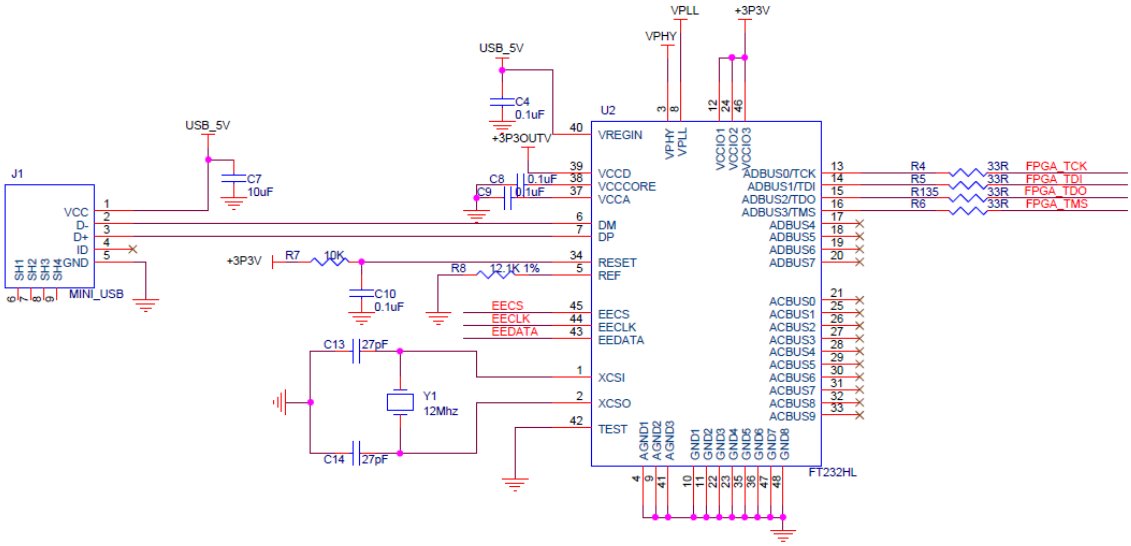


Figure 2-7-1

8. User LED

The AX7021 has 3 red LEDs, one of which is the power indicator (PWR) and two of which are user LEDs (LED1~LED2). When the expansion board is powered on, the power indicator will light; 2 user LED lights are connected to the MIO of the PS, and one is connected to the IO of the PL. The user can control the light on and off through the program when connecting the IO voltage of the user LED lights. When it is high, the user's LED light goes out, and when the connected IO voltage is low, the user's LED will be lit. The schematic diagram of the LED lamp hardware connection is shown in Figure 2-8-1.

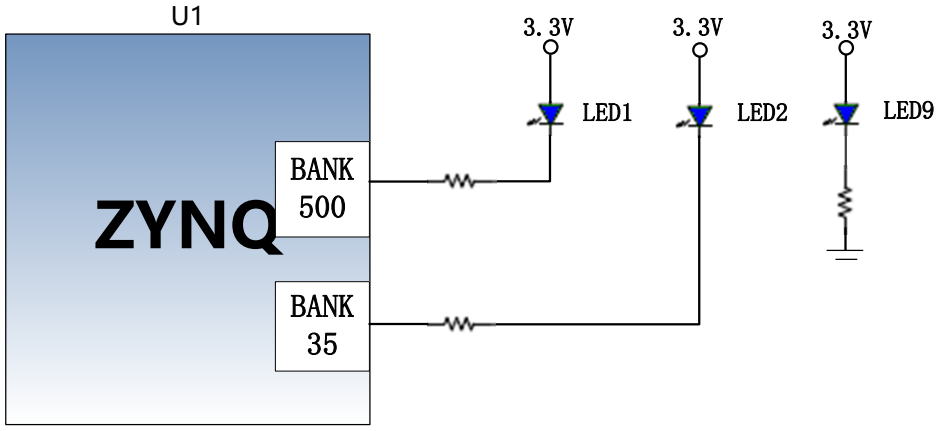


Figure 2-8-1

Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
PS_LED	PS_MIO9_500	C4	PS LED
PL_LED	B35_L9_P	A16	PL LED

9. User Key

There are two user buttons KEY1 and KEY2 on the AX7021 board. KEY1 is connected to the MIO pin of the ZYNQ chip PS, and KEY2 is connected to the IO pin of the ZYNQ chip PL. When the button is pressed, the signal is low and the ZYNQ chip detects a low level to determine whether the button is pressed. The schematic diagram of the user's key connection is shown in Figure 2-9-1:

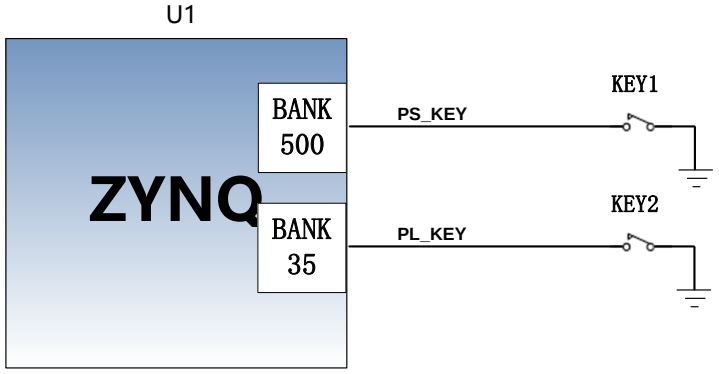


Figure 2-9-1

Pin Assignment:

Pin	Signal Name	Pin Name	Pin Number
PS_KEY	PS_MIO11_500	B4	PS User Key
PL_KEY	B35_L9_N	A17	PL User Key

10. Expansion

The AX7021 base board has two 40-pin expansion ports J15 and J16 with 2.54mm standard spacing, which are used to connect the modules or the user's own external circuit design. The expansion port has 40 signals. Never directly connect IO directly to 5V devices to avoid burning the ZYNQ7000 chip. If you want to connect 5V equipment, you need to connect the level conversion chip.

A 33 ohm resistor is connected in series between the expansion port and the ZYNQ7000 connection to protect the ZYNQ7000 chip from damage due to excessive external voltage or current. The circuit of the expansion port (J15) is shown in Figure 2-10-1.

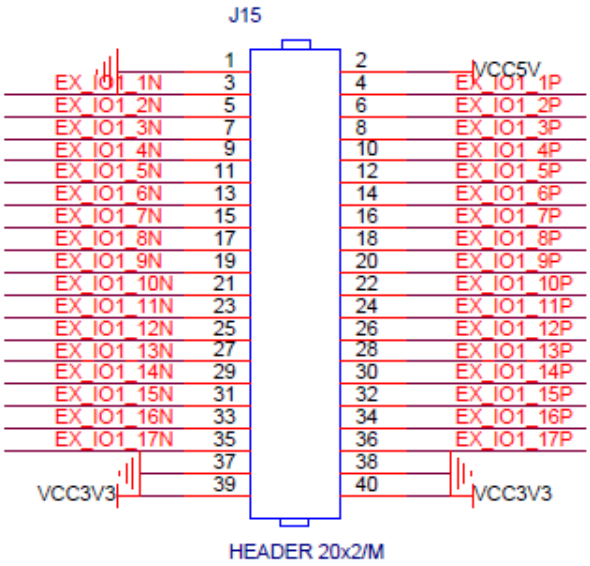


Figure 2-10-1

J15 Pin Assignment:

Pin	Signal Name	Pin Name	Pin Number
1	GND	2	+5V（Input）
3	T21	4	U21
5	U20	6	V20
7	Y19	8	AA19
9	J21	10	J22
11	K21	12	J20
13	P16	14	R16
15	M17	16	L17
17	T18	18	R18
19	P20	20	P21
21	T19	22	R19
23	P15	24	N15
25	M16	26	M15
27	AB19	28	AB20
29	W22	30	V22
31	W21	32	W20
33	AA21	34	AB21
35	Y21	36	Y20
37	GND	38	GND
39	+3.3V	40	+3.3V（Output）

The circuit of the expansion port (J16) is shown in Figure 2-10-2.

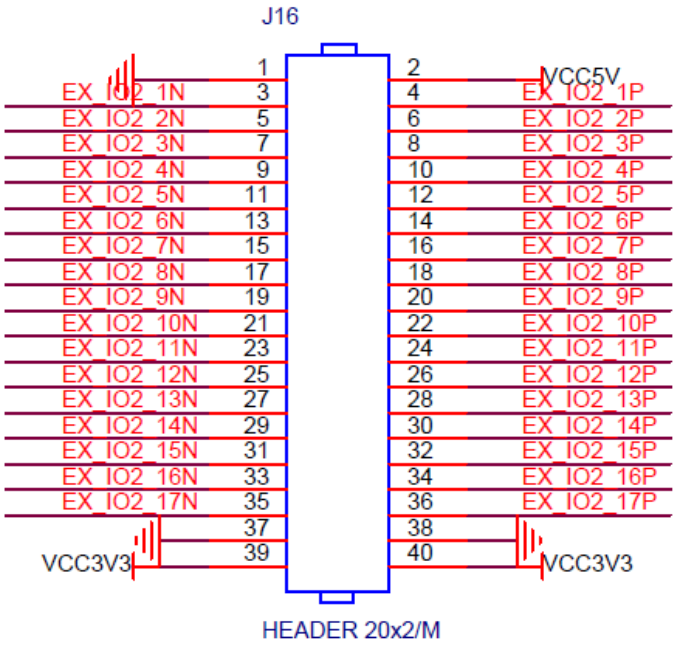


Figure 2-10-2

J16 Pin Assignment:

Pin	Signal Name	Pin Name	Pin Number
1	GND	2	+5V
3	V12	4	W12
5	U12	6	U11
7	U9	8	U10
9	T6	10	R6
11	U5	12	U6
13	U4	14	T4
15	W10	16	W11
17	Y10	18	Y11
19	W8	20	V8
21	AA6	22	AA7
23	AA11	24	AB11
25	AB4	26	AB5
27	AB1	28	AB2
29	Y4	30	AA4
31	AB10	32	AB9
33	AA9	34	AA8
35	AB7	36	AB6
37	GND	38	GND
39	+3.3V	40	+3.3V

11. Power

The power input voltage of the development board is DC12V. Please use the power supply of the development board. Do not use other specifications of the power supply to avoid damage to the development board. The base plate is converted to +5V, +1.2V, +3.3V and 1.8V four power supplies via one-way DC/DC power supply chip MP2303 and three-way DC/DC power supply chip MP1482. Because the +5V power supply powers the core board through the inter-board connector, the DCDC power supply has a current output of 3A and the other three power supply current outputs are 2A. There is also a LDO chip on the board. The default output is 3.3V. If the BANK33 and BANK34 BANK power supplies of the core board are replaced with other voltage levels, the LDO chip output on the expansion board also needs to be modified accordingly.
The power supply on the expansion is shown in Figure 2-11-1.

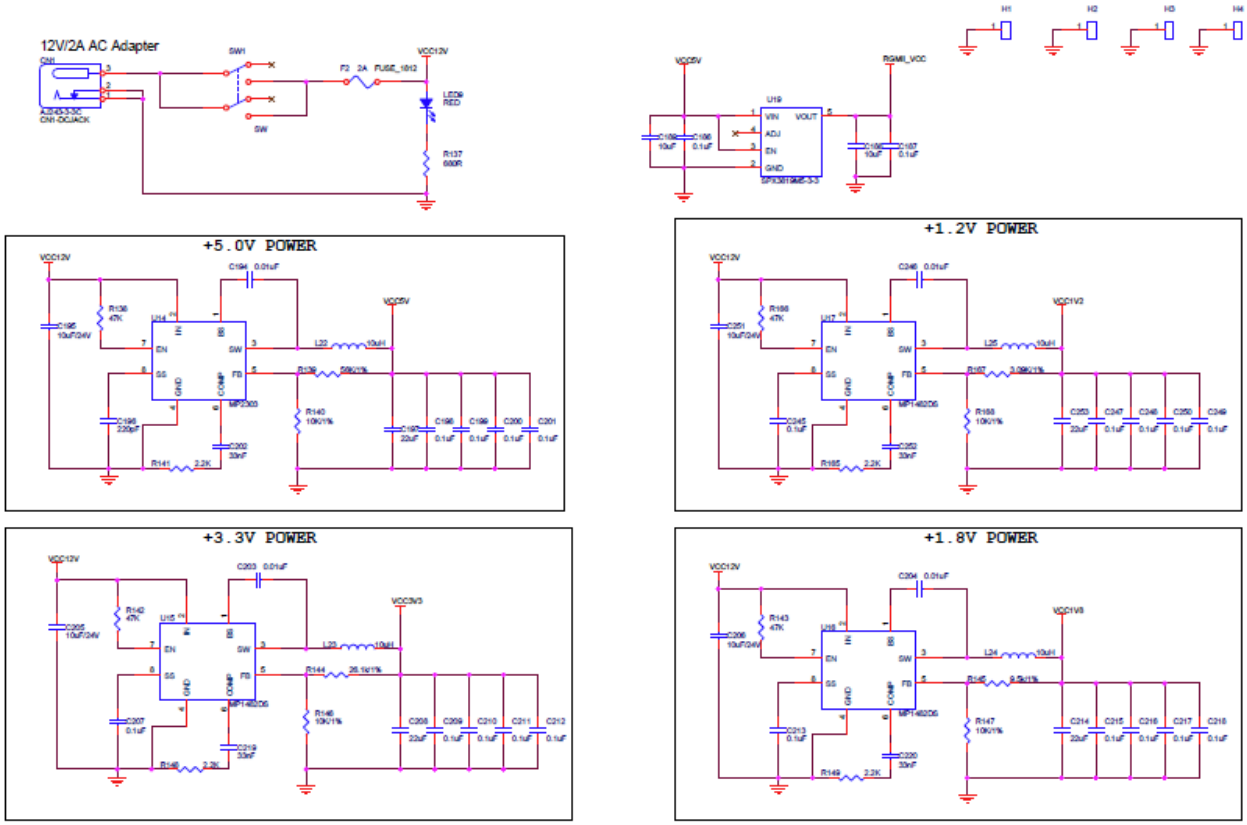


Figure 2-11-1

12. Structure