# THDB-HTG

## **User Manual**

Terasic HSTC to GPIO Daughter Board







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## Introduction



The THDB-HTG board is designed to convert a High-Speed Terasic connector (HSTC) or a High-Speed Mezzanine connector (HSMC) I/Os to three 40-pin expansion prototype connectors, which are compatible with Terasic GPIO expansion headers. Users can connect up to three Altera DE2/DE1 boards (or associated daughter cards) onto a HSTC/HSMC-interfaced host board via a THDB-HTG board.

#### **Features**

Figure 1.1 shows the photo of a THDB-HTG board. The important functions of the THDB-HTG are listed below:

- Convert HSTC/HSMC-interfaced I/O to standard 40-pin expansion connectors.
- Allow users to connect Altera DE2/DE1 boards to a HSTC/HSMC-interfaced host board.
- Provide test points for signal measurement.

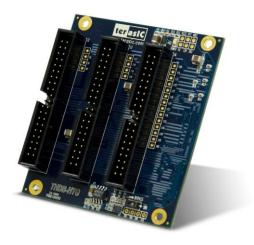


Figure 1.1. The picture of a THDB-HTG board

#### **Getting Help**

Here are some places to get help if you encounter any problem:

- ✓ Email to support@terasic.com
- ✓ Taiwan & China: +886-3-550-8800
- √ Korea: +82-2-512-7661
- ✓ English Support Line: +1-408-512-12336

This chapter describes the architecture of the THDB-HTG board, including block diagram and components.

## **Layout and Componets**

Figure 2.1, Figure 2.2, and Figure 2.3 depict the layout of the board and indicate the locations of the connectors and key components.

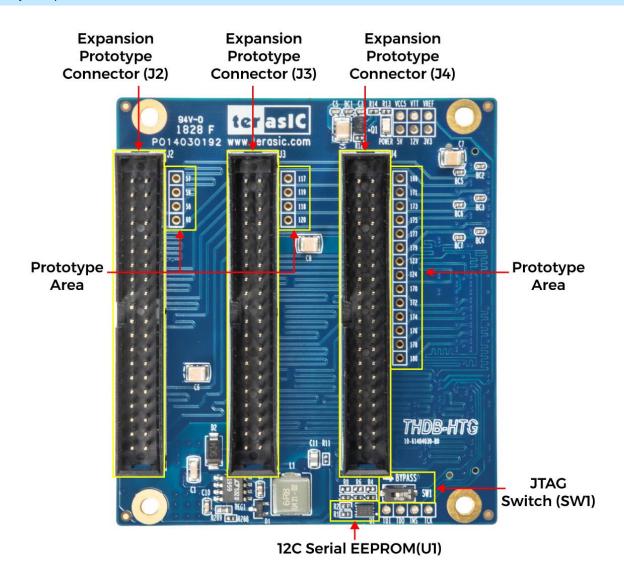


Figure 2.1 Top view of the TDRB-HTG board

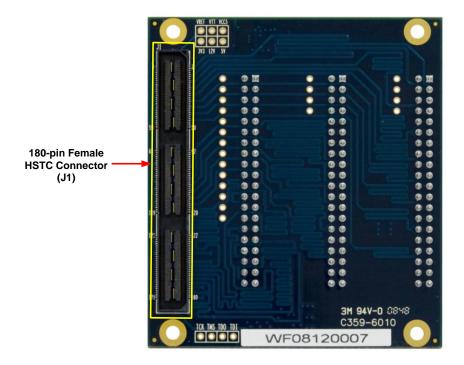


Figure 2.2 Back side of the TDRB-HTG board – HSTC version

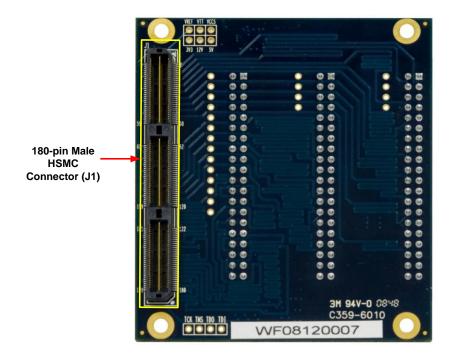


Figure 2.3 Back side of the TDRB-HTG board - HSMC version

#### The following components are provided on the THDB-HTG board:

- HSTC/HSMC expansion connector (J1)
- Expansion prototype connectors (J2,J3,J4)
- I2C serial EEPROM (U1)

## **Block Diagram**

Figure 2.4 shows the block diagram of the THDB-HTG board.

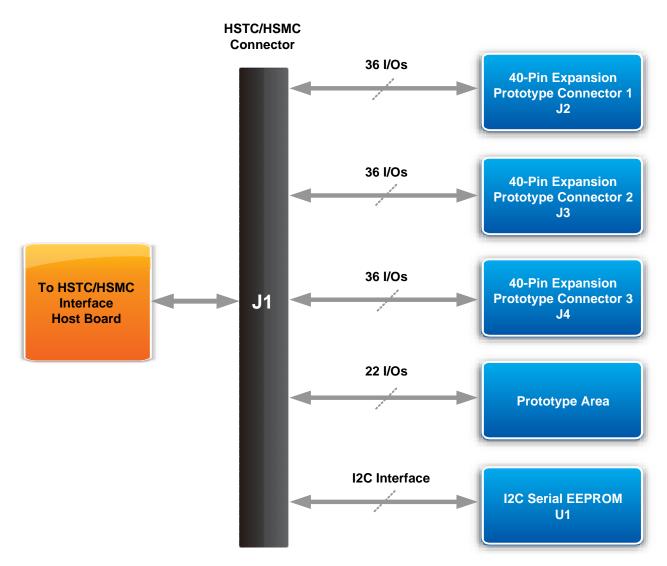


Figure 2.4. The block diagram of the THDB-HTG board

# 3 Board Components terasic

This section will describe the information of components, connector interfaces, and pin mappings on the THDB-HTG board in details.

#### **HSTC/HSMC Expansion Connector**

#### This section describes the HSTC/HSMC connector on the THDB-HTG board

There are two options of high speed connector on the THDB-HTG board. One is a 180-pin female HSTC connector for HSTC-interfaced host board such as Altera DE3 board and Terasic PCI board. The other one is a 180-pin male connector for Altera HSMC-interfaced host board. All other interfaces on the THDB-HTG board are connected to the HSTC/HSMC connector. Figure 3.1 shows the pin-outs of the HSTC and HSMC connector.

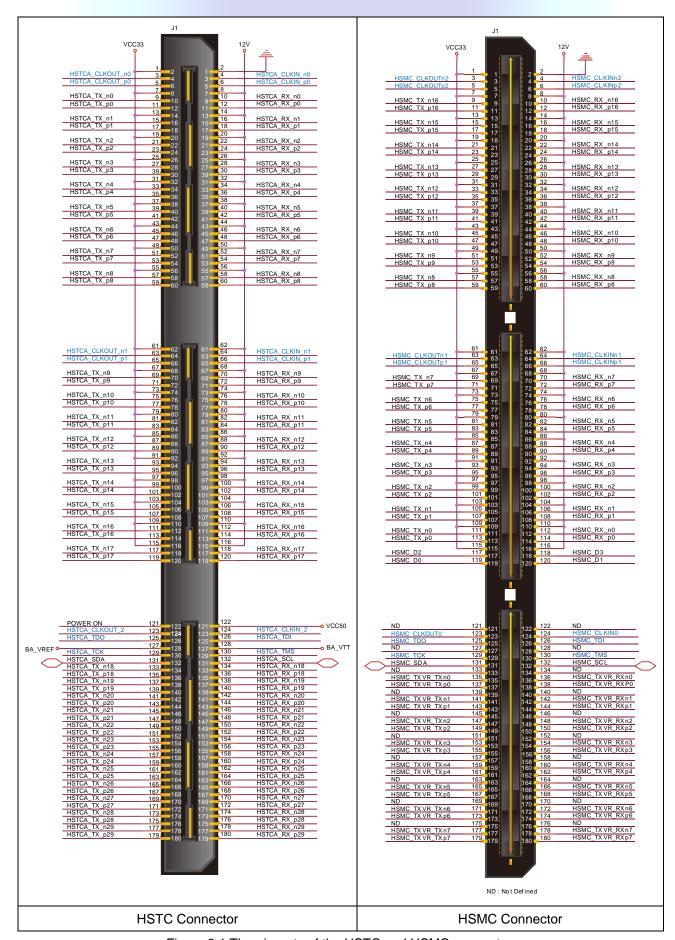


Figure 3.1 The pin-outs of the HSTC and HSMC connector.

## **Expansion Prototype Connectors**

#### This section describes the expansion prototype connectors on the THDB-HTG board.

The THDB-HTG board has three expansion prototype connectors (J2, J3, and J4) connected to the HSTC/HSMC connector directly. Each of the connectors has 36 prototyping I/Os and 3.3/5 volts power supply from the HSTC/HSMC interface and on-board regulator. Users can connect FPGA development kits which has GPIO connector or custom daughter boards to a HSTC/HSMC-interfaced host board. Figure 3.2 and Figure 3.3 show the pin-outs of the expansion prototype connectors for HSTC and HSMC version, respectively. Detailed pin mappings to HSTC/HSMC connector are listed in Table 3.1, Table 3.2, and Table 3.3. Note that, If users connect THDB-HTG to HSMC-interfaced host board, J4 connector can only be connected to transceiver I/O of FPGA and no other basic I/O available.

	J2			J3			J4	
HSTC_CLKIN_n0	1 2 ○	HSTC_RX_n0	HSTC_CLKIN_n1	↑ 1 2 ○	HSTC_RX_n9	HSTC_TX_n18	□ 1 2 □	HSTC_RX_n18
HSTC_CLKIN_p0	3 4 🔾	HSTC_RX_p0	HSTC_CLKIN_p1	3 4 🔾	HSTC_RX_p9	HSTC_TX_p18	3 4 🔾	HSTC_RX_p18
HSTC_TX_n0	5 6 🔾	HSTC_RX_n1	HSTC_TX_n9	O 5 6 O	HSTC_RX_n10	HSTC_TX_n19	○ 5 6 ○	HSTC_RX_n19
HSTC_TX_p0	7 8 0	HSTC_RX_p1	HSTC_TX_p9	7 8 🔾	HSTC_RX_p10	HSTC_TX_p19	7 8 🔾	HSTC_RX_p19
HSTC_TX_n1	9 10	HSTC_RX_n2	HSTC_TX_n10	9 10	HSTC_RX_n11	HSTC_TX_n20	9 10	HSTC_RX_n20
5V	11 12	GND	5V	11 12	GND	5V	11 12	GND
HSTC_TX_p1	O 13 14 O	HSTC_RX_p2	HSTC_TX_p10	O 13 14 O	HSTC_RX_p11	HSTC_TX_p20	O 13 14 O	HSTC_RX_p20
HSTC_TX_n2	O 15 16 O	HSTC_RX_n3	HSTC_TX_n11	O 15 16 O	HSTC_RX_n12	HSTC_TX_n21	O 15 16 O	HSTC_RX_n21
HSTC_TX_p2	O 17 18 O	HSTC_RX_p3	HSTC_TX_p11	O 17 18 O	HSTC_RX_p12	HSTC_TX_p21	O 17 18	HSTC_RX_p21
HSTC_CLKOUT_n0	<sup>™</sup> 🔾 19 20 🔾	HSTC_RX_n4	HSTC_CLKOUT_n1	ັ⊜ 19 20 ⊝	HSTC_RX_n13	HSTC_TX_n22	O 19 20 🔾	HSTC_RX_n22
HSTC_CLKOUT_p0	O 21 22 O	HSTC_RX_p4	HSTC_CLKOUT_p1	O 21 22 O	HSTC_RX_p13	HSTC_TX_p22	O 21 22 O	HSTC_RX_p22
HSTC_TX_n3	23 24	HSTC_RX_n5	HSTC_TX_n12	23 24	HSTC_RX_n14	HSTC_TX_n23	23 24	HSTC_RX_n23
HSTC_TX_p3	25 26	HSTC_RX_p5	HSTC_TX_p12	25 26	HSTC_RX_p14	HSTC_TX_p23	25 26	HSTC_RX_p23
HSTC_TX_n4	27 28	HSTC_RX_n6	HSTC_TX_n13	27 28	HSTC_RX_n15	HSTC_TX_n24	27 28	HSTC_RX_n24
3.3V	29 30	GND	3.3V	29 30	GND	3.3V	29 30	GND
HSTC_TX_p4	31 32	HSTC_RX_p6	HSTC_TX_p13	31 32	HSTC_RX_p15	HSTC_TX_p24	31 32	HSTC_RX_p24
HSTC_TX_n5	33 34	HSTC_RX_n7	HSTC_TX_n14	33 34	HSTC_RX_n16	HSTC_TX_n25	33 34	HSTC_RX_n26
HSTC_TX_p5	35 36	HSTC_RX_p7	HSTC_TX_p14	35 36	HSTC_RX_p16	HSTC_TX_p25	35 36	HSTC_RX_p26
HSTC_TX_n6	37 38	HSTC_TX_n7	HSTC_TX_n15	37 38	HSTC_TX_n16	HSTC_TX_n26	37 38	HSTC_RX_n25
HSTC_TX_p6	○ 39 40 ○	HSTC_TX_p7	HSTC_TX_p15	○ 39 40 ○	HSTC_TX_p16	HSTC_TX_p26	39 40	HSTC_RX_p25

Figure 3.2 Pin-outs of the expansion prototype connectors for HSTC version

	J2			J3		J4	
HSMC_CLKINn2	0 1 2 0	HSMC_RX_n16	HSMC_CLKINn1	1 2 HSMC_RX_n7	ND	O 1 2 O	ND
HSMC_CLKINp2	3 4 🔾	HSMC_RX_p16	HSMC_CLKINp1	3 4 HSMC_RX_p7	ND	0 3 4 O	ND
HSMC_TX_n16	0 5 6 0	HSMC_RX_n15	HSMC_TX_n7	5 6 HSMC_RX_n6	ND	0 5 6 O	ND
HSMC_TX_p16	0 7 8 0	HSMC_RX_p15	HSMC_TX_p7	7 8 HSMC_RX_p6	ND	0 7 8 0	ND
HSMC_TX_n15	0 9 10 0	HSMC_RX_n14	HSMC_TX_n6	9 10 HSMC_RX_n5	ND	0 9 10 0	ND
5V	11 12	GND	5V	11 12 GND	5V	11 12	GND
15q_HSMC_TX	O 13 14 O	HSMC_RX_p14	HSMC_TX_p6	13 14 HSMC_RX_p5	ND	0 13 14 O	ND
HSMC_TX_n14	O 15 16 O	HSMC_RX_n13	HSMC_TX_n5	15 16 HSMC_RX_n4	ND	0 15 16 O	ND
HSMC_TX_p14	O 17 18 O	HSMC_RX_p13	HSMC_TX_p5	17 18 HSMC_RX_p4	ND	0 17 18 O	ND
HSMC_CLKOUTn2	O 19 20 O	HSMC_RX_n12	HSMC_CLKOUTn1	19 20 HSMC_RX_n3	ND	0 19 20 O	ND
HSMC_CLKOUTp2	O 21 22 O	HSMC_RX_p12	HSMC_CLKOUTp1	21 22 HSMC_RX_p3	ND	21 22	ND
HSMC_TX_n13	23 24	HSMC_RX_n11	HSMC_TX_n4	23 24 HSMC_RX_n2	ND	23 24 🔾	ND
HSMC_TX_p13	25 26	HSMC_RX_p11	HSMC_TX_p4	25 26 HSMC_RX_p2	ND	25 26	ND
HSMC_TX_n12	27 28	HSMC_RX_n10	HSMC_TX_n3	27 28 HSMC_RX_n1	ND	27 28	ND
3.3V	29 30	GND	3.3V	29 30 GND	3.3V	29 30	GND
HSMC_TX_p12	31 32	HSMC_RX_p10	HSMC_TX_p3	31 32 HSMC_RX_p1	ND	31 32 O	ND
HSMC_TX_n11	33 34	HSMC_RX_n9	HSMC_TX_n2	33 34 HSMC_RX_n0	ND	33 34	ND
HSMC_TX_p11	35 36	HSMC_RX_p9	HSMC_TX_p2	35 36 HSMC_RX_p0	ND	35 36	ND
HSMC_TX_n10	37 38	HSMC_TX_n9	HSMC_TX_n1	37 38 HSMC_TX_n0	ND	37 38	ND
HSMC_TX_p10	○ 39 40 ○	HSMC_TX_p9	HSMC_TX_p1	39 40 HSMC_TX_p0	ND	39 40	ND
						ND : Not Defined	

Figure 3.3 Pin-outs of the expansion prototype connectors for HSMC version

Table 3.1 Pin mappings of the expansion prototype connector J2

Expansion Prototype Connector 1 – J2					
IO Din	Id Die				
J2 Pin	J1 Pin	J1 (HSTC Version) Signal	J1 (HSMC Version) Signal	GPIO Sgnal Name	
Number	Number	Name	Name		
1	4	HSTC_CLKIN_n0	HSMC_CLKIN_n2	GPIO0	
2	10	HSTC_RX_n0	HSMC_RX_n16	GPIO1	
3	6	HSTC_CLKIN_p0	HSMC_CLKIN_p2	GPIO2	
4	12	HSTC_RX_p0	HSMC_RX_p16	GPIO3	
5	9	HSTC_TX_n0	HSMC_TX_n16	GPIO4	
6	16	HSTC_RX_n1	HSMC_RX_n15	GPIO5	
7	11	HSTC_TX_p0	HSMC_TX_p16	GPIO6	
8	18	HSTC_RX_p1	HSMC_RX_p15	GPIO7	
9	15	HSTC_TX_n1	HSMC_TX_n15	GPIO8	
10	22	HSTC_RX_n2	HSMC_RX_n14	GPIO9	
11	N/A	N/A	N/A	5V	
12	N/A	N/A	N/A	GND	
13	17	HSTC_TX_p1	HSMC_TX_p15	GPIO10	
14	24	HSTC_RX_p2	HSMC_RX_p14	GPIO11	
15	21	HSTC_TX_n2	HSMC_TX_n14	GPIO12	
16	28	HSTC_RX_n3	HSMC_RX_n13	GPIO13	
17	23	HSTC_TX_p2	HSMC_TX_p14	GPIO14	
18	30	HSTC_RX_p3	HSMC_RX_p13	GPIO15	
19	3	HSTC_CLKOUT_n0	HSMC_CLKOUT_n2	GPIO16	
20	34	HSTC_RX_n4	HSMC_RX_n12	GPIO17	
21	5	HSTC_CLKOUT_p0	HSMC_CLKOUT_p2	GPIO18	
22	36	HSTC_RX_p4	HSMC_RX_p12	GPIO19	
23	27	HSTC_TX_n3	HSMC_TX_n13	GPIO20	
24	40	HSTC_RX_n5	HSMC_RX_n11	GPIO21	
25	29	HSTC_TX_p3	HSMC_TX_p13	GPIO22	
26	42	HSTC_RX_p5	HSMC_RX_p11	GPIO23	
27	33	HSTC_TX_n4	HSMC_TX_n12	GPIO24	
28	46	HSTC_RX_n6	HSMC_RX_n10	GPIO25	
29	N/A	N/A	N/A	3.3V	
30	N/A	N/A	N/A	GND	
31	35	HSTC_TX_p4	HSMC_TX_p12	GPIO26	
32	48	HSTC_RX_p6	HSMC_RX_p10	GPIO27	
33	39	HSTC_TX_n5	HSMC_TX_n11	GPIO28	
34	52	HSTC_RX_n7	HSMC_RX_n9	GPIO29	
35	41	HSTC_TX_p5	HSMC_TX_p11	GPIO30	
36	54	HSTC_RX_p7	HSMC_RX_p9	GPIO31	
37	45	HSTC_TX_n6	HSMC_TX_n10	GPIO32	
38	51	HSTC_TX_n7	HSMC_TX_n9	GPIO33	
39	47	HSTC_TX_p6	HSMC_TX_p10	GPIO34	
40	53	HSTC_TX_p7	HSMC_TX_p9	GPIO35	

Table 3.2 Pin mappings of the expansion prototype connector J3

	Expansion Prototype Connector 1 – J3					
J3 Pin	J1 Pin	J1 (HSTC Version) Signal	J1 (HSMC Version) Signal			
		, , , , , , , , , , , , , , , , , , ,		GPIO Sgnal Name		
Number	Number	Name	Name			
1	64	HSTC_CLKIN_n1	HSMC_CLKIN_n1	GPIO0		
2	70	HSTC_RX_n9	HSMC_RX_n7	GPIO1		
3	66	HSTC_CLKIN_p1	HSMC_CLKIN_p1	GPIO2		
4	72	HSTC_RX_p9	HSMC_RX_p7	GPIO3		
5	69	HSTC_TX_n9	HSMC_TX_n7	GPIO4		
6	76	HSTC_RX_n10	HSMC_RX_n6	GPIO5		
7	71	HSTC_TX_p9	HSMC_TX_p7	GPIO6		
8	78	HSTC_RX_p10	HSMC_RX_p6	GPIO7		
9	75	HSTC_TX_n10	HSMC_TX_n6	GPIO8		
10	82	HSTC_RX_n11	HSMC_RX_n5	GPIO9		
11	N/A	N/A	N/A	5V		
12	N/A	N/A	N/A	GND		
13	77	HSTC_TX_p10	HSMC_TX_p6	GPIO10		
14	84	HSTC_RX_p11	HSMC_RX_p5	GPIO11		
15	81	HSTC_TX_n11	HSMC_TX_n5	GPIO12		
16	88	HSTC_RX_n12	HSMC_RX_n4	GPIO13		
17	83	HSTC_TX_p11	HSMC_TX_p5	GPIO14		
18	90	HSTC_RX_p12	HSMC_RX_p4	GPIO15		
19	63	HSTC_CLKOUT_n1	HSMC_CLKOUT_n1	GPIO16		
20	94	HSTC_RX_n13	HSMC_RX_n3	GPIO17		
21	65	HSTC_CLKOUT_p1	HSMC_CLKOUT_p1	GPIO18		
22	96	HSTC_RX_p13	HSMC_RX_p3	GPIO19		
23	87	HSTC_TX_n12	HSMC_TX_n4	GPIO20		
24	100	HSTC_RX_n14	HSMC_RX_n2	GPIO21		
25	89	HSTC_TX_p12	HSMC_TX_p4	GPIO22		
26	102	HSTC_RX_p14	HSMC_RX_p2	GPIO23		
27	93	HSTC_TX_n13	HSMC_TX_n3	GPIO24		
28	106	HSTC_RX_n15	HSMC_RX_n1	GPIO25		
29	N/A	N/A	N/A	3.3V		
30	N/A	N/A	N/A	GND		
31	95	HSTC_TX_p13	HSMC_TX_p3	GPIO26		
32	108	HSTC_RX_p15	HSMC_RX_p1	GPIO27		
33	99	HSTC_TX_n14	HSMC_TX_n2	GPIO28		
34	112	HSTC_RX_n16	HSMC_RX_n0	GPIO29		
35	101	HSTC_TX_p14	HSMC_TX_p2	GPIO30		
36	114	HSTC_RX_p16	HSMC_RX_p0	GPIO31		
37	105	HSTC_TX_n15	HSMC_TX_n1	GPIO32		
38	111	HSTC_TX_n16	HSMC_TX_n0	GPIO33		
39	107	HSTC_TX_p15	HSMC_TX_p1	GPIO34		
40	113	HSTC_TX_p16	HSMC_TX_p0	GPIO35		

Table 3.3 Pin mappings of the expansion prototype connector J4

Expansion Prototype Connector 1 – J4 (Only can be used on HSTC version)					
J4 Pin	J1 Pin	J1 (HSTC Version) Signal	J1 (HSMC Version) Signal		
Number	Number	Name	Name	GPIO Sgnal Name	
1	133	HSTC_TX_n18	ND	GPIO0	
2	134	HSTC_RX_n18	ND	GPIO1	
3	135	HSTC_TX_p18	ND	GPIO2	
4	136	HSTC_RX_p18	ND	GPIO3	
5	137	HSTC_TX_n19	ND	GPIO4	
6	138	HSTC_RX_n19	ND	GPIO5	
7	139	HSTC_TX_p19	ND	GPIO6	
8	140	HSTC_RX_p19	ND	GPIO7	
9	141	HSTC_TX_n20	ND	GPIO8	
10	142	HSTC_RX_n20	ND	GPIO9	
11	N/A	N/A	ND	5V	
12	N/A	N/A	ND	GND	
13	143	HSTC_TX_p20	ND	GPIO10	
14	144	HSTC_RX_p20	ND	GPIO11	
15	145	HSTC_TX_n21	ND	GPIO12	
16	146	HSTC_RX_n21	ND	GPIO13	
17	147	HSTC_TX_p21	ND	GPIO14	
18	148	HSTC_RX_p21	ND	GPIO15	
19	149	HSTC_TX_n22	ND	GPIO16	
20	150	HSTC_RX_n22	ND	GPIO17	
21	151	HSTC_TX_p22	ND	GPIO18	
22	152	HSTC_RX_p22	ND	GPIO19	
23	153	HSTC_TX_n23	ND	GPIO20	
24	154	HSTC_RX_n23	ND	GPIO21	
25	155	HSTC_TX_p23	ND	GPIO22	
26	156	HSTC_RX_p23	ND	GPIO23	
27	157	HSTC_TX_n24	ND	GPIO24	
28	158	HSTC_RX_n24	ND	GPIO25	
29	N/A	N/A	ND	3.3V	
30	N/A	N/A	ND	GND	
31	159	HSTC_TX_p24	ND	GPIO26	
32	160	HSTC_RX_p24	ND	GPIO27	
33	161	HSTC_TX_n25	ND	GPIO28	
34	166	HSTC_RX_n26	ND	GPIO29	
35	163	HSTC_TX_p25	ND	GPIO30	
36	168	HSTC_RX_p26	ND	GPIO31	
37	165	HSTC_TX_n26	ND	GPIO32	
38	162	HSTC_TX_n25	ND	GPIO33	
39	167	HSTC_TX_p26	ND	GPIO34	
40	164	HSTC_TX_p25	ND	GPIO35	

## **Cyclone III Starter Board HSMC Connector**

The naming convention used to assign the pin names for the HSMC connector is different for the Cyclone III Starter Board and the standard HSMC connector. Figure 3.4 shows the pin-outs of the expansion prototype connectors for Cyclone III Starter board HSMC version.

	J2			J3			J4	
HSMC_CLKIN_n2	O 1 2 O	HSMC_RX_n16	HSMC_CLKIN_n1	O 1 2 O	HSMC_RX_n7	NC	0 1 2 0	NC
HSMC_CLKIN_p2	O 3 4 O	HSMC_RX_p16	HSMC_CLKIN_p1	3 4 0	HSMC_RX_p7	ND	O 3 4 O	ND
HSMC_TX_n16	0 5 6 0	HSMC_RX_n15	HSMC_TX_n7	5 6	HSMC_RX_n6	ND	O 5 6 O	ND
HSMC_TX_p16	0 7 8 0	HSMC_RX_p15	HSMC_TX_p7	7 8 0	HSMC_RX_p6	NC	0 7 8 0	NC
HSMC_TX_n15	O 9 10 O	HSMC_RX_n14	HSMC_TX_n6	9 10	HSMC_RX_n5	ND	O 9 10O	ND
5V	□ 11 12 □	GND	5V	11 12	GND	5V	11 12	GND
HSMC_TX_p15	O 13 14 O	HSMC_RX_p14	HSMC_TX_p6	O 13 14 O	HSMC_RX_p5	ND	O 13 14O	ND
HSMC_TX_n14	O 15 16 O	HSMC_RX_n13	HSMC_TX_n5	O 15 16 O	HSMC_RX_n4	NC	O 15 16O	NC
HSMC_TX_p14	O 17 18O	HSMC_RX_p13	HSMC_TX_p5	0 17 180	HSMC_RX_p4	ND	O 17 18O	ND
HSMC_CLKOUT_n2	ັ () 19 20 ()	HSMC_RX_n12	HSMC_CLKOUT_n1	ັ 🔾 19 20 🔾	HSMC_D19	ND	O 19 20 O	ND
HSMC_CLKOUT_p2	O 21 22 O	HSMC_RX_p12	HSMC_CLKOUT_p1	O 21 22 O	HSMC_D17	NC	O 21 22 O	NC
HSMC_TX_n13	23 24	HSMC_RX_n11	HSMC_TX_n4	23 24	HSMC_D15	ND	23 24	ND
HSMC_TX_p13	O 25 26 O	HSMC_RX_p11	HSMC_TX_p4	25 26	HSMC_D13	ND	O 25 26O	ND
HSMC_TX_n12	O 27 28O	HSMC_RX_n10	HSMC_D18	27 28	HSMC_D11	NC	O 27 28O	NC
3.3V	<b>29</b> 30	GND	3.3V	29 30	GND	3.3V	29 30	GND
HSMC_TX_p12	31 32 ○	HSMC_RX_p10	HSMC_D16	31 32	HSMC_D9	ND		ND
HSMC_TX_n11	33 34	HSMC_RX_n9	HSMC_D14	33 34	HSMC_D7	ND	33 34	ND
HSMC_TX_p11	35 36	HSMC_RX_p9	HSMC_D12	35 36	HSMC_D5	NC	35 36	ND
HSMC_TX_n10	37 38	HSMC_TX_n9	HSMC_D10	37 38	HSMC_D6	ND	37 38	ND
HSMC_TX_p10	○ 39 40 ○	HSMC_TX_p9	HSMC_D8	39 40	HSMC_D4	ND	○ 39 40○	NC
							ND : Not Defined	
						ı	IC : Not Connecte	ed

Figure 3.4 Pin-outs of the expansion prototype connectors for Cyclone III Starter board HSMC version

#### **Prototyping Area**

The THDB-HTG board provides users a prototyping area for signal measurement or debug. These prototyping points are connected to the HSTC/HSMC connector directly. Detailed I/O maps for HSTC and HSMC version are provided to help users locate the corresponding prototyping points, as shown in Figure 3.4 and Figures 3.5, respectively.

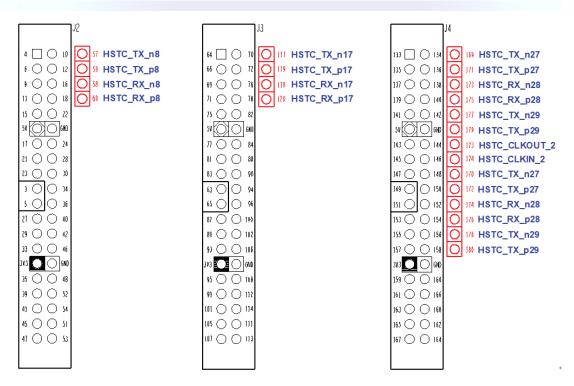


Figure 3.4 Pin distribution of the prototype area for TDHB-HTG HSTC version

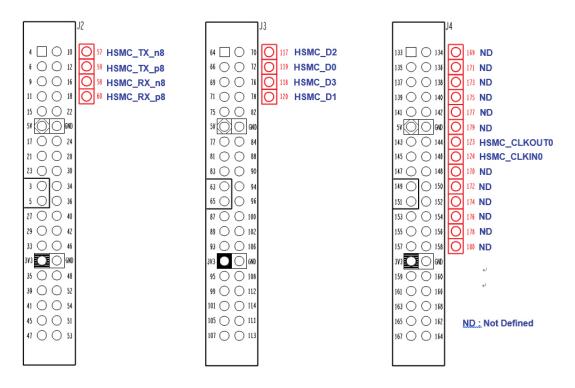


Figure 3.5 Pin distribution of the prototype area for TDHB-HTG HSMC version

#### JTAG Switch

The THDB-HTG board provides a JTAG switch (SW1) to short the JTAG signal "HSTC\_TDI" and "HSTC\_TDO" together. When the THDB-HTG board is connected to a HSTC host board, this feature can bypass the JTAG signal from host board to form a close loop of JTAG chain. For example, if users connect a

THDB-HTG with Altera DE3 board, this switch must be turned on, or the Stratix III FPGA device will not be detected because the JTGA chain is not a close loop on DE3 board. Figure 3.6 shows the JTAG switch being turned on.

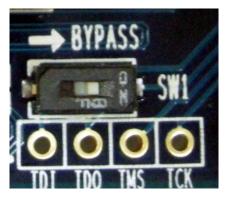


Figure 3.6 The JTAG Switch in "ON" position

#### **Power ON Control Pin**

Pin 121 of the HSTC connector is defined as a "Power ON" control signal. This signal allows host board to turn on/off the power supply on THDB-HTG board. When the Power ON signal is in logic low level, the 3.3V and 5V on the expansion header will not supply any power. This feature is designed for THDB-HTG HSTC version only.

#### **I2C Serial EEPROM**

#### This section describes the I2C Serial EEPROM on the THDB-HTG board

The THDB-HTG board provides a Microchip 24LC02BT EEPROM (U1) which can be configured by the I2C interface. The size of the EEPROM is 2K-bit that can store the board information or user's data. The detailed pin description between EEPROM and HSMC connector is listed in the Table 3.4.

Table 3.4 The pin assignments of the I2C serial EEPROM

EEPROM	EPPROM	HSMC Pin
Pin Number	Signal Name	Number
U1-1	A0	N/A
U1-2	A1	N/A
U1-3	A2	N/A
U1-4	GND	N/A
U1-5	HSTC_SDA	J1-131
U1-6	HSTC_SCL	J1-132
U1-7	WP	N/A
U1-8	VCC33 (3.3 volts)	N/A

## **Power Supply**

#### This section describes the power supply on the THDB-HTG board.

The power distribution on the THDB-HTG board is shown in Figure 3.7.

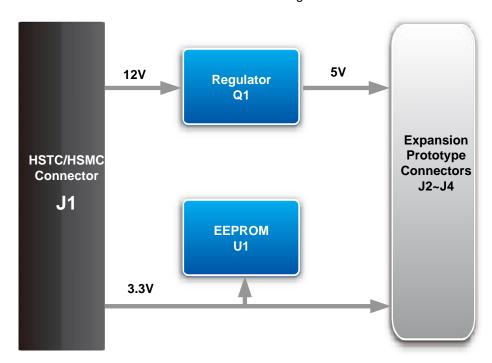


Figure 3.7 THDB-HTG board power distribution diagram.

This chapter illustrates how to use the THDB-HTG board to a HSMC-interfaced host board.

## Connecting THDB-HTG Board to a Cyclone III Starter Board

This section describes how to use the THDB-HTG board with a Cyclone III Starter Board.

Figure 4.1 illustrates how the THDB-HTG board is connected to the Cyclone III starter board. Users need to pay extra attention to the following two points:

- Observe the orientation of the HSMC connector when connecting the THDB-HTG to the Cyclone III Starter Board.
- Note that there are two LVDS pairs on the HSMC connector: the HSMC\_CLK\_p1/n1 (form a close loop via R3) and HSMC\_CLKIN\_p2/n2 (form a close loop via R4). Therefore, using any one of the signal in a LVDS pair under single-ended mode will prevent users from using the other signal in the same pair.



Figure 4.1 Connecting the THDB-HTG board to the Cyclone III starter board

### **Connecting THDB-HTG Board to Altera DE3 Board**

#### This section describes how to use the THDB-HTG board with Altera DE3 Board.

Figure 4.2 illustrates how the THDB-HTG board is connected to the Altera DE3 board. Users need to pay extra attention to the following three points:

- 1. THDB-HTG board can be connected to any of the HSTC connectors J1, J3, J5, and J7 on the DE3 board.
- 2. The JTAG Switch on the THDB-HTG board MUST be switched to "Bypass" position, or the FPGA device on DE3 board will not be detected.
- 3. Users can use DE3\_System\_builder to create Quartus II project. Please refer to Figure 3.2 for the corresponding signal names.

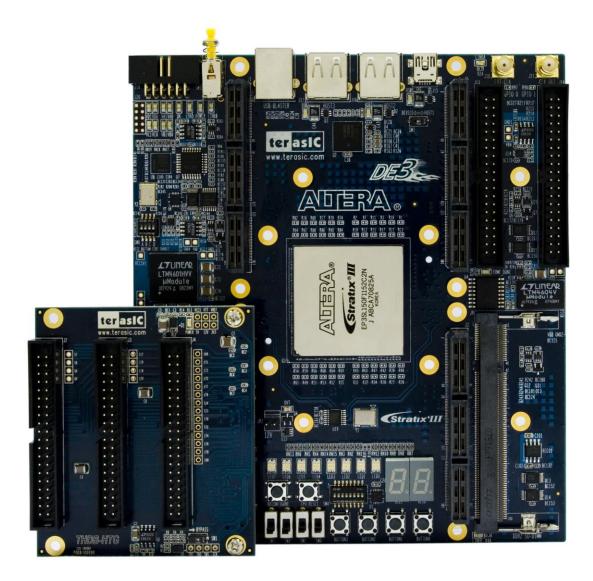


Figure 4.2 Connecting the THDB-HTG board to the Cyclone III starter board



## **Revision History**

Date	Change Log	
JAN 04, 2009	Initial Version	
Oct 20, 2009	Added Cyclone III Starter Board HSMC Connector section	
April 08, 2010	Modified pin names for Cyclone III Starter Board HSMC Connector	
	section	
Dec 24, 2010	Corrected Table 3.1 Pin Mapping	
July 20,2011	Change cover page	
2017.04	Modify Section 1.5 and Figure 3.3	
2018.12	Modify Figure 2.1, Figure 3.4 and Figure 3.5	

## Always Visit THDB-HTG Webpage for New Main board

We will be continuing providing interesting examples and labs on our THDB-HTG

webpage. Please visit www.altera.com or HTG.terasic.com for more information.

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