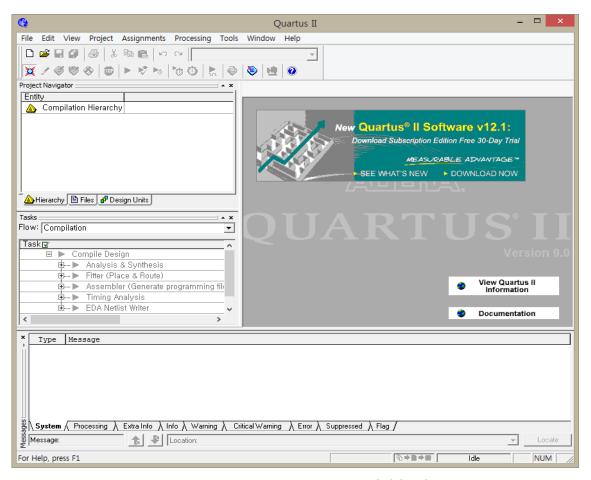


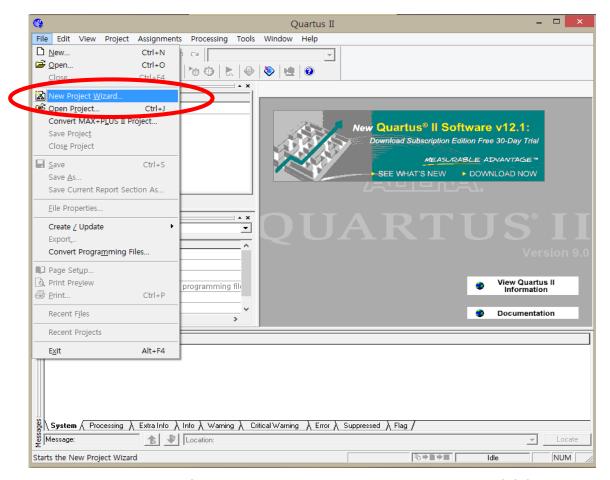
논리 설계 및 실험

Date : 2016 . 04 . 1

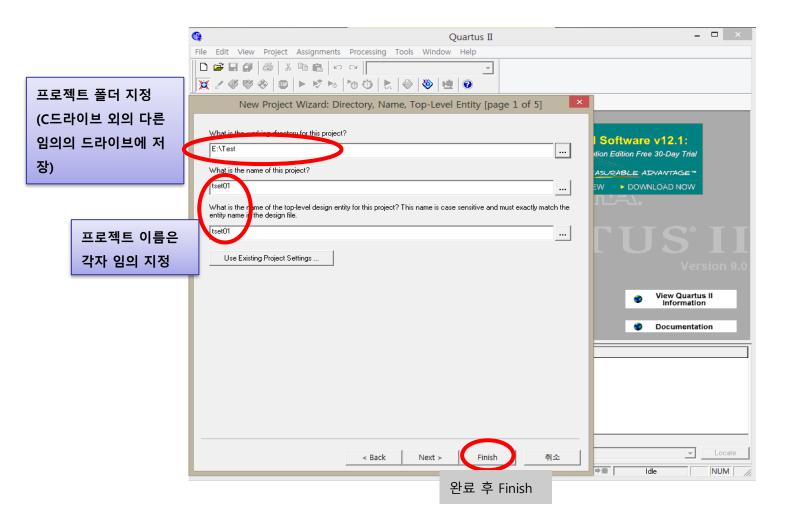
김영대

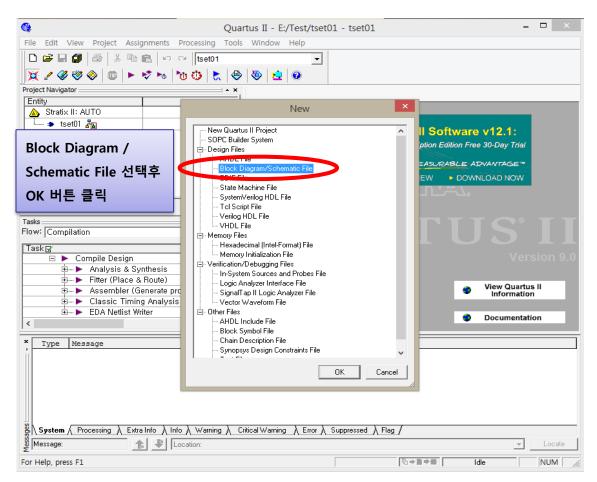


Quartus II 9.0 초기화면

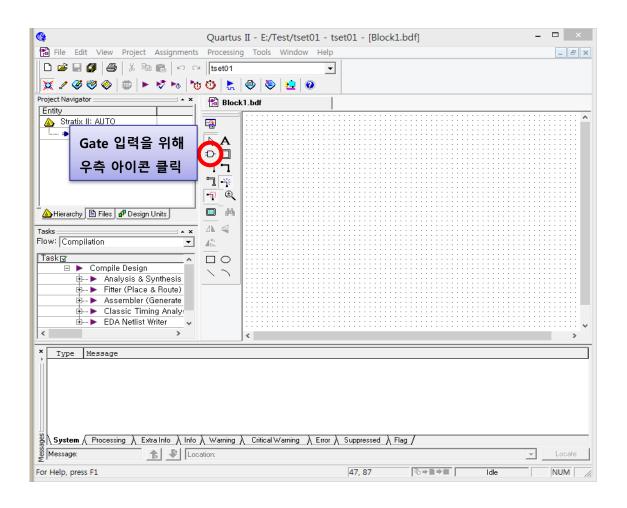


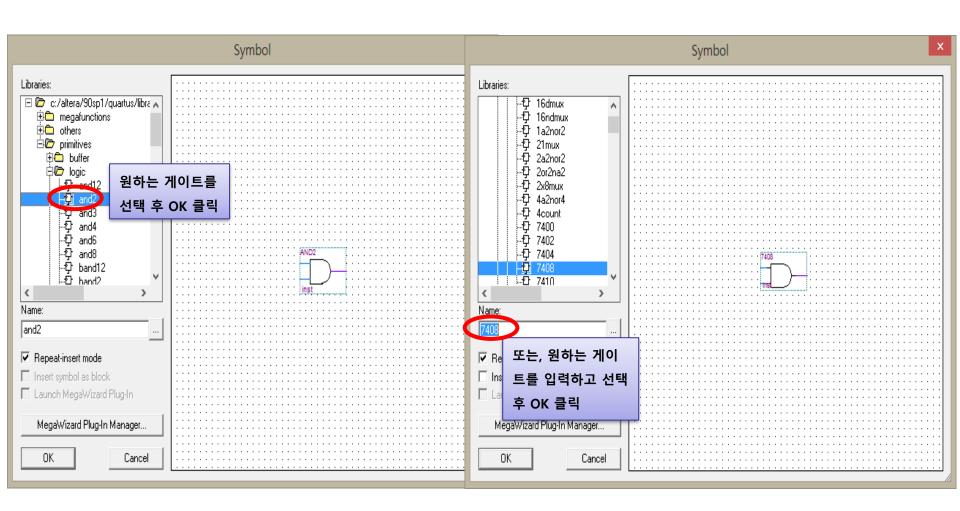
File 메뉴 → New Project Wizard 실행

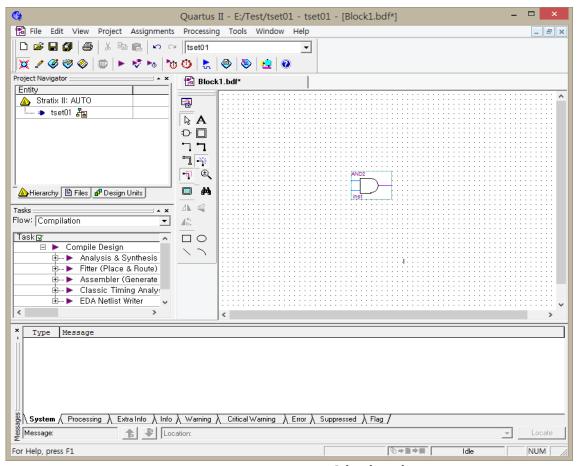




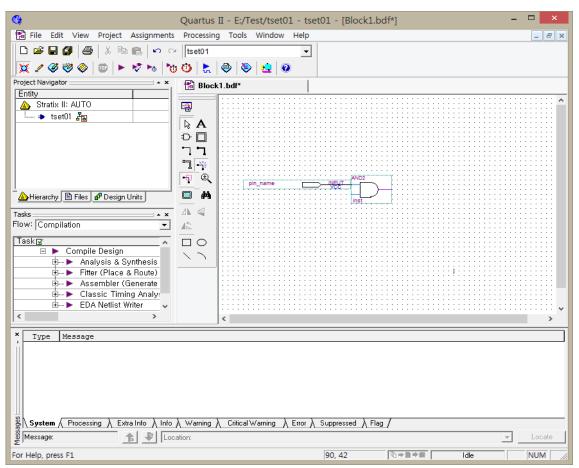
File 메뉴 → New 실행



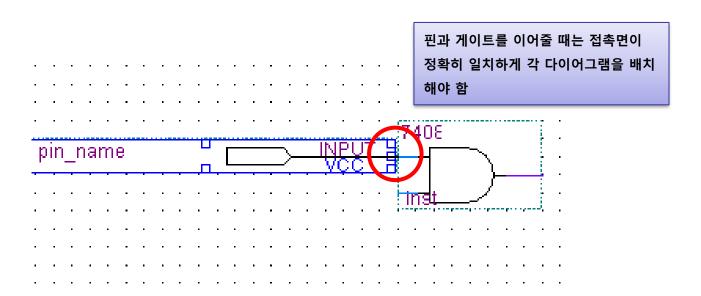


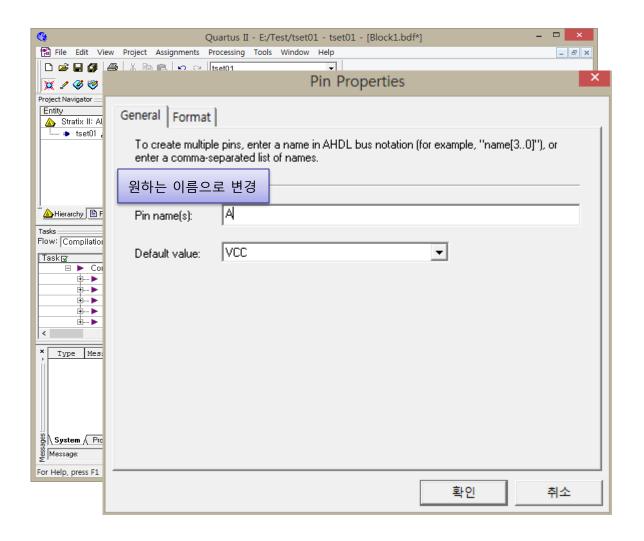


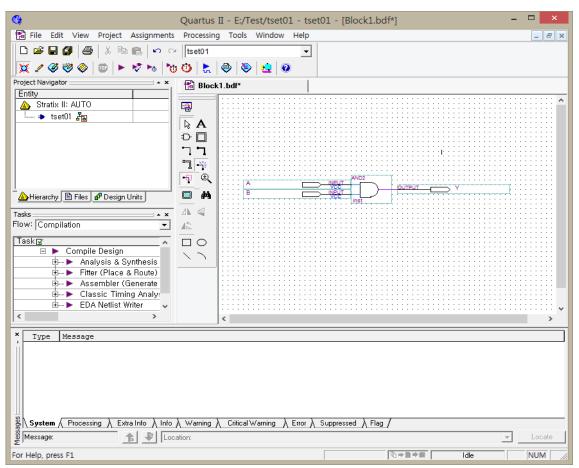
AND Gate 입력 완료



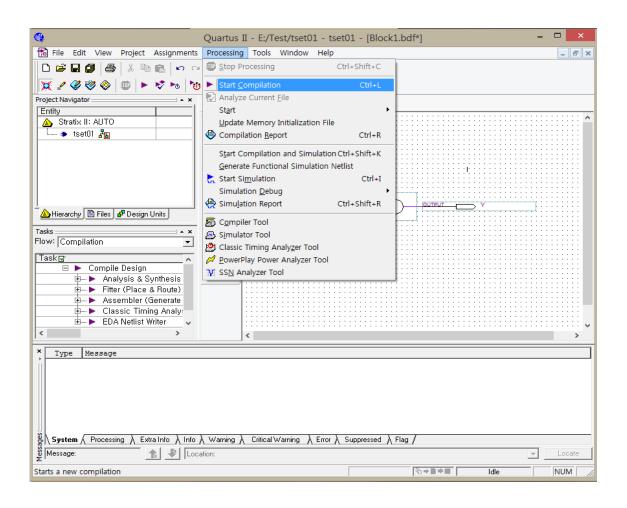
input Pin을 추가 (AND 게이트를 입력하는 방법과 동일, input 으로 검색)

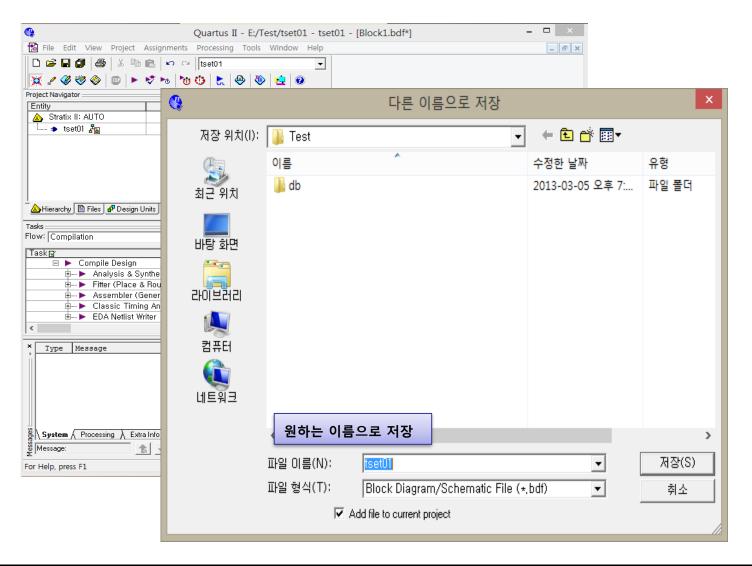


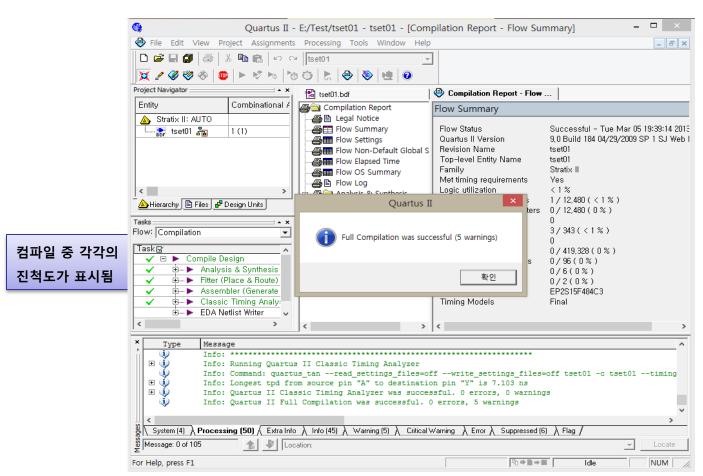




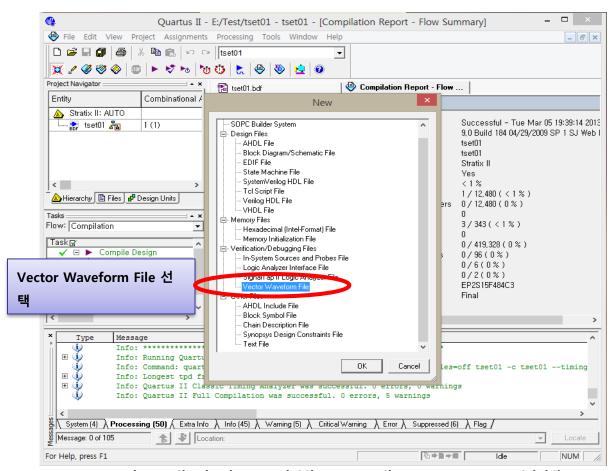
위와 같이 회로 구성 (output 추가 역시 동일한 방법, output 으로 검색)



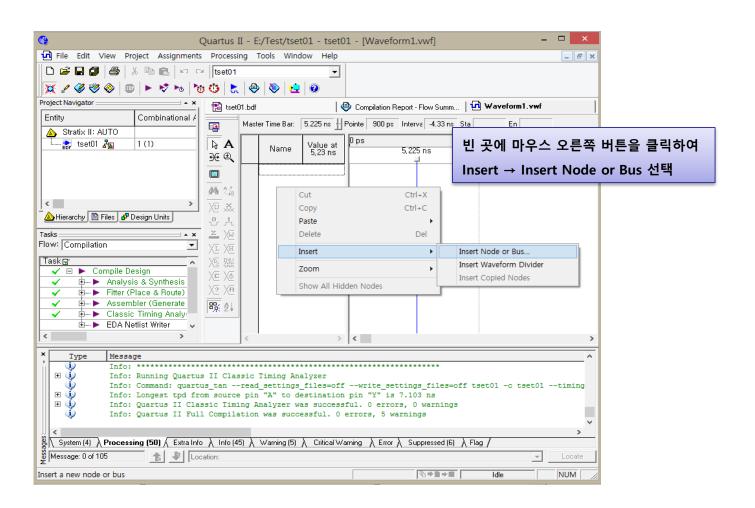


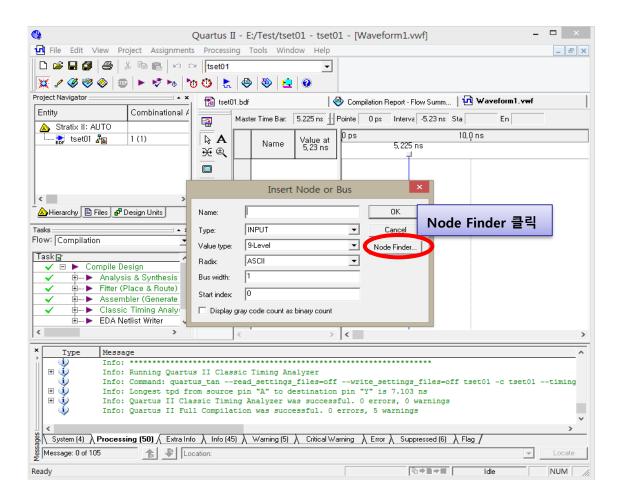


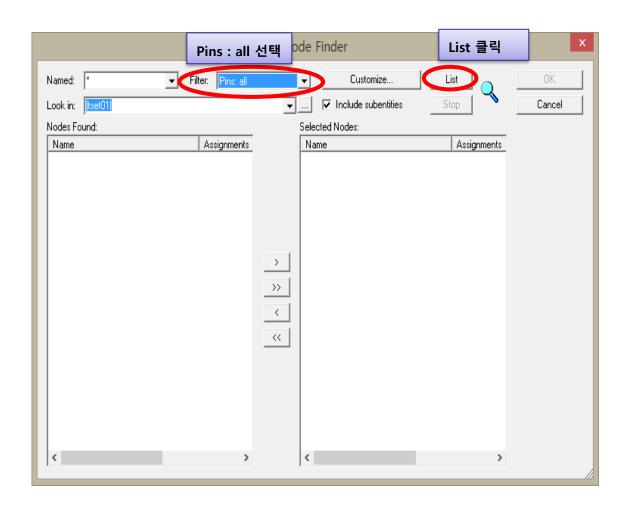
성공적으로 컴파일 완료

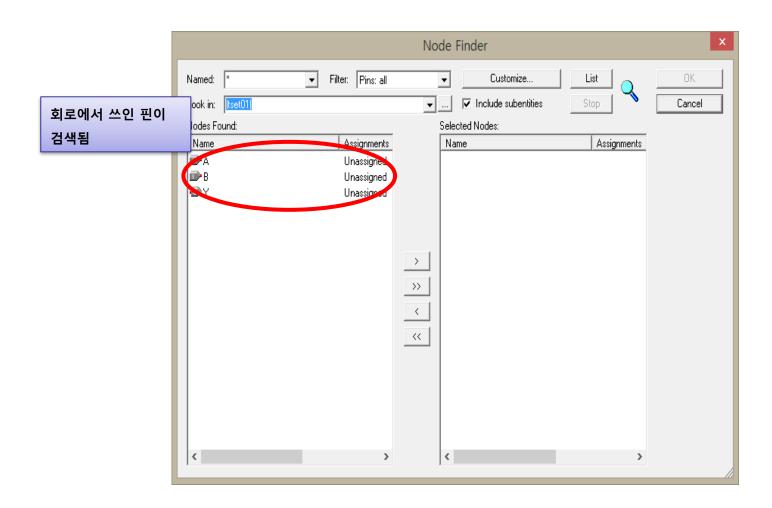


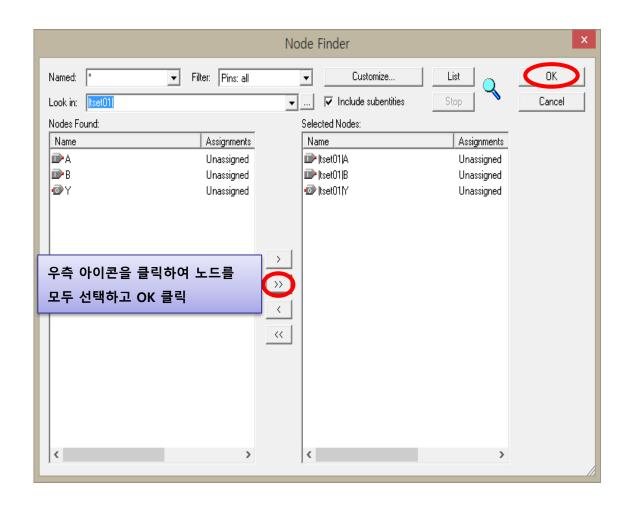
시뮬레이팅을 위해 File 메뉴 → New 실행

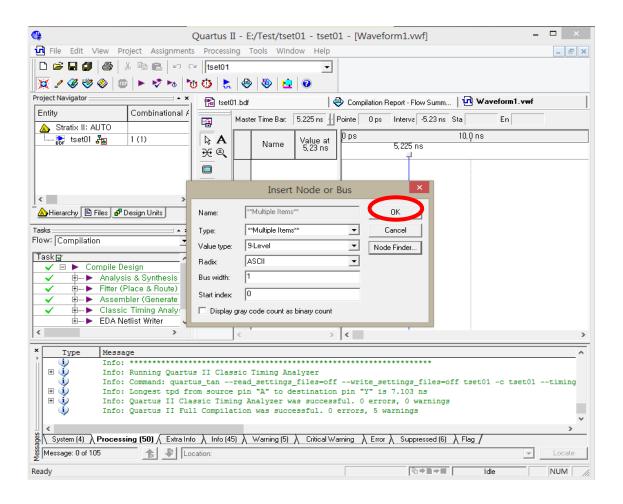


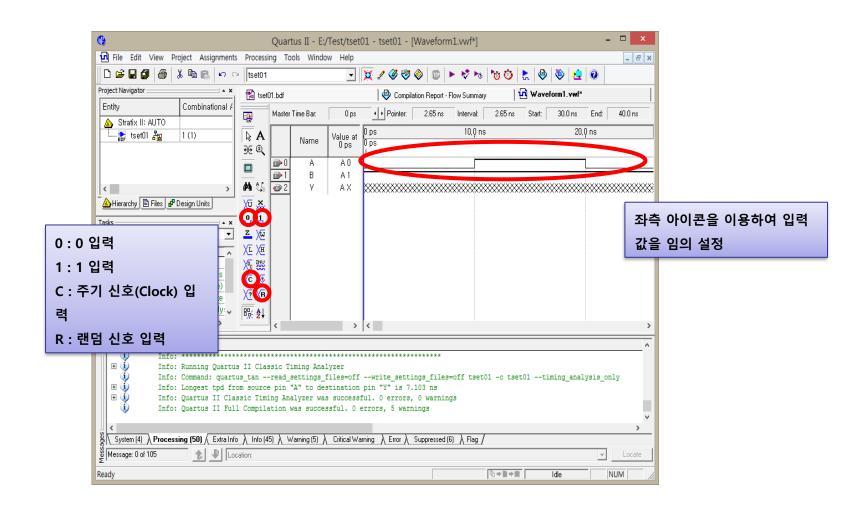


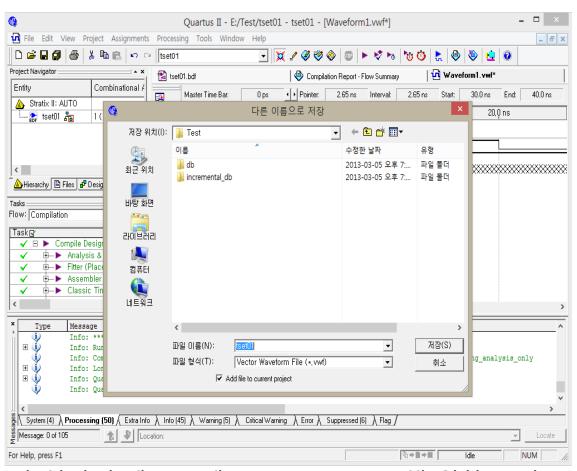




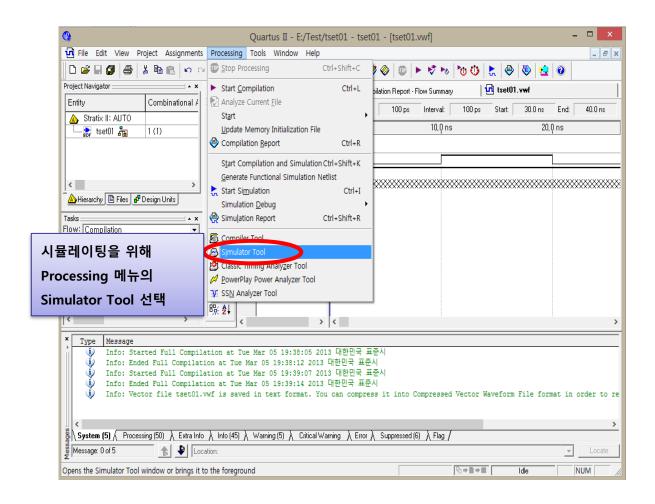


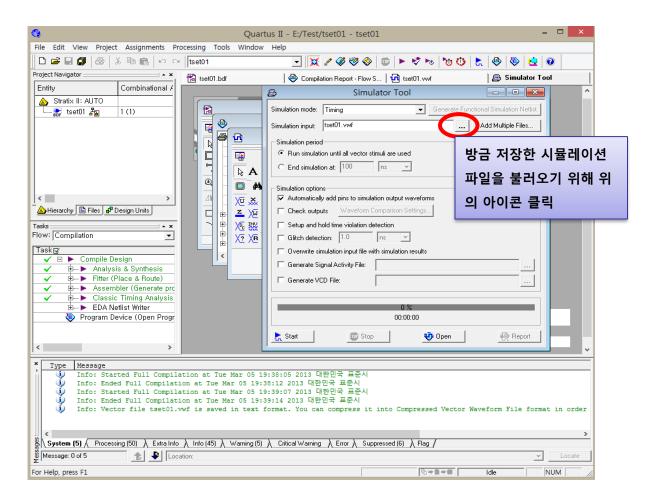


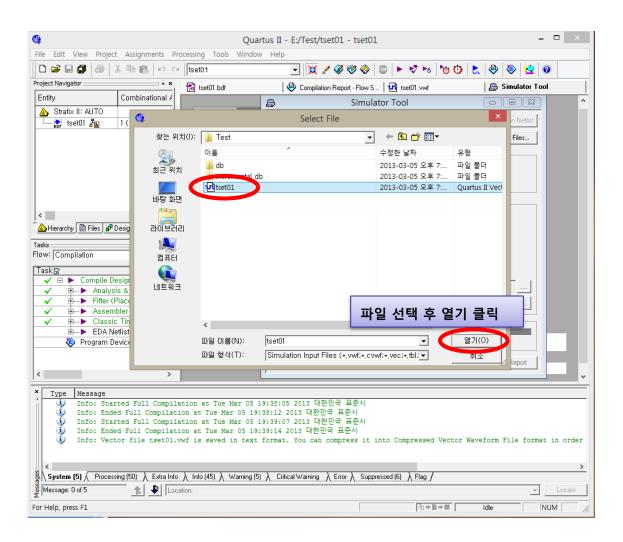


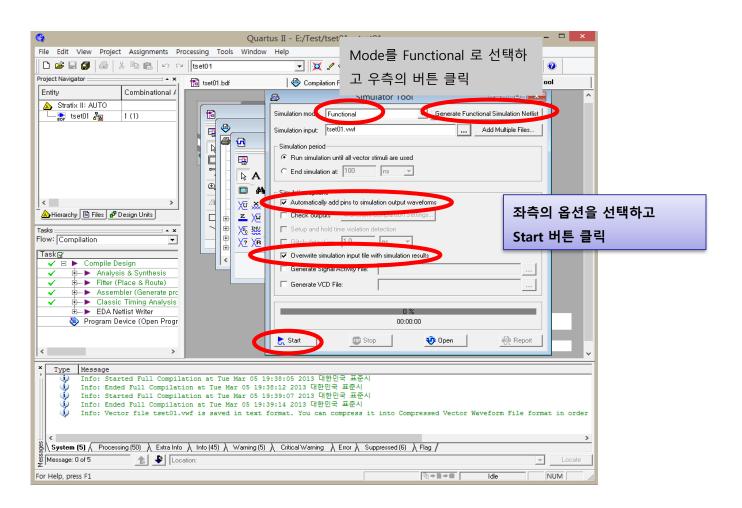


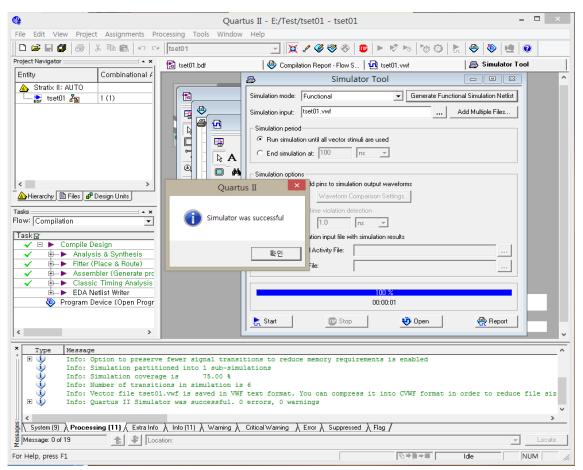
입력 값 설정 후에 File 메뉴 → Save 를 통해 원하는 이름으로 저장



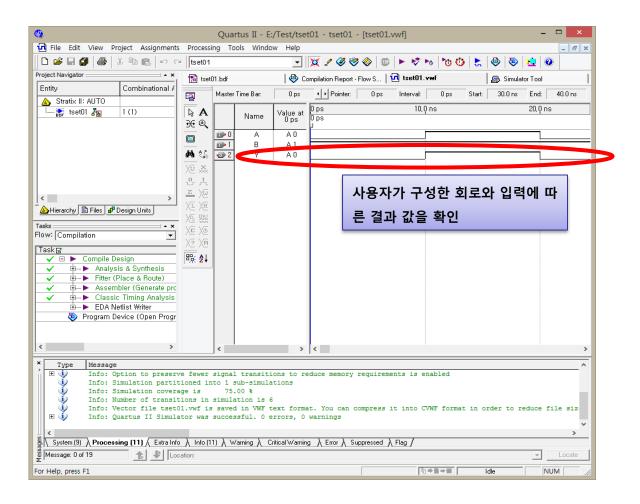






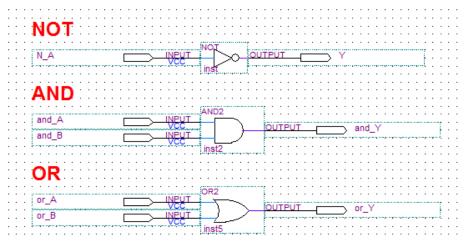


성공적으로 Simulator 완료



기본 논리 Gate 실습

■ 다음의 b가지 논리 Gate를 그리시오.



NAND				
Nand_A INPUT Nand_B INPUT	NAND2	OUTPUT	Nand_Y	I :
NOR	inst1			
Nor_A	NOR2	OUTPUT	Nor_Y] ;] ;
XOR	inst3			
Xor_A NPUT Xor_B NPUT	XOR	OUTPUT	Xor_Y	: :] :

실습 과제

■ AND게이트를 사용하지 말고 XOR 구현하라

■ 아래 논리식을 부울 대수 정리를 사용하여 간략화하고 회로, 진리표, 카르노맵을 그리시오.

$$Y = \overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC} + ABC$$

• 한글 파일로 정리 및 설명해서 e캠퍼스 과제로 제출