Radiation Test Results for Common CubeSat Microcontrollers and Microprocessors

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***Abstract*-- SEL, SEU, and TID results are presented for microcontrollers and microprocessors of interest for small satellite systems such as the TI MSP430F1611, MSP430F1612 and MSP430FR5739, Microchip PIC24F256GA110 and dsPIC33FJ256GP710, Atmel AT91SAM9G20, and Intel Atom E620T, and the Qualcomm Snapdragon APQ8064.**

I. Introduction

Interest is increasing in low cost, small physical size missions, such as CubeSats and other experimental spacecraft. These missions are accessible to many groups and enable novel technologies and architectures to perform in space missions. This has resulted in interest in a set of microcontrollers and microprocessors that have not previously been studied for radiation effects [1][2][3][4][5].

In this work, we focus on single event effects (SEE) and total ionizing dose (TID) on several microcontrollers of interest in CubeSat systems. In particular, most CubeSat programs lack the funding to support parts programs and radiation testing. Flight avionics are critical for operation of spacecraft, and CubeSats are no exception. However, it is often the case that these missions require only a small amount of processing power for avionics. To assist CubeSat programs, there are several manufacturers that provide kits [6][7][8][9].

The NASA Electronic Parts and Packaging (NEPP) program's CubeSat microcontrollers effort has been exploring the radiation effects of the most common CubeSat microcontrollers and microprocessors. This effort focused on devices where little or no radiation effects data were available.

We focus on the most problematic radiation effects, followed by specific SEE types. The most important radiation effects of interest were single event latchup (SEL), and TID leading to device failure. Although TID performance is expected to be lot specific, this work did not include wafer lot traceability. The approach taken was to obtain devices consistent with the expected procurement approach of CubeSat system builders. Although not of primary focus, where incidentally enabled by our test equipment, we obtained single bit upset (SBU) data.

We surveyed the available CubeSat kit providers indicated above and others. Based on the survey, a key set of devices and device families were identified that are currently in use. They are: the Texas Instruments (TI) MSP430 series, the Microchip PIC series, ARM-based devices produced by Atmel, several field programmable gate array (FPGA) solutions, and 8051-based devices from Silicon Labs.

In addition to CubeSat devices, we have also performed limited SEE testing of some mobile processors. It is expected that as CubeSat systems continue to bring commercial devices into the small satellite market, more capable devices are likely to be used. To that end we have identified a couple categories of devices that may be of interest. These are the Intel Atom devices, and Qualcomm Snapdragon devices. Both devices are available in inexpensive hobbyist boards.

This paper follows a basic structure of reviewing test setup and results for each of the three primary types of devices studied. The first is the TI MSP430F1611, MSP430F1612, and MSP430FR5739, then the Microchip PIC24F256GA110 and dsPIC33FJ256GP710, the Atmel AT91SAM9G20 device, the Intel Atom E620, and finally we will provide a brief review of efforts on the Snapdragon APQ8064.

II. TI MSP430F1611 and MSP430F1612

The MSP430F1611 and MSP430F1612 are from the same family of 16-bit Ultra-Low-Power micro controller units (MCUs) from TI. These devices are mixed signal, utilizing a 16-bit reduced instruction set (RISC) processor, and multiple built-in peripherals [10,11]. These devices have built-in flash memory for program storage, and SRAM for on-chip embedded execution. The primary differences between these two devices, for this work, are the sizes of the flash and SRAM. The 1611 has 48 kB of flash and 10 kB of SRAM, while the 1612 has 55 kB of flash, and 5 kB of SRAM.

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A. Test Setup

MSP430F1612 devices were tested for SEL, SEE, and TID, and MSP430F1611 devices were tested for TID. The SEE exposures are summarized in Table I below. The TID exposures depended on the ability of the devices to function properly at each exposure point and failure levels are indicated in the test results below.

Table I: Heavy ion exposures of MSPF1612 devices.

DUT ID	Ion	Energy	Degrader	LET eff	Exposure
92	Au	15 MeV/amu	No	85.6	1.10E+07/cm^2
22	Au	15	No	85.6	1.00E+07
20	Au	15	No	85.6	1.00E+06
92	Kr	25	No	20	2.20E+05
21	Ar	15	No	8.3	4.30E+06
21	Ar	15	Yes	14	4.00E+05

Testing of the MSP devices was performed using the MSP430 64-pin Target Board (MSP-TS430PM64). This board uses a ZIF socket to hold the DUT and provides a JTAG header for interfacing to the TI IAR Embedded Workbench application running on a development computer. The TS430PM64 board was modified to provide a UART port for report and logging of SEE observations. The DUTs were operated at around 700 kHz.

For SEL and SEE testing, the DUTs were prepared by acid etching the plastic above the die. For this testing, the DUT was operated in one of two modes. The first is a standby mode, or whatever mode the device would "reset" into. If a device is programmed with an LED blinker program, it is expected to boot up and run this program. We also ran an SRAM test where an alternating pattern of all 1s and all 0s was written and read back to determine the SRAM upset sensitivity. During high fluence test runs (the majority of test runs), the DUTs are believed to have reset themselves. However it was not possible to directly verify this without hindering the use of high fluences necessary for SEL testing.

Biased TID testing was conducted by loading the DUT with an LED blinker program during irradiation. Unbiased TID testing was conducted by securing the DUT to conducting foam and irradiating. Before and after each irradiation step, each DUT was tested for operating current and ability to operate three test applications. The applications were: (a) an LED blinker, (b) read and write of the device's flash memory in the debug environment, and (c) operation of a whetstone benchmark program.

B. SEL Test Results

MSP1612, devices tested for SEL, immediately showed 10 mA current increases upon exposure to the beam. These increases produce a stair-step type plot and never exhibited a reduction in current draw. Devices went from less than 1 mA of current to over 500 mA. We counted individual current steps as SEL because each step is believed to be caused by activation of another site. The resulting cross section curve is shown in Fig. 1. This also includes checks with increased bias and increased temperature resulting in increased event sensitivity. Difficulty with the rate at which steps accumulate at high LET result in the very large error bars seen. After $1.1\text{x}10^7$/cm^2 Au testing (LET 85.6 MeV-cm^2/mg), we observed that one device was no longer properly identified by the programming system. Instead of MSP430F1612, it was identified as MSP430F169 and the programming tools would not program the device in this configuration. Otherwise, all devices functioned nominally after their full exposures.

C. SEE Test Results

SEE testing was performed when possible, but the primary effort was on SEL results. For this reason, and the very disruptive effect of the high current events on the normal operation of the test software, SEE data was only collected at the LET 20 MeV-cm^2/mg test point. At this LET, we observed 64 0-to-1 errors and 53 1-to-0 errors, in a total fluence of 2.2×10^5/cm^2, yielding per bit cross sections of 1.4×10^{-7} and 1.2×10^{-7}cm^2/bit, respectively. This difference is too small to claim an asymmetry.

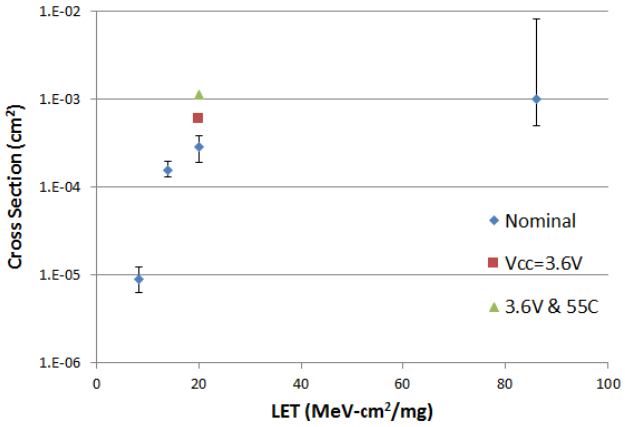

Fig. 1: SEL response of the MSP430F1612 test devices. All markers at LET 20 MeV-cm^2/mg have the same 2-σ error bars (some excluded for clarity). Large uncertainty at LET 85.6 is due to saturation of SEL counting.

D. TID Test Results

TID testing was performed with 10 of each type of MSP430 device, with half of each set tested unbiased and the other half tested biased. TID testing resulted in several different types of error modes. The error modes observed are the following:

1. LED fails to blink
2. Flash returns bit errors compared to upload image
3. Stack is full
4. Debugger starts without user control
5. Some registers are not readable
6. LED blinks even after a new program is uploaded to the DUT
7. Code does not run

TID results are summarized in Table II below. Note that we truncated the unbiased testing because it is not likely to be an operating scenario. However it may be possible to explore options for cold sparing. Biased devices were not functional at the 10 or 20 krad(Si) test points, but all were functional at the 5 krad(Si) test point.

Table II: Summary of TID test results for MSP430F1611 and 1612.

Device Type	Condition	# Tested	TID Result
1611	Unbiased	5	Good > 20 krad(Si)
1611	Biased	5	Fail between 5 and 10 krad(Si)
1612	Unbiased	5	Good > 20 krad(Si)
1612	Biased	5	Fail between 5 and 10 krad(Si)

III. TI MSP430FR5739

A. Test Setup

Given the construction of the MSP430F1611 and 1612, it was not unexpected that they would show SEL. An alternate device, the MSP430FR5739 is made on a much more modern process and includes both an epitaxial layer and ferroelectric random access memory (FRAM) [12]. We tested this device for SEL and limited SEE.

DUTs were mounted in the TI MSP-TS430RHA40A evaluation board. Test software operated at 1 MHz. The board was modified as follows. The socket was modified by removing the upper part of the clamshell and lowering the deck height of the lower portion. This allowed for using a metal plate to hold the DUT into the socket and make contact. Devices were acid etched to expose the die, with the outer lip left intact to contact the metal plate. The DUT's UART receive and transmit pins were connected to an added UART circuit to perform translation between logic levels and UART signal levels. The test setup used is shown in Fig. 2.

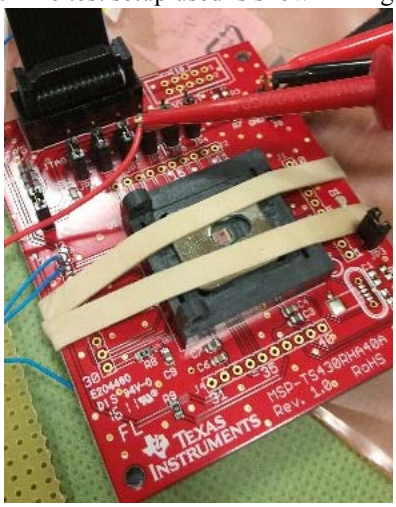

Fig. 2: MSP430FR5739 in MSP-TS430RHA40A evaluation board for SEE testing.

B. SEL and SEE Testing

DUTs were exposed to heavy ions at TAMU. The beams used are listed in Table III. All exposures were performed at normal incidence with the 15 MeV/amu beams.

The test sample was limited to one primary device due to extensive verification of a problem that occurred during SEL testing.

Throughout all beam exposures, including at elevated temperature and voltage (3.6 V and 85°C), the primary device did not exhibit any changes in current that were observable. During exposure, the DUT power draw was primarily to power up the UART ports and an LED port. Thus only a few mA were delivered to the DUT throughout all testing.

Table III: MSP430FR5739 heavy ion beam exposures at TAMU

Ion	Energy MeV/amu	Effective LET MeV-cm^2/mg	Fluence (cm^{-2})
Ne	15	2.6	1.10E+06
Ne	15	3.6	1.00E+06
Ar	15	8.1	1.52E+06
Au	15	86	2.00E+06

We were able to sensitize the on-chip SRAM for SEE testing during the SEL test effort. A limited amount of SEE data were collected and are presented in Fig. 3. Compare the apparent saturation cross section of around 1x10^{-8}cm^2/bit to the MSP430F1611/1612 at around 1.3x10^{-7}cm^2/bit.

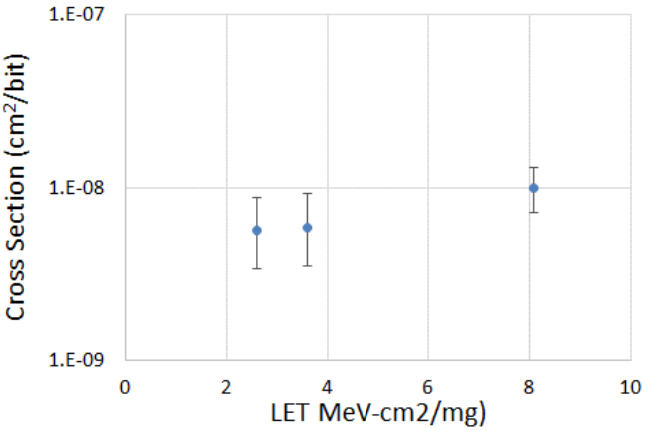

Fig. 3: SEE sensitivity of on chip SRAM cells in the MSP430FR5739. Error bars are 2-σ.

C. Discussion

Although the primary test sample was limited to one DUT, the SEE results presented indicate that SEL is not a concern. No changes in operating current were observed during exposure except for minimal oscillations that appeared similar to normal behavior.

After exposing the DUT to 2x10^6 there was a permanent problem with operating the DUT that required significant recovery of the test system to verify the extent of the failure. Upon recovery (requiring power cycle of all equipment including the programming computer) it was verified that the DUT was no longer programmable, as indicated by the programming tool included with Code Composer Studio. The specific complaint was that the DUT's configuration information was inconsistent and the tool suggested the DUT should be discarded. It is believed that this recovery scenario will be required on any devices that behave this way. It is not clear what the cross section for the behavior is, and further exploration is required.

IV. MICROCHIP PIC24F256GA110 AND DSPIC33FJ256GP710

We tested two devices from Microchip for SEL and SEE. The devices are the Microchip PIC24F256GA110 and dsPIC33FJ256GP710. Because the test board used is the

same for the two devices and the test approach and programming tools were the same, we report them together. The Microchip PIC24F256GA110 is a general purpose 16-bit microcontroller with built-in flash memory and a CPU capable of performing general purpose computing tasks. The microcontroller incorporates a set of varied peripherals including SPI, I^2C, UART and other devices for input/output (IO) operations [13]. It has 256 kB of flash and 16 kB of SRAM. The dsPIC33FJ256GP710 is a 16-bit digital signal controller. It also has built-in flash memory and a similar CPU to the PIC24. It shares a lot of features with the PIC24, and also includes analog to digital converters and analog comparators. It has 256 kB of flash and 30 kB of SRAM [14].

A. Test Setup

Heavy ion testing was performed at TAMU using several beams. The beams used are summarized in Table III.

Table IV: PIC24 and dsPIC33 heavy ion exposures at TAMU

DUT ID	Ion	Energy	Degrader	LET eff	Exposure
25 - PIC24	Au	15 MeV/amu	No	85.6	1.00E+07/cm²
17 - PIC24	Au	15	No	85.6	1.06E+07
11 - PIC33	Au	15	No	85.6	1.00E+07
13 - PIC33	Au	15	No	85.6	6.90E+05
13	Xe	25	No	44	7.20E+03
13	Kr	25	No	20	1.82E+04
12 - PIC33	Ar	15	Yes	14	5.90E+04
23 - PIC24	Ar	15	Yes	14	4.60E+04
12	Ar	15	No	8.3	3.40E+05
13	Ar	15	No	8.3	3.60E+05
11	Ne	15	No	1.8	1.00E+06
17	Ne	15	No	1.8	2.00E+06

Testing was performed with the Microchip Explorer 16 Development board, operating PIC devices at 8 MHz. This board uses a Plug-In Module (PIM) hardware setup that enables the preparation of independent DUT boards. We prepared DUT PIM boards with several delidded PIC24 and dsPIC33 devices.

For SEL testing, we monitored the current draw for the entire board. This is not ideal, but it turned out to be relatively straightforward, as the board draws only between 30 and 40 mA, but upon exposure to heavy ions instantly jumps by more than 200 mA. For this reason, SEL detection was set to 250 mA for most test runs, and the increase was usually obvious.

For SEE testing, the MPLAB software and hardware from Microchip were used to enable uploading of custom test programs. Two software applications were developed. One for testing the flash and another for testing the SRAM. The SRAM test was based on a write/wait/read approach. The SRAM test wrote a complementary pattern on each write/wait/read cycle. (SEE testing of the PICs will be presented in the full workshop.)

For TID testing a special set of adapter cables was made that allowed the DUT to be separated from the DUT board and powered with a separate power supply. Devices were tested for proper operation by utilizing three sets of test software. One was a flash test code that utilizes the device flash to store a large amount of text to be output during testing. The second was the Whetstone benchmark code [15]. And the final test code was a synchronous random access memory (SRAM) test that writes and reads to memory during testing. The flash memory test was utilized for exercising the test parts during exposure. TID testing was conducting using the JPL high dose rate facility. Exposures were performed at 17 r/s. Before and after each exposure level all three test programs were run to ensure the device was still functioning well. The TID levels at which these tests were performed are given in Table V. Test samples started with three devices for each test condition – Unbiased PIC24, Unbiased dsPIC33, and Biased dsPIC33. At the 5 krad(Si) test point one of the PIC24 devices was not functional and is believed to be unrelated to TID – thus it was removed from the results.

Table V: TID exposure levels for PIC24 and PIC33 devices

PIC24 - Unbiased	dsPIC33 - Unbiased	dsPIC33 - Biased
-	1 krad(Si)	1 krad(Si)
-	2	2
5 krad(Si)	5	5
10	10	10
15	15	15
20	20	20
50	50	-

B. SEL Test Result

SEL was detected readily in the PIC devices. A plot of SEL cross section is presented in Fig. 4, below. Sensitivity of the device to SEL was also explored with increased temperature, which is shown on the figure. The error bars on LET 20 and 44 MeV-cm^2/mg points with elevated temperature are about the same size as for the room temperature counterparts, as an example of temperature dependence expected in SEL. We could not increase the voltage with the Explorer 16 Board. Note that we could not run the DUTs at significantly elevated temperature because the thermal protection of the on-board power regulation would sometimes trip and actually recover SEL events creating questionable data. Significant issues with event counting while exposing devices to high fluence resulted in the large error bars for the LET 85.6 MeV-cm^2/mg point.

C. SEE Test Results

Although the primary intent of our SEE testing was to determine the SEL sensitivity, we were able to collect upset data on the on-chip SRAM on the PIC24 devices. The observed cross section is shown in Fig. 5. Note that in this case we separate the 0 to 1 and 1 to 0 SEUs, but there is no significant difference between these.

During Flash testing no changes were ever observed in the output data, indicating no changes to the stored program.

D. TID Test Results

All PIC devices showed no change in functional currents for any of the test programs for all TID levels at which they could be tested. The primary failure mechanism was that the devices could not be reprogrammed to run all of the test programs.

Table VI provides a summary of all the PIC TID testing. As indicated above, the PIC24 sample only includes two devices because of a problem with one at 5 krad(Si) that we do not believe was due to TID. As can be seen, unbiased devices generally fail between 15 and 20 krad(Si), while biased devices fail around 10 krad(Si).

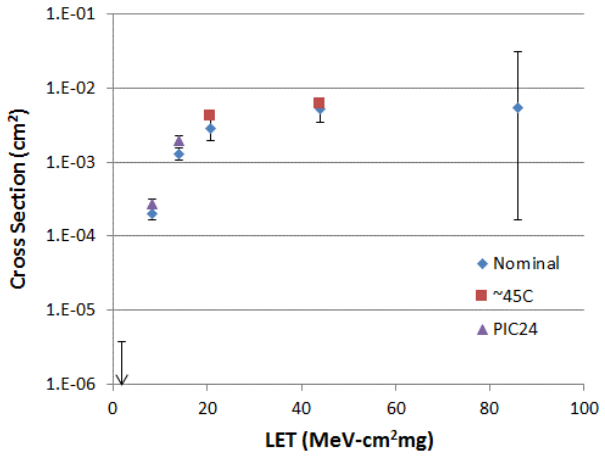

Fig. 4: SEL cross section of the dsPIC33 devices. Error bars are 2-σ.

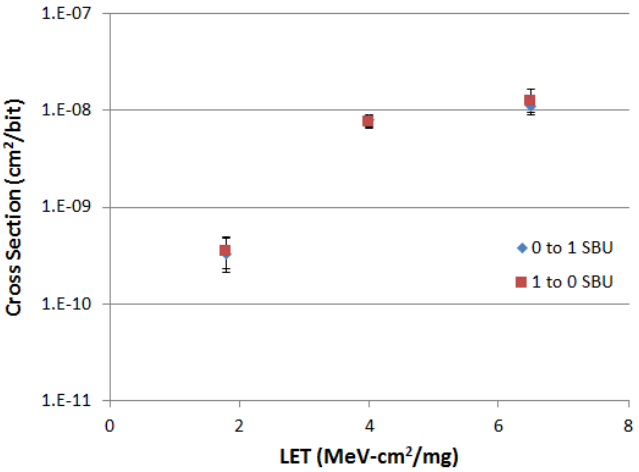

Fig. 5: The SRAM SEU sensitivity of the PIC24 DUTs. Error bars are 2-σ.

Table VI: Summary of TID results for PIC24 and dsPIC33 devices

TID Level	PIC24 - Unbiased	dsPIC33 - Unbiased	dsPIC33 - Biased
1 krad(Si)	-	0 fails	0 fails
2	-	0	0
5	0 fails	0	0
10	0	0	2 fails
15	0	2 fails	all fail
20	1 fail	all fail	
50	all fail		

A. *Discussion*

The testing of PIC devices was very similar to the MSP devices in terms of both failure levels and the primary failure mechanism. It is unknown how long the devices would function if the between exposure verification requirements did not include reprogramming the device. A repeat of this testing without the requirement of reprogramming the devices is expected. However, it should be understood that there is clearly something failing in the devices (most likely the flash cells), and without an extensive verification suite preprogrammed into the device, it is unclear how useful the result will be if the device functions to a significantly higher level than the results observed here.

V. ATMEL AT91SAM9G20

The AT91SAM9G20 microcontroller incorporates an ARM926EJ-S Thumb processor. The processor has separate 32 kB instruction and data caches. The device also includes additional on chip memories (including two 16 kB SRAMs), as well as a set of peripheral devices including USB ports and Ethernet communication [16].

A. *Test Setup*

SEE testing was performed at TAMU and the Los Alamos Neutron Science Center (LANSCE). The beams used are summarized in Table VII. Note that neutron exposure is with a white source intended to duplicate the terrestrial environment and contains a spectrum of energies.

Table VII: Beam exposures for AT91SAM9G20 devices for SEE testing.

DUT ID	Facility	Ion	Energy	Angle	LET eff	Exposure
4	TAMU	Au	15 MeV/amu	0	85.4	2.00E+07/cm²
2	TAMU	Au	15	0	85.4	2.00E+07
2	TAMU	Ar	15	0	8.3	2.30E+05
4	TAMU	Ar	15	0	4	1.00E+05
4	TAMU	Ne	15	0	2.7	1.10E+05
2	TAMU	Ne	15	0	2.7	3.60E+05
2	TAMU	Ne	15	60	5.6	3.60E+05
2	LBL	B	10	0	0.89	8.50E+06
2	LBL	B	10	60	1.78	2.20E+06
2	LBL	Cu	10	0	21.2	1.70E+05
2	LBL	Cu	10	60	42.4	2.85E+04
2	LBL	Cu	10	70	61.9	1.95E+04
1	LANSCE	n	*	*	*	1.29E+09
3	LANSCE	n	*	*	*	1.75E+08

Testing was performed on AT91SAM9G20-EK evaluation kits. The evaluation kit provides a useful platform for interacting with the DUT. The DUT is a surface mount device. It is directly soldered to the test board. We did not modify the test boards or create a socket for the DUTs. In order to expose the DUTs to heavy ions, it was necessary to acid-etch the plastic over the die. We were able to do this on two test boards without damaging the test boards. For neutron testing we did not modify the DUTs.

The test boards were set up (by jumper connections) to enable an external HP6629 power supply to provide both power sources for the DUT. The 1 V supply line was configured with a 200 mA SEL detection threshold, and the 3.3 V supply line was configured with a 300 mA SEL detection threshold. For SEL testing, these supply lines were set at 1.1 V and 3.6 V. The heat gun available for users at TAMU was used to heat the DUTs during SEL testing. For SEU testing, lower voltages of 0.9 V and 3.0 V were used for

some of the testing, but the results were somewhat statistically limited and showed no clear correlation between operating voltage and SEU sensitivity.

One on chip memory (OCM) 16 kB SRAM was tested on each DUT for SEU sensitivity. Testing was performed by using the Atmel SAM-BA software. This software enabled directly uploading a pre-defined memory pattern, and later downloading it to a file. Analysis software was then able to identify differences in the OCM. Testing was performed by loading a given pattern (all 1s or all 0s), irradiating the device, then reading the device back to observe SEUs.

B. SEL Test Results

Both DUTs 2 and 4 were exposed to $2x10^7/cm^2$ Au ions with an LET of 85.4 MeV-cm^2/mg for SEL testing. Each DUT was exposed to $1x10^7/cm^2$ Au ions at room temperature. Each DUT was also exposed to $1x10^7/cm^2$ Au ions at a temperature of 85°C. No significant change in the current draw on either of the power supplies was observed. No SEL was observed on the AT91SAM9G20.

C. SEE Test Results

Using the method discussed above, DUTs 2 and 4 were tested for SEU in the OCM with heavy ions, and DUTs 1 and 3 were tested with neutrons. Events at higher LET were obviously higher multiplicity than at lower LET, with the multiplicity being about 1.5 for LET 8.3 MeV-cm^2/mg and going up to about 4.5 for LET 85.4. The MBU cross section results are shown in Fig. 6, along with the average event multiplicity (dotted line).

Neutron results included SBU, MBU and resets. Resets were isolated to only one test board. Since the resets were significantly different between the two test boards it is believed the resets were not due to the processor. Between both boards, an MBU cross section of $1.10x10^{-12}cm^2$/bit (1.02,1.17) was observed. The multiplicity of MBU events with white neutrons was 1.19.

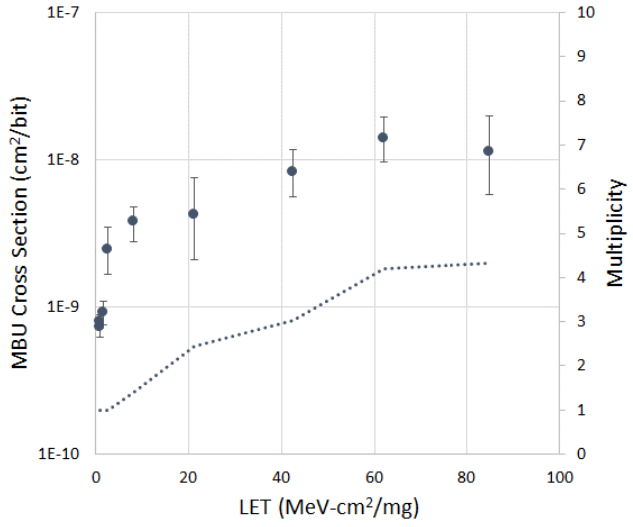

Fig. 6: Per bit cross section for MBUs in the AT91SAM9G20 OCM (data points). The dotted line shows the multiplicity of the average MBU event.

D. Discussion

The selection of the PIC and MSP devices (other than the MSP430FR5739) as well as this Atmel AT91SAM9G20 was based on identification of the devices being used by CubeSat kit manufacturers, made publically available. Of the parts tested, only the Atmel AT91SAM9G20 did not show SEL.

TID testing for further comparison is planned in the near future.

VI. Intel Atom E620T

A. Test Setup

The Intel Atom E620T was tested on the conga QA6 module [17] which was mounted to a conga-MCB/Qseven carrier board which operates the processor at 600 MHz [18]. The combination of both elements produces essentially a full computer. The E620T processor features a Low-Power Intel Architecture Core with on-die 32 kB 4-way L1 instruction cache, and 24 kB 6-way L1 data cache. It also includes a 512 kB on-die L2 cache [19]. The test setup, at the end of the beamline, is shown in Fig. 7 below. In this setup, a thinned E620T DUT card is shown, mounted to the conga-MCB. Two fans, mounted to the aluminum plate, blow air across the thinned DUT. A thermal monitoring circuit is positioned facing the DUT to monitor the temperature. The board was connected to a monitor via the HDMI port and a USB keyboard. For SEE testing, a custom build of the GRUB boot-loader with test code embedded was used – this was booted using a USB memory stick. 12V power was delivered to the board by a generic power supply which was monitored and logged with an external laptop control computer.

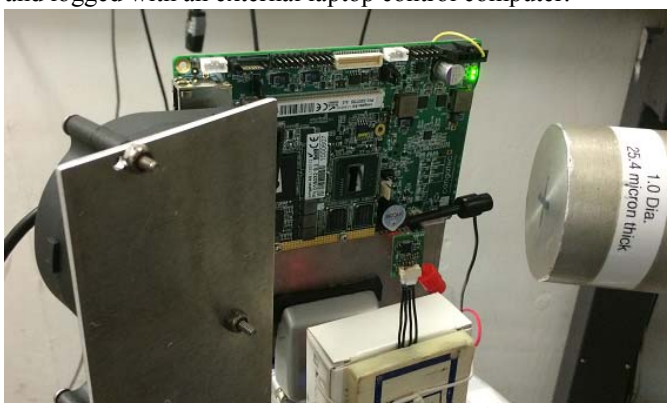

Fig. 7: The Conga QA6 - Intel E620 DUT board is shown mounted to the Conga MCB/Qseven board.

Reported radiation testing of the Intel Atom E620 includes SEL and SEE testing. The E620 requires a power control integrated circuit that was not possible to duplicate for this testing [19], so for SEL testing it was necessary to monitor the board current and analyze changes for possible signs of SEL. For SEE testing we operated the device in two general approaches: (1) we would boot the device to the BIOS screen and utilize periodic keystrokes or monitor the updating of the system clock to ensure operation continued; and (2) we developed custom software that performs write-dwell-read operations in order to attempt to test the data cache.

Testing was performed at TAMU, utilizing the two general operating modes listed above. A list of exposures is provided in Table VIII.

SEL testing was performed by monitoring the 12V power delivery to the board and noting if the current increased significantly. SEL testing was performed at 85°C, using a heat gun and a thermal detection system to control the temperature of the die.

Table VIII: TAMU beams used in SEE testing of Intel E620

DUT #	Ion	Energy MeV/amu	Effective LET MeV-cm^2/mg	Fluence (cm^{-2})
1	He	15	0.15	1.20E+07
1	Ne	15	3.3	2.08E+05
1	Ar	15	10.4	8.39E+03
1	Kr	25	57.1	4.13E+07
2	Kr	25	57.1	2.14E+07
1	Kr	25	75	7.67E+07

SEE testing was performed by using the method where test SW on the DUT attempts to sensitize and detect upsets in the device. The SW was designed to write a pattern (all 0s or all 1s) to a section of memory, then wait till a character was detected on a USB keyboard connected to the DUT, at which point the SW would read the section of memory and determine if any bits have changed. Any discrepancies are reported for SEE analysis. The test code was configurable between 16 and 64kB, so that in one configuration the test data will reside in the L1 cache, while the other configuration uses the L2 cache. Data were accessed in order from a start address to an end address, guaranteeing that during the read back, the final data in the L1 cache is pushed out to the L2 cache, and the first data are read in from the L2 cache (thus under the 64 kB setting, there is still significant L1 sensitivity). The conga-MCB provides a connection to a video display via an High Definition Multimedia Interface (HDMI) port. It does not provide a Universal Asynchronous Receiver Transmitter (UART), so the software is designed to use the video display for reporting collected test data. Because of this time-sensitive display, much of the testing was performed while video recording the output screen.

B. SEL Test Results

The conga MCB was used to irradiate test samples for SEL. A heat gun was used to maintain the temperature of the test device at 85°C. One device was exposed to a total of $2x10^7$/cm^2 at LET 75 MeV-cm^2/mg, while another was exposed to $2x10^7$ at LET 57.1 MeV-cm^2/mg. It was not possible to directly supply power to the DUT using the test hardware, however no significant changes to the operating current of the test board were observed (reductions were observed and were generally related to the processor in a lower functioning state, such as crashed). The 12 V power supply delivered between 590 and 700 mA during all testing, with current generally decreasing between the start and end of SEL exposures.

C. SEE Test Results

As indicated earlier, the E620 running on the conga Qseven board does not have a serial output port. Because of this, we have been only able to use the HDMI output port, which connects directly to the E620 (that is, there is no other video chip).

Two types of SEE have been observed. First, when leaving the device in the BIOS screen, we observed the system clock stop updating. Second, in the BIOS test, and in the custom software test, we have observed crashes, where the video output turns off. This is usually followed by the device resetting and the video output turning back on.

For the BIOS screen, the cross section for both execution stop and crash/restart was measured at $2.80x10^{-4}$cm^2/device (1.40,5.01) at LET 58 MeV-cm^2/mg.

For the memory test SW, the observed cross section for execution stop and crash/restart was characterized over a limited LET range and is given in Fig. 8.

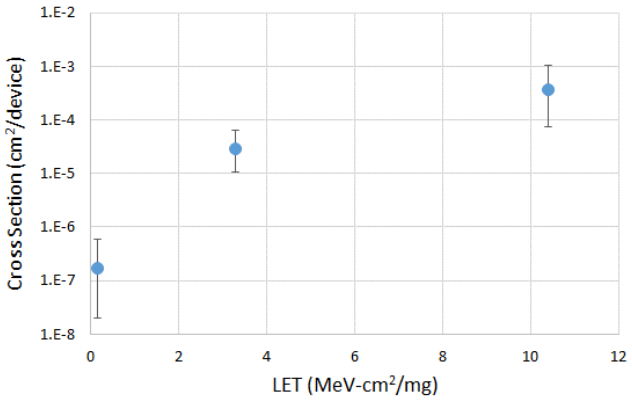

Fig. 8: Cross section for crashes during execution of memory test SW on the Intel E620T. Error bars are 2-σ.

D. Discussion

The test board used for this test did not provide a UART port. This created a significant lack of visibility into the state of the processor at the point where an unexpected behavior occurred. The tested configuration only included HDMI output which would usually turn off (with unclear indication if the interface shut down, the device was resetting, or any other condition occurred). Future work includes improving visibility of the system at the point where a crash occurs.

Although two methods of testing were tried, some others are still possible. It should be noted that the methods used are believed to be good for establishing the SEE sensitivity of the caches which are expected to contribute the most to the crash rate. Alternate test methods being explored include disabling the cache and creating an immediate output indication of the state of the device when something goes wrong. The use of a hardware debugger is also being considered.

Future work is expected to include additional Atom devices, such as the 22 nm E3825. The newer generations of Intel Atom devices include an on-chip UART which is expected to alleviate some of the development and test efforts discussed here.

VII. Qualcomm Snapdragon APQ8064

A. Test Setup

The Qualcomm Snapdragon APQ8064 device was tested for SEL and limited SEE. Because of issues with the reliability of the general SEE performance, quantitative results are limited to SEL results on this device and a single LET for SEE behavior.

Testing was performed using heavy ions at the TAMU cyclotron. The test board used was the IFC6410, from inforce [20]. The APQ8064 contains four Krait processing cores. The four Krait cores operate at 1.7 GHz, however there are five other processors inside the APQ8064 which operate at different frequencies.

Table IX: TAMU beams used in SEE testing of APQ8064 devices.

DUT #	Ion	Energy MeV/amu	Effective LET MeV-cm^2/mg	Fluence (cm^{-2})
2	Kr	25	23.1	1.45E+03
1	Kr	25	57.1	2.70E+07
1	Kr	25	75	2.05E+07
2	Kr	25	75	2.40E+07

B. SEL and SEE Testing

No SELs were observed during 75 MeV-cm^2/mg exposures of 2.1×10^7/cm^2 at 65°C, and 2.3×10^7/cm^2 at room temperature.

SEE usually resulted in the reporting of an exception or failure of the device to continue operating. In order to have reliable results, controlled SEE testing was only performed at 23.1 MeV-cm^2/mg. At this LET, the cross section for crashes and exceptions (mostly parity events) was 4.8×10^{-3}cm^2/device (1.9,9.9).

C. Discussion

The general SEE results (non SEL) obtained are of limited value because the DUT boards were observed to have different SEE performance during various stages of boot, making it difficult to interpret any crash or upset information. And unfortunately the full boot sequence takes several minutes and was not considered worth the expense during heavy ion testing. Thus, most of the SEE results were obtained during various stages of the boot sequence, which do not represent any particular operating configuration. The single data point provided at LET 23.1 gives a rough value for future reference.

Future work on this device is targeted at establishing a much faster boot sequence that boots the device to a prepared test algorithm very quickly, enabling collection of higher quality SEE data. There are tools that enable custom boot behavior that can enable booting to test code in only a few seconds, which will significantly reduce the dead time between events and confusion associated with the system state during boot.

VIII. Conclusion

The findings here are focused on microcontrollers of interest in CubeSat and other small or low-budget missions, as well as mobile microprocessors. The tested devices include TI MSP, Microchip PIC, Atmel ARM-based devices, Intel Atom, and Qualcomm Snapdragon. Results show sensitivity to SEL in some devices, SEE sensitivity in all devices, and TID limitations in the MSP and PIC devices.

The SEL results in the MSP and PIC devices, although drawing high current, generally did not result in failed devices, though there is always a danger of latent failures. Tested MSP devices were observed to not operate correctly after 1×10^6/cm^2 at 86 MeV-cm^2/mg LET. PIC, Atmel, Intel, and Qualcomm devices continued to function correctly (after power cycle) after exposure to more than 1×10^7/cm^2 at LETs of at least 75 MeV-cm^2/mg.

TID results in the MSP devices showed no failures to 20 krad(Si), for unbiased devices. Biased devices, both the 1611 and 1612 types, all failed by 20 krad(Si). Identification of the failure mechanisms was limited by problems we had with the devices, and are related to both ability of the programming system to reprogram the part, and the ability of the part to correctly run a set of test programs. PIC devices showed failures in essentially the same TID ranges, with unbiased devices failing between 15 and 20 krad(Si), while biased dsPIC33 devices failed between 10 and 15 krad(Si).

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