CSCE230 – Digital Design I
Homework 4

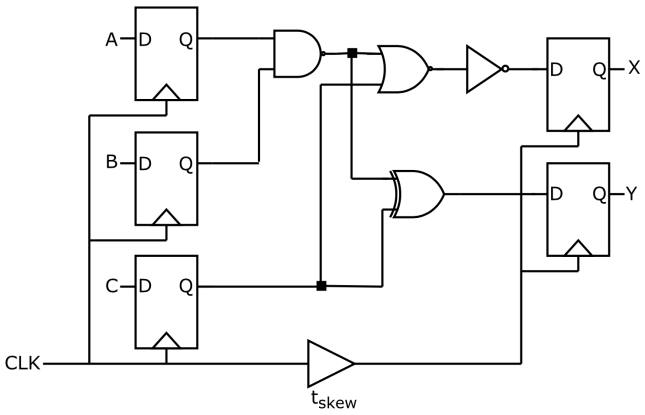
1. For the following state transition table

P.S.	N.S.		O/P	
	X=0	X=1	X=0	X=1
S0	S0	S4	1	0
S1	S0	S4	0	0
S2	S1	S5	0	0
S3	S1	S5	0	0
S4	S2	S6	0	1
S5	S2	S6	0	1
S6	S3	S7	0	1
S7	S3	S7	0	1

   a) [2 pts] What type of FSM does the above state transition table specify?
   b) [8 pts] Minimize the number of states using the implication table method.

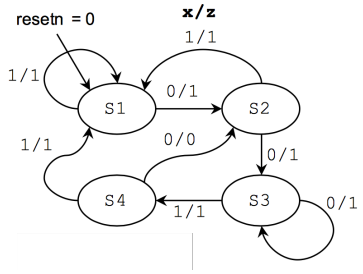
2. [10 Pts] Synthesis a decade counter (counts: 0, 1, 2, …, 8, 9, 0, 1, 2, …) as a Moore FSM.

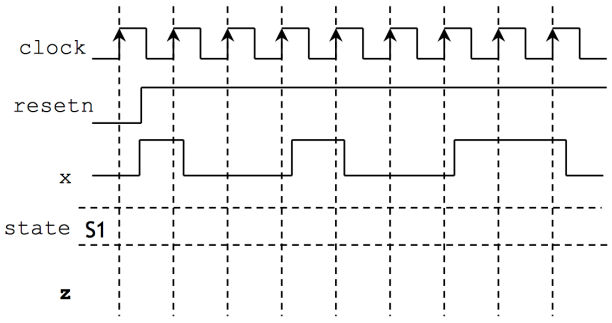
3. Consider the following circuit



   Assume that propagation delay is 15ps for the inverter, 20ps for the NAND gate, 30ps for the NOR gate and 60ps for the XOR gate. Also, assume that all the flip-flops are identical with t_{CQ}=35ps and t_{su}=30ps.
   c) [10 Pts] What is maximum clock frequency for reliable operation (t_{skew}=0).
   d) [10 Pts] Assume that the circuit is modified so that the clock reaches X and Y before A, B and C (negative clock skew). What is the amount of negative clock skew the circuit can tolerate if it needs to operate at 5 Ghz.

4. [20 Pts] Complete the timing diagram of the following state machine. Verify your solution by implementing the FSM in Verilog and simulate it using CloudV. You need to include a screenshot of your simulation.





5. A sequential circuit has one input and one output. The output becomes 1 and remains 1 thereafter when at least two 0's and at least two 1's have occurred as inputs, regardless of the order of occurrence.
   a) [5 pts] Draw a state graph (Moore type) for the circuit (nine states are sufficient). Your final state graph should be neatly drawn with no crossed lines.
   b) [5 pts] Reduce the number of states using the implication table method.

6. [10 pts] Design a three-bit counter-like circuit controlled by the input w. If w=1, then the counter adds 2 to its contents, wrapping around if the count reaches 8 or 9. Thus if the present state is 8 or 9, then the next state becomes 0 or 1, respectively. If w=0, then the counter subtracts 1 from its contents, acting as a normal down counter. Use D flip-flops in your circuit.

7. [5 pts] Repeat problem 2 using JK flip-flops.

8. [5pts] Repeat problem 2 using T flip-flops.

9. [5 Pts] Draw the state diagram of a vending machine controller (FSM) that releases a product when 15 cents are deposited. The vending machine has one coin slot that accepts dimes (10¢) or nickels (5¢). The coin slot is attached to a coin detector that has the 2 outputs (connected to the controller) **N** and **D**. The controller has the output **O**. **O** is activated when the controller detects the deposition of 15 cents. Also, the controller has another output (**R**) to deposit the change (a nickel).

10. [10 Pts] Reduce the state diagram of 9.

You must hand in the homework to the TA by hand before Thursday April 27th, 2017 (3:30 PM).