

CSCE2301 – Digital Design I

Homework 4

- 1) [45 Pts] Using cloudv (cloudv.io) model the following components. Verify each model through simulation (the testbenches must be self-checking):
 - a) [5 Pts] 1-bit FA (functional model)
 - b) [5 Pts] 4-bit Carry Lookahead Adder (CLA)
 - c) [15 Pts] n-bit RCA using the 1-bit FA module (configurable n-bit Carry Ripple Adder; check the attached material).
 - d) [20 Pts] n-bit carry select adder with m k-bit stages ($n = m \times k$; m, n, and k are integers). The stage could be RCA or CLA (parameterized). For CLA stages k must be 4.
- 2) [10 Pts] Add/subtract the following pair of numbers:
 - a) $(AB)_{16} + (CD)_{16}$
 - b) $1000 + 1001$
 - c) $(234)_8 + (121)_8$
 - d) $(0101)_2 + (0011)_2$
 - e) $(120)_3 + (101)_3$
- 3) [10 Pts] Express each of the following numbers as an 8-bit signed magnitude, 1's complement and 2's complement binary number:
 - a) -31
 - b) +17
 - c) 0
 - d) -128
 - e) -127
- 4) [10 Pts] Design a 4-bit 2's complementer. (The output generates the 2's complement of the input binary number) Show that the circuit can be constructed with XOR gates.
- 5) [10 Pts] Sometimes the term contraction is used to describe the procedure of designing a new logic circuit starting from an existing circuit when the inputs are fixed (constant). Use contraction to design increment-by-3 circuit with carry out starting with 4-bit ripple carry adder.
- 6) [10 Pts] Design a circuit that multiplies a 4-bit multiplicand by the constant 1010_2 (10). Use contraction to simplify your design.
- 7) [5 Pts] Show how 3-input LUT's can be used to implement 1-bit Full Adder.
- 8) [5 Pts] Using the CLA design outlined on slides 30 and 31, calculate the delay of the 4-bit CLA using the following delay models for the gates:
 - AND, OR, NAND, NOR, NOT: delay = $(8 + 2 \cdot n) \tau$
 - XOR: delay = $(12 + 2 \cdot n) \tau$Where n is the number of inputs to the gate, and τ is a time constant. Assume that all inputs to your design are available at time zero.

Submission deadline: Wed. Nov. 1st, 2017 1:59PM. The TA will post the submission instructions.