CSU22022 Computer Architecture I

Introduction

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Module Objective

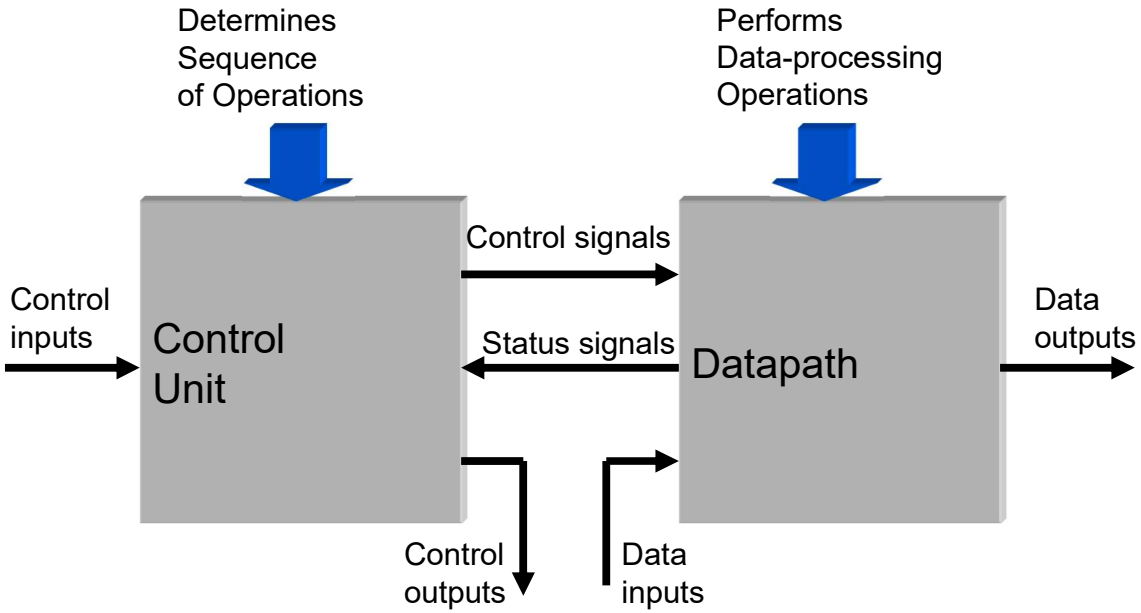
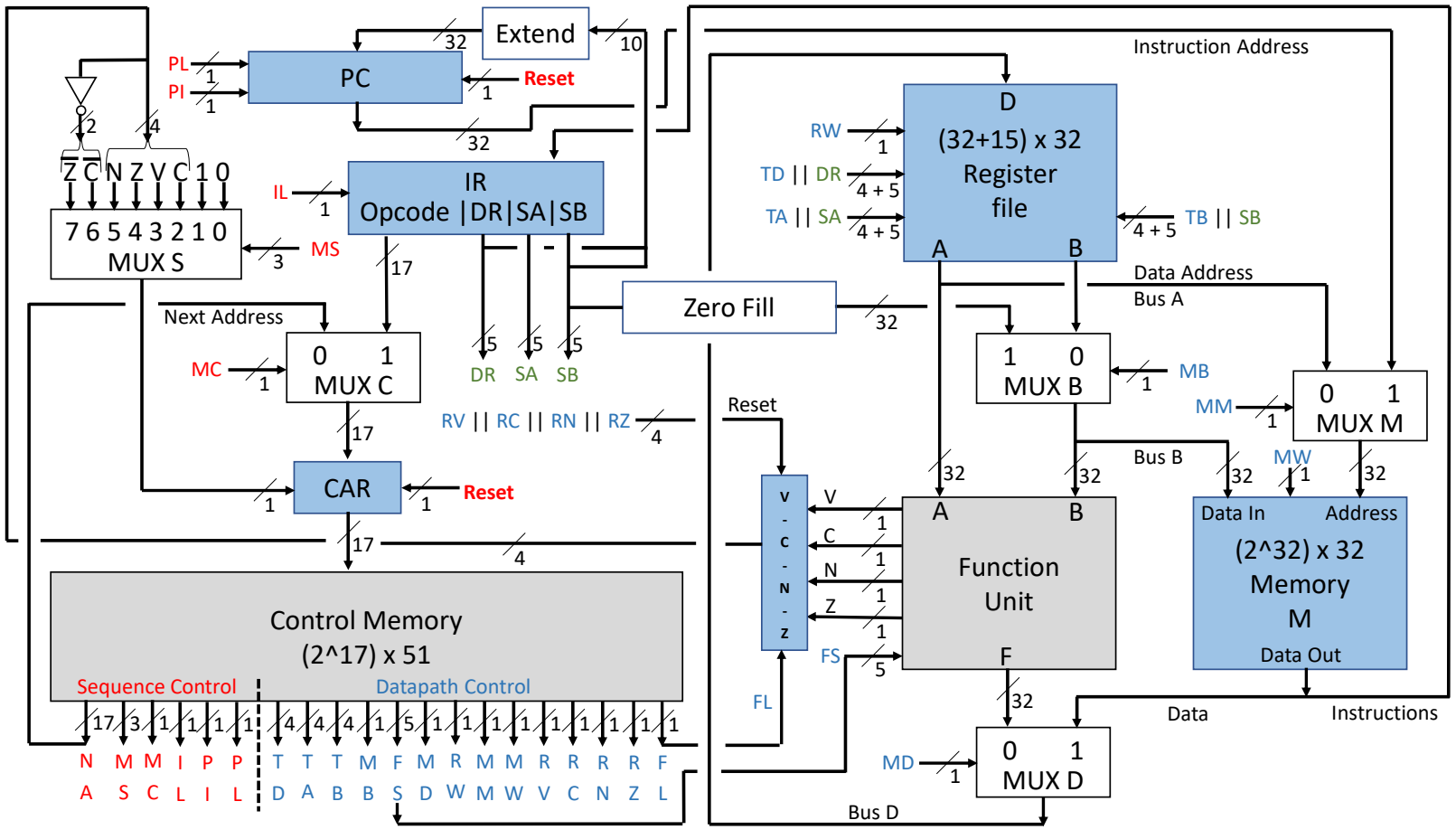


Figure 1: This is the caption for this figure

The aim is to give you a good understanding of the design and operation of an instruction processing unit and the functional subsystems which execute these instructions.

We Design and Simulate a 32-bit Processor



Hardware Description Language (HDL)

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity ANDGate is
5      Port ( x : in STD_LOGIC;
6             y : in STD_LOGIC;
7             F : out STD_LOGIC);
8  end ANDGate;
9
10 architecture Behavioral of ANDGate is
11
12 begin
13
14     F <= x AND y after 3ns;
15
16 end Behavioral;
```

Listing 1: We will use VHDL to design and simulate the processor

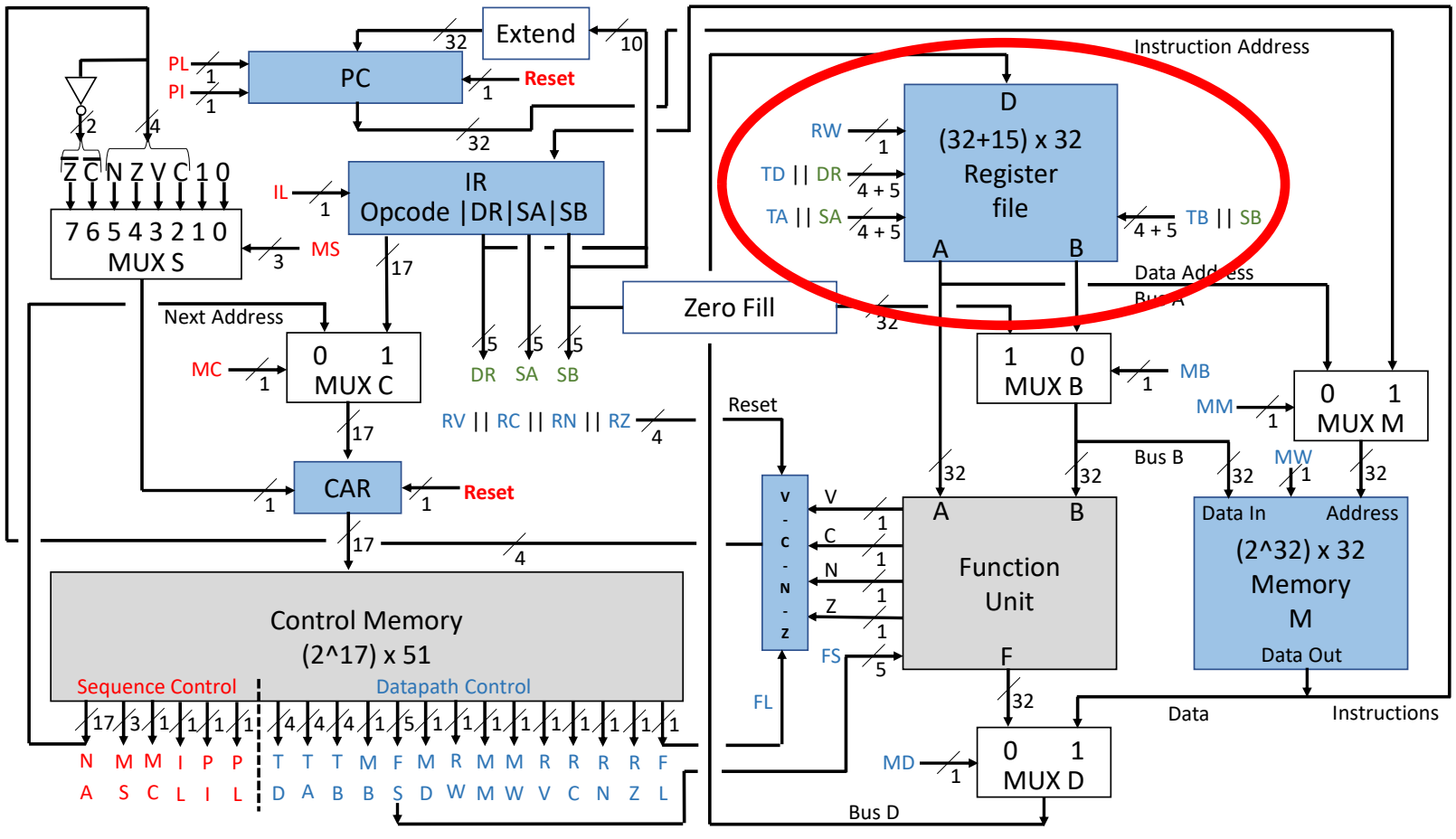
Assessment

- The module is assessed by coursework [100%]
  - Lab Assignments [Total 16%]
    - 8 Lab Assignments
  - Milestones [Total 14%]
    - 3 Milestones
    - These are marks for completion on time
    - You will have to resubmit this work as one of your full processor instalments
  - Full Processor Assignment [Total 70%]
    - 4 Instalments of the entire processor
- Reassessment
  - 5-hour take-home exam
  - in August

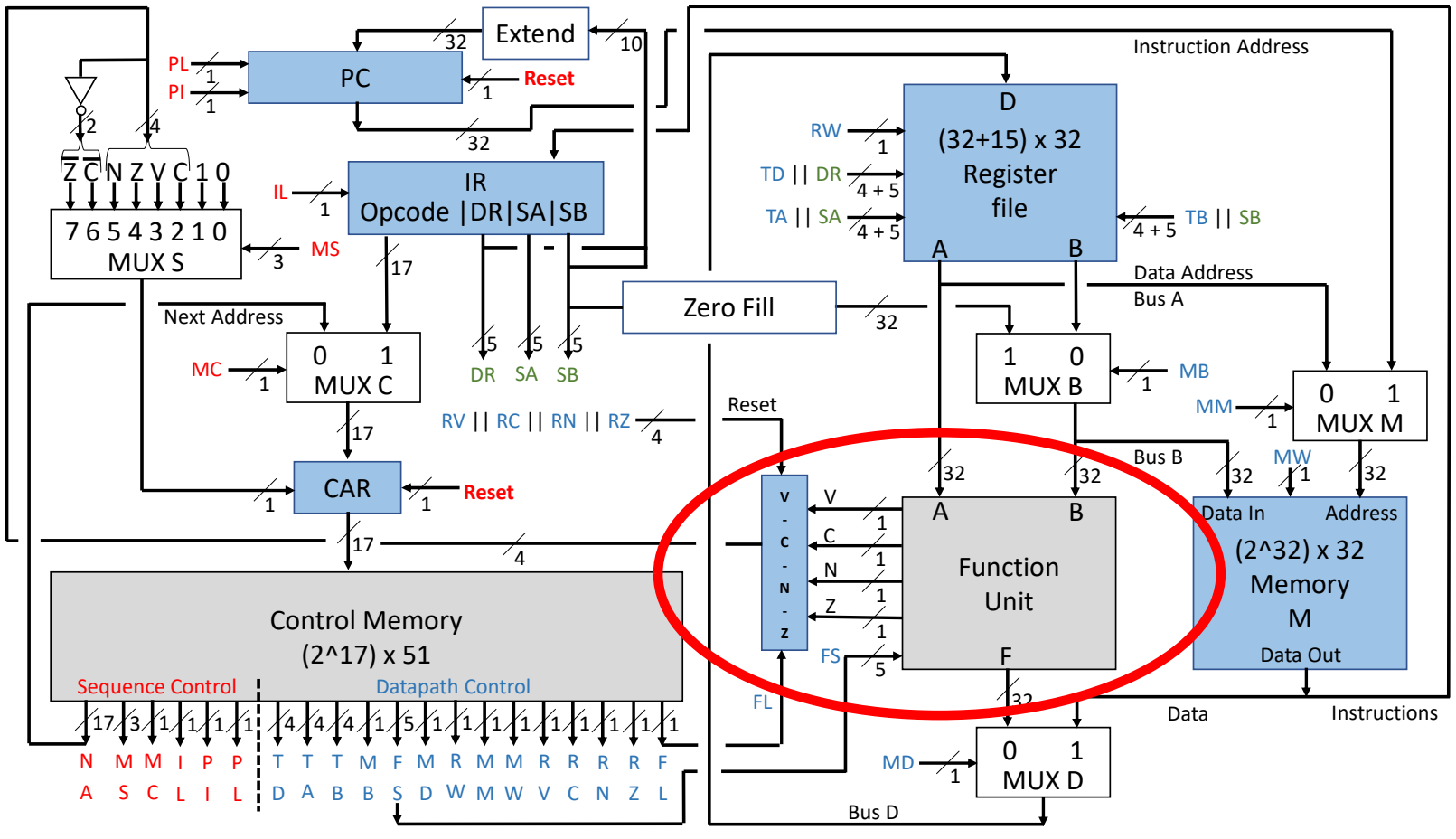
Lab Assignments [16%]

- 1st Lab Assignment – Combinational Logic [2%]
- 2nd Lab Assignment – Synchronous Sequential Logic [2%]
- 3rd Lab Assignment – Port Map instantiation in VHDL [2%]
- 4th Lab Assignment – 3-bit Parallel Adder [2%]
- 5th Lab Assignment – Register file [2%]
- 6th Lab Assignment - Binary Multiplier Datapath [2%]
- 7th Lab Assignment - Binary Multiplier, Datapath with Sequence Register and Decoder Control [2%]
- 8th Lab Assignment - Binary Multiplier, Datapath with Control Memory [2%]

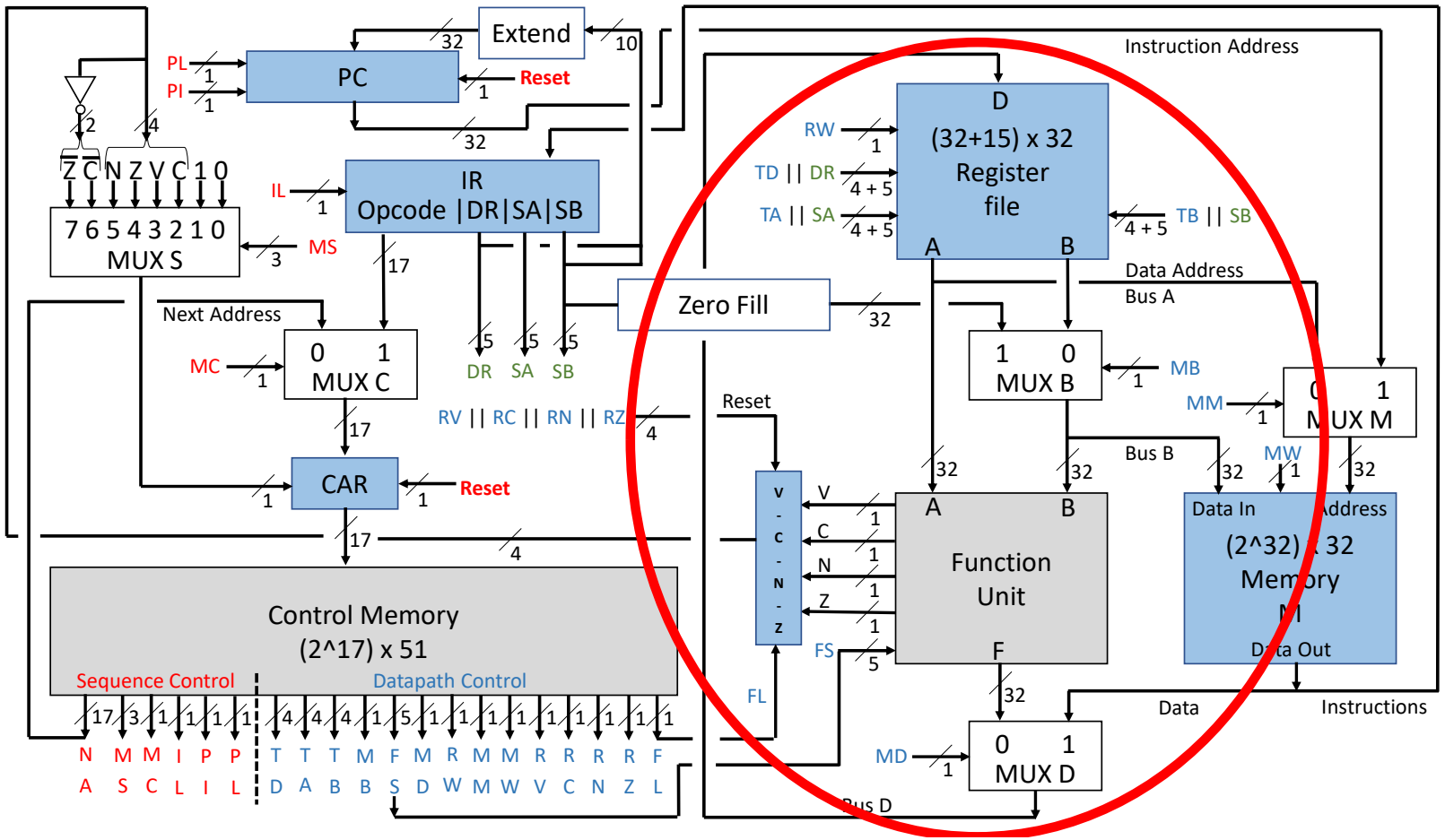
Milestone - Register File - Due Date 20th October [5%]



Milestone - Function Unit - Due Date 3rd November [4%]



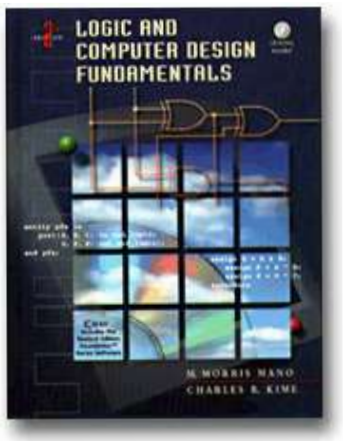
Milestone - Datapath - Due Date 10th November [5%]



Full Processor Assignment [70%]

1. Full Processor Project (1st instalment) [20%]
   - Due Date 30th November
   - All entities related to the Register File
2. Full Processor Project (2nd instalment) [10%]
   - Due Date 7th December
   - All entities related to the Function Unit
3. Full Processor Project (3rd instalment) [10%]
   - Due Date 14th December
   - All entities related to the Datapath
4. Full Processor Project (Last instalment) [30%]
   - Due Date 21st December
   - All entities related to the Control

Textbooks



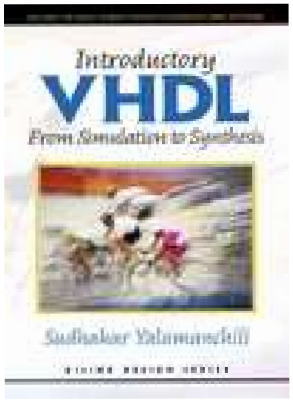


Figure 6: Textbooks

- Introductory VHDL: From Simulation to Synthesis
- Logic and Computer Design Fundamentals 2nd Edition updated, Mano

Lesson Plan - Week 1 to 5

- 1st Week (Teaching)
  - 1st Lab Assignment – Combinational Logic [2%]
    - Hardware Description Language VHDL
    - Simulation
- 2nd Week (Teaching)
  - 2nd Lab Assignment – Synchronous Sequential Logic [2%]
    - Flip-flop
- 3rd Week (Teaching)
  - 3rd Lab Assignment – Port Map instantiation in VHDL [2%]
- 4th Week (Teaching)
  - 4th Lab Assignment – 3-bit Parallel Adder [2%]
    - Register Transfer Level
- 5th Week (Teaching)
  - 5th Lab Assignment – Register file [2%]

Lesson Plan - Week 6 to 10

- 6th Week (Teaching)
  - Milestone - Register File Due Date 20th October [5%]
- 7th Week (Teaching)
  - Study/Review
- 8th Week (Teaching)
  - 6th Lab Assignment - Binary Multiplier Datapath [2%]
  - Milestone - Function Unit Due Date 3rd November [4%]
- 9th Week (Teaching)
  - 7th Lab Assignment - Binary Multiplier, Datapath with Sequence Register and Decoder Control [2%]
  - Milestone - Datapath Due Date 10th November [5%]
- 10th Week (Teaching)
  - 8th Lab Assignment - Binary Multiplier, Datapath with Control Memory [2%]

Lesson Plan - Week 11 to 3rd Week after Teaching Term

- 11th Week (Teaching)
  - Labs to answer questions
- 12th Week (Teaching)
  - Labs to answer questions
  - Full Processor Project - Due Date 30th November [20%]
    - 1st instalment – all entities related to the Register File
- 1st week after Teaching Term
  - Full Processor Project - Due Date 7th December [10%]
    - 2nd instalment – all entities related to the Function Unit
- 2nd week after Teaching Term
  - Full Processor Project - Due Date 14th December [10%]
    - 3rd instalment – all entities related to the Datapath
- 3rd week after Teaching Term
  - Full Processor Project - Due Date 21st December [30%]
    - Last instalment – all entities related to the Control