

# CSU22022 Computer Architecture I

## Seventeenth Lecture - Control Unit

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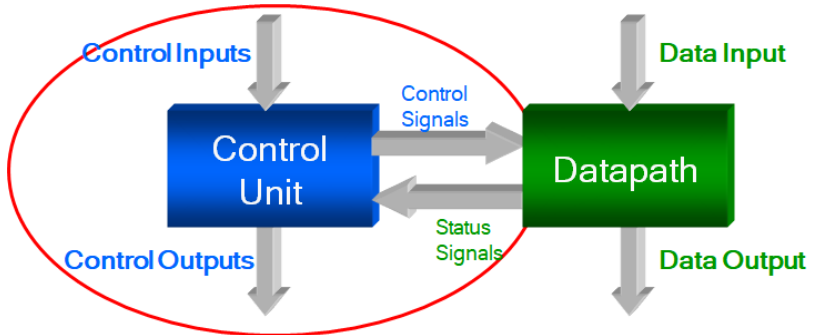
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# Control Unit

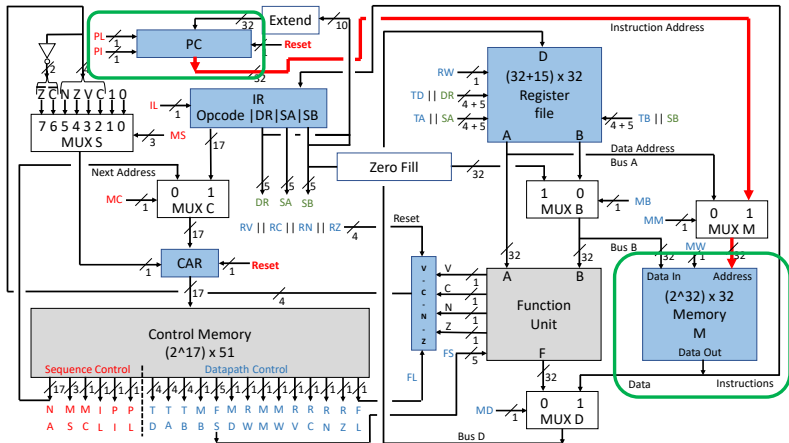
- The Control Unit:
  - Supplies all the control signals to the datapath
  - Responds appropriately to the datapath's status signals
    - e.g., C, V, Z, and N



# Von Neumann Architecture (Processor)

- Input to the control unit:
  - A stream of instructions coming from memory M
  - This stream must be converted to a sequence of micro-operations for the datapath
- Control Unit uses:
  - Program counter PC to index in M the next executable instruction

# Program counter **PC** and Memory **M**



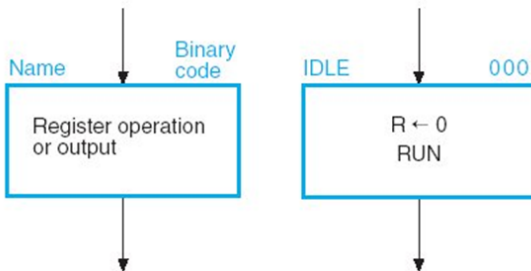
# Algorithmic State Machine (ASM)

- Data processing may be achieved through:
  - Sequencing Register transfer operations
  - May be specified as hardware algorithm
    - Consists of a finite number of procedural steps
- ASMs are used:
  - in the Control Unit

- Algorithmic State Machine (ASM) Chart
  - Defines the hardware algorithm
  - Defines the relationship to time
    - Clock
- Three basic elements:
  - State Box
  - Decision Box
  - Conditional Output Box

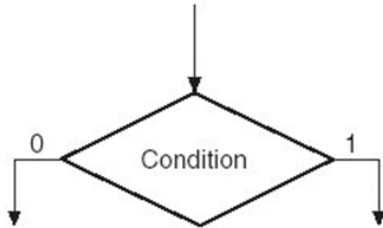
# State Box

- State Box contains:
  - Register transfer operation or output signals that are activated while the control unit is in this state
  - RUN is 1 for any box it appears and 0 for any box it does not appear



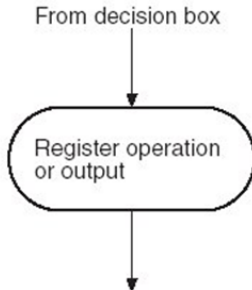
## Decision Box

- Exit path is taken if input condition is:
  - True (1)
  - False (0)

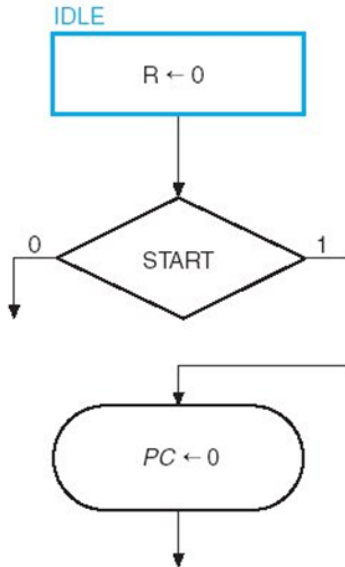




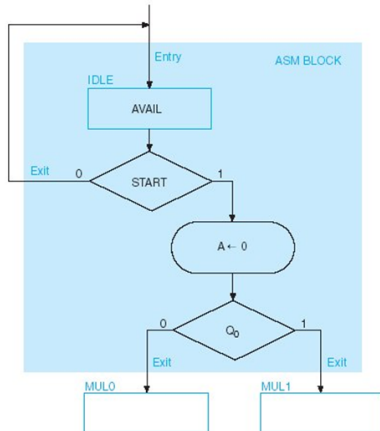
Conditional Output Box entry path must pass through one or more decision boxes



## ASM Box Example

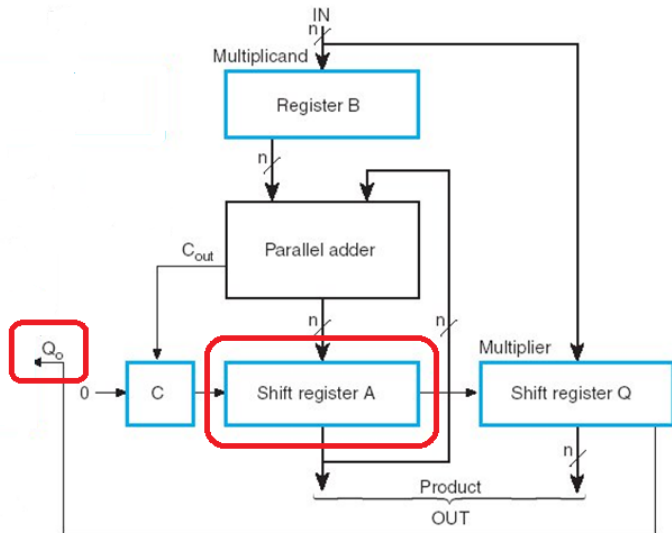


# ASM Block

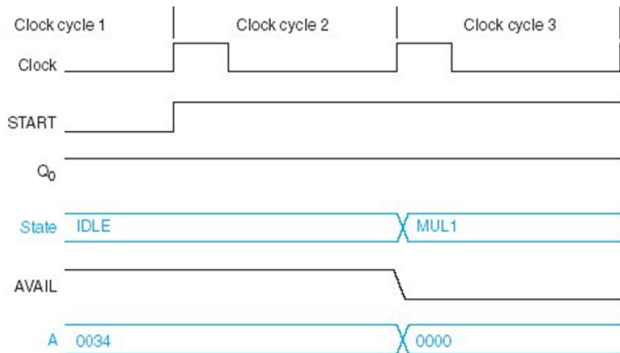


**Figure 1:** This ASM block controls the Binary Multiplier. See lecture notes Sixteenth

## Shift Register A and Signal $Q_0$



# Timing Diagram

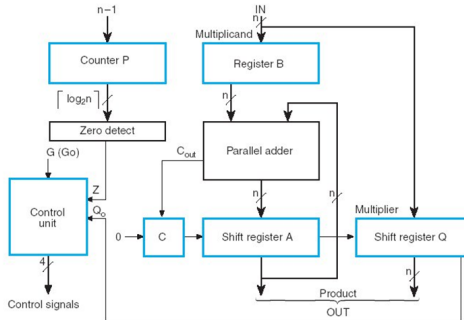


**Figure 2:** This vector and signals are driven by the ASM Block shown in figure 12

- Two contrasting approaches to control unit design have evolved:
  - Hard-wired
  - Micro-coded

# Hard-wired Binary Multiplier Control

- The VHDL schematic below shows:
  - Datapath
  - Status signals  $Z$  and  $Q_0$
  - External Input
  - $G = G_0$
  - Output



# Binary Multiplier ASM (Hard-wired)

