CSU22022 Computer Architecture I

Twenty-first Lecture - Status Register and CAR

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CPU_DFlipFlop_XXXXXXXX

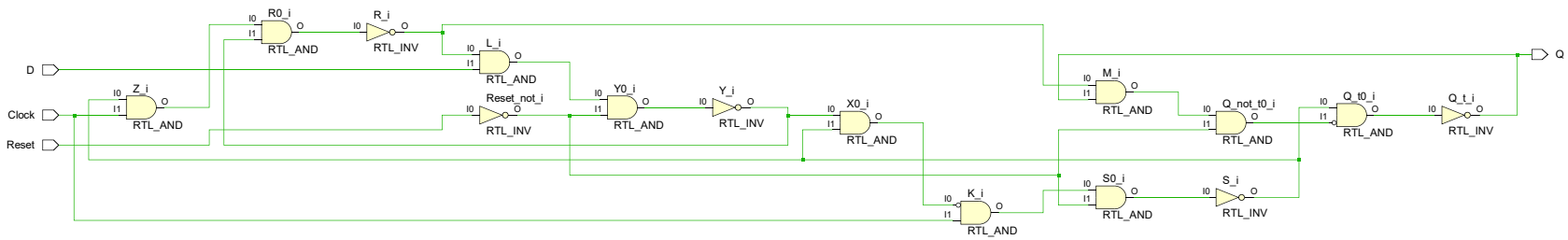
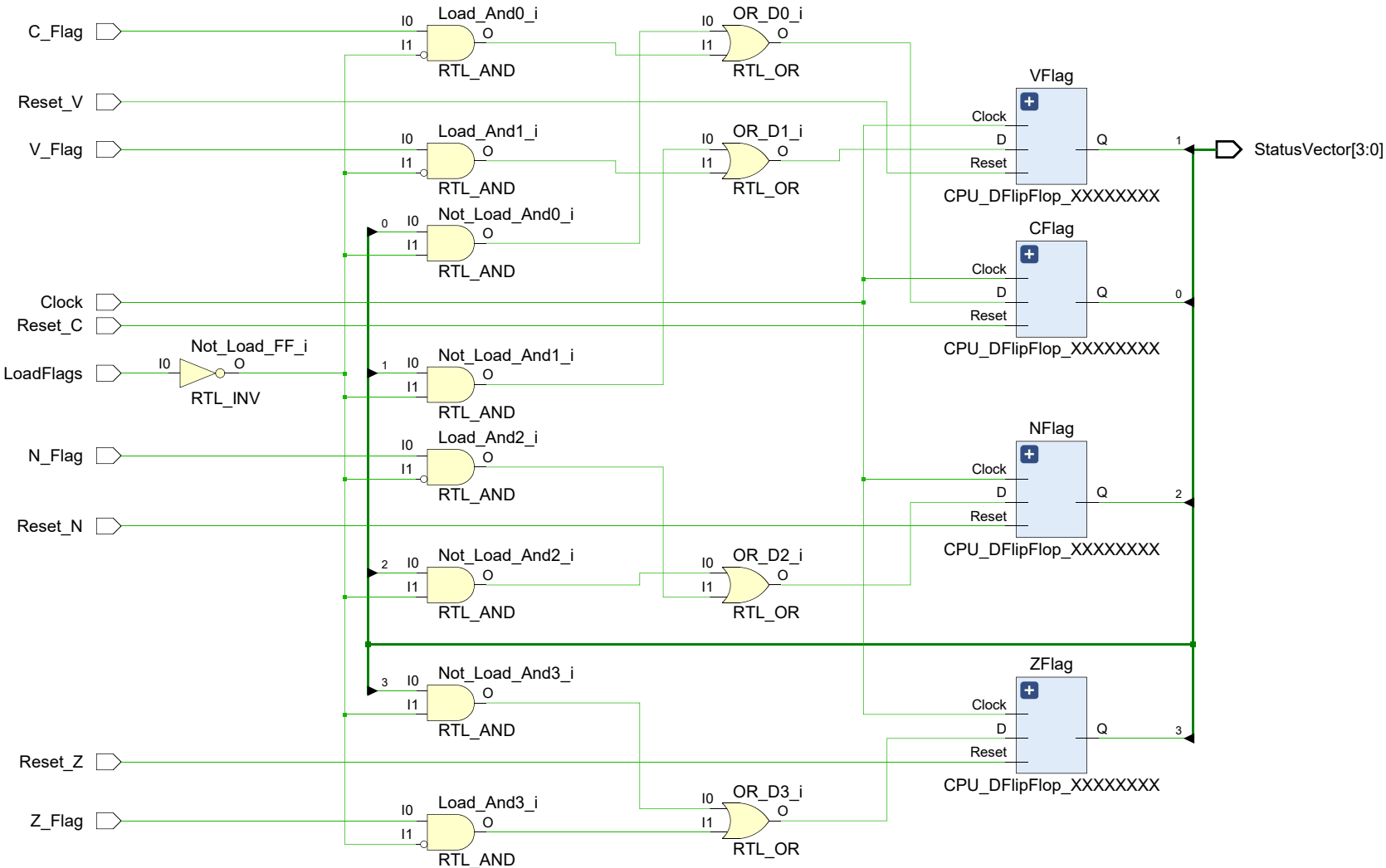


Figure 1: The CPU_DFlipFlop_XXXXXXXX is required for the implementation of the CPU_StatusRegister_XXXXXXXX

CPU_StatusRegister_XXXXXXXX



CPU_DFlipFlop_Qnot_XXXXXXXX

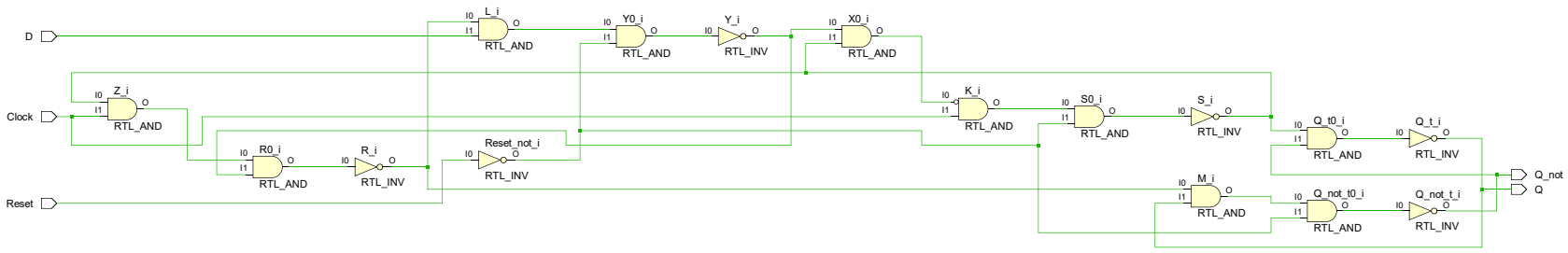


Figure 2: The CPU_DFlipFlop_Qnot_XXXXXXXX is required for the implementation of the CPU_JKFlipFlop_XXXXXXXX.

CPU_JKFlipFlop_XXXXXXXX

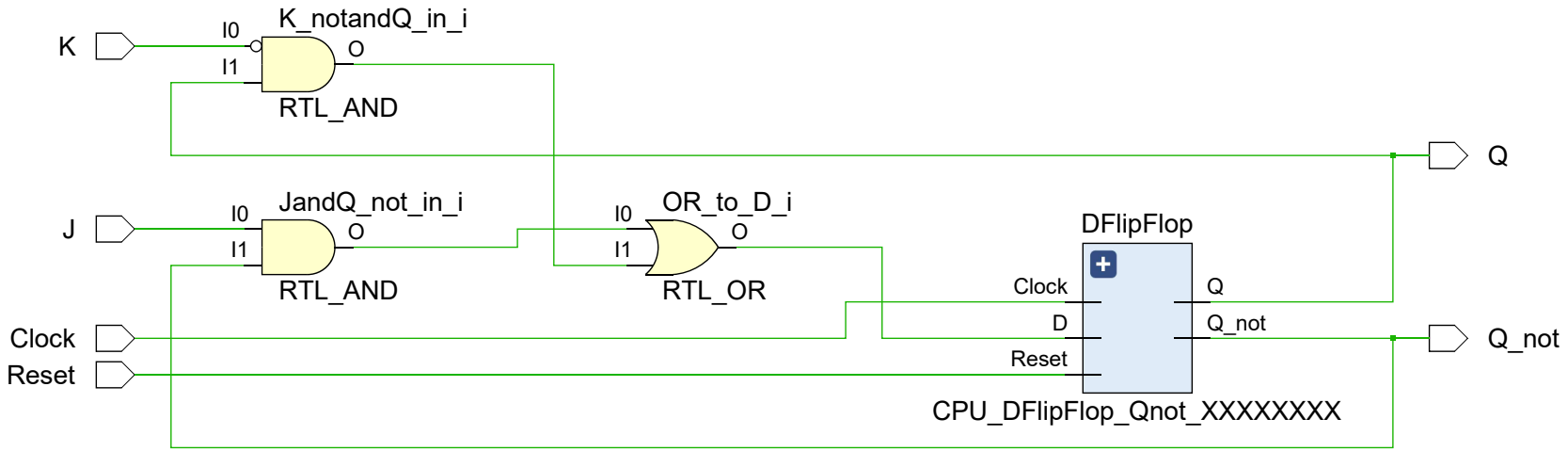


Figure 3: The CPU_JKFlipFlop_XXXXXXXX is required for the implementation of the CPU_CAR_XXXXXXXX.

CPU_CAR_XXXXXXXX

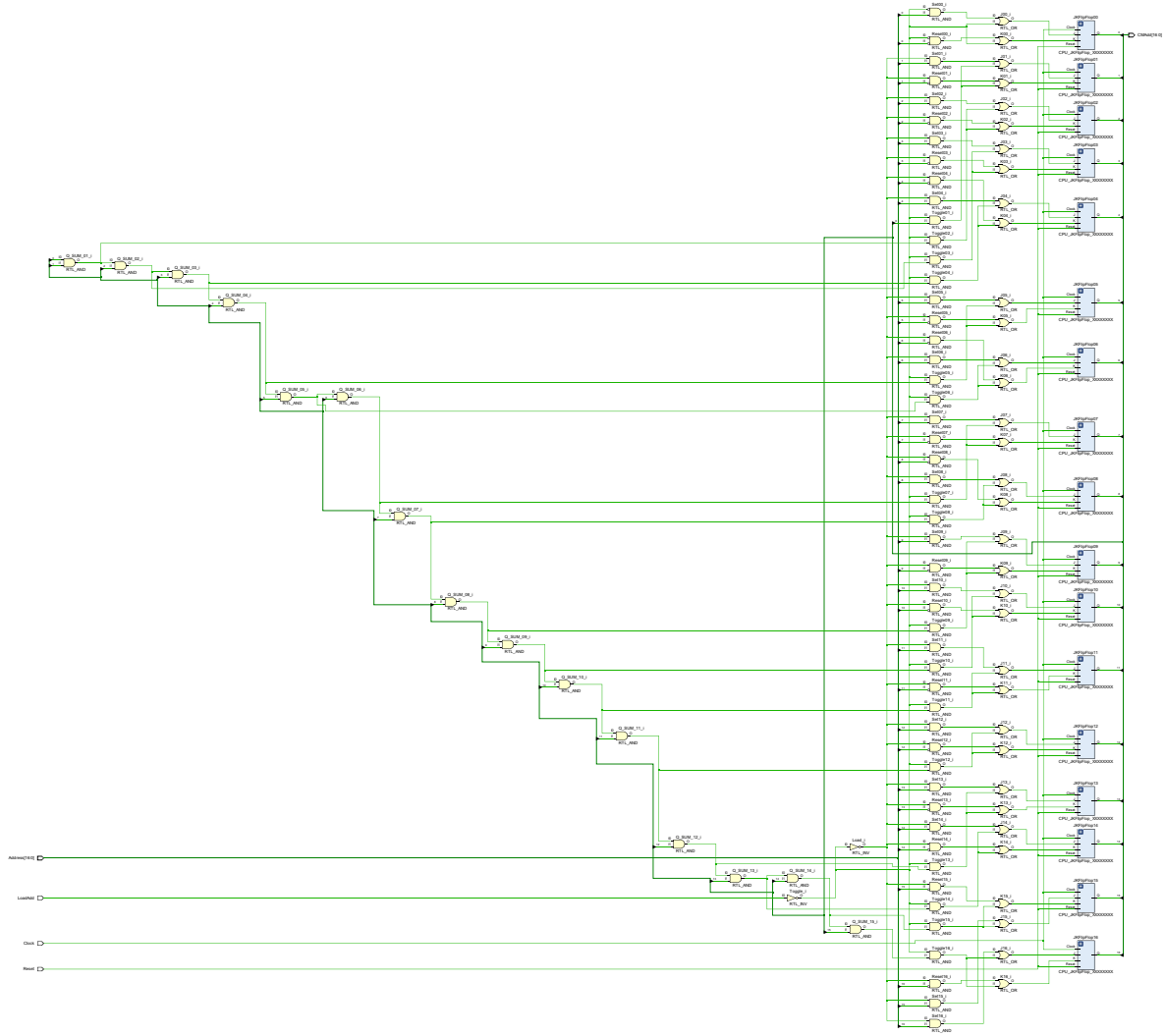


Figure 4: 17-Bit Binary Counter with Parallel Load

CPU_CAR_XXXXXXXX Timing Diagram

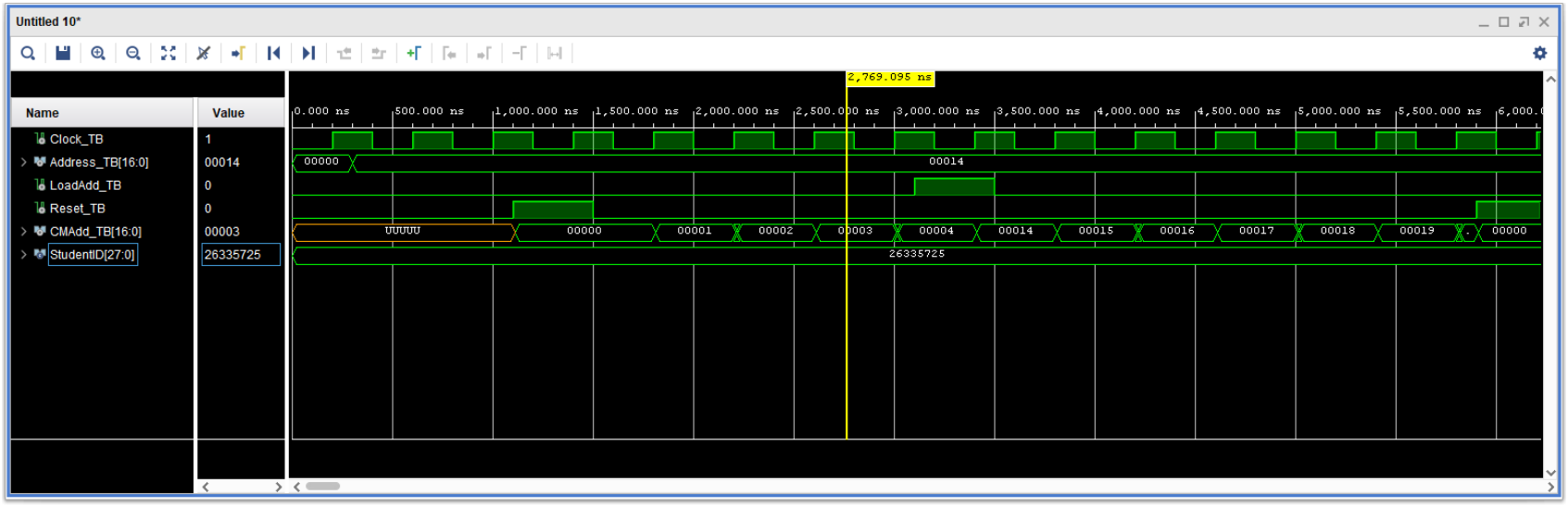


Figure 5: 17-Bit Binary Counter with Parallel Load operation