CSU22022 Computer Architecture I

Eighteenth Lecture - Hardwired Control

Michael Manzke

2023-2024

Trinity College Dublin

Shift-and-Add Multiplication ASM

- Note the concatenation notation
  - $C \leftarrow 0, C \| A \| Q \leftarrow srC \| A \| Q, P \leftarrow P - 1$
- From the ASM we can write out the RT description of the system in terms of:
  - System state
  - Input signals
- Table 2 on the following slides allows us to deduce the design of each register:

Control and Sequencing

- Two distinct aspects in control unit design:
  - Control of micro-operations
  - Sequencing
- We separate the two aspects by providing:
  - A state table
    - Defines signals in terms of states and inputs
  - A simplified ASM chart
    - Represents only state transitions

Shift-and-Add Multiplication ASM

- Again, from the ASM we can write out the RT description of the system in terms of:
  - System state
  - Input signals
- By gathering, the RTs loading each register we may easily deduce the design of each register. See Table 2 on the next slide

Control Signals for Binary Multiplier

Storage	Microoperation	Control Signal	Control Expression
Register A	$A \leftarrow 0$	Init	$IDLE \cdot G$
	$A \leftarrow A + B$	Add	$MUL0 \cdot Q_0$
	$C \| A \| Q \leftarrow srC \| A \| Q$	Shift	$MUL1$
Register B	$B \leftarrow IN$	LoadB	LOADB
Flip-Flop C	$C \leftarrow 0$	Init+Shift	$IDLE \cdot G + MUL1$
	$C \leftarrow C_{out}$	Add	$MUL0 \cdot Q_0$
Register Q	$Q \leftarrow IN$	LoadQ	LOADQ
	$C \| A \| Q \leftarrow srC \| A \| Q$	Shift	$MUL1$
Counter P	$P \leftarrow n - 1$	Init	$IDLE \cdot G$
	$P \leftarrow P - 1$	Shift	$MUL1$

Table 1: Control signals for all register transfers.

Sequencing Part of ASM Chart

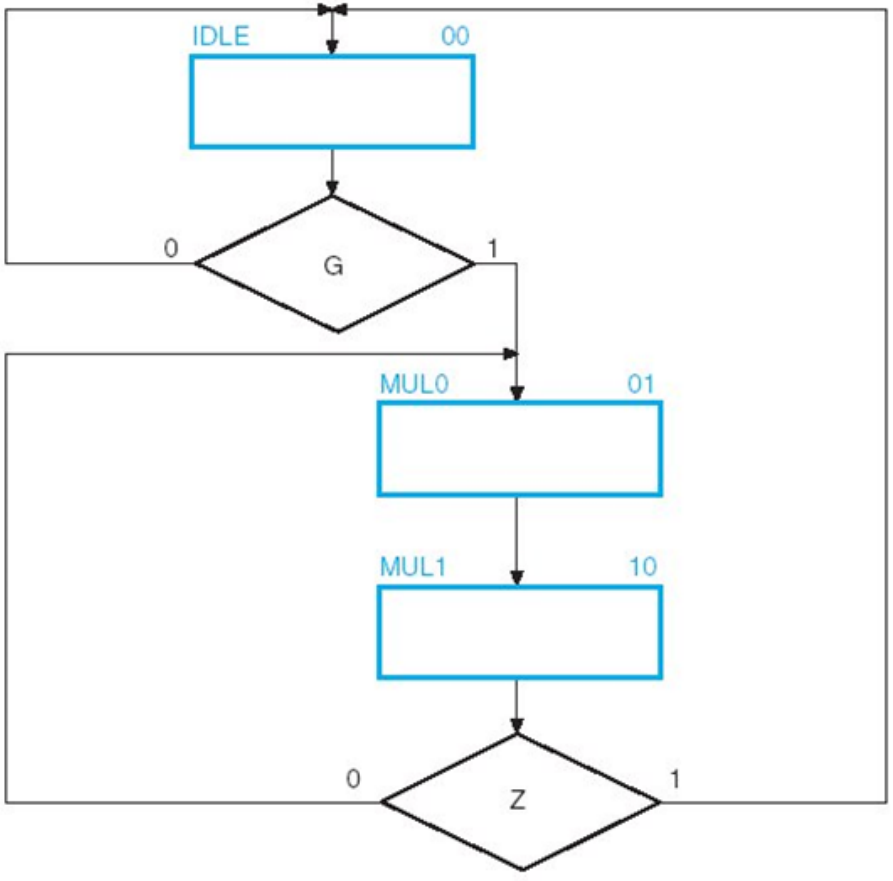


Figure 1: States IDLE, MUL0, and MUI1 are encoded as "00", "01", and "10" respectively. Therefore, 2 Flip-Flops can store the current state of the ASM.

Sequence Register and Decoder

- This method uses:
  - Sequence Register:
    - That holds control states (current state)
    - Register with n flop-flops has 2^n states
  - Decoder:
    - Provides output signal for each state
    - A n-to-2^n decoder has 2^n outputs

State Table

Present state			Inputs		Next state		Decoder Output		
Name	M_1	M_0	G	Z	M_1	M_0	IDEL	MUL0	MUL1
IDEL	0	0	0	x	0	0	1	0	0
	0	0	1	x	0	1	1	0	0
MUL0	0	1	x	x	1	0	0	1	0
MUL1	1	0	x	0	0	1	0	0	1
	1	0	x	1	0	0	0	0	1
-	1	1	x	x	x	x	x	x	x

Table 2: Derived from the Sequencing Part of ASM Chart

$$D_{M_0} = IDEL \cdot G + MUL1 \cdot \overline{Z}$$

$$D_{M_1} = MUL0$$

Control Unit for Binary Multiplier

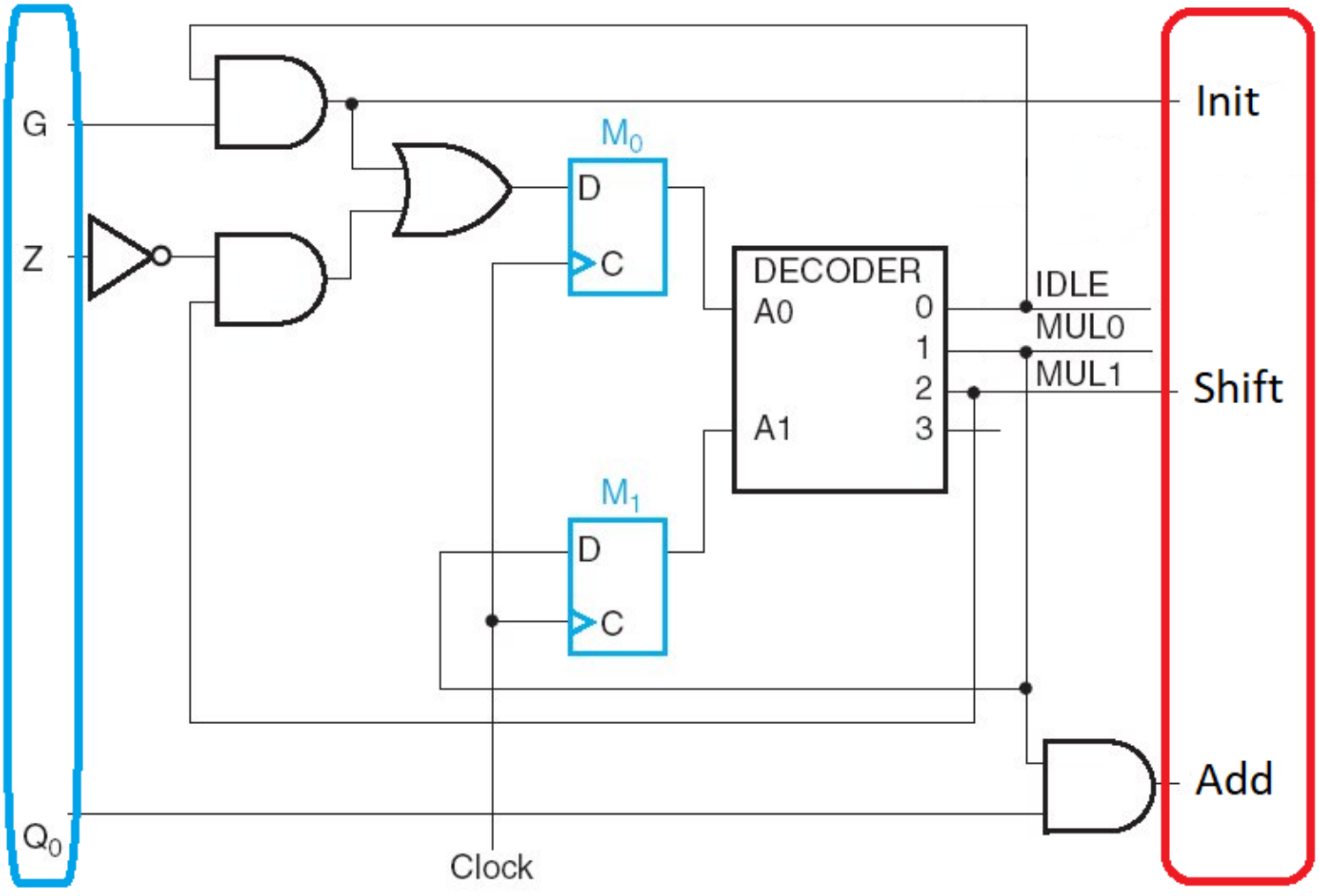


Figure 2: The circuit implements the sequencing and the control signals.

IDLE $M_1 = 0$, $M_0 = 0$, and $G = 0$

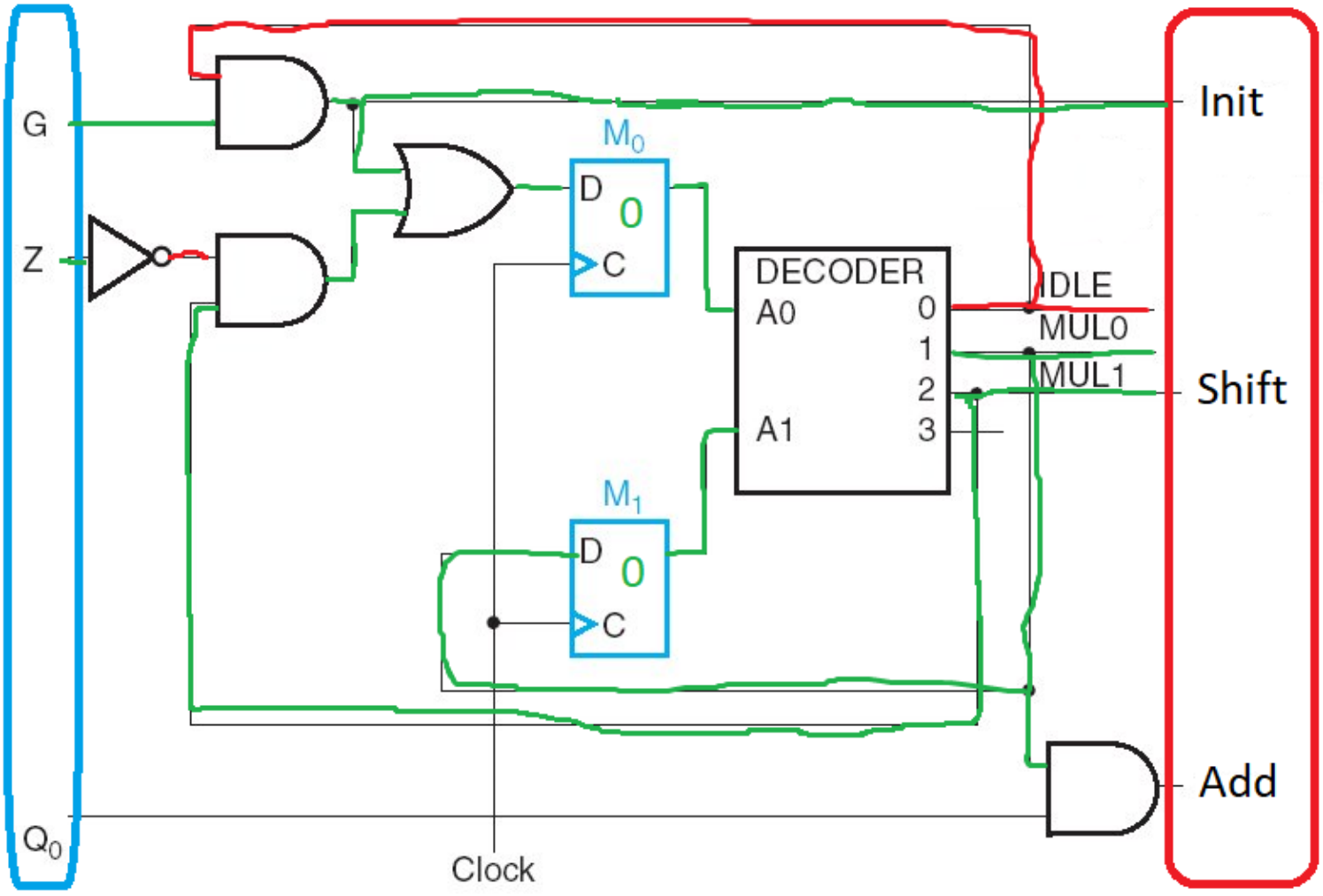


Figure 3: $D_{M_0} = IDEL \cdot G + MUL1 \cdot \overline{Z}, D_{M_1} = MUL0$

IDLE $M_1 = 0$, $M_0 = 0$, and $G = 1$

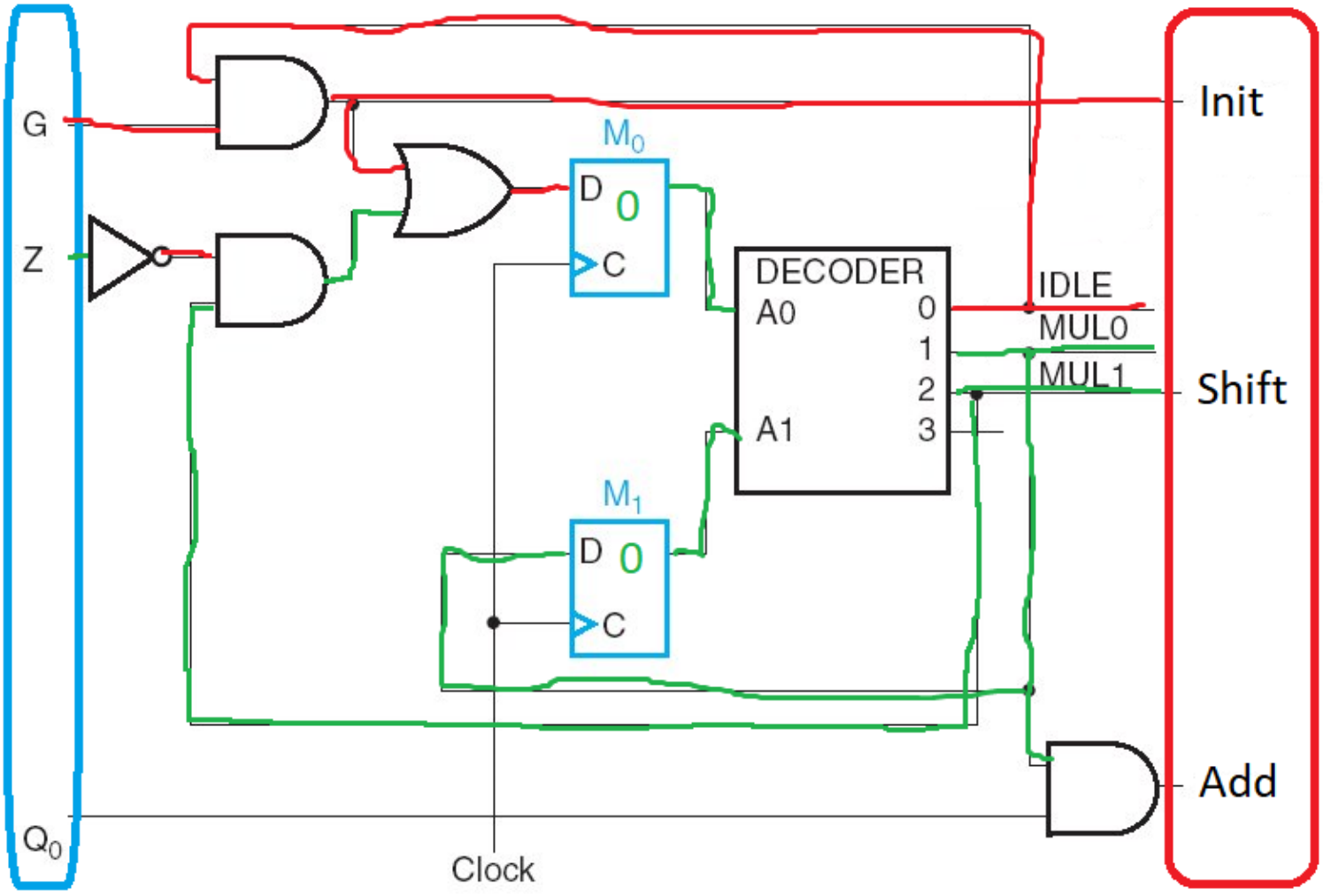


Figure 4: $D_{M_0} = IDEL \cdot G + MUL1 \cdot \overline{Z}, D_{M_1} = MUL0$

MUL0 $M_1 = 0,\ M_0 = 1$

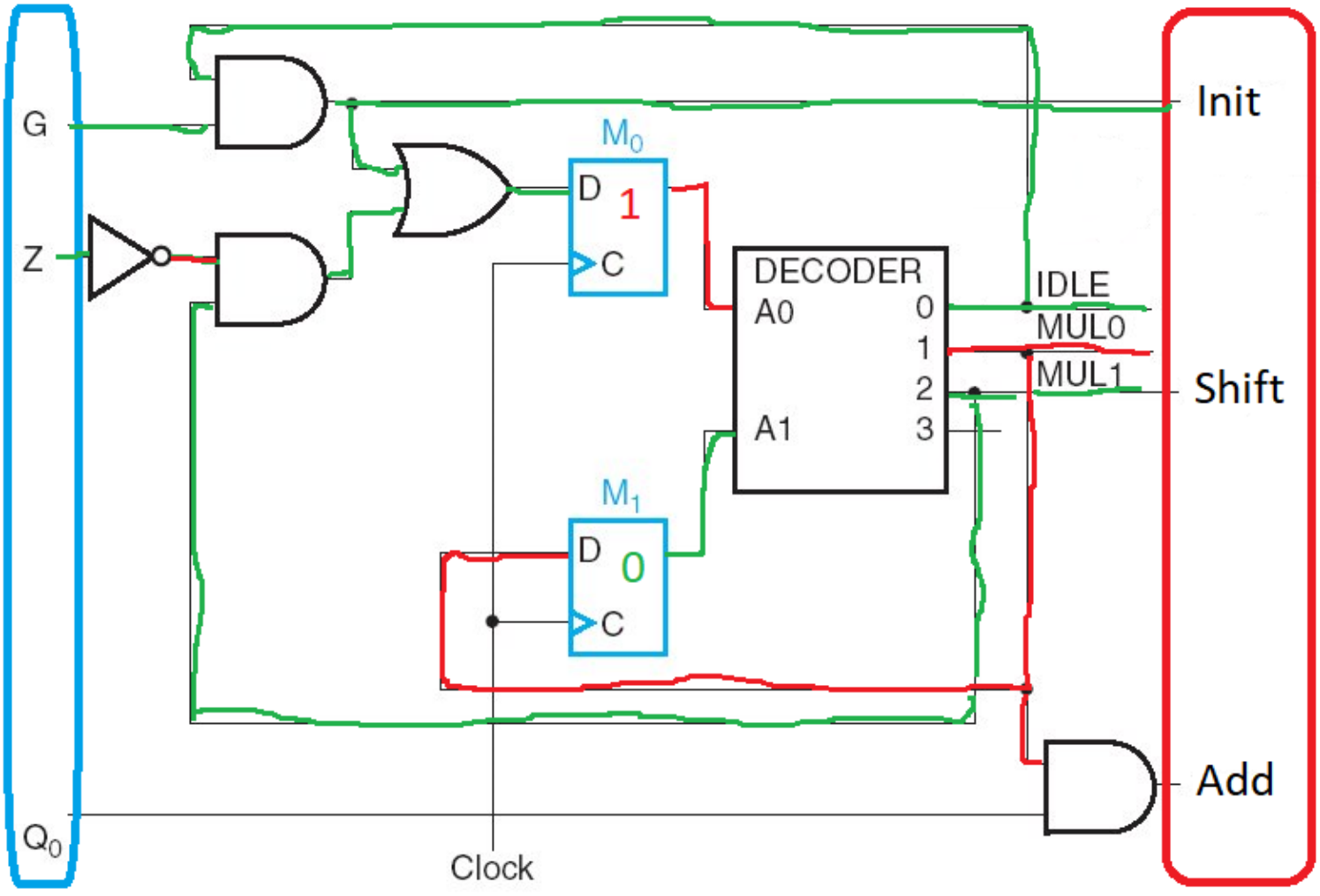


Figure 5: $D_{M_0} = IDEL \cdot G + MUL1 \cdot \overline{Z}, D_{M_1} = MUL0$

MUL1 $M_1 = 1$, $M_0 = 0$, and $Z = 0$

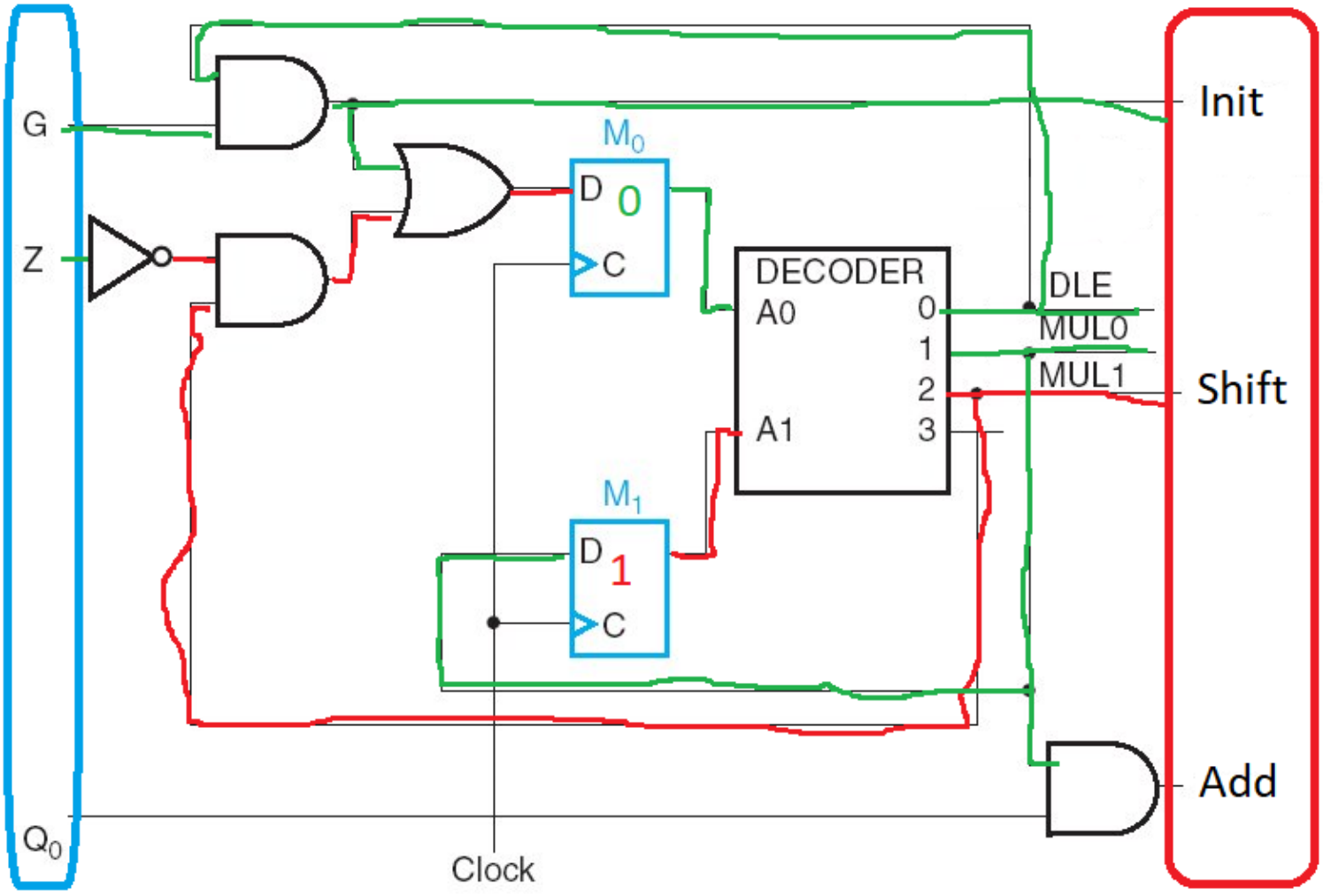


Figure 6: $D_{M_0} = IDEL \cdot G + MUL1 \cdot \overline{Z}, D_{M_1} = MUL0$

MUL1 $M_1 = 1$, $M_0 = 0$, and $Z = 1$

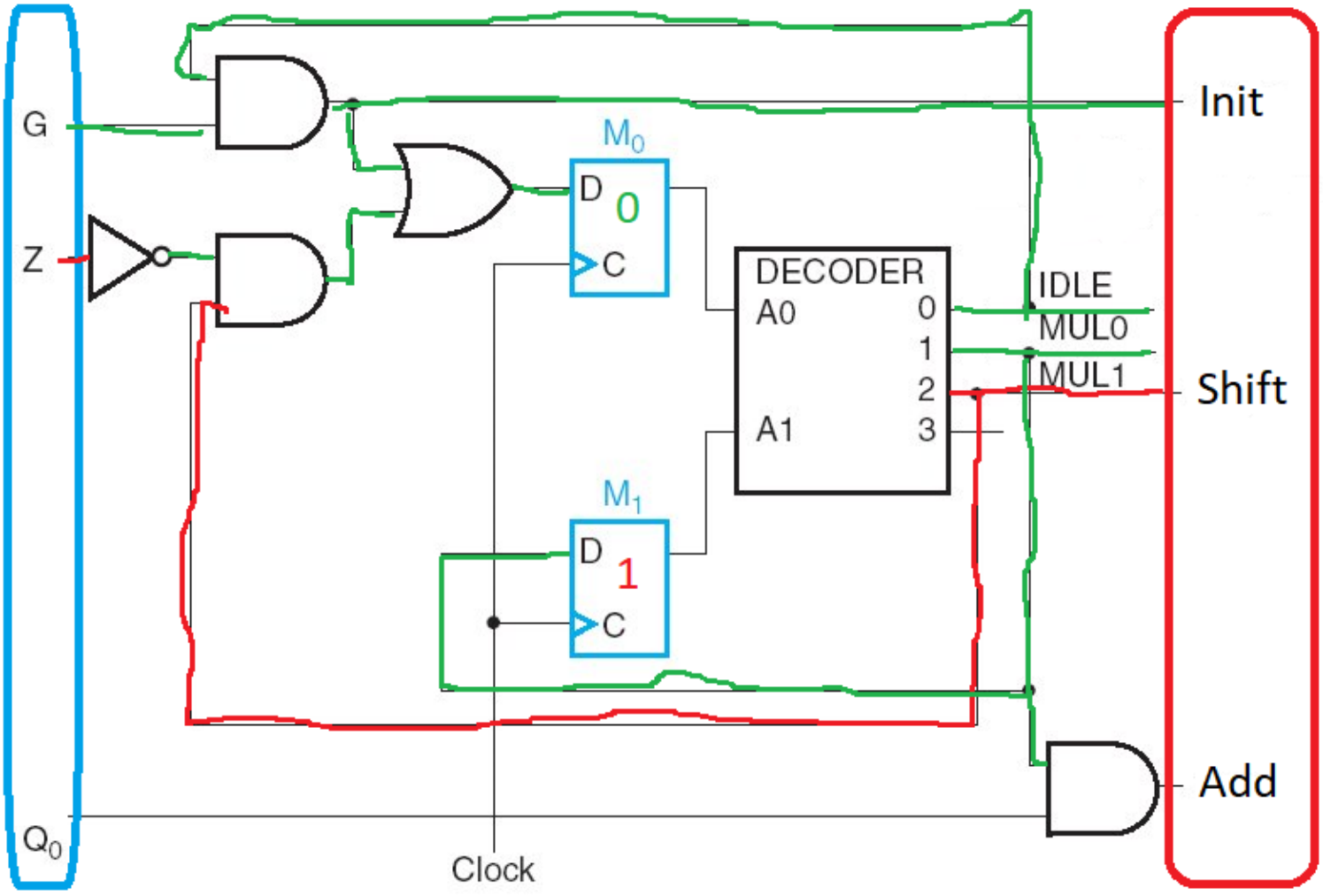
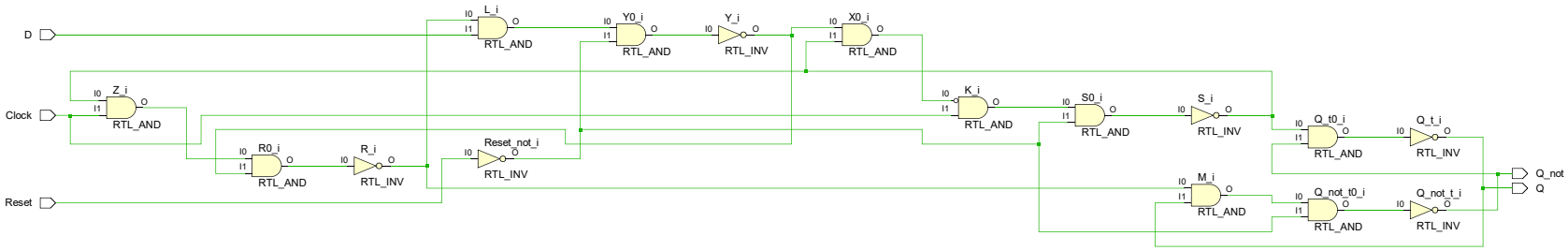
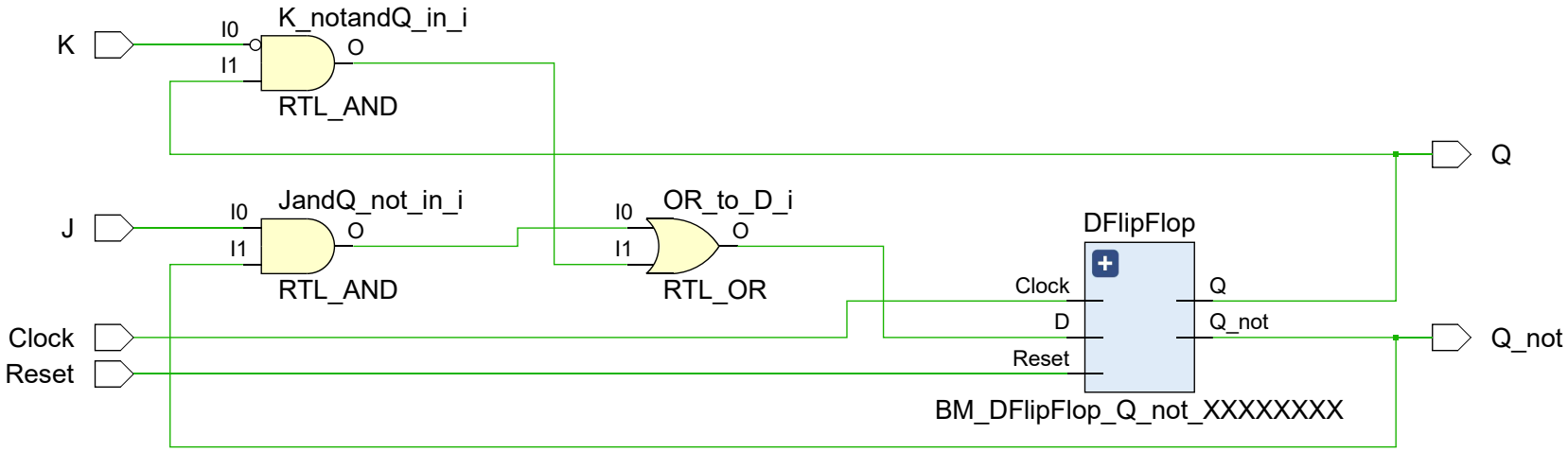


Figure 7: $D_{M_0} = IDEL \cdot G + MUL1 \cdot \overline{Z}, D_{M_1} = MUL0$

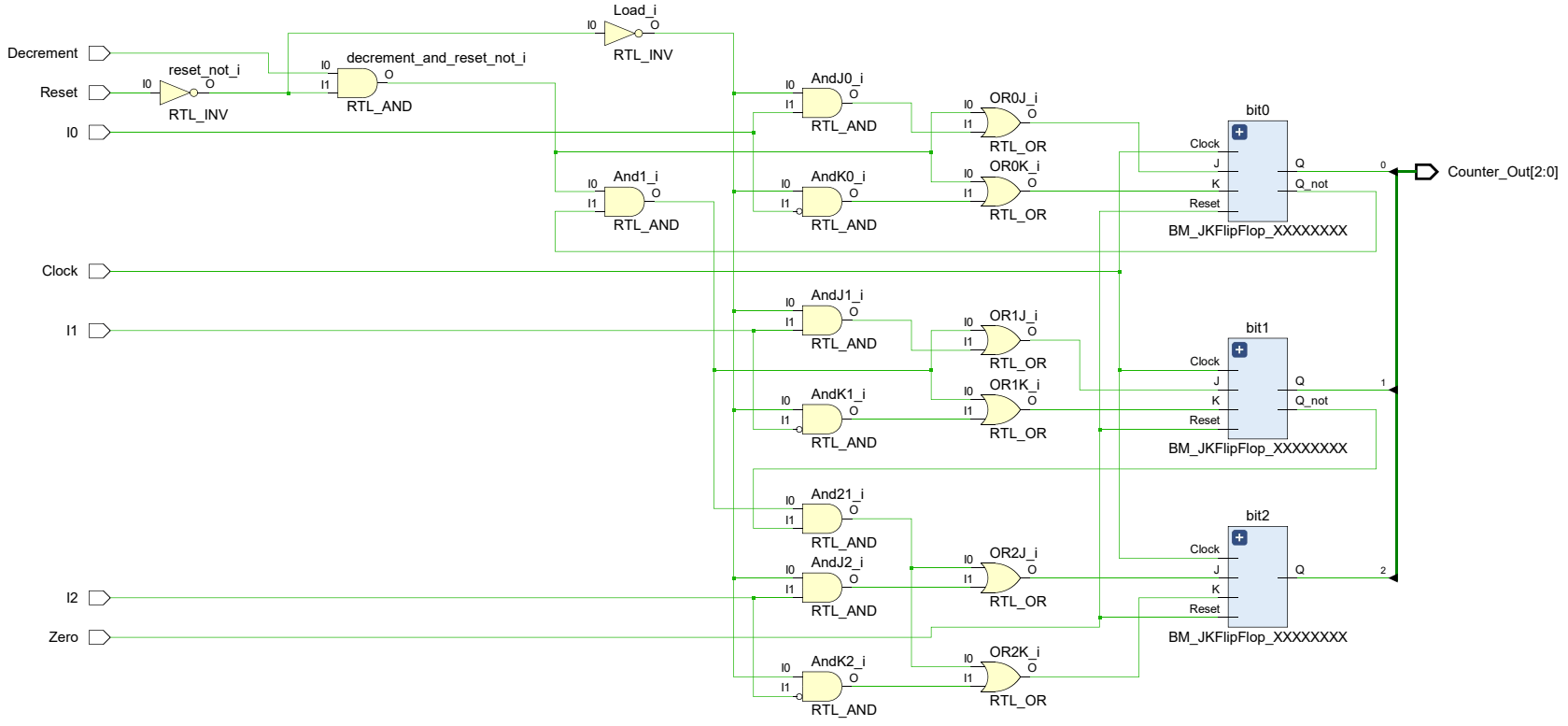
BM_DFlipFlop_Q_not_XXXXXXXX_Schematic



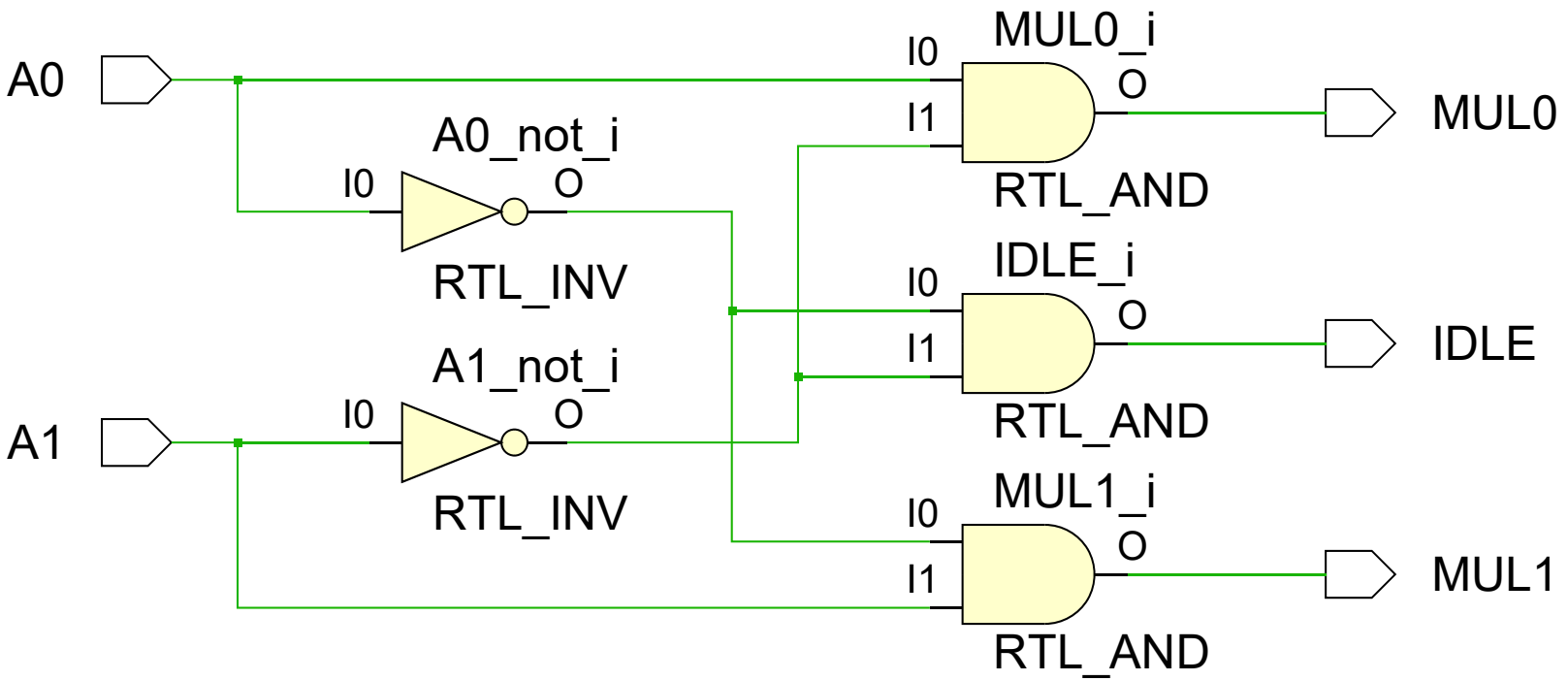
BM_JKFlipFlop_XXXXXXXX_Schematic



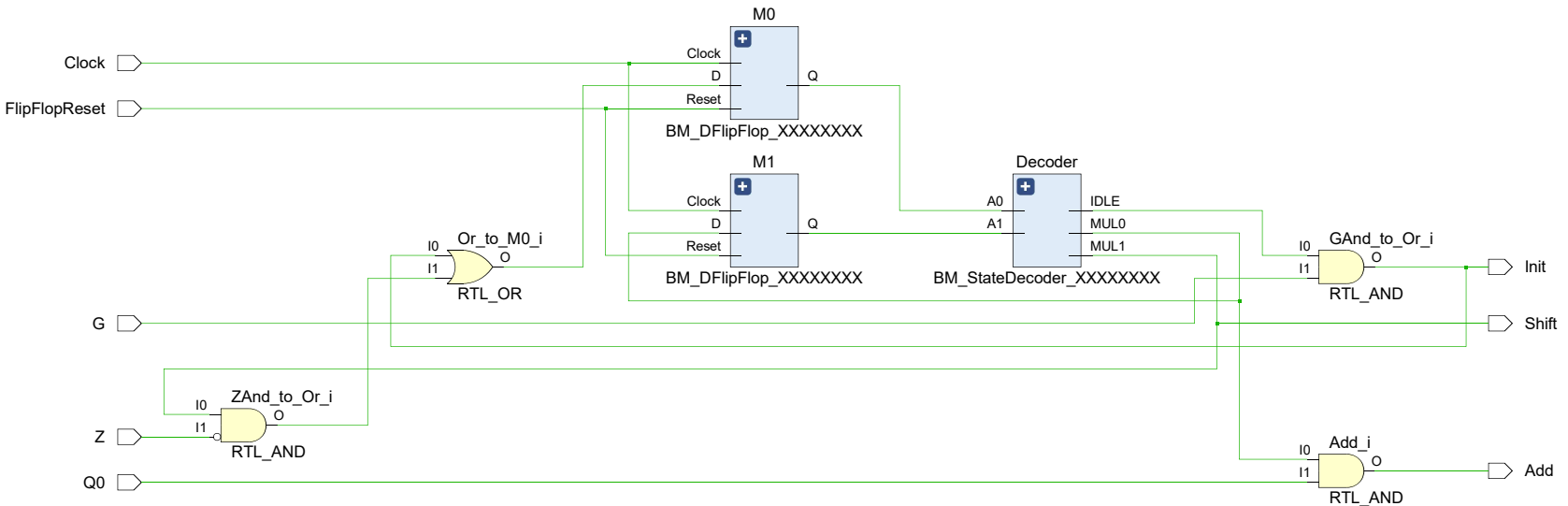
BM_Counter_XXXXXXXX_Schematic



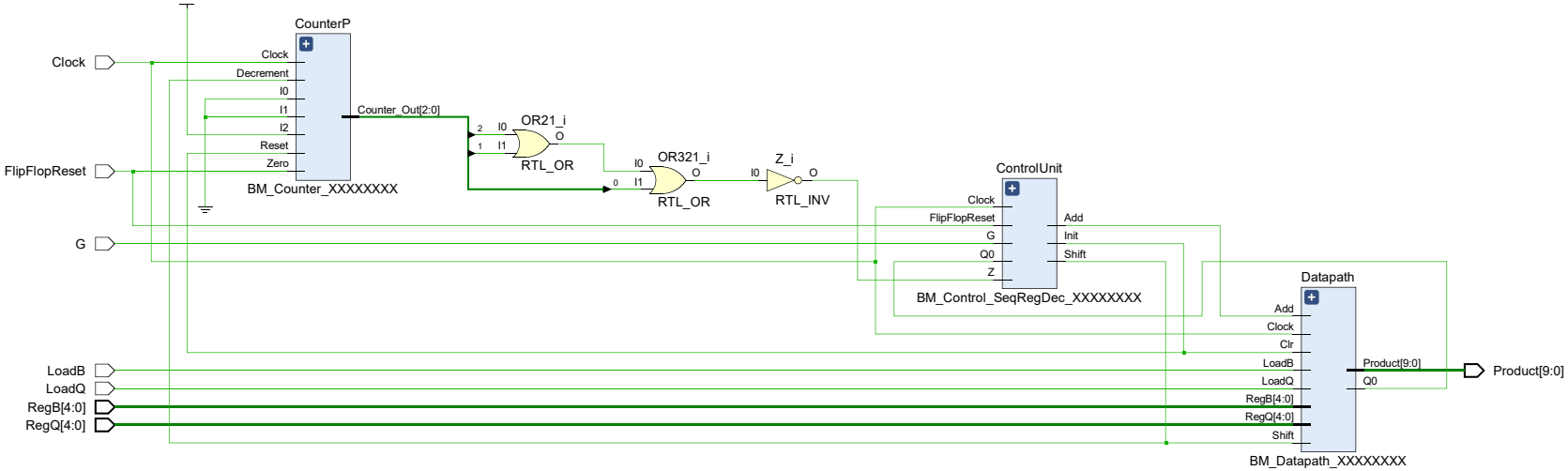
BM_StateDecoder_XXXXXXXX_Schematic



BM_Control_SeqRegDec_XXXXXXXX_Schematic



BM_SeqRegDec_Multipier_XXXXXXXX_Schematic



BM_SeqRegDec_Multipier_XXXXXXXX_TD01