

CSU22022 Computer Architecture I

Twenty-second Lecture - Control Memory

Michael Manzke

2023-2024

Trinity College Dublin

CPU_ControlMemory_XXXXXXX [One of Six]

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.NUMERIC_STD.ALL;
4
5 entity CPU_ControlMemory_XXXXXXX is
6     Port ( Address : in STD_LOGIC_VECTOR (16 downto 0);
7           NA : out STD_LOGIC_VECTOR (16 downto 0); — 34–50
8           MS : out STD_LOGIC_VECTOR (2 downto 0); — 31–33
9           MC : out STD_LOGIC; — 30
10          IL : out STD_LOGIC; — 29
11          PI : out STD_LOGIC; — 28
12          PL : out STD_LOGIC; — 27
13          TD : out STD_LOGIC_VECTOR (3 downto 0); — 23–26
14          TA : out STD_LOGIC_VECTOR (3 downto 0); — 19–22
15          TB : out STD_LOGIC_VECTOR (3 downto 0); — 15–18
16          MB : out STD_LOGIC; — 14
17          FS : out STD_LOGIC_VECTOR (4 downto 0); — 09–13
18          MD : out STD_LOGIC; — 08
19          RW : out STD_LOGIC; — 07
20          MM : out STD_LOGIC; — 06
21          MW : out STD_LOGIC; — 05
22          RV : out STD_LOGIC; — 04
23          RC : out STD_LOGIC; — 03
24          RN : out STD_LOGIC; — 02
25          RZ : out STD_LOGIC; — 01
26          FL : out STD_LOGIC); — 00
27 end CPU_ControlMemory_XXXXXXX;
```

Listing 1: CPU_ControlMemory_XXXXXXX Entity.

CPU_ControlMemory_XXXXXXX [Two of Six]

[illegible]Listing 2: Control Memory Addresses 00_{16} to $1F_{16}$

CPU_ControlMemory_XXXXXXX [Three of Six]

[illegible]Listing 3: Control Memory Addresses 20_{16} to $3F_{16}$

CPU_ControlMemory_XXXXXXX [Four of Six]

2	50	34/33	31/30	28	27/26	23/22	19/18	15	14/13	09	08	07	06	05	04	03	02	01	00	Control Memory	
3	Next Address	MS	[MC]	IL	PI	PL	TD	TA	TB	MB	FS	MD	RW	MM	MV	RV	RC	RN	RZ	FL	Address
4	"0000000001000000" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	40
5	"0000000001000001" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	41
6	"0000000001000010" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	42
7	"0000000001000011" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	43
8	"0000000001000100" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	44
9	"0000000001000101" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	45
10	"0000000001000110" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	46
11	"0000000001000111" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	47
12	"0000000001001000" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	48
13	"0000000001001001" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	49
14	"0000000001001010" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	4A
15	"0000000001001011" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	4B
16	"0000000001001100" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	4C
17	"0000000001001101" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	4D
18	"0000000001001110" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	4E
19	"0000000001001111" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	4F
20	50	34/33	31/30	29	28	27/26	23/22	19/18	15	14/13	09	08	07	06	05	04	03	02	01	00	Control Memory
21	Next Address	MS	[MC]	IL	PI	PL	TD	TA	TB	MB	FS	MD	RW	MM	MV	RV	RC	RN	RZ	FL	Address
22	"0000000001010000" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	50
23	"0000000001010001" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	51
24	"0000000001010010" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	52
25	"0000000001010011" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	53
26	"0000000001010100" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	54
27	"0000000001010101" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	55
28	"0000000001010110" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	56
29	"0000000001010111" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	57
30	"0000000001011000" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	58
31	"0000000001011001" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	59
32	"0000000001011010" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	5A
33	"0000000001011011" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	5B
34	"0000000001011100" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	5C
35	"0000000001011101" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	5D
36	"0000000001011110" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	5E
37	"0000000001011111" < "000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0000"	<	"0000"	<	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	5F

Listing 4: Control Memory Addresses 40_{16} to $5F_{16}$

CPU_ControlMemory_XXXXXXX [Five of Six]

2	50	34	33	31	30	29	28	27	26	23	22	19	18	15	14	13	09	08	07	06	05	04	03	02	01	00	Control Memory
3		Next Address	MS	[MC]	IL	PI	PL	TD	TA	TB	MB	FS	MD	RW	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD	MD	Address
4	"	00000000001100000	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-60
5	"	00000000001100001	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-61
6	"	00000000001100010	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-62
7	"	00000000001100011	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-63
8	"	00000000001100100	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-64
9	"	00000000001100101	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-65
10	"	00000000001100110	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-66
11	"	00000000001100111	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-67
12	"	00000000001101000	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-68
13	"	00000000001101001	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-69
14	"	00000000001101010	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-70
15	"	00000000001101011	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-71
16	"	00000000001101100	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-72
17	"	00000000001101101	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-73
18	"	00000000001101110	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-74
19	"	00000000001101111	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-75
20	"	00000000001110000	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-76
21	"	00000000001110001	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-77
22	"	00000000001110010	'000	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	'0	-78
23	"	00000000001110011	'000	'0	'0	'0	'																				

Listing 5: Control Memory Addresses 60_{16} to $7F_{16}$

CPU_ControlMemory_XXXXXXX [Six of Six]

5	4	4	4	4	4	4	4	4	4	4	3	3	3	3	3	3	3	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0				
Next Address										MS		M C L	I L	P L	TD		TA		TB		M B	FS		M D	R W	M M	R V	R C	R N	F Z	L													

```

1 signal content_at_address : STDLOGIC_VECTOR (50 downto 0);
2
3 begin
4
5 content_at_address <= ROM(to_integer(unsigned(Address(6 downto 0)))) after 2ns;
6
7     NA <= content_at_address(50 downto 34);    — 34–50
8     MS <= content_at_address(33 downto 31);    — 31–33
9     MC <= content_at_address(30);              — 30
10    IL <= content_at_address(29);               — 29
11    PI <= content_at_address(28);               — 28
12    PL <= content_at_address(27);               — 27
13    TD <= content_at_address(26 downto 23);     — 23–26
14    TA <= content_at_address(22 downto 19);     — 19–22
15    TB <= content_at_address(18 downto 15);     — 15–18
16    MB <= content_at_address(14);               — 14
17    FS <= content_at_address(13 downto 9);      — 09–13
18    MD <= content_at_address(8);               — 08
19    RW <= content_at_address(7);                — 07
20    MM <= content_at_address(6);                — 06
21    MV <= content_at_address(5);                — 05
22    RV <= content_at_address(4);                — 04
23    RC <= content_at_address(3);                — 03
24    RN <= content_at_address(2);                — 02
25    RZ <= content_at_address(1);                — 01
26    FL <= content_at_address(0);                — 00
27
28 end Behavioral;
```

Listing 6: Entity's output signals and vectors.

Processor's ASM Snippet

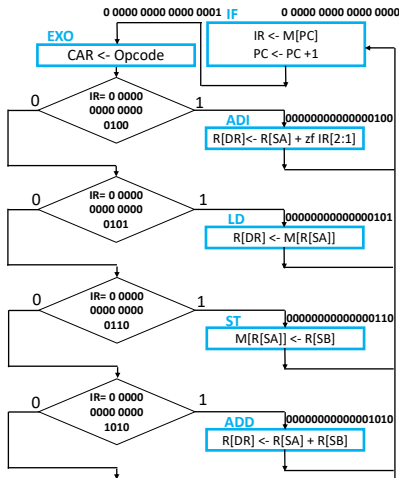


Figure 1: This ASM snippet shows the IF, EXO, ADI, LD, ST, and ADD micro-operations.

Processor's Control Memory Snippet

2	50	34	33	31	30	29	28	27	26	23	22	19	18	17	14	13	09	08	07	06	05	04	03	02	01	00	Control Memory		
3	Next	Address	MS	MC	IL	PI	PL	PL	TD	TA	TB	TB	MB	PS	MD	RW	MM	MV	RV	RV	RC	RN	RZ	FL	FL	Address			
4	"	0000000000000000	&	'000'	&	'0	'0	'0	'0	'0	'0	'0	'0	'0000	&	'0000	&	'0000	&	'0	'0	'0000	&	'0	'0	'0	'0	'0	00 IF
5	"	0000000000000000	&	'000'	&	'0	'0	'0	'0	'0	'0	'0	'0	'0000	&	'0000	&	'0000	&	'0	'0	'0000	&	'0	'0	'0	'0	'0	01 EXO
6	"	0000000000000001	&	'000'	&	'0	'0	'0	'0	'0	'0	'0	'0	'0000	&	'0000	&	'0000	&	'0	'0	'0000	&	'0	'0	'0	'0	'0	02
7	"	0000000000000011	&	'000'	&	'0	'0	'0	'0	'0	'0	'0	'0	'0000	&	'0000	&	'0000	&	'0	'0	'0000	&	'0	'0	'0	'0	'0	03
8	"	0000000000000100	&	'000'	&	'0	'0	'0	'0	'0	'0	'0	'0	'0000	&	'0000	&	'0000	&	'0	'0	'0000	&	'0	'0	'0	'0	'0	04 ADI
9	"	0000000000000101	&	'000'	&	'0	'0	'0	'0	'0	'0	'0	'0	'0000	&	'0000	&	'0000	&	'0	'0	'0000	&	'0	'0	'0	'0	'0	05 LD
10	"	0000000000000110	&	'000'	&	'0	'0	'0	'0	'0	'0	'0	'0	'0000	&	'0000	&	'0000	&	'0	'0	'0000	&	'0	'0	'0	'0	'0	06 ST
11	"	0000000000000111	&	'000'	&	'0	'0	'0	'0	'0	'0	'0	'0	'0000	&	'0000	&	'0000	&	'0	'0	'0000	&	'0	'0	'0	'0	'0	07
12	"	0000000000001000	&	'000'	&	'0	'0	'0	'0	'0	'0	'0	'0	'0000	&	'0000	&	'0000	&	'0	'0	'0000	&	'0	'0	'0	'0	'0	08
13	"	0000000000001001	&	'000'	&	'0	'0	'0	'0	'0	'0	'0	'0	'0000	&	'0000	&	'0000	&	'0	'0	'0000	&	'0	'0	'0	'0	'0	09
14	"	0000000000001010	&	'000'	&	'0	'0	'0	'0	'0	'0	'0	'0	'0000	&	'0000	&	'0000	&	'0	'0	'0000	&	'0	'0	'0	'0	'0	0A ADD

Listing 7: This ASM snippet shows the IF EXO ADI LD ST and ADD mico operations.

Figure 2: This control memory snippet shows the IF, EXO, ADI, LD, ST, and ADD micro-operations.