ASMEDIA TECHNOLOGY INC

ASM2464PDX Data Sheet

USB4/Thunderbolt to PCIe Gen4 x4 Controller for Multi-PCIe Devices

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Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	Feburary 16, 2023	Initial Release
0.2	**June 8, 2023**	**Updated Introduction** **Updated Figure 3.** **Updated Pin Descriptions** **Added PCIe Port Mapping Table** **Updated Chip Temperature (TJ, TT) Calculation** **Updated voltage range of VCCL in Recommended Operating Conditions** **Updated power supply voltage in General Features** **Kept Power Consumption as TBD.**

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List of Acronyms

No.	Acronyms	Description
1	BMC	Bi-phase Mark Coding
2	BOT	Bulk Only Transport
3	CC	Configuration Channel
4	FCCSP	Flip Chip-Chip Scale Package
5	GPIO	General Purpose Input Output
6	I2C	Inter-Integrated Circuit
7	NVMe	Non-Volatile Memory Express
8	P2P	PCIe Peer-to-Peer
9	PCIe	Peripheral Component Interconnect Express
10	PHY	Physical Layer
11	RoHS	Reduction of Hazardous Substances
12	RAM	Random Access Memory
13	ROM	Read-Only Memory
14	SCSI	Small Computer System Interface
15	SPI	Serial Peripheral Interface
16	SSC	Spread Spectrum Clock
17	SSD	Solid State Drive
18	TBT	Thunderbolt
19	TMU	Time Measurement Unit
20	UART	Universal Asynchronous Receiver Transmitter
21	UAS	USB Attached SCSI
22	UFP	Upstream Facing Port
23	UNMAP	SCSI Command
24	USB	Universal Serial Bus

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1. Introduction

ASM2464PDX, a new generation of USB4/Thunderbolt to PCIe/NVMe Accessory controller which is built on ASMedia in-house designed PHYs. USB4/Thunderbolt technology enables PCIe and USB protocols to be encapsulated into the USB4/Thunderbolt fabric and tunneled across USB4/Thunderbolt domains. ASM2464PDX can be implemented with various types of general PCIe devices in addition to NVMe SSD.

The ASM2464PDX USB connection is able to provide data rate at a speed of USB4/Thunderbolt 20Gbps x2 and is also compatible with existing legacy USB 3.2 interfaces, as well as Thunderbolt 3. In addition, the downstream port link of ASM2464PDX is also upgraded to PCIe Gen4 x4. The downstream PCIe lanes are configurable to support up to four PCIe devices.

ASM2464PDX integrates USB4/Thunderbolt Gen3 x2, and PCI Express Gen4 with 1.9V and 1.05V voltage power source. A USB Type-C CC logic circuit and BMC PHY are integrated for supporting cable orientation, flipping, and PD Sink mode with the capability to communicate via PD protocols including USB4/TBT3 Discovery and Entry with host. A discrete PD controller can be supported through I2C to achieve advanced USB PD functions. ASM2464PDX is driven by local 25MHz crystal in a compact RoHS Green compact package with the support of multiple GPIO pins for customization.

The ASM2464PDX is also designed to be compliant with the Thunderbolt 4 specification and ASMedia is targeting the Thunderbolt certification by the end of Q2 2023. Once the certification has been granted, end-product devices utilizing the ASM2464PDX would also be eligible for Thunderbolt certification testing.

2. Features

General Features

- ◇ USB4/Thunderbolt to PCI Express NVMe SSD Bridge.
- ◇ Integrated two USB 20Gbps PHYs.
- ◇ Integrated UFP CC Logic for USB Type-C cable orientation and detection.
- ◇ Integrated BMC PHY for PD fixed 5V UFP/Sink mode.
- ◇ 3.3V/1.9V/1.05V Power Supply.
- ◇ Support SPI interface with External ROM for Customized RAM Code.
- ◇ Support I2C and GPIOs and UART Interface.
- ◇ Local 25MHz Crystal.

Universal Serial Bus Features

- ◇ Support up to USB4/Thunderbolt Gen3 x2 with USB 3.2 and USB 2.0 (backward compatibility).
- ◇ Support BOT and UAS Protocol.
- ◇ Support USB Link Power Management.
- ◇ Support USB Hot Plug.
- ◇ Support Spread Spectrum Clock Control.
- ◇ Support UNMAP Command Set.
- ◇ Support SCSI Vendor Specific Command Set.
- ◇ Compliant with Universal Serial Bus 4 (USB4™) Specification Rev. 1.0 (including Interoperability with Thunderbolt™ 3 (TBT3) Systems)
- ◇ Compliant with Universal Serial Bus Type-C Cable and Connector Specification Revision 2.1
- ◇ Compliant with Universal Serial Bus Power Delivery Specification Revision 3.1 Version 1.3

PCI Express Features

- ◇ Support up to PCI Express Gen4 x4.
- ◇ Configurable PCIe lanes (1 x4, 2 x2, 4 x1, and 1 x2+2 x1), supporting up to 4 PCIe devices
- ◇ Support PCI Express NVMe SSD.
- ◇ Support Spread Spectrum Clock Control.
- ◇ 100MHz Differential Reference Clock Output.
- ◇ Support Various Types of PCI Express Socket including M.2, U.2, and CFexpress.
- ◇ Support PCI Express Link Power Management.
- ◇ Compliant with PCI Express Base Specification Rev. 4.0
- ◇ Compliant with PCIe M.2 Specification Rev. 1.1

NVM Express Features

- ◇ Support NVMe Power Management.
- ◇ Support NVMe: SCSI Translation Reference Rev. 1.5
- ◇ Support NVMe Error Reporting & Recovery.
- ◇ S.M.A.R.T Drive Monitoring.
- ◇ Compliant with NVM Express Base Specification Rev. 1.4c

2.1 Package Type

- ◇ Green Package 10x10 mm^2 FCCSP (Pb-free).
- ◇ RoHS Compliance.

3. Block Diagram

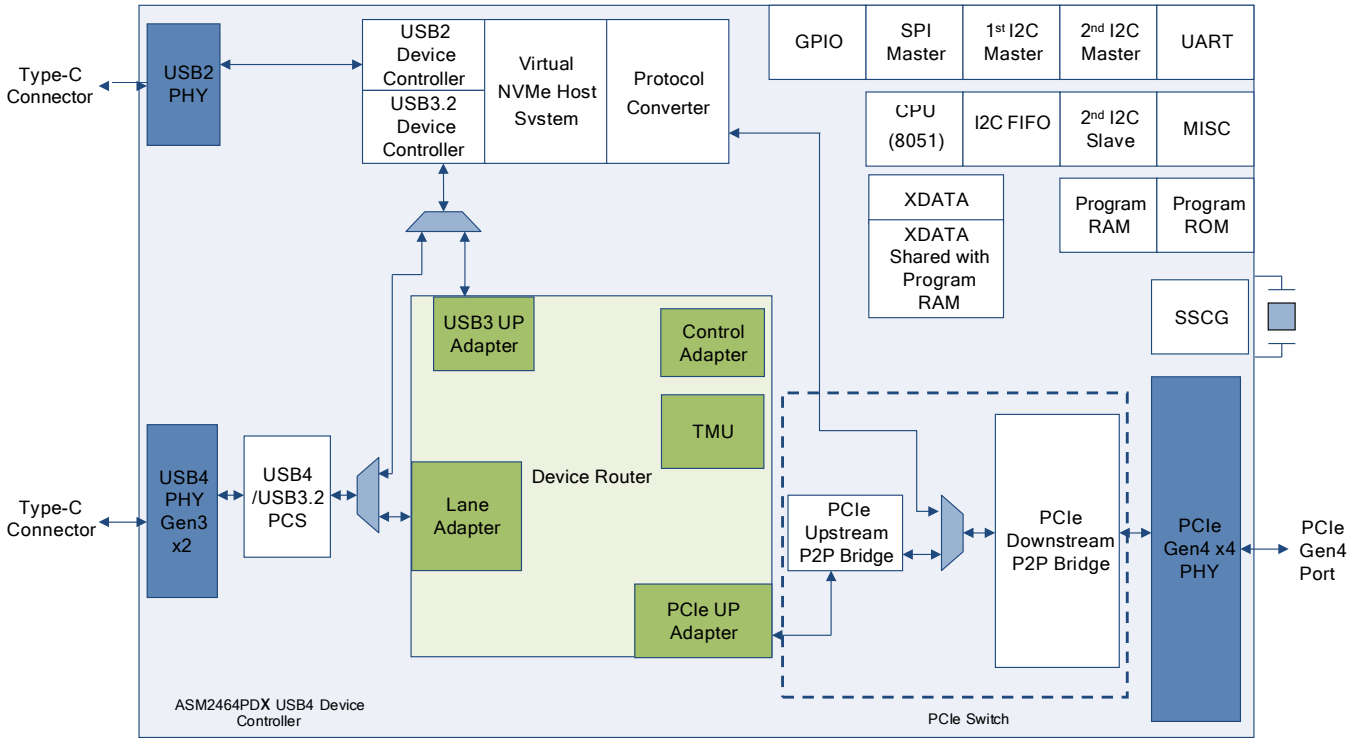


Figure 1 ASM2464PDX Block Diagram

4. Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	GPIO3	SPI_CS#	SPI_DO	SPI_DI	SPI_CLK	GPIO15	GPIO16	GPIO17	GPIO18	GPIO19	GPIO20	GPIO21	GPIO22	GPIO23	GPIO24	GPIO25	GPIO26	GPIO27	GPIO8	GPIO14	UART_RX	A
B	GPIO2	NC/B2	NC/B3	NC/B4	NC/B5	NC/B6	NC/B7	NC/B8	NC/B9	NC/B10	NC/B11	NC/B12	NC/B13	NC/B14	NC/B15	NC/B16	NC/B17	NC/B18	NC/B19	NC/B20	UART_TX	B
C	GPIO1	NC/C2																		NC/C20	HDDPC	C
D	GPIO0	NC/D2		GND	GND	VCCH		VCCH	VCCH		GND		VCCH	VDD		VDD	GND	GND		NC/D20	PERST3#	D
E	I2C_CLK_P	NC/E2		GND	GND	VCCH		VCCH	VCCH		VDD		VCCH	VDD		VDD	GND	GND		NC/E20	PERST2#	E
F	I2C_DATA_P	NC/F2		GND	GND	VCCH		GND	VDD		VDD		VCCH	VDD		VDD	GND	GND		**NC/F20**	PERST1#	F
G	VBUS	NC/G2																		**NC/G20**	PERST0#	G
H	RST#	NC/H2		GND	VCCA33	VCCH		GND	VDD		VDD		VDD	VDD		VDD	GND	GND		**NC/H20**	TEST_EN	H
J	SBU2	NC/J2		GND	GND	GND		VDD	VDD		GND		VDD	VDD		VDD	VDD	VDD		VDD	VDD	J
K	SBU1	GND																		VDD	VDD	K
L	GNDA	GNDA		GNDA	GNDA	VCCL		VDD	GND		VDD		GND	VDD		VCCL	VCCL	VCCL		VCCL	VCCL	L
M	UDP	UDM																		GNDA	GNDA	M
N	GNDA	GNDA		GNDA	GNDA	VCCL		VDD	GND		GND		GND	VDD		VCCL	GNDA	GNDA		PRXN0	PRXP0	N
P	URXP0	URXN0		GNDA	GNDA	VCCL		VDD	GND		GND		VDD	VDD		VCCL	GNDA	GNDA		GNDA	GNDA	P
R	GNDA	GNDA																		PTXP0	PTXN0	R
T	UTXP0	UTXN0		GNDA	GNDA	VCCL		VDD	VDD		VDD		VDD	VDD		VCCL	GNDA	GNDA		GNDA	GNDA	T
U	GNDA	GNDA		GNDA	GNDA	VCCL		VDD	VDD		VCCL		VCCL	VCCL		VCCL	GNDA	GNDA		PTXP1	PTXN1	U
V	UTXN1	UTXP1		GNDA	GNDA	GNDA		GNDA	GNDA		GNDA		GNDA	GNDA		GNDA	GNDA	GNDA		GNDA	GNDA	V
W	GNDA	GNDA																		PRXN1	PRXP1	W
Y	URXN1	URXP1	GNDA	XO	GNDA	CC2	REFCLKN3	REFCLKN0	GNDA	REFCLKN2	REFCLKN1	GNDA	PRXN3	GNDA	PTXP3	GNDA	PTXP2	GNDA	PRXP2	GNDA	GNDA	Y
AA	GNDA	GNDA	REXT	XI	GNDA	CC1	REFCLKP3	REFCLKP0	GNDA	REFCLKP2	REFCLKP1	GNDA	PRXP3	GNDA	PTXN3	GNDA	PTXN2	GNDA	PRXN2	GNDA	GNDA	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

Figure 2 ASM2464PDX Pinout Diagram

5. Pin Description

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
Di	Differential pin
P	Power pin
G	Ground pin
OD	Open Drain

Pin Name	Pin No.	TYPE	Power	Description
UDP	M1	IO	VCC	Positive Signal of USB2.0 on Type-C.
UDM	M2	IO	VCC	Negative Signal of USB2.0 on Type-C.
UTXP0	T1	Di O	VCCL	Positive Signal of SuperSpeed USB Lane 0 Transmitter for Type-C Configuration Channel 1. To minimize crosstalk, DO NOT use multi-line/port TVS/ESD package.
UTXN0	T2	Di O	VCCL	Negative Signal of SuperSpeed USB Lane 0 Transmitter for Type-C Configuration Channel 1. To minimize crosstalk, DO NOT use multi-line/port TVS/ESD package.
UTXP1	V2	Di O	VCCL	Positive Signal of SuperSpeed USB Lane 1 Transmitter for Type-C Configuration Channel 2. To minimize crosstalk, DO NOT use multi-line/port TVS/ESD package.
UTXN1	V1	Di O	VCCL	Negative Signal of SuperSpeed USB Lane 1 Transmitter for Type-C Configuration Channel 2. To minimize crosstalk, DO NOT use multi-line/port TVS/ESD package.
URXP0	P1	Di I	VCCL	Positive Signal of SuperSpeed USB Lane 0 Receiver for Type-C Configuration Channel 1. To minimize crosstalk, DO NOT use multi-line/port TVS/ESD package.
URXN0	P2	Di I	VCCL	Negative Signal of SuperSpeed USB Lane 0 Receiver for Type-C Configuration Channel 1. To minimize crosstalk, DO NOT use multi-line/port TVS/ESD package.
URXP1	Y2	Di I	VCCL	Positive Signal of SuperSpeed USB Lane 1 Receiver for Type-C Configuration Channel 2. To minimize crosstalk, DO NOT use multi-line/port TVS/ESD package.
URXN1	Y1	Di I	VCCL	Negative Signal of SuperSpeed USB Lane 1 Receiver for Type-C Configuration Channel 2. To minimize crosstalk, DO NOT use multi-line/port TVS/ESD package.
VBUS	G1	I	VCCH	USB VBUS input. This is a **5V tolerant** pin.
CC1	AA6	IO	VCCH	USB Type-C Configuration Channel 1 with built-in 5.1K-ohm Rd resistor.
CC2	Y6	IO	VCCH	USB Type-C Configuration Channel 2 with built-in 5.1K-ohm Rd resistor.
SBU1	K1	IO	VCCH	Side Band Use 1.
SBU2	J1	IO	VCCH	Side Band Use 2.
REFCLKN0	Y8	Di O	VCCL	Negative Signal of PCI Express Differential Clock 0.
REFCLKP0	AA8	Di O	VCCL	Positive Signal of PCI Express Differential Clock 0.
REFCLKN1	Y11	Di O	VCCL	Negative Signal of PCI Express Differential Clock 1.
REFCLKP1	AA11	Di O	VCCL	Positive Signal of PCI Express Differential Clock 1.
REFCLKN2	Y10	Di O	VCCL	Negative Signal of PCI Express Differential Clock 2.
REFCLKP2	AA10	Di O	VCCL	Positive Signal of PCI Express Differential Clock 2.
REFCLKN3	Y7	Di O	VCCL	Negative Signal of PCI Express Differential Clock 3.
REFCLKP3	AA7	Di O	VCCL	Positive Signal of PCI Express Differential Clock 3.
PRXN1	W20	Di I	VCCL	Negative Signal of PCI Express Lane 1 Receiver.

Pin Name	Pin No.	TYPE	Power	Description
PRXP1	W21	Di I	VCCL	Positive Signal of PCI Express Lane 1 Receiver.
PRXN0	N20	Di I	VCCL	Negative Signal of PCI Express Lane 0 Receiver.
PRXP0	N21	Di I	VCCL	Positive Signal of PCI Express Lane 0 Receiver.
PTXN1	U21	Di O	VCCL	Negative Signal of PCI Express Lane 1 Transmitter.
PTXP1	U20	Di O	VCCL	Positive Signal of PCI Express Lane 1 Transmitter.
PTXN0	R21	Di O	VCCL	Negative Signal of PCI Express Lane 0 Transmitter.
PTXP0	R20	Di O	VCCL	Positive Signal of PCI Express Lane 0 Transmitter.
PRXN3	Y13	Di I	VCCL	Negative Signal of PCI Express Lane 3 Receiver.
PRXP3	AA13	Di I	VCCL	Positive Signal of PCI Express Lane 3 Receiver.
PRXN2	AA19	Di I	VCCL	Negative Signal of PCI Express Lane 2 Receiver.
PRXP2	Y19	Di I	VCCL	Positive Signal of PCI Express Lane 2 Receiver.
PTXN3	AA15	Di O	VCCL	Negative Signal of PCI Express Lane 3 Transmitter.
PTXP3	Y15	Di O	VCCL	Positive Signal of PCI Express Lane 3 Transmitter.
PTXN2	AA17	Di O	VCCL	Negative Signal of PCI Express Lane 2 Transmitter.
PTXP2	Y17	Di O	VCCL	Positive Signal of PCI Express Lane 2 Transmitter.
PERST0#	G21	O	VCCH	Reset Signal for PCI Express interface 0.
PERST1#	F21	O	VCCH	Reset Signal for PCI Express interface 1.
PERST2#	E21	O	VCCH	Reset Signal for PCI Express interface 2.
PERST3#	D21	O	VCCH	Reset Signal for PCI Express interface 3.
RST#	H1	I	VCCH	Power on Reset.
TEST_EN	H21	I	VCCH	Test enable pin, internal weak pull down.
GPIO0	D1	IO	VCCH	GPIO0, internal weak pull high. (NVMe Active LED1)
GPIO20	A11	IO	VCCH	GPIO20, HDDPC1,internal weak pull high.
GPIO21	A12	IO	VCCH	GPIO21, INS2# (PRSNT2#), internal weak pull high.
GPIO22	A13	IO	VCCH	GPIO22, PE_WAKE#, internal weak pull high.
GPIO1	C1	IO	VCCH	GPIO1, internal weak pull high, I2C_INT for PDC.
GPIO2	B1	IO	VCCH	GPIO2, internal weak pull high. (PRSNT# for PCIe 4 x1)
GPIO3	A1	IO	VCCH	GPIO3, internal weak pull high. (NVMe Active LED2)
SPI_CS#	A2	IO	VCCH	GPIO4, SPI Chip Select for external SPI Flash, internal weak pull high.
SPI_DO	A3	IO	VCCH	GPIO5, SPI data output for external SPI Flash, internal weak pull high. This is also the strapping pin for "SKT_DET" when power on. Please refer to strapping information for more details.
SPI_CLK	A5	IO	VCCH	GPIO6, SPI clock output for external SPI Flash, I2C_CLK, internal weak pull high. (This I2C interface supports master mode only)
SPI_DI	A4	IO	VCCH	GPIO7, SPI data input for external SPI Flash, I2C_DATA, internal weak pull high. (This I2C interface supports master mode only)
GPIO8	A19	IO	VCCH	GPIO8, CLKREQ#, internal weak pull high.
I2C_DATA_P	F1	IO	VCCH	I2C data, internal weak pull high. (This I2C interface can be configured to be either master or slave mode)
I2C_CLK_P	E1	IO	VCCH	I2C clock, internal weak pull high. (This I2C interface can be configured to be either master or slave mode)
UART_TX	B21	O	VCCH	UART transmitter, internal weak pull high. This is also the strapping pin for "MEMREPAIR" when power on.
UART_RX	A21	I	VCCH	UART receiver, INS0# (PRSNT0#), internal weak pull high.
HDDPC	C21	O	VCCH	Power control for PCIe device, internal weak pull high.
GPIO14	A20	IO	VCCH	GPIO14, CLKREQ1#, internal weak pull high.
GPIO15	A6	IO	VCCH	GPIO15, internal weak pull high. (P1_LED)
GPIO16	A7	IO	VCCH	GPIO16, internal weak pull high. (P2_LED)
GPIO17	A8	IO	VCCH	GPIO17, internal weak pull high. (P3_LED)
GPIO18	A9	IO	VCCH	GPIO18, internal weak pull high. (P4_LED)
GPIO19	A10	IO	VCCH	GPIO19, INS1# (PRSNT1#), internal weak pull high.

Pin Name	Pin No.	TYPE	Power	Description
GPIO23	A14	IO	VCCH	GPIO23, CLKREQ2#, internal weak pull high.
GPIO24	A15	IO	VCCH	GPIO24, CLKREQ3#, internal weak pull high.
GPIO25	A16	IO	VCCH	GPIO25, internal weak pull high. (NVMe Active LED3)
GPIO26	A17	IO	VCCH	GPIO26, internal weak pull high. (NVMe Active LED4)
GPIO27	A18	IO	VCCH	GPIO27, INS3# (PRSNT3#), internal weak pull high.

Pin Name	Pin No.	TYPE	Power	Description
NC	J2, H2, G2, F2, E2, D2, C2, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, C20, D20, E20, F20, G20, H20	IO	VCCH	No Connections.
REXT	AA3	I	VCCH	External resistor 12.1 kΩ+/-1%.
XI	AA4	I	VCCH	Crystal Input.
XO	Y4	O	VCCH	Crystal Output.
VDD	J21, J20, K21, K20, J18, J17, J16, H16, F16, E16, D16, J14, J13, H14, H13, F14, E14, D14, L11, L14, N14, P14, T14, P13, T13, E11, F11, H11, T11, F9, H9, J9, J8, L8, N8, P8, T9, T8, U9, U8,	P	VDD	Core power supply input.
VCCL	L21, L20, L18, L17, L16, N16, P16, T16, U16, U14, U13, U11, U6, T6, P6, N6, L6,	P	VCCL	Low voltage VCC power.
VCCH	D13, E13, F13, D9, E9, D8, E8, D6, E6, F6, H6,	P	VCCH	High voltage VCC power.
VCCA33	H5	P	VCCA33	Analog high voltage VCC power.
GNDA	M21, M20, P21, P20, T21, T20, V21, V20, Y21, Y20, AA21, AA20, Y18, Y16, Y14, Y12, Y9, Y5, Y3, AA18, AA16, AA14, AA12, AA9, AA5, N18, N17, P18, P17, T18, T17, U18, U17, V18, V17, V16, V14, V13, V11, V9, V8, V6, L5, L4, N5, N4, P5, P4, T5, T4, U5, U4, V5, V4, AA1, AA2, W1, W2, U1, U2, R1, R2, N1, N2, L1, L2,	G		Analog Ground.
GND	K2, D4, E4, F4, H4, J4, D5, E5, F5, J5, J6, F8, H8, L9, N9, P9, D11, J11, N11, P11, L13, N13, D17, E17, F17, H17, D18, E18, F18, H18,	G		Digital Ground.

PCIe Port Mapping Table:

PCIe ports	PCIe Clock Pair				CLKREQ#				PE_RST#				PE_WAKE#	PRSNT#/INS#			
P0 P1 P2 P3	P0	P1	P2	P3	P0	P1	P2	P3	P0	P1	P2	P3	P0/P1/P2/P3	P0	P1	P2	P3
x4 --- --- ---	REFCLKP0 REFCLKN0	-	-	-	GPIO8	-	-	-	PERST0#	-	-	-	GPIO22	GPIO2	-	-	-
x2 --- x2 ---	REFCLKP0 REFCLKN0	-	REFCLKP2 REFCLKN2	-	GPIO8	-	GPIO23	-	PERST0#	-	PERST2#		GPIO22	UART_RX	-	GPIO21	-
x1 x1 x1 x1	REFCLKP0 REFCLKN0	REFCLKP1 REFCLKN1	REFCLKP2 REFCLKN2	REFCLKP3 REFCLKN3	GPIO8	GPIO14	GPIO23	GPIO24	PERST0#	PERST1#	PERST2#	PERST3#	GPIO22	UART_RX	GPIO19	GPIO21	GPIO27
x2 --- x1 x1	REFCLKP0 REFCLKN0	-	REFCLKP2 REFCLKN2	REFCLKP3 REFCLKN3	GPIO8	-	GPIO23	GPIO24	PERST0#	-	PERST2#	PERST3#	GPIO22	UART_RX	-	GPIO21	GPIO27
x1 x1 x2 ---	REFCLKP0 REFCLKN0	REFCLKP1 REFCLKN1	REFCLKP2 REFCLKN2	-	GPIO8	GPIO14	GPIO23	-	PERST0#	PERST1#	PERST2#	-	GPIO22	UART_RX	GPIO19	GPIO21	-

5.1 Strapping Information

The GPIO5 pin was used to support the PCIe hot-plug function. The function is enabled if GPIO5 is strapped to high. The UART_TX pin was used to support the internal memory repair function. The function is enabled if UART_TX is strapped to high.

Function control for PCIe hot-plug support

GPIO5	SKT_DET
H	Support
L	No support

Function control for internal memory repair

UART_TX	MEMREPAIR
H	Enable
L	Disable

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Absolute maximum ratings are conditions that should never be exceeded, even momentarily. Supplying a voltage over the maximum rating and/or using in environments outside of the temperature range may cause deterioration of IC characteristics or even damage.

The following stress parameters are references for stress ratings only. The operating device which functions beyond these recommended parameter ranges or conditions will not be applied. It is recommend to use a clamping circuit to protect the device when abnormal voltage spikes are encountered while power is switched on or off.

Parameter	Range	Unit
Power Supply	-0.5 ~ VCC+0.5	V
DC Input Voltage	-0.5 ~ VCC+0.5	V
Output Voltage	-0.5 ~ VCC+0.5	V
Storage Temperature	JEDEC J-STD-033B MSL 3	

6.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCH}	High voltage VCC power supply	3.0	3.3	3.6	V
V_{CCL}	Low voltage VCC power supply	1.85	1.9	1.95	V
V_{DD}	Core power supply	1.0	1.05	1.1	V
T_T	Top Center Temperature	0	25	90	ºC
T_J	Silicon Junction Temperature	0	25	90	ºC
HBM	Human Body Mode		TBD		KV
CDM	Charged Device Mode		TBD		V

Note: The **typical voltage** values specified above are recommended to be measured near the pin of the chip (e.g. the capacitors mounted beneth the chip.)

6.2.1 Chip Temperature (T_J, T_T) Calculation

Thermal data with heatsink UB15-15B 15x15x15 mm^3 under T_A=35°C

Symbol	Parameter	Method of Calculation
T_A	Ambient temperature	Measured temperature around the chip
T_J	Operating junction temperature	$T_J = \Theta_{JA} * P_H + T_A$
T_T	Operating top center temperature	$T_T = T_J - \Psi_{JT} * P_H$
Θ_{JA}	Junction-to-ambient thermal resistance	V_{air}=0 (m/s): 17.38 V_{air}=1 (m/s): 8.24 V_{air}=2 (m/s): 6.25
Ψ_{JT}	Junction-to-top-center thermal characterization parameter	V_{air}=0 (m/s): 0.22 V_{air}=1 (m/s): 0.29 V_{air}=2 (m/s): 0.31
Ψ_{JB}	Junction-to-board thermal characterization parameter	V_{air}=0 (m/s): 4.88 V_{air}=1 (m/s): 2.84 V_{air}=2 (m/s): 2.37
P_H	Chip power disspation	Measured chip power consumption

- EIA/JESD51-2, Integrated circuit Thermal Test Method Enviornment Conditions – Natural Convention (Still Air)
- EIA/JESD51-6, Integrated circuit Thermal Test Method Enviornment Conditions – Forced Convention (Moving Air)
- EIA/JESD51-8, Integrated circuit Thermal Test Method Enviornment Conditions – Junction-to-Board.
- EIA/JESD51-9, Test Board for Area Array Surface Mount Package Thermal Measurements.

- **Note:** It is recommended to implement an appropriate system level thermal solution (e.g. heatsink, silicone thermal interface pad, metal housing, etc.) to disspate excess heat.

6.3 AC/DC Characteristics

6.3.1 PCI Express Electrical Specification

(Refer to PCI Express Base Specification Rev. 4.0)

6.3.2 USB4 Electrical Specification

(Refer to Universal Serial Bus 4 Specification Rev. 1.0)

6.3.3 USB Type-C Specification

(Refer to Universal Serial Bus Type-C Cable and Connector Specification Rev. 2.1)

6.3.4 USB Power Delivery Specification

(Refer to Universal Serial Bus Power Delivery Specification Rev. 3.1)

6.3.5 USB2.0 Electrical Specification

(Refer to Universal Serial Bus Specification Rev. 2.0)

6.3.6 DC Electrical Characteristics for Digital Pins

(For VBUS, and I2C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage Level	2.0		3.6	V
V_{IL}	Input Low Voltage Level	-0.3		0.8	V
V_{HYS}	Input Hysteresis	0.47	0.48	0.49	V
V_{TH-L2H}	Threshold of Schmitt Trigger low to high	1.58	1.71	1.86	V
V_{TH-H2L}	Threshold of Schmitt Trigger high to low	1.11	1.23	1.37	V
V_{OH}	Output High Voltage Level	2.4			V
V_{OL}	Output Low Voltage Level			0.4	V
I_{OH}	Output Driving Current while V_{OH}	12			mA
I_{OL}	Output Driving Current while V_{OL}	12			mA
R_{UP}	Internal Pull-up resistance while V_{IN}=0V	51	75	116	KΩ
R_{DN}	Internal Pull-down resistance while V_{IN}=VCC	54	84	145	KΩ
I_{IL}	Input pull-up leakage current after V_{IN} is read, R_{UP} is off & I_{IL} < 1μA when V_{IN}=0			+/-10	μA
	Input pull-up leakage current after V_{IN} is read, R_{UP} is off & I_{IL} < 1μA when V_{IN}=VCC/2			+/-10	μA

(For PERST, UART, HDDPC, and GPIOs)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage Level	2.0		3.6	V
V_{IL}	Input Low Voltage Level	-0.3		0.8	V
V_{HYS}	Input Hysteresis	0.57	0.57	0.58	V
V_{TH-L2H}	Threshold of Schmitt Trigger low to high	1.66	1.77	1.92	V
V_{TH-H2L}	Threshold of Schmitt Trigger high to low	1.08	1.2	1.34	V
V_{OH}	Output High Voltage Level	2.4			V
V_{OL}	Output Low Voltage Level			0.4	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{OH}	Output Driving Current while V_{OH}	12			mA
I_{OL}	Output Driving Current while V_{OL}	12			mA
R_{UP}	Internal Pull-up resistance while V_{IN}=0V	57	83	129	KΩ
R_{DN}	Internal Pull-down resistance while V_{IN}=VCC	59	92	159	KΩ
I_{IL-UP}	Input pull-up leakage current after V_{IN} is read, R_{UP} is off & I_{IL} < 1μA when V_{IN}=0			+/-10	μA
I_{IL-DN}	Input pull-down leakage current after V_{IN} is read, R_{DN} is off & I_{IL} < 1μA when V_{IN}=VCC			+/-10	μA

(For SBU1, and SBU2, please refer to **Table 3.1** SBTX and SBRX specification in Universal Serial Bus 4 Specification Rev. 1.0)

6.3.7 DC Electrical Characteristics for RST# Pin

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage Level	2.0			V
V_{IL}	Input Low Voltage Level			0.8	V
V_{HYS}	Input Hysteresis	0.32	0.37	0.4	mV
V_{TH-L2H}	Threshold of Schmitt Trigger low to high	1.58	1.71	1.86	V
V_{TH-H2L}	Threshold of Schmitt Trigger high to low	1.11	1.23	1.37	V
Input	Input pull-up leakage current while V_{IN}=0V			1	μA

6.3.8 External Crystal Electrical Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{XTAL}	Frequency		25		MHz
Δf_{XTAL}	Long Term Stability (at 25° C)	-30		30	ppm
t_C	Temperature Stability	-30		30	ppm
F_A	Aging	-5		5	ppm
C_L	Load Capacitance (Single-end mode)		16		pF
C_0	Shunt Capacitance	1	3	7	pF

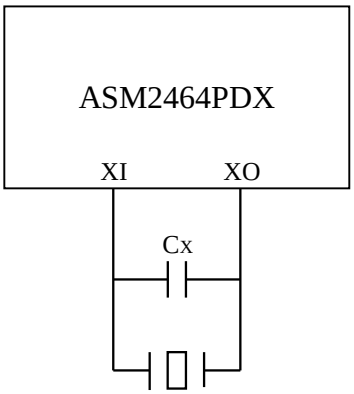


Figure 3 Differential Crystal Design

6.3.9 Differential Clock Oscillator Electrical Specification

The following table describes the specification of clock with external 25MHz crystal. Please refer to Figure 3.

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{XTAL}	Frequency		25		MHz
Δf_{XTAL}	Long Term Stability (at 25° C)	-150		150	ppm
C_X	External Load Capacitance (Differential mode)		10		pF

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{TOTAL}	Total external equivalent Capacitance from XI pin to XO pin (Differential mode)	9	11	15	pF
R_{TOTAL}	Total external equivalent Series Resistance from XI pin to XO pin (Differential mode)			60	Ω

6.3.10 PCI Express 100MHz Output Clock Electrical Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OH}	Differential Output High Voltage	150			mV
V_{OL}	Differential Output Low Voltage			-150	mV
V_{CROSS}	Absolute crossing point voltage	250		550	mV
t_{CROSS_DELTA}	Variation of V_{CROSS} over all rising clock edges			140	mV
t_{PERIOD_AVG}	Average clock period accuracy	-300		300	ppm
t_{CCJ}	Cycle to Cycle Jitter			150	Ps
t_{DC}	Reference Duty Cycle	40		60	%
RT_{RISING}	Rising Edge Rate	0.6		4.0	V/ns
$RT_{FALLING}$	Falling Edge Rate	-4.0		-0.6	V/ns

6.3.11 Internal Linear Regulator Electrical Specification

TBD

6.3.12 Power Consumption Specification

Symbol	Parameter	Max.	Unit
I_{CCHMAX} (Note 1)	Maximum Current consumption of V_{CCH}	TBD	mA
I_{CCLMAX}	Maximum Current consumption of V_{CCL}	TBD	mA
I_{DDMAX}	Maximum Current consumption of V_{DD}	TBD	mA

Note 1: The number could vary depending on the use of GPIO pins

7. Power on Sequence

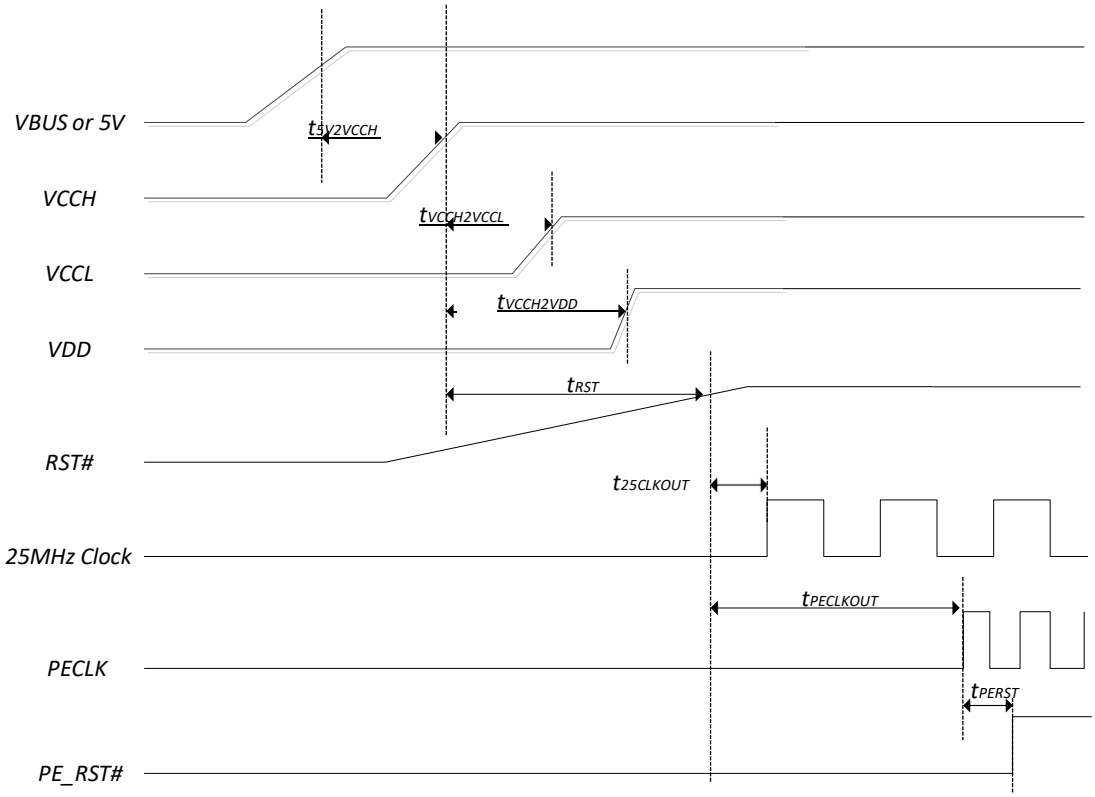


Figure 4 Waveform of Power on Sequence

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{5V2VCCH}$	V_{CCH} (90%) available after the presence of 5V or VBUS (90%)		3	6	ms
$t_{VCCH2VCCL}$	V_{CCL} (90%) available after the presence of V_{CCH} (90%)	0	5	10	ms
$t_{VCCH2VDD}$	V_{DD} (90%) available after the presence of V_{CCH} (90%)			90	ms
t_{RST}	RST (90%) ready after the presence of V_{CCH} (90%)	0			ms
$t_{25CLKOUT}$	25MHz clock available after the presence of RST#(90%) assertion			10	ms
$t_{PECLKOUT}$	PCI Express Reference Clock output after the presence of RST#(90%) assertion	100			ms
t_{PERST}	PCI Express Reset (90%) assertion after the presence of PCI Express Reference Clock output	100			µs

8. Recommended PCB Layout

It is recommended to use 7 X 13 mil oblong pads as the footprint for outer rows of ASM2464PDX Package.

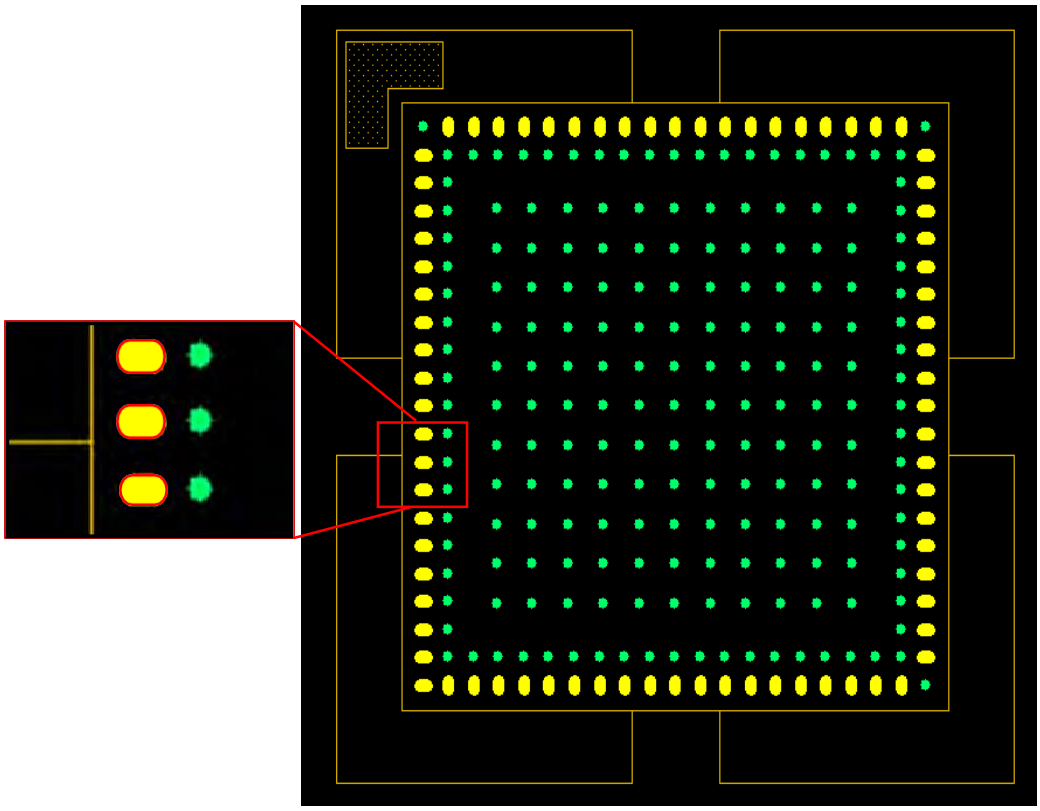


Figure 5 Pads for ASM2464PDX Outer Rows

Beware of the direction of AA1 pad for ensuring the USB trace can be routed from the inner row pad.

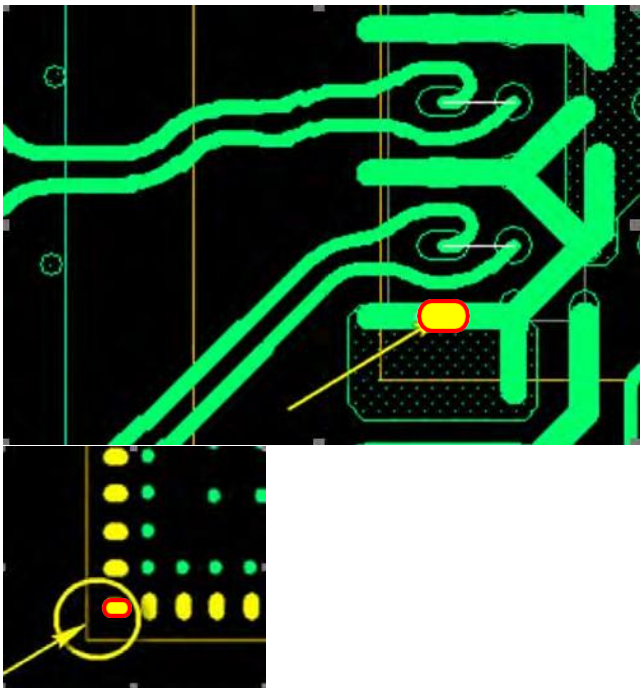
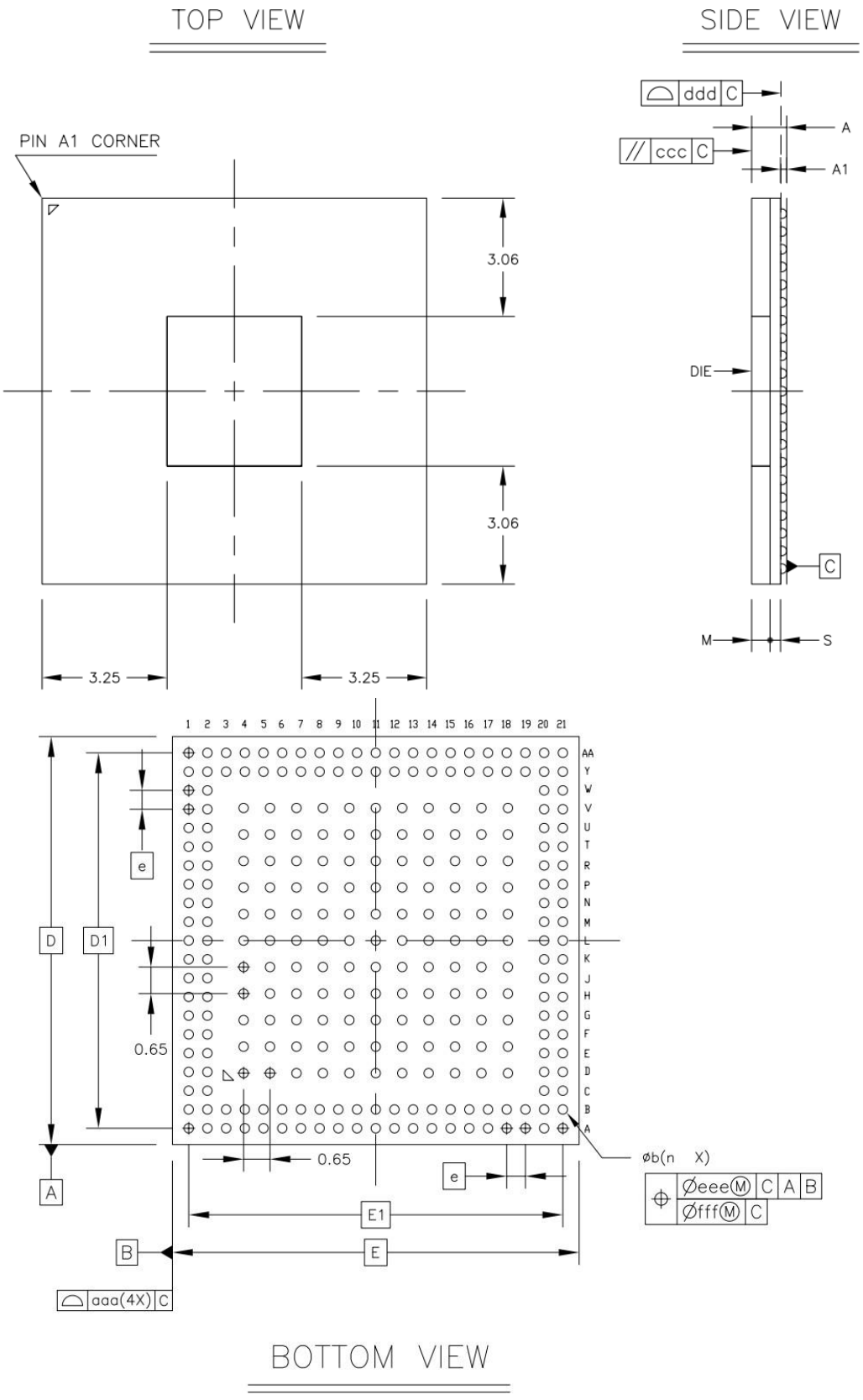


Figure 6 Pad AA1 Implementaion

9. Package Information

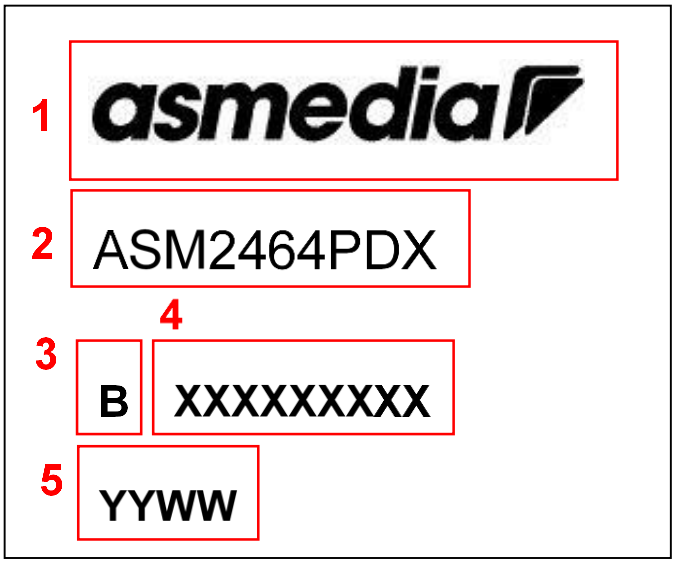


		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			FCCSP		
Body Size:	X	E	10.000		
	Y	D	10.000		
Ball Pitch :		e	0.460		
Total Thickness :		A	–	–	0.982
Mold Thickness :		M	0.480 Ref.		
Substrate Thickness :		S	0.272 Ref.		
Ball Diameter :			0.230		
Stand Off :		A1	0.120	–	0.200
Ball Width :		b	0.170	–	0.270
Package Edge Tolerance :		aaa	0.100		
Mold Parallelism :		ccc	0.200		
Coplanarity:		ddd	0.150		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.050		
Ball Count :		n	273		
Edge Ball Center to Center :	X	E1	9.200		
	Y	D1	9.200		

Figure 7 Mechanical Specification

			Common Dimensions (mm)		
		Symbol	MIN.	NOM.	MAX.
Package :			FC CSP		
Body Size :	X	E	10.000		
	Y	D	10.000		
Ball Pitch :		e	0.460		
Total Thickness :		A	–	–	0.982
Mold Thickness :		M	0.480 Ref.		
Substrate Thickness :		S	0.272 Ref.		
Ball Diameter :			0.230		
Stand Off :		A1	0.120	–	0.200
Ball Width :		b	0.170	–	0.270
Package Edge Tolerance :		aaa	0.100		
Mold Parallelism :		ccc	0.200		
Coplanarity :		ddd	0.150		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.050		
Ball Count :		n	273		
Edge Ball Center to Center :	X	E1	9.200		
	Y	D1	9.200		

10. Top Marking Information



1. asmedia: ASMedia Logo
2. ASM2464PDX: Product Name
3. B: Version of ASMedia Marking Rule
4. XXXXXXXXX: Serial No. Reserved for Vendor
5. YYWW: Date Code