September 5, 2023: Project Kickoff and Requirement Gathering We began our project with a focus on understanding its scope and outlining requirements. As the Scrum Master, I facilitated brainstorming sessions to identify potential features and functionalities, emphasizing the need for a clear roadmap and establishing the use of the Digilent Nexys A7 board for initial implementation.

September 7, 2023: Material Outlining and Work Division I led the team in outlining essential materials and dividing the workload, ensuring that each member had a clear understanding of their responsibilities. This session was crucial for establishing a structured approach to our diverse project requirements.

September 12, 2023: Architecture and Technical Specifications Our discussions advanced into defining the project's technical aspects. I guided the team in determining the architecture, focusing on integrating a Xilinx MicroBlaze soft-core CPU and emphasizing the importance of a robust plan for technical challenges.

September 14, 2023: Vivado Installation and Debugging I conducted a comprehensive walkthrough of the Vivado installation process, addressing common issues to ensure a unified development environment across the team.

September 19, 2023: Progress Update and Research Review We reviewed our progress, focusing on coding efforts and Vivado implementation issues. I encouraged the team to share individual research insights, enhancing our collective understanding and refining our project approach.

September 21, 2023: MicroBlaze Tutorial and Research I spearheaded a tutorial session on MicroBlaze, fostering a deeper understanding of its implementation and potential challenges. The session reinforced our collaborative approach to problem-solving.

September 26 & 28, 2023: Continued Exploration of MicroBlaze and IPs I guided the team in exploring MicroBlaze and delving into the implementation of various IPs, emphasizing their integration and potential interdependencies within our system.

October 3, 2023: Planning for Digilent Nexys A7 Implementation Our focus shifted towards transitioning to the Digilent Nexys A7 board. I led the planning and testing procedures, considering hardware compatibility and potential adjustments.

October 5 & 10, 2023: HTML Design and Functionality As a team we discussed the HTML design, exploring user-friendly interface patterns and the integration of dynamic content for our web server. The HTML Was then redesigned by Conrad and he identified the scripting utilized by the webserver example design.

October 17 & 19, 2023: FreeRTOS "Hello World" Implementation and Debugging Our team focused on implementing and debugging a FreeRTOS "Hello World" design. I spent considerable time helping both Ricky, Morgan and Jack in their execution of this example design.

October 24, 2023: Collaborative Efforts and Backlog Management Working alongside Ricky, I initiated the construction of an example design project on his Vivado. I updated the backlog for the current sprint, and we overhauled it for the semester. Following the customer's directive, we split the project into a hardware/FPGA design team and a software design team, with the hardware team focusing heavily on communication. I also directed the discussion with Jack about the implementation of the 1 Pulse Per Second functionality.

October 31, 2023: Team Coordination and Vivado/SDK Troubleshooting I convened a meeting to discuss sprint deliverables and strategized the finalization of environment setup. I aided the team in resolving Vivado and SDK installation issues. My focus extended to redesigning diagrams for clarity and discovering the need to downgrade to Vivado 2018.1 for the STDIO connection in our design. In the Software Requirement Specification (SRS), I removed superfluous requirements, refined formatting, and tweaked existing requirements based on feedback. In the Software Design Specification (SDS), I incorporated a Context Diagram, a Use Case Diagram, addressed all TA feedback, and added descriptive elements for each diagram.

November 7 & 9, 2023: Refining SDD, SRS, and Test Plan I led the team in enhancing our Software Design Document, Software Requirement Specification, and Test Plan, ensuring comprehensive and accurate documentation.

November 14 & 16, 2023: FreeRTOS WebServer Implementation The implementation of the FreeRTOS WebServer began under my guidance. I focused on integration challenges and fostering a dynamic problem-solving atmosphere.

November 19-20, 2023: Extensive FPGA Redesign and Troubleshooting I dedicated 18 hours to completely rebuild the FPGA block design from scratch,

integrating micro blaze, the memory interface generator, the ethernet block, and all components necessary for handling MicroBlaze interrupts, the AXI interface, and necessary clocking generation. I navigated through several challenges, including memory FPGA pin locations, which I found to be identical to those on the Nexys 3 dev board. Additionally, I resolved memory clocking rate issues, establishing that the correct rates were 100 and 200 MHz.

November 21, 2023: SDK Integration and Design Testing I integrated the SDK into our design and undertook its uploading to the board. My testing confirmed partial functionality, as evidenced by the ethernet link's LED indicators, providing critical insight into the clock rate to the PHY.

November 23, 2023: Final Presentation and Documentation I spearheaded the creation of the final presentation and the refinement of project documentation, consolidating our achievements and challenges for an impactful conclusion.

December 1, 2023: SRS & SDS Finalization: I have incorporated our block design within the detailed design section for the hardware. Along with this is a description of the components that make up the block design and some details about how these components play a role in the bigger picture of the project. Additionally, I've created a description to go along with the Context Diagram.

December 3, 2023: Final Presentation: As a team we all worked on developing a final presentation according to the specifications in canvas. We cleaned up some of our diagrams but did not include them on our presentation as we focused more on the requirements for this presentation. In addition to this we spoke with our customer to confirm that they are satisfied with our performance thus far.

December 7, 2023: Finally Jack Capuano and I worked on the Test Plan once we had a break from work in all of our classes. I did the majority of the flushing out of our test plan but overall this document is not complete as all of our requirements are not testable due to the fact that our software is behind our hardware (verilog) implementation. Hamilton developed our 3 minute video pitch after a discussion with the team and I finished up my work on the project for this semester.

Semester 1 Note: After this first semester, we have made some significant progress but I am determined to make some significant progress over this winter break on the project. This progress will mainly be the implementation of the base software on the

developed FPGA hardware and soft CPU. All in all this semester was decent and with better communication we will have a very good final semester in finising up the project.