Comilla University
Faculty of Engineering
Department of Computer Science and Engineering

2nd Year 1st Semester Final Examination - 2020
Course Code: CSE 2105 Session: 2018 - 2019
Course Title: Digital Logic Design

[Answer any Five of the following questions. Figures in the right-hand margin indicate full marks.]

Time: 3 Hours **Full Marks: 60**

Writing anything on the question paper is strictly prohibited.

1 a) What is meant by the base of a number system? Explain principle of Duality. 1+2
b) Which of the codes are called invalid codes in BCD and why? 3
c) Why is Gray code not suitable for arithmetic operations? Explain with example. 4
d) Convert the binary code 101101 to Gray code. 2

2 a) Distinguish between a Half-Adder and a Full-Adder. 2
b) Implement a Full-Adder using two Half-Adders and an External OR gate. 3
c) Construct a 16-bit Parallel Binary Adder using 4-bit Parallel Binary Adder ICs. 3
d) Represent the decimal number -27 as an 8-bit number in i) sign-magnitude representation, ii) 1's complement representation, and iii) 2's complement representation. 4

3 a) Differentiate between Combinational circuit and Sequential Circuit. 3
b) Design a combinational logic circuit that controls the passage of a signal A according to the following requirement: 6
i) Output Y will equal A when control inputs B and C are same.
ii) Y will remain HIGH when B and C are different.

c) Implement the following function using only NAND gates: 3

$$f(A, B, C) = A\bar{B} + \bar{A}B + C$$

4 a) Minimize the following function using k-map and realize using NOR gates only 5

$$\Pi M (1, 2, 3, 8, 9, 10, 11, 14). d(6, 7, 15)$$

b) Design a 2-bit magnitude comparator circuit. 4
c) What are the difference between a ripple carry adder and a look-ahead carry adder? 3

5 a) Using binary arithmetic evaluate the binary arithmetic expression: 2

$$101110+1101111$$

b) The binary ripple-carry addition algorithm used in (a), can be implemented using a one-bit full adder that takes two input bits a and b and a carry-in bits c and compute a sum bit z and a carry-out bit d. The diagram below illustrates the input and outputs of a one-bit adder.
i. Draw a truth table for the one-bit full adder. 2
ii. Based on the truth table obtained in (i) write the logical expressions for the sum bit z and carry-out bit d. 4

iii. Simplify the logical expressions obtained in (ii), and draw one circuit diagram for one-bit full adder.

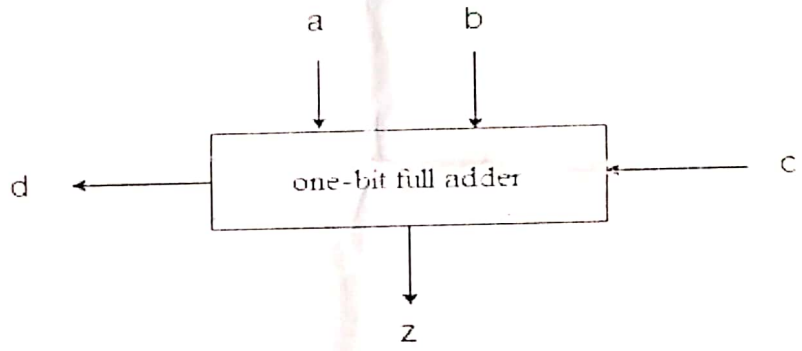

Fig. 1

6 a) Design a 16:1 multiplexer using 4:1 multiplexer ICs. Mention some applications of multiplexers.
b) Implement a full adder logic circuit using multiplexers.
10 c) Design a 1-to-8-line Demultiplexer.

8 a) What is the difference between a Latch and a Flip-Flop?
b) Design an S-R latch using two 2-input NAND gates.
12 c) How can Race-Around Condition be eliminated with necessary diagram
d) Draw the logic diagram with truth table of a clocked D-type Flip-Flop.

(a) diff → shift regi and counter

(b) explain → siso shift regis operate