COMILLA UNIVERSITY
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
2nd Year 2nd Semester Final 2019

Course Code: CSE-2206 **Course Title:** Computer Architecture & Organization
Session: 2017-2018 Full Marks: 60 Time: 3 Hours

(Answer any **05 (five)** questions from the following)

1. a. State Amdahl's law for multiprocessors with necessary equation and graph. [3]

   b. What is the overall speedup if you make 90% of a program 10 times faster? [2]

   c. Explain the principles of Cache Memory. [3]

   d. Draw the typical Cache organization. [2]

   e. Conclude the general relationship among access time, memory cost and capacity. [2]

2. a. There is a Sequence of nine memory references to an empty eight-block cache, including the action for each reference. Show the contents of the cache change on each miss and after handling all misses of address. [4]

Decimal Address of Reference	22	26	22	26	16	3	16	18	16
Hit or Miss	Miss	Miss	Hit	Hit	Miss	Miss	Hit	Miss	Hit

   b. How does an implementation of 2-way cache compare with that of a fully-associative cache? [4]

   c. Describe four states of a simple cache controller. [4]

3. a. Explain Flynn classification. [3]

   b. Draw the block diagram of Intel Core i7-990X. [3]

   c. Why designers choice a multicore organization rather than increase parallelism within a single processor? Give your reasons. [3]

   d. Explain the register organization of Intel 8086 processor. [3]

4. a. Consider the instruction "ADD R1, (R2)". Now write down the corresponding Micro instruction and control sequence for the given instruction. [3]

   b. How Pipeline Works? [3]

   c. What are the advantages and disadvantages of Hardware Control Unit? [2]

   d. Write the functionality of Microprogrammed Control Unit. [2]

   e. What are the primary benefits of parallel processing systems? [2]

5. a. Draw the block diagram of the CPU and describe how instructions are executed inside it. [4]

b. Describe the construction of main memory which has 1MB space and each cell contains 16bit data. [4]

c. Suppose address of A=1001, address of B=1010, address of C=1011, and content of A=01, content of B=10. Execute the instruction C=A+B and explain it according to the block diagram of CPU. [4]

6. a. Briefly define the main structural components of a processor. [3]

b. Explain the structure and memory format of IAS computer. [3]

c. List out the key characteristics of a computer family. [3]

d. A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count: [3]

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate and execution time for this program.

7. a. Describe different types of Hazards in pipelining. [4]

b. Draw the diagram of Microarchitecture of AMD Opteron X4 pipeline. [4]

c. Find the average time to read or write a 512-byte sector for a typical disk rotating at 15,000 RPM. The advertised average seek time is 4 ms, the transfer rate is 100MB/sec, and the controller overhead is 0.2 ms. Assume the disk is idle so that there is no waiting time. [4]

8. a. What are the major strategical differences among sequential access, direct access and random access? [3]

b. Clarify the following terms: [3]

i. EPROM
ii. EEPROM
iii. SRAM

c. Explain the Booth's algorithm for Two's complement multiplication. [3]

d. Show the differences among positive overflow, exponent overflow and significant overflow. [3]