

A Scan-Chain-Based Built-In Self-Test for ILV in Monolithic 3-D ICs

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Abstract—In comparison with through-silicon vias (TSVs) used in 3-D integrated circuits (3D ICs), nanoscale interlayer via (ILV) employed in monolithic 3D ICs offers higher integration density. However, the elevated integration density, coupled with the corrosive scaling of interlayer dielectric (ILD) and immature manufacturing processes, can lead to failures in ILVs. Built-in self-test (BIST) can be used to test and diagnose ILVs. Previous research on ILVs in monolithic 3D ICs assumed 1-D ($1 \times D$) placement and limited bridging faults (shorts) occurring only between ILVs in the same direction. However, to minimize the wiring length in monolithic 3-D (M3D), the layout of ILVs may adopt an irregular arrangement, and at the same time, bridging faults may occur between ILVs in different orientations. To detect and locate all possible ILV faults in a real ILV layout, a new BIST method is proposed, which can detect open, stuck-at faults (SAFs), and all possible shorts in ILVs by using the scan chain encapsulated in the active layer. The simulation results using HSPICE and Vivado show that the proposed BIST method can effectively detect and locate faulty ILVs.

Index Terms—Built-in self-test (BIST), interlayer vias (ILVs), monolithic 3-D (M3D).

I. INTRODUCTION

TO CONTINUE Moore's law, 3-D integration technology allows for higher density integration compared with traditional 2-D integrated circuits. Based on the basic structure, 3-D integration technology can be categorized into two types: die stacking, known as 3-D stacked chips, and monolithic 3D ICs. These two methods employ different vertical interconnections in terms of size and spacing. The silicon via (TSV) used in 3-D stacked chips typically operates at the micrometer level, while the interlayer via (ILV) utilized in monolithic 3-D (M3D) integrated circuits operates at the nanometer level. Consequently, M3D integrated circuits offer increased integration density and

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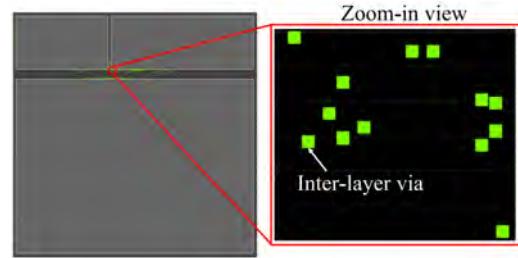


Fig. 1. Irregular ILV placement [4].

reduced interconnect length compared with traditional 3-D integrated circuits based on TSV. However, the immaturity of the M3D process and the aggressive scaling of interlayer dielectrics (ILDs) to achieve high-density integration make ILVs particularly vulnerable to defects. In [1], the challenges associated with fabricating top-layer transistors in M3D are discussed. The increased integration density of ILVs amplifies the likelihood of bridging failures (shorts) occurring between neighboring ILVs. When the ILV is faulty, the consequences extend to the active devices in the active layer, resulting in significant negative impacts on the overall circuit. Although ILVs can be tested with active layers, defect isolation and yield learning still require a test solution that can effectively target ILV faults.

The ILV built-in self-testing (BIST) methods proposed in [2] and [3] both assume that the ILVs are arranged in a 1-D configuration, and that one of them may have short faults with at most two neighboring ILVs. Furthermore, the current BIST structure also assumes that shorts solely occur between upgoing and downgoing ILVs, with no occurrence of shorts between upgoing and downgoing ILVs, as the upgoing ILVs are physically distant from the downgoing ILVs. However, [4] mentions that during automatic algorithm-driven place-and-route by a commercial tool, ILVs may not necessarily be arranged in 1-D arrays. The actual distribution can be more complex as shown in Fig. 1.

This irregular arrangement makes the ILV fault scenario becomes more complex, while shorts may occur between the upgoing and downgoing ILVs. Although the BIST capture engine proposed in [3] can detect potential shorts between neighboring ILVs in a 1-D placement during the test, when the ILVs are irregularly distributed, more test iterations are required to cover all possible shorts. A switch box was added in [4] and used to detect shorts between upgoing and downgoing ILVs. A defect graph is also constructed with the coordinates of the ILVs and the potential shorts between

them. The IFA [5] procedure is used to identify the pairs of ILVs where shorts are likely to occur and prune the defect graph, to cover all the most probable shorts with the smallest possible number of test iterations to complete the detection and localization of the ILV faults. Although this method considers the irregular arrangement of ILVs, its BIST structure can only detect shorts between neighboring ILVs during one test iteration. It can only consider shorts with a higher likelihood of occurrence.

This article proposes a scan-chain-based BIST method to detect and locate opens, stuck-at faults (SAFs) in ILVs while considering all possible shorts as much as possible. The main contributions are as follows.

- 1) A BIST architecture is proposed that works by multiplexing the scan chain in the active layer, which has two modes: functional mode and test mode. The functional mode ensures the normal use of the ILVs; the test mode performs tests on the ILVs using the scan chain encapsulated in the active layer, which is used to detect and locate opens, SAFs, and all possible shorts between the ILVs.
- 2) To save test overheads, the test structure is improved to achieve grouping tests, and the improved BIST structure selects only one group of ILVs for testing at a time until all ILVs have been tested. The k -means algorithm is introduced to divide the nonuniform distributed ILVs equally into multiple clusters, with each cluster acting as a test group to achieve wire overhead minimization.
- 3) The fault detection capability of the proposed BIST structure was simulated and evaluated by HSPICE using the 45-nm Nangate open cell library.
- 4) The BIST controller in the proposed BIST structure was simulated by Vivado to demonstrate the feasibility of the test flow.
- 5) The coupling between adjacent ILVs was analyzed, and specific test patterns were used to induce and detect crosstalk faults caused by coupling, proving that the test structure has detectability for crosstalk faults.
- 6) We compared the test structure with similar works in 3D-IC and designed two fault-tolerant schemes for the test structure.

The remainder of this article is presented as follows. Section II overviews the M3D technique and related prior work on BIST structures for ILV testing. Section III describes the proposed BIST test structure for detecting and localizing ILVs. Section IV describes a grouping test structure that uses a clustering algorithm to divide ILVs into multiple test groups, improves the BIST controller, and presents the test flow of the improved architecture. Section V presents the experimental evaluation results, and Section VI concludes this article.

II. BACKGROUND

A. M3D Fabrication Process

In monolithic 3D IC fabrication, the underlying transistors and their interconnections are first processed using standard high-temperature processes. Then, when the underlying devices and internal interconnections are complete, a very thin

layer of ILD is applied for insulation between the layers. Next, the next layer of devices and internal interconnects is generated vertically using low-temperature molecular bonding of the silicon-on-insulator (SOI) substrate under strict thermal constraints [5], [6]. Finally, ILVs are fabricated to connect the two active layers. If additional active layers need to be fabricated, the steps above are repeated.

The two most critical and essential processes in the manufacturing process are as follows:

- 1) a low-temperature process to form a thin silicon film on the surface of the bottom layer;
- 2) processes for fabricating the top-layer transistor without damaging the bottom interconnect or degrading the performance of the bottom transistor.

Although processes have been developed to fabricate transistors at low temperatures, these processes can still lead to a performance mismatch of up to 20% between the devices in different layers [7].

B. ILV Irregularly Placement

The arrangement layout of ILVs has been discussed in [4]. It is typically determined by the M3D wiring, which aims to minimize the line length for optimized M3D wiring. A commercial 2-D placement and wiring tool with a partition-first (partitioning-last) strategy is used for this purpose. This involves partitioning the 2-D netlist into multiple layers using a layer partitioning algorithm, typically a min-cut algorithm. The goal is to determine the number of ILVs while minimizing yield loss due to ILV faults. Once the logical units are divided and placed into different layers, the ILVs are usually positioned near the logical gates to reduce path delay [8].

Through the above steps, the final ILV arrangement is not necessarily a 1-D arrangement, so the number of ILV faults, especially shorts, increases dramatically, leading to an increase in the cost of testing the M3D chip.

C. ILV Fault Models

The reliability of ILVs is a major concern in M3D ICs. Traditional interconnects, such as TSVs, which use copper as a filler metal, cannot be used as an interconnect between layers in M3D due to the risk of possible contamination during the fabrication of the upper layers and the thermal instability of low-k dielectrics after the annealing process [9]. Instead, ILVs in modern processes are usually made of titanium nitride (TiN) as an insulating layer and internally filled with tungsten (W) metal [3]. These two materials are more compatible with the thermal budget in the M3D fabrication process and have good thermal stability. At the same time, it prevents diffusion of the metal inside the ILVs into the surrounding dielectrics, reducing the probability of short occurring. However, under the analysis of finite-element software Q3D, the equivalent resistance is three times higher than that of copper metal of the same dimensions, which may increase RC delay in the device layer [10].

ILV faults usually occur during metal plating processes, and typically, only the resistance and capacitance parameters of the ILVs are considered when modeling these faults. The typical

fault models are opens, shorts, and SAFs [11], [12]. Based on the type and degree of faults, these faults can be further classified into hard and resistive faults.

Hard faults are of a higher degree and are usually due to immature manufacturing processes [13]. Hard shorts can occur when the manufacturing process introduces foreign particle contamination that causes connections between ILVs. Hard opens can occur when ILVs are manufactured without accurate connections between their bottom ends and landing pads, creating gaps that lead to very high open-circuit resistances, typically around $M\Omega$ s [14], [15].

Resistive faults are less severe. Resistive shorts occur when the insulation layer outside the ILV is incompletely deposited, and the filler metal inside the ILV diffuses into the dielectric to form a connection with another ILV [10]. These types of faults typically have short resistances in the intermediate range, typically between a few $K\Omega$ s and a few $100 K\Omega$ s [15].

Resistive opens are usually caused by bonding defects [10], pinhole defects [16], and cracks generated during the manufacturing process. These types of faults occur to a lesser extent than hard opens, which typically have resistances in the range of a few $K\Omega$ s to a few $100 K\Omega$ s [8].

D. Prior Work on ILV Test

For ILV testing, considering that both ILVs and TSVs are used as vertical interconnects, one potential approach is to use TSV test methods for ILV testing. However, due to the different manufacturing processes of ILVs compared with TSVs, and the higher integration density (30 million per mm^2 [17]) of ILVs, using a TSV-based test method may introduce significant test overhead. TSV test methods can be divided into prebond and postbond tests from a production process perspective. Traditional prebonding test methods often use probe-based test methods, which can solve the problem of limited on-chip test resources for TSV fault detection [18] but do not apply to ILVs. ILVs are the last step in the M3D fabrication process and will be exposed less than TSVs. In addition, the current state-of-the-art wafer-probe test techniques cannot support the spacing requirements of ILVs (100–200 nm) [19]. The bound TSV test method can be extended to M3D. However, recently proposed methods, such as [20], which add a test wrapper unit to both ends of each TSV, cause an exceptionally high area overhead, since the number of ILVs in M3D is one to two orders of magnitude higher than that of TSVs. There is also a class of test methods using a ring oscillator [21] that can reflect the transmission delay of a faulty TSV by changes in the oscillation period of the ring oscillator. However, due to the higher integration of the M3D circuits and the nanoscale size of the ILVs, the accuracy of the ring oscillator is unable to satisfy the test requirements of the ILVs. Interconnect testing based on automatic test pattern generation (ATPG), as described in [22], may be less effective for ILVs. The test vectors generated by ATPG with the test response obtained from feedback must be propagated to the ILVs under test through multiple active layers and layer-to-layer ILVs. Meanwhile, in the case of M3D circuits, the I/O pins are only present in the top active layer of the M3D, and various types of faults generated in the test path may affect testability.

To detect ILV faults more accurately, [23] proposes an interlayer BIST method using interface register units and twisted ring counters, which can effectively detect ILV short and open faults. However, it requires a dedicated test layer, and the method assumes that the number of upgoing ILVs between two layers is equal to the number of downgoing ILVs, which is not valid in real ILV distribution. Chaudhuri et al. [2] assume a 1-D arrangement of ILVs and propose a low-cost BIST method. This method can detect opens, shorts, and SAFs in ILVs using two test modes. However, it can only detect shorts between neighboring ILVs, and the test escapes exist.

III. SCAN-CHAIN-BASED BIST ARCHITECTURE

A. Proposed BIST Architecture

The scan chain is improved without affecting its original functionality, and using the modified scan chain, a BIST test architecture is proposed that can detect and locate opens, SAFs, and all possible shorts in irregularly distributed ILVs. The BIST scheme for ILV fault detection and localization is illustrated in Fig. 2. The scheme has five components as follows: 1) BIST test controller; 2) ILV input scan chain; 3) ILV output scan chain; 4) ILV fault localization module; and 5) ILV fault-masking module; as well as two modes as follows: 1) functional mode, which will be presented in Section III-C and 2) test mode, which will be presented in Section III-E.

The BIST test controller consists of the finite state machine (FSM) in the bottom and top layers. The FSM is controlled by the testing pulse clk, which controls the BIST architecture through input signals to test the ILV according to the designed testing flow. The test flow is introduced in Section III-E.

The ILV input scan chain includes the bottom layer scan chain. Four tristate gates are controlled separately by different control signals. The tristate gates ensure the smooth transmission of both function and test signals in the BIST architecture's function and test modes.

The ILV output scan chain includes the top-layer scan chain, the same tristate gates in the input module, and the XNOR gate. The XNOR gate compares the ILV output with the top-layer scan-chain output. Since both the top-layer and bottom-layer scan chains transmit the same test patterns, comparing their inputs and outputs can detect ILV faults.

The ILV fault localization module consists of an encoder and the 2:1 MUXs. The encoder takes the output of the XNOR gate and generates two signals: Lab (to indicate whether there is a fault in the ILV after the scan chain has been shifted) and Loc (to indicate the location of the faulty ILV). The control signal of the MUX is the masking signal.

The ILV fault-masking module comprises a decoder, two rows of D flip-flops, and the 2:1 MUXs. The decoder receives the Loc from the encoder, which is sent to the D-trigger, generating the masking signal to locate multiple faults, while preventing repetitive location of already located fault ILVs.

B. Improved Scan Chain

The improved scan chain is shown in Fig. 3(b). Compared with the conventional scan chain, a DEMUX controlled by

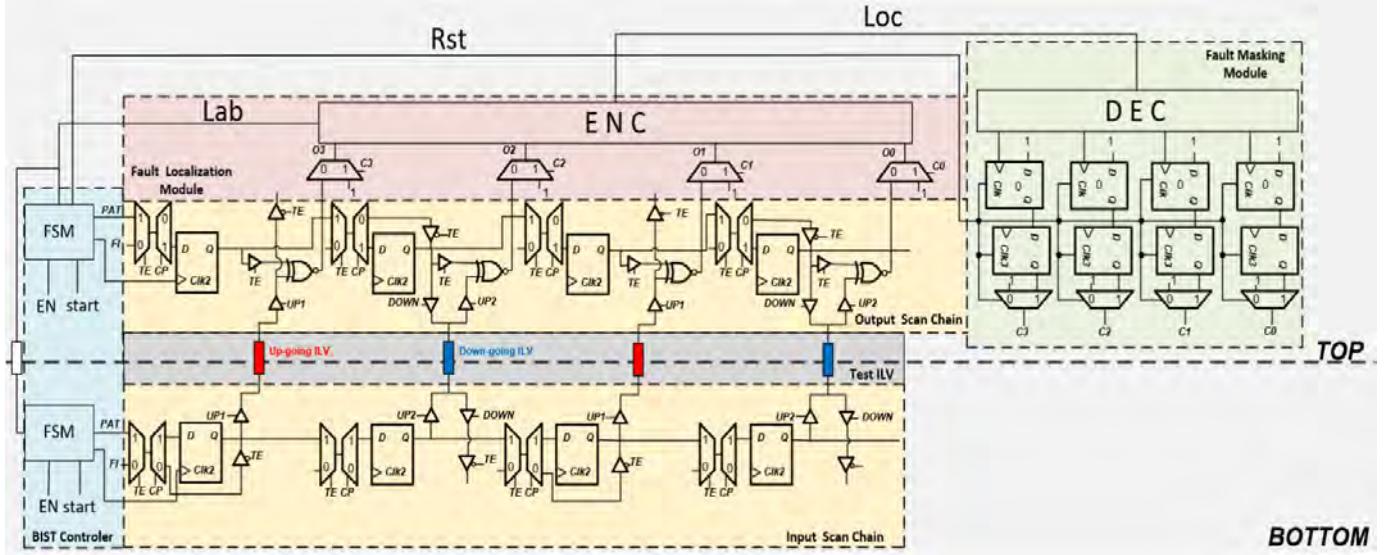


Fig. 2. Proposed BIST architecture.

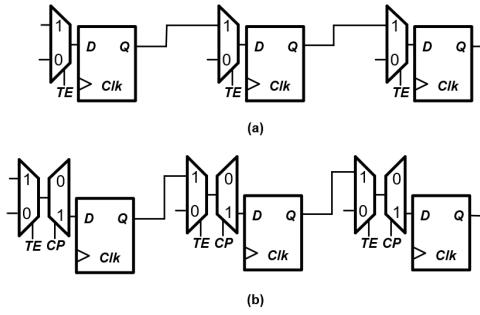


Fig. 3. (a) Traditional scan chain. (b) Improved scan chain.

the control signal CP is added at the input of each scan cell. During the scan test, the signal CP is always 1. When TE=1, the improved scan chain is in shift mode to transmit the test signal; when TE=0, the improved scan chain is in capture mode to capture the test response of the functional circuits into the scan cell.

C. Two Modes

This BIST architecture has two modes: functional mode and test mode. In the functional mode ($TE = CP = 0$), for the upgoing ILV: the control signal $UP1 = 1$; for the downgoing ILV: the control signal $UP2 = 1$ and $DOWN = 0$. The bottom function signal is generated by the bottom function circuit and transmitted to the top function circuit through the upgoing ILV, and the top function signal is generated by the top function circuit and transmitted to the bottom function circuit through the downgoing ILV. In the test mode ($TE = CP = 1$), for upgoing ILV: the control signal $UP1 = 1$; for downgoing ILV: the control signal $UP2 = 1$ and $DOWN = 0$. The bottom test signal is generated by the bottom FSM, enters the input scan chain, and is transmitted to the output scan chain through the ILV; the top test signal is generated by the top FSM and enters the output scan chain; the XNOR gate in the output scan chain outputs the comparison results and sent to the encoder.

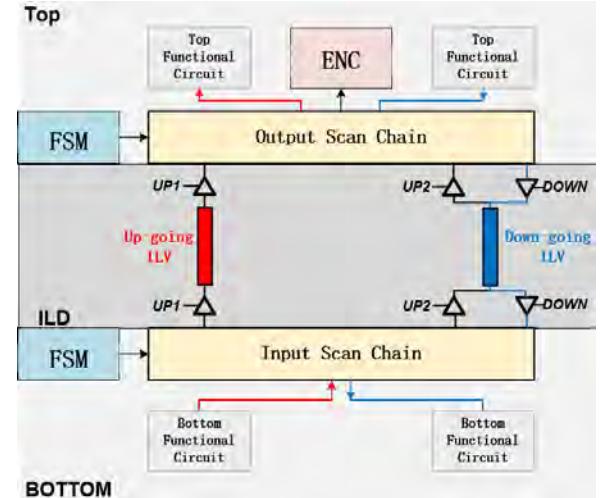


Fig. 4. Switching based on tristate gates to form corresponding signal transmission paths.

As shown in Fig. 4, by controlling the tristate gate, the function signal and the test signal can be transmitted normally, so that the short between the upgoing ILV and the downgoing ILV can be detected.

D. Detection of ILV Faults

The circuit model used in this scheme for testing ILV faults, including open, short, and SAFs, is illustrated in Fig. 5.

Fig. 5(a) illustrates the model for testing the SAF. When the ILV has a stuck-at-1 (stuck-at-0) fault, the output of the ILV is 1 (0), and after a certain shift in the scan chain, V_{in} is 0 (1); currently, V_{out} is 0, which indicates that a fault has occurred in the ILV under test. Therefore, this scheme can detect SAFs.

Fig. 5(b) illustrates the lumped circuit model for testing a resistive open. The on-state equivalent resistance of the tristate gate is denoted by R_{on} , C_{on} is the switching capacitance when the tristate gate is on, the equivalent resistance of the ILV

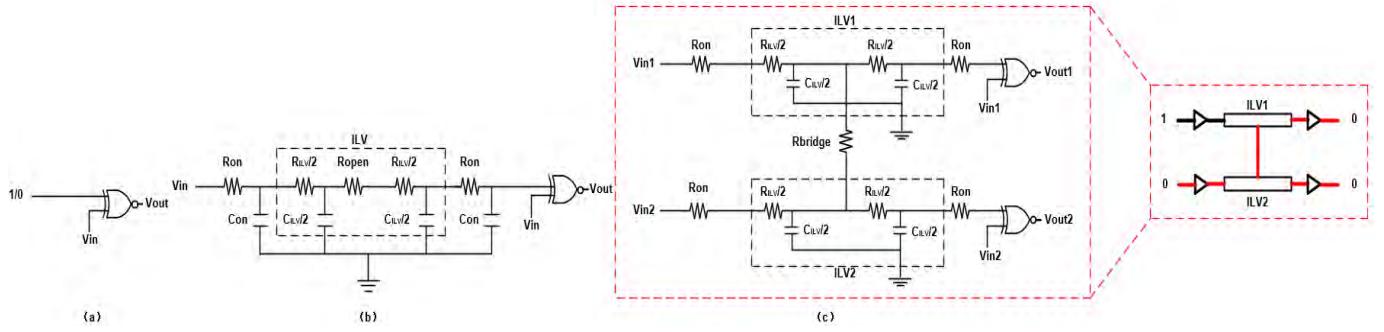


Fig. 5. ILV test models: (a) SAF, (b) open, and (c) short.

is denoted by R_{ILV} , C_{ILV} is the parasitic capacitance from the ILV to the substrate, which is divided into two equivalent parts by the open, and the open equivalent resistance is denoted by R_{open} . For a given test clock period T_{clk} , the RC delay D from V_{in} to V_{out} is calculated using the Elmore delay model for this model, which can be expressed as follows:

$$D = \ln 2 \times (3R_{on}C_{on} + R_{on}C_{ILV}) + \ln 2 \times \left(\frac{R_{ILV}}{2} \cdot \frac{3C_{ILV}}{2} + R_{ILV}C_{on} \right). \quad (1)$$

The condition for detecting open is $D + \Delta XNOR > T_{clk}$, where $\Delta XNOR$ is the fixed delay of the XNOR gate. Thus, when T_{clk} is modified, the range of detection of open changes. V_{in} is shifted through the scan chain during a certain test clock cycle to get 1. When the opening occurs in the ILV, its output is passed to the XNOR gate, and V_{out} is 0, which indicates that the ILV under test is faulted. Therefore, this scheme can detect open.

Fig. 5(c) illustrates the lumped circuit model for testing a resistive short, and R_{bridge} is the short equivalent resistance. After a certain shift in the scan chain, two neighboring ILVs get inputs 1 and 0. HSPICE simulation results show that the ILV that gets input 0 is the aggressor in a pair of short ILVs, while the ILV that gets input 1 is the victim, corresponding to the XNOR gate output is 0, which indicates that the victim ILV is faulted. Therefore, this scheme can detect short.

E. Test Flow

The testing flow for the proposed BIST architecture is as follows.

When the BIST test is not enabled, the M3D IC operates normally, the BIST architecture is in functional mode, and the BIST test controller output signal $RST = 0$ ensures that the masking signal in the ILV fault masking module is initially set to 1, so that the Lab is initially set to 0. At the same time, all the D flip-flops in the BIST architecture are initialized, including the D flip-flops in the two scan chains of the bottom and top layers, and two rows of D flip-flops in the fault masking module are prepared for the ILV test in the BIST test mode.

When the BIST controller receives the EN signal, $RST = 1$, it starts generating the test pattern for ILV testing, ensuring that only one ILV in the scan chain always gets 1. When the BIST test controller receives the start signal, the BIST architecture is

Truth Table for ENC							Truth Table for DEC						
O_3	O_2	O_1	O_0	$Lab[1]$	$Lab[0]$	Loc	Loc	$Lab[1]$	$Lab[0]$	S_3	S_2	S_1	S_0
1	1	1	1	X	X	0	0	X	X	0	0	0	0
1	1	1	0	0	0	1	1	0	0	0	0	0	1
1	1	0	X	0	1	1	1	0	1	0	0	1	0
1	0	X	X	1	0	1	1	1	0	0	1	0	0
0	X	X	X	1	1	1	1	1	1	1	0	0	0

Fig. 6. Truth table for ENC and DEC.

in test mode, signal $TE = 1$, $CP = 1$, and the scan chain enters the shifting state. At the same time, the BIST test controller generates the test pulse $Clk2$ for the scan-chain shift or the test pulse $Clk3$ for the transmission of the marking signal, depending on the current feedback signal Lab (Lab is initially 0). Since the Lab signal needs to be fed back to both the top and bottom FSMs, an additional ILV is required to send the feedback signal Lab to the bottom FSM.

The scan chain is shifted under the control of the pulse $Clk2$. Every time it is shifted, the XNOR gate in the ILV output scan chain outputs the comparison results to the encoder. When the output of the XNOR gate is 1, it represents that the ILV inputs and outputs are consistent, indicating no failure of the corresponding ILVs detected after this shifting. On the other hand, when the output of the XNOR gate is 0, the ILV inputs and outputs are inconsistent, indicating a fault in the ILV being detected after this shift.

In the case of four ILVs, when the output of the four XNOR gates is 1111, no fault is detected after this shift. The encoder truth table is shown in Fig. 6, with the output $Lab = 0$, indicating the absence of any faults. However, if the output $Lab = 1$, a faulty ILV has been detected. At the same time, Loc is generated to locate the faulty ILV. The number of Loc bits is two when there are four ILVs.

In the process of fault localization by the encoder, Lab can only localize a faulty ILV due to the existence of a scan chain shifted once and multiple ILV faults being detected, so it is necessary to send Lab from the output of the encoder to the decoder to mask the faulty ILV that has already been localized.

Example 1: Taking four ILVs as an example, assuming after a shift, the outputs of the XNOR gate correspond to the inputs of the encoder, resulting in 1100 (indicating that O_1 and O_0 are faulty), and with $Lab = 1$ and $Loc = 01$, it indicates that O_1 has been located. To locate O_0 as well, it is necessary to ensure that the scan chain does not shift. This can be achieved

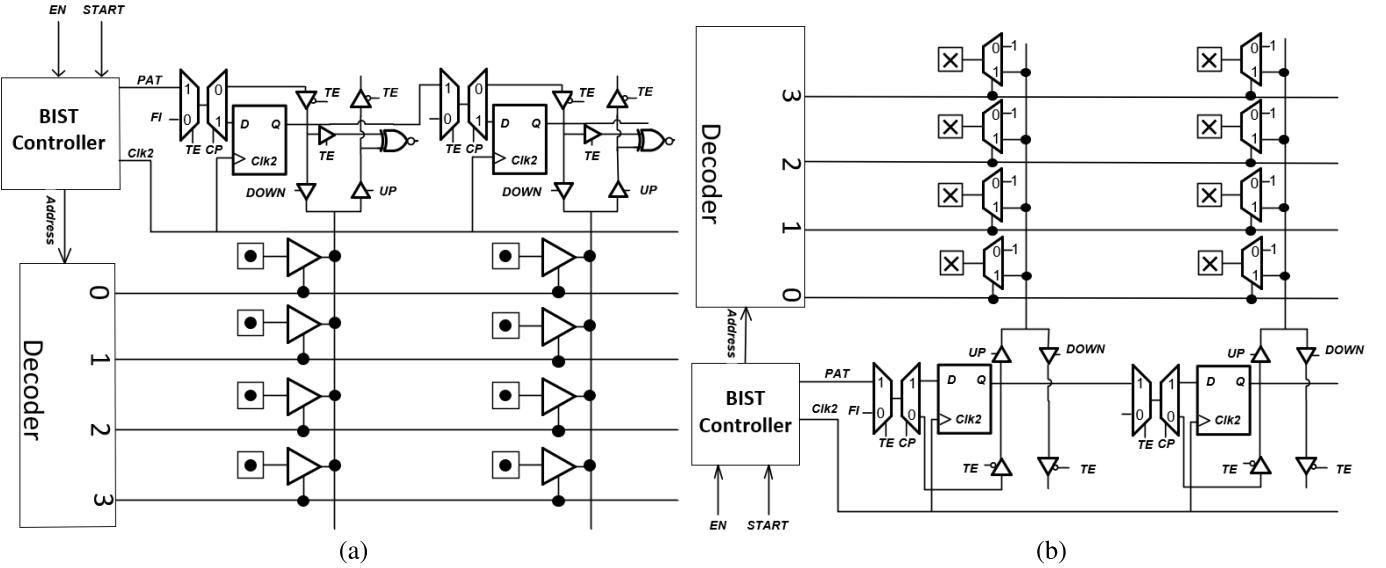


Fig. 7. Grouping test architecture. (a) Top architecture. (b) Bottom architecture.

by feeding back $\text{Lab} = 1$ to the BIST testing controller, which will stop generating the test pulse $\text{Clk}2$ and start generating the test pulse $\text{Clk}3$. At the same time, the Loc signal is sent to the decoder, which generates 0010 according to the truth table of Fig. 5, and the third D flip-flop in the first row gets a rising edge signal and, thus, outputs 1. The third D flip-flop in the second row, under the control of the test pulse $\text{Clk}3$, sends 1 to the control terminal of the third MUX of the encoder input, which masks the result of the comparison of the XNOR gate at this position, and the encoder input changes from 1100 to 1110; the O1 is masked; at this point, $\text{Lab} = 1$, $\text{Loc} = 00$, and O0 has been located. In the same step, O0 is masked, and the encoder input changes from 1110 to 1111; currently, $\text{Lab} = 0$, indicating that all faults are detected and masked; Lab is fed back to the FSM, stopping the generation of the test pulse $\text{Clk}3$ and generating $\text{Clk}2$ to restart the shifting of the scan chain.

Example 2: Taking four ILVs as an example, if O1 has a stuck-at-1 fault, the fault will be detected during the first, second, and fourth shifts of the scan chain. Our goal is to locate O1 during the first shift and avoid redundant locating in subsequent shifts. Therefore, when a fault is detected in any of the ILVs, we need to ensure that the corresponding position's masking signal remains set to 1 consistently. The first row of D flip-flops in the proposed scheme performs this function. Since Lab is 0, the decoder outputs 0 and sends it to the clk terminal of the first row of the D flip-flop. When the ILV fault is first detected, the decoder outputs 1. As a rising edge signal is obtained, the first row of D flip-flops will be permanently set to 1. During the subsequent scan-chain shifts, the faulty ILV will always be masked after localization, thus reducing the test time.

IV. GROUPING TEST ARCHITECTURE

A. Improved BIST Architecture

The number of ILVs in M3D IC is generally large, and considering that the length of the scan chain may not be able

to be matched, to save test overheads, we consider improving the test structure for grouping tests. Grouping test is usually categorized into parallel and serial test. For parallel test, some complex issues arise, including high test power consumption and the inability to detect block-to-block short faults when testing multiple ILV blocks in parallel. To fully consider all possible short faults in ILVs, the serial test is chosen, and only one group of ILVs is selected for each test, which avoids the problem of high power consumption and also detects block-to-block short faults. In general, serial test increases the test time, but M3D ICs usually operate in high-frequency environments where a single test of a group of ILVs takes less time, so the increase in test time is acceptable.

The supplementary designed BIST architecture for group testing of ILVs by multiplexing the architecture in III is proposed, as shown in Fig. 7. The architecture adds an address counter and an address decoder. The address counter is used to generate the address code, which is sent to the address decoder. The output of the decoder is used as a selection signal for the ILV group: a 2:1 MUX selection signal in the bottom architecture, and the control signal for the tristate gate in the top architecture are used to select a particular group of ILVs for testing. The selected group of ILVs has its inputs generated by the bottom scan chain, and its outputs are transmitted to the XNOR gates in the top scan chain, while the unselected group of ILVs always has its inputs at 1 and the tristate gates block its outputs. The address counter and the FSM in III form the new BIST test controller.

B. ILV Grouping Algorithm

Although the test structure selects only one group of ILVs for testing at a time, for each group of ILVs, a complete and independent test structure is still required. By connecting each ILV to the test structure, the wire overhead increases significantly. To solve this problem, we introduce a block partitioning algorithm. The distribution of interlayer interconnections of 3D ICs includes uniform distribution in memory

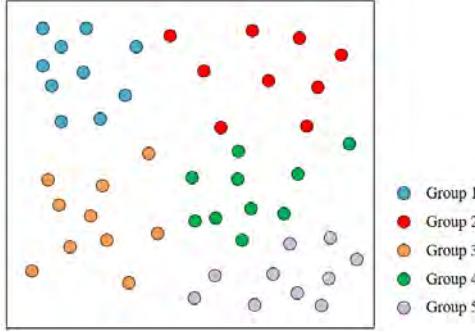


Fig. 8. Grouping using the K -means algorithm.

and nonuniform distribution in SOC. The method of dividing blocks for uniform distribution is simple, and each block can be divided evenly. However, due to the immature fabrication process of M3D, the distribution of ILVs is nonuniform and it is difficult to divide them into suitable blocks.

To provide a division method for the grouping test, clustering algorithms are used. A clustering algorithm is a commonly used analytical method in data mining and machine learning, and the algorithm can be used to group the clusters. The k -means algorithm is a suitable method for the average grouping of ILVs, where k is the number of clusters. The ILVs in each cluster are grouped closer to each other, which minimizes the length of the control wires in the test structure used by the address decoder for selecting a group of ILVs to be tested to improve the performance and reduce the wire overhead. For the nonuniform distributed ILVs, the position of each ILV is represented with a set of coordinates (x, y) . The k -means algorithm is as follows.

- 1) K ILVs are randomly selected from the ILVs as the initial block centers.
- 2) Calculate the Euclidean distance from each ILV to each initial center. Each ILV is assigned to the closest initial block center under the constraint that the number of ILVs in each block cannot exceed the number of scan cells.
- 3) After dividing the blocks, recalculate the initial block centers for each group. The block center is updated with the average of ILVs in each block.
- 4) Partition the ILVs into clusters based on the updated centers.
- 5) Repeat steps 2)–4) until none of the ILVs change their block.

Fig. 8 illustrates an example of grouping using the K -means algorithm.

C. Improved Test Flow

The complete test flow for the improved BIST test architecture is shown in Fig. 9.

The specific testing flow is as follows.

- 1) When ILV detection is not performed, the BIST test architecture remains in normal function mode ($TE = 0$ and $CP = 0$). The ILV functions normally, the initialization signal RST is kept at 0, and all D flip-flops are controlled to be set to 0. The initial masking signal is

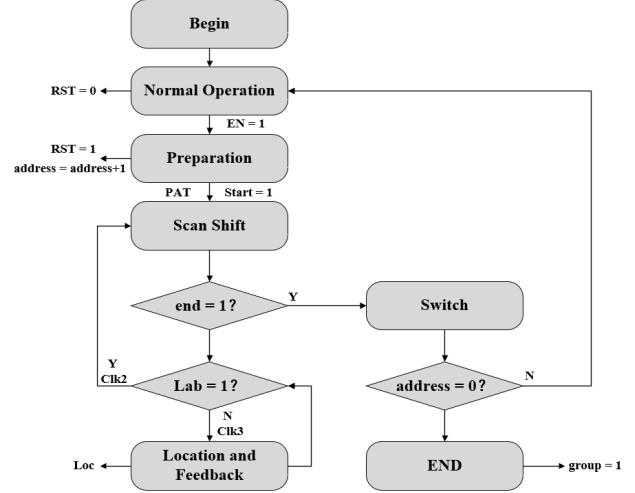


Fig. 9. Test flow.

also controlled to be 1 to ensure that the detection signal Lab is initially 0 in the function mode.

- 2) *Step 1—Preparation State:* The BIST test controller receives the signal $EN = 1$ to make $RST = 1$. The BIST controller generates the address code through the address counter and sends it to the address decoder in Fig. 8, which controls the selection of the ILV grouping for the test. At the same time, the FSM starts generating the test pattern PAT , which ensures that the initial test pattern of the scan chain is “1000...”
- 3) *Step 2—Scan Shift State:* The controller receives a signal: $start = 1$, generates the signal $TE = 1$, $CP = 1$, and the BIST architecture is in test mode. As Lab is initially 0, it generates the test pulse signal $Clk2$ used for scan-chain shifting and controls the two scan chains of the bottom and top layers to enter the shifting state.
- 4) *Step 3—Location and Feedback State:* The specific test flow for ILV fault localization and masking is the same as in Section III-E.
- 5) *Step 4—Switch State:* After the “1” in the scan chain has traversed each ILV, it is output and fed back to the FSM in the BIST controller. The FSM generates the end signal, indicating that this group of ILVs has been tested. At this point, the BIST architecture returns to regular operation. The scan chain and the two rows of D flip-flops are initialized, and the masking signal is cleared. When the EN signal is received again, the address counter can generate the next address code to test the next group of ILVs.
- 6) *Step 5—End State:* When the address counter counting is completed and the address returns to zero, a feedback signal $group = 1$ is generated, which represents that all groups of ILVs have been tested. The test is finished, and the BIST architecture returns to normal operation.

Fig. 10 shows the BIST controller used in this scheme.

D. Analysis of Crosstalk Fault Detection

Currently, the M3D fabrication process is still immature, so we expect the problem of ILV coupling-induced

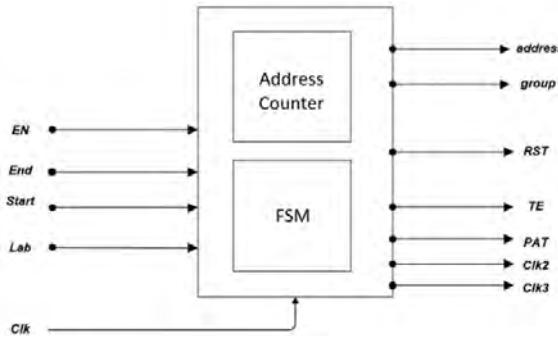


Fig. 10. BIST controller.

crosstalk noise in ILV-based M3D ICs to be similar to that of TSVs in conventional 3D IC designs, which are subject to coupling-induced crosstalk faults [25], [26].

We classify a pair of ILVs where coupling occurs between victim and aggressor, and note that the identity of the victim and aggressor may switch during different cycles of the testing process. Crosstalk faults due to coupling between neighboring ILVs are classified as glitch and delay faults. A glitch is when the victim propagates a signal $s \in \{0, 1\}$, while the aggressor is experiencing a signal rise or fall, which leads to an abnormal circuit behavior; a delay fault is when the victim and the aggressor all experience the signal rise or fall, which leads to incorrect logic propagation.

Depending on the reasons for the generation of glitch and delay faults, the set of test patterns p is required when only crosstalk faults occurring between a pair of ILVs are considered, and the same ILV may act in different roles in different cycles of the detection

$$p = \{00, 10, 01, 00\}$$

where the i th test pattern $p_i = I_0 I_1$, where I_0 is the propagated signal of the left ILV in a pair of ILVs and I_1 is the propagated signal of the right ILV.

When the test pattern transforms, i.e., $p_{i-1} \rightarrow p_i$, it includes the following three cases.

- 1) The signal of the left ILV remains fixed, while the signal of the right ILV undergoes a transition.
- 2) The signal of the left ILV undergoes a transition, while the signal of the right ILV remains fixed.
- 3) The signal of the left ILV undergoes a transition, while the signal of the right ILV also undergoes a transition.

Thus, crosstalk faults due to coupling can be induced and detected at p_i moments.

As an example, to detect four ILVs, we use a test pattern initially with $PAT = 1000$, and in subsequent test cycles, the test patterns are changed using scan-chain shifts, resulting in a set of test patterns of q

$$q = \{0000, 0100, 0010, 0001, 0000\}$$

where the i th test pattern $q_i = O_0 O_1 O_2 O_3$, where O_0 , O_1 , O_2 , and O_3 represent the input signals of each of the four ILVs.

TABLE I
ILV MODEL PARAMETERS

Parameter	Parameter Interpretation			
	Unit	Description	Value	Material
L	nm	ILV length	300	Tungsten
r_{ILV}	nm	ILV radius	25	Tungsten
t_{TiN}	nm	Insulating layer thickness	0.5	Titanium nitride
h_{IMD}	nm	IMD height	150	Silicon dioxide
h_{Si}	nm	Si height	50	Si
h_{ILD}	nm	ILD height	100	Silicon dioxide

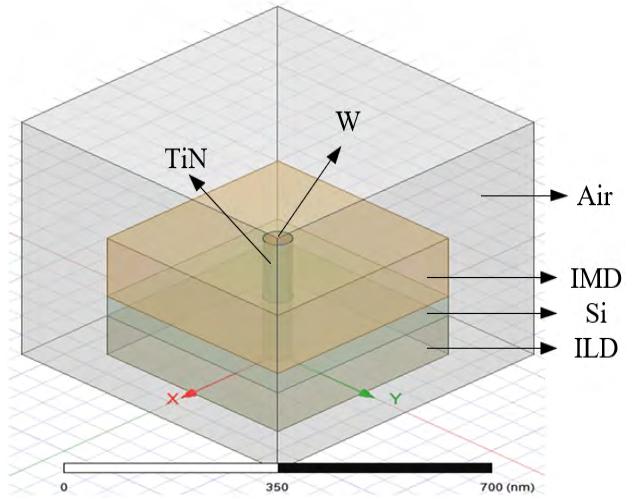


Fig. 11. ILV physical model.

For any two of these neighboring ILVs, the set of input signals will contain p . Take $O_1 O_2$ as an example

$$q_{1,2} = \{00, 10, 01, 00, 00\}.$$

Take $O_2 O_3$ as an example

$$q_{2,3} = \{00, 00, 10, 01, 00\}.$$

Either test pattern set $q_{1,2}$ or $q_{2,3}$ satisfies

$$p \subseteq p_{12}$$

$$p \subseteq p_{23}.$$

A detection method that induces the occurrence of crosstalk faults by generating a specific test pattern is proposed in [3]. It is shown that the designed test structure can also be used to characterize and detect crosstalk faults (glitch and delay faults) individually.

V. EXPERIMENTAL RESULTS

A. Experimental Setup

We utilized the Nangate 45-nm open-cell library in HSPICE to assess the fault detectability and location ability of the BIST structure. Our test scenario comprised four ILVs, and four test clock frequencies are considered: 0.5, 1, 2, and 4 GHz. In each of these ILVs, we injected various levels of open, short, and SAFs. The supply voltage is 1 V.

In addition, we assessed the detectability of short occurring within the ILVs between groups following the grouping of ILVs. To verify the correctness of the test flow of the designed

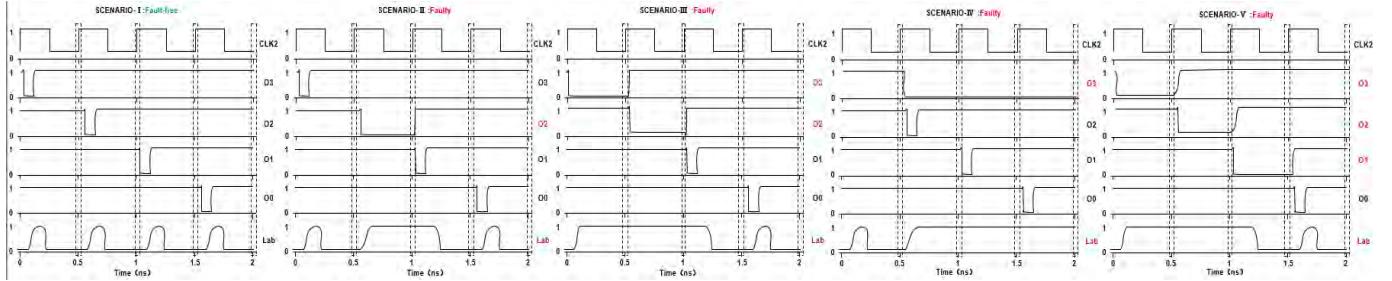


Fig. 12. Multiple scene detection results.

BIST architecture, we evaluated the designed BIST controller through simulation in Vivado.

We use the finite-element analysis software Q3D to physically model the ILV, to extract the resistance R_{ILV} and capacitance C_{ILV} corresponding to the fault-free ILV. The specific parameter values of the model are shown in Table I, and the model is shown in Fig. 11. The ILV model is cylindrical, its conductive metal material is tungsten, the insulating layer is TiN, and the ILD and the metal dielectric (IMD) are silicon dioxide. An air cavity is added at the periphery of the model.

B. ILV Fault Detectability

Since stuck-at-0 fault and open have an equivalent effect on the output of the ILV (when input 1 is provided, the output of the ILV will be 0 regardless of whether the ILV has a stuck-at-0 fault or an open circuit fault), we only consider injecting opens, shorts, and stuck-at-1 faults for fault detection. The following scenarios were selected to verify the detectability of the fault detection module in our designed BIST architecture for ILV faults at a test frequency of 2 GHz: in the first scenario, no faults are injected. In the second scenario, we randomly inject a hard open ($10 \text{ M}\Omega$). In the third scenario, we randomly inject a hard short (1Ω). In the fourth scenario, we randomly inject a stuck-at-1 fault. In the fifth scenario, we randomly inject a resistive open ($35 \text{ K}\Omega$) and a resistive short ($5 \text{ K}\Omega$). The test result is determined by the output signal Lab. The scan chain is shifted four times, and when $\text{Lab} = 1$, it indicates the presence of a faulty ILV in that shift; when $\text{Lab} = 0$, it indicates the absence of a faulty ILV in that shift. The test result is shown in Fig. 12, which demonstrates that $\text{Lab} = 0$ only in the case of no faults (Scenario 1). In the other scenarios, the Lab changes to 1 during at least one test cycle when faults are injected, indicating the presence of a fault in that group of ILVs, and the results validate the capability of the designed BIST architecture to detect faults.

Table II shows the detection range of open and short at different test frequencies. At a test frequency of 2 GHz, we can detect resistive open with a minimum of $34 \text{ K}\Omega$ and resistive short with a maximum of $10 \text{ K}\Omega$.

C. ILV Fault Location Ability

Fault localization in the BIST architecture is based on the fault localization and masking module. We selected Scenarios II and III in B to conduct HSPICE experiments on the

TABLE II
IMPACT OF TEST FREQUENCY ON OPEN AND SHORT DETECTION RANGE

Frequency(GHZ)	$R_{o,min}(\Omega)$	$R_{s,max}(\Omega)$
0.5	130k	10k
1	68k	
2	34k	
4	17k	

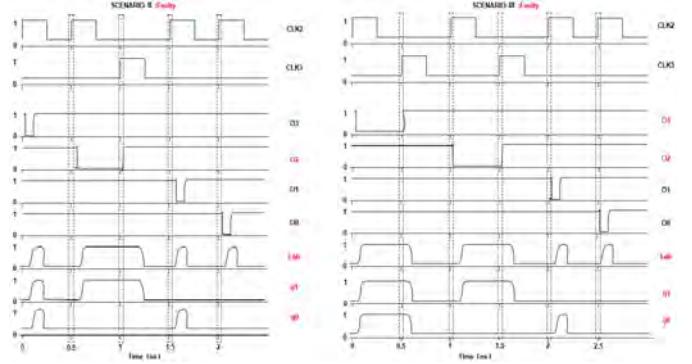


Fig. 13. Multiple scene detection and location results.

location ability of the BIST architecture at 2 GHz. The results are presented in Fig. 13. In Scenario II, $\text{Lab} = 1$ was detected after the second scan-chain shift, while $q1q0 = 10$, indicating that a fault had occurred in O2. A total of five test cycles equivalent to 2.5 ns were consumed to determine the location of this fault. In Scenario III, $\text{Lab} = 1$ was detected after both the first and second scan-chain shifts, corresponding to Loc ($q1q0 = 11, 10$), showing that faults had developed in O3 and O2, and a total of six test cycles corresponding to 3 ns were used to localize these faults. We can obtain the test time t as follows:

$$t = \frac{1}{f_{\text{test}}} \times (N_{ILV} + N_{\text{fault}} + N_{\text{group}}) \quad (2)$$

where f_{test} is the test frequency, N_{ILV} is the number of ILVs, N_{fault} is the number of faulty ILVs, and N_{group} is the number of ILV groups. N_{group} is added, because each group of ILVs requires an additional test cycle to move the test pattern in the scan chain out of the scan chain to generate the end signal, which means that this group of ILVs has been tested.

It can be seen that the test time is proportional to the number of faulty ILVs, since for every fault detected, a test cycle is required to locate it. In Example 2, we discussed the problem

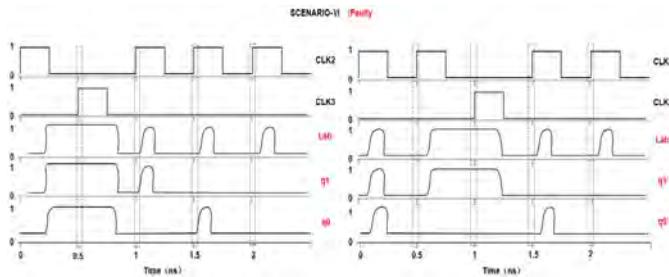


Fig. 14. Intergroup short detection and location.

of repeated fault detection precisely, because when the fault is repeatedly detected, multiple test cycles are spent to repeat the location, resulting in an increase in test time.

D. Intergroup ILV Short Detection

In experiments A and B, the injected short is intergroup short, meaning that the short occurs between two ILVs in a group of ILVs. To verify the detectability of intergroup ILV short, we injected intergroup short in the two groups of ILVs. The first group of ILVs is O3O2O1O0, and the second group of ILVs is O3'02'01'00'. We injected a short ($5\text{ K}\Omega$) between O3 and O2' and simulated it using HSPICE. The detection results are shown in Fig. 14. According to the detection results of the first group of ILVs, Lab = 1 is detected when the scan chain moves once, while q1q0 = 11, indicating that O3 has a fault. During the detection of the second group of ILVs, Lab = 1 is detected when the scan chain is moved twice, while q1q0 = 10 indicates that there is a fault in O2'. Thus, the designed BIST architecture can detect and locate intergroup short.

E. Experimental Validation of the BIST Controller

The BIST controller was verified through experiments using Vivado. A test frequency of 2 GHz was selected. Four ILVs were used, with O3 injected with stuck-at-1 faults and O2 injected with open faults ($35\text{ K}\Omega$). The experimental result is shown in Fig. 15 and explained as follows.

First, the BIST controller is in the normal operating state, the controller output is TE = 0 (CP = 0), Rst = 0, the BIST architecture is in functional mode, and Lab is initially 0. After receiving the EN signal, the BIST controller enters the preparation state and generates the test pattern PAT and address code. After receiving the start signal, the BIST controller enters the scan-chain shift state, and the BIST architecture is in the test mode; currently, TE = 1 (CP = 1). Since Lab is initially 0, the BIST controller first generates the test pulse Clk2, and the scan chain starts to shift.

- 1) In the first cycle, the scan chain is shifted for the first time. The four ILV inputs and outputs are 1000, and the result of the XNOR gate comparison is 1111, Lab = 0. This indicates that there is no faulty ILV in this shift, and the BIST controller continues to generate the test pulses Clk2 according to Lab = 0.

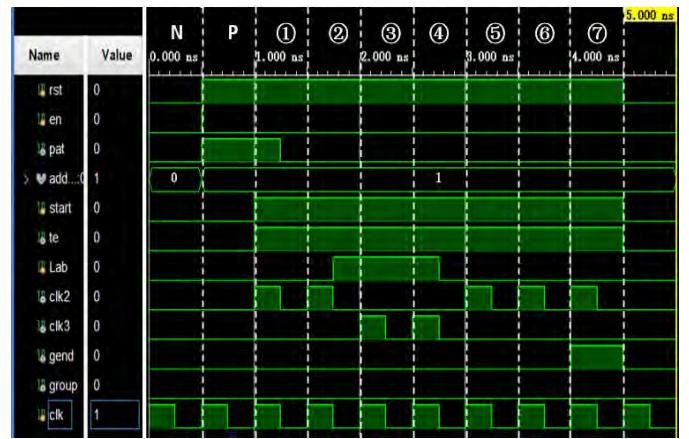


Fig. 15. Test result by using the Vivado.

- 2) In the second cycle, the scan chain is shifted for the second time, the four ILV inputs are 0100, the output is 1000, the result of the XNOR gate comparison is 0011, Lab = 1, indicating that there is a faulty ILV, the BIST controller stops the generation of Clk2 in the next test cycle according to Lab = 1 and starts the generation of Clk3, the scan chain maintains the current state, the BIST controller enters into the locate and feedback state, Loc = 11, and O3 is located.
- 3) In the third cycle, the fault masking signal of ILV3 is transmitted, the fault of ILV3 is masked, and the encoder input is changed from 0011 to 1011, but Lab is still equal to 1, because O2 is still faulted. The BIST controller still generates the test pulse Clk3 in the next test cycle according to Lab = 1. The BIST controller remains in the localization and feedback state with Loc = 10, and O2 is located.
- 4) In the fourth cycle, the fault masking signal of ILV3 is transmitted, the fault of ILV2 is masked, and the encoder input changes from 1011 to 1111; currently, both O3 and O2 are localized; therefore, Lab = 0. The BIST controller stops generating the test pulses Clk3 in the next test cycle according to Lab = 0 and instead generates Clk2, the BIST controller enters the scan-chain shift state, and the scan chain starts shifting again.
- 5) In the fifth and sixth cycles, the scan chain is shifted for the third and fourth time, the four ILV inputs are 0010 and 0001 in turn, the outputs are 1010 and 1001 in turn, and the results of the XNOR gate comparisons are 0111 and 0111 in turn, which can detect that a fault has occurred in the O3. However, since O3 has been located and masked in the second test cycle, Lab is equal to 0 in both cycles, the BIST controller continues to generate Clk2, and the scan chain continues to shift.
- 6) In the seventh cycle, the scan chain is shifted for the last time, and the "1" in the scan chain is shifted out and fed back to the BIST controller, so that the end signal is equal to 1, and the BIST controller enters the switching state, which means that the first group of ILVs has been tested. Since the address counter is not equal

TABLE III
COMPARISON OF 3D IC TEST STRUCTURES FOR INTERLAYER INTERCONNECT FAULT DETECTION AND LOCALIZATION

Criteria	Proposed Method	Method In [4]	Method In [2]	Method In [27]	Method In [28]	Method In [19]
Fault detection	Yes	Yes	Yes	Yes	Yes	Yes
Fault localization	Yes	Yes	No	Yes	Yes	No
Fault detection time(cycles)	N	3t	2	$\frac{N}{N_{ch}}$	$\frac{N}{N_{ch}}$	SC
Localization time(cycles)	k	3k	-	N_{ch}	N_{ch}	SC
Localization granularity	1	3	N	N_{ch}	N_{ch}	-
Detectable faults	Short/Open/SAF	Short/Open/SAF	Neighbourhood Short/Open/SAF	Short/Open	Short	-
Intergroup bridge faults	Yes	-	-	No	No	-
Number of BIST engines	1	m	-	1	1	-

$$t = \left\lceil \frac{N}{mc} \right\rceil + t_s; SC = [\log_2 N] \cdot (2N + 1) + 2N$$

to 0, in the next test cycle, the BIST controller returns to the normal operating state, TE = 0 (CP = 0), and Rst = 0, in preparation for the next group of ILV tests.

F. Fault Detection and Localization Features

We compare the fault detection and localization features of our proposed test structures with similar related works. Table III summarizes the key features of ILV-BIST [2], [4] for test structures to detect ILVs, postbond test frameworks proposed for TSVs in [27] and [28], and the IEEE 1838 Standard on die-wrapper-based 3D IC testing [16]. In [27], the N TSVs are divided into multiple test groups based on their distribution in the circuit layout, and each group contains N_{ch} (≈ 10) TSVs.

Assuming that the equal number of ILVs in each test group is N_{ch} , $((N/N_{ch}))$ is the number of test groups formed, and at the time of testing, $((N/N_{ch}))$ groups are tested in parallel, and N_{ch} ILVs in each group are tested at the same time to obtain the pass/fail status of that test group.

For the proposed BIST structure, one test group is selected for testing at a time. The number of faulty ILVs in the test group is denoted by k ($\leq N_{ch}$), and when a faulty ILV is detected, it is immediately tested. Note that the localization time here refers to the number of test cycles required to localize to a specific ILV when a fault is detected in a group of ILVs. Thus, for the proposed ILV-BIST, the localization time is 1. For [27] and [28], the localization time is equal to N_{ch} ; since once a faulty ILV is detected in a concurrent test group, it takes N_{ch} test cycles to locate faults in sequence for all ILVs in the group.

For the test structure proposed in [4], m is the Pareto-optimum number of BIST engines, c is the number of ILVs tested simultaneously by a single test engine, and t_s is the number of test iterations required to detect potential bridging failures between ILVs. In [2], the XNOR and XOR networks were used to test a set of ILVs, giving the pass/fail status of the set after two test cycles, but it was not possible to locate the exact location of a particular faulty ILV.

In addition to the fault detection and location functions, we consider adding redundant ILVs to the test structure for repair. The mainstream repair schemes include shift repair and replacement repair. Shift repair selects the ILV adjacent to

TABLE IV
COMPARISON OF ILV FAULT-TOLERANCE SCHEMES

Fault Tolerance Scheme	Number Of Redundant ILVs	Fault Tolerance		
		Open Fault	Short Fault	SAF
Shift Repair	200	Yes	Yes	Yes
Replacement Repair	1000	Yes	No	No

the ILV under test for replacement when the ILV fails. If the adjacent ILV also fails, it continues to shift until additional redundant ILVs are added. Replacement repair selects the corresponding redundant ILV for replacement when the ILV fails.

We have two schemes for the types of repairs. One uses shift repair based on the proposed ILV grouping test structure to add a redundant ILV group, including an upgoing ILV and a downgoing ILV, for each ILV test group. The other scheme directly uses replacement repair to set up redundant ILVs for each ILV without adding additional test structures. Assuming $N = 1000$ and $N_{ch} = 10$, both schemes are evaluated in terms of the number of redundant ILVs and fault-tolerance effect. Table IV shows that the number of redundant ILVs in the shift repair scheme is lower than in the replacement repair scheme. Considering the fault-tolerance effect, the faulty ILVs can be detected and located using the ILV grouping test structure and, thus, are fault-tolerant for open, short, and SAF faults. For the ILV replacement repair scheme, although the hardware overhead is very low due to the lack of additional test structures, more redundant ILVs have been added. It can be fault-tolerant for open faults, but not fault-tolerant for short and SAF faults.

VI. CONCLUSION

We propose the BIST architecture for ILV faults based on the scan chain in the active layer. It considers the length of the encapsulated scan chain in the active layer and groups the ILVs using the K-means algorithm. Each group of ILVs is tested sequentially using BIST, enabling the detection of opens, SAFs, all possible shorts of the ILVs, and localization of faulty ILVs. We also analyzed the detectability of the test structure for crosstalk faults and considered adding redundant ILVs to the test structure to achieve fault tolerance. We injected faults in multiple scenarios, and the effectiveness of the BIST

architecture in detecting various ILV faults was verified using HSPICE simulation results. The feasibility of the test flow was confirmed by analyzing the timing diagrams obtained by simulating the BIST controller using Vivado. This scheme allows for independent testing of ILVs by reusing the scan chain in the active layer and serves as an essential component of the M3D IC test flow.

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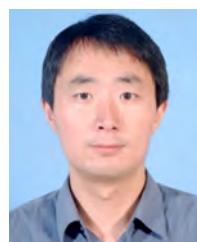
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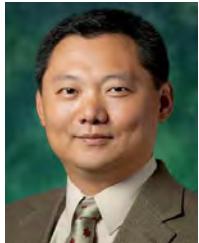
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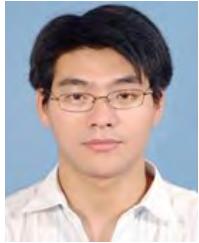
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