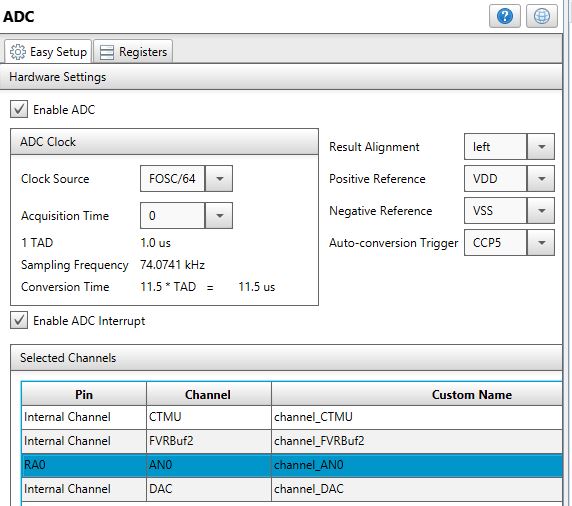
PB Control Box – Speed Pulse Application – PIC18F26K22 13Feb2020

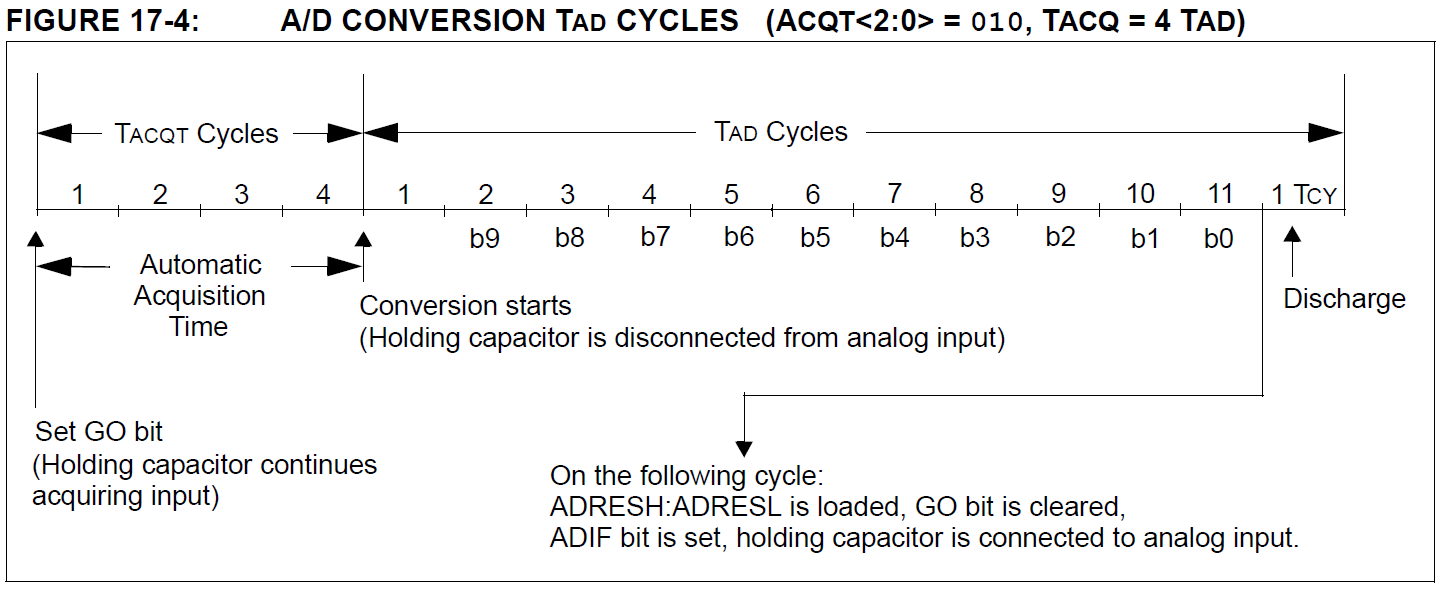
ADC

**Reference: Microchip datasheet DS40001412G**

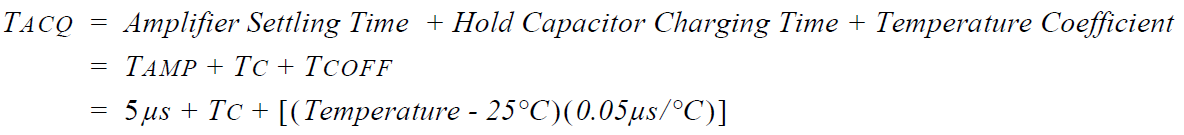
The chip is configured using MCC to TAD == 1 µs



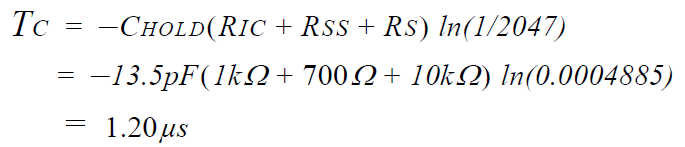
Due to relatively high input impedance and higher operating temperature range, the sampling rate of the ADC should be reduced. The calculations below estimate TACQ. As shown in the *Figure 17-4*, this quantity is the sampling period required to charge up the sampling capacitor prior to AD conversion:



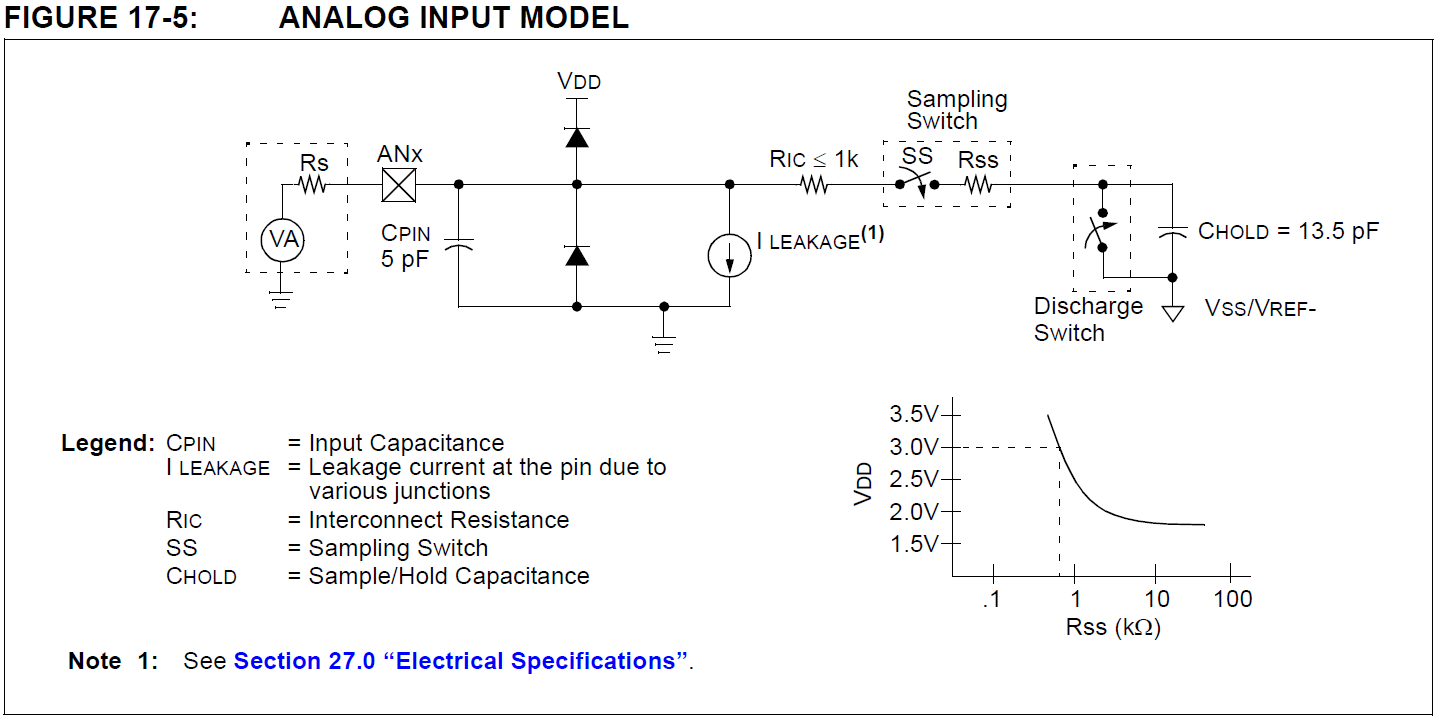
This equation is used as printed on the Microchip datasheet:



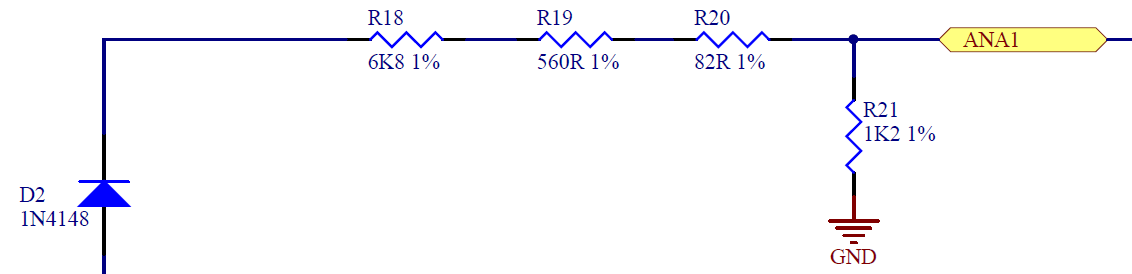
The middle term TC is given by



The third term in brackets RS is our source resistance (but not 10kΩ) as depicted in *Figure 17-5*.



In the BP Control Box application circuit as shown below



RS = 6800 + 560 + 82 = 7442 Ω (ignoring the effect of R21). Plug into second equation:

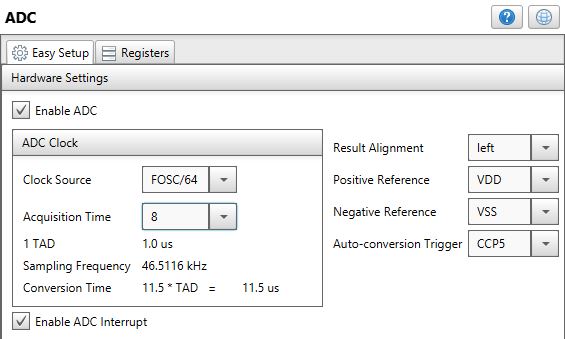
Obtains

It is desired to specify a higher operating temperature of 80˚C, substitute into first equation:

Obtains

This is our estimate value.

If the following nearest relaxed value TACQ == 8 is used, this setting corresponding to Sampling Frequency of 46.5116 kHz. Due to various latency, the achievable sampling interval will be slower.



When an ADC conversion has finished, the hardware will generate an interrupt. Code execution jumps to the ISR has interrupt latency. It will take a number of machine instructions to service the interrupt such as copying the ADC result to a local variable. Finally, the  bit needs to be set ‘1’ to start the next conversion.

An alternative is to set “Acquisition Time” field to ‘0’ as shown in the first screen capture. It such case TACQ is not inserted by hardware and this “wait time” is not automated. Our source code will cater for this “ADC sample and hold settling time” in each successive conversion.

As a side note, the PIC18F26K22 MCU is configured to run at PLL frequency of 64 MHz giving 64 / 4 == 16 MIPS. Within a time interval of 1 µs, 16 instructions would have been executed.

**Reference**:

<https://honda-tech.com/forums/tech-misc-15/92-95-speedometer-frequency-speed-specification-3237962/>

This forum suggested 4000 pulses per mile. Base on this, the following estimates 100 MPH:

Out sampling frequency 46.5116 kHz when divided by 111 Hz gives 418.60 times over-sampling. If this assumption is correct, the sampling rate is a comfortable one.