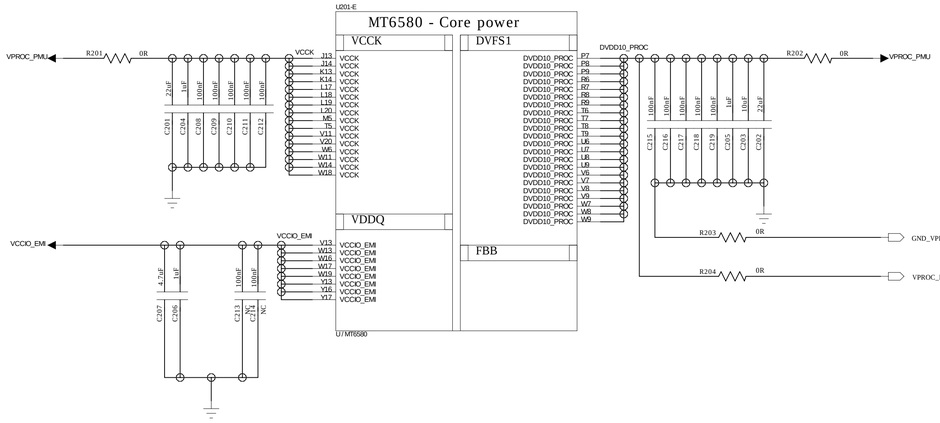
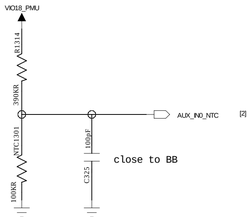
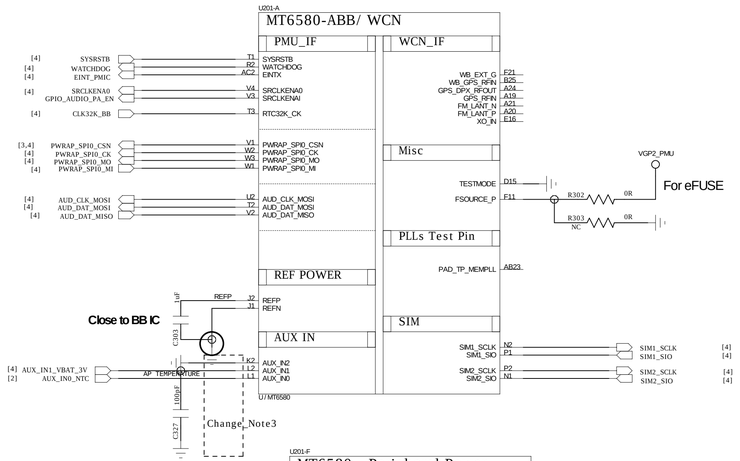
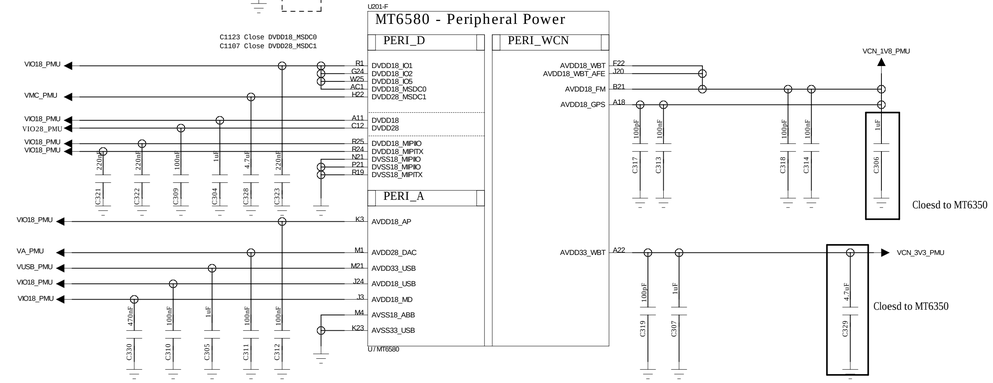
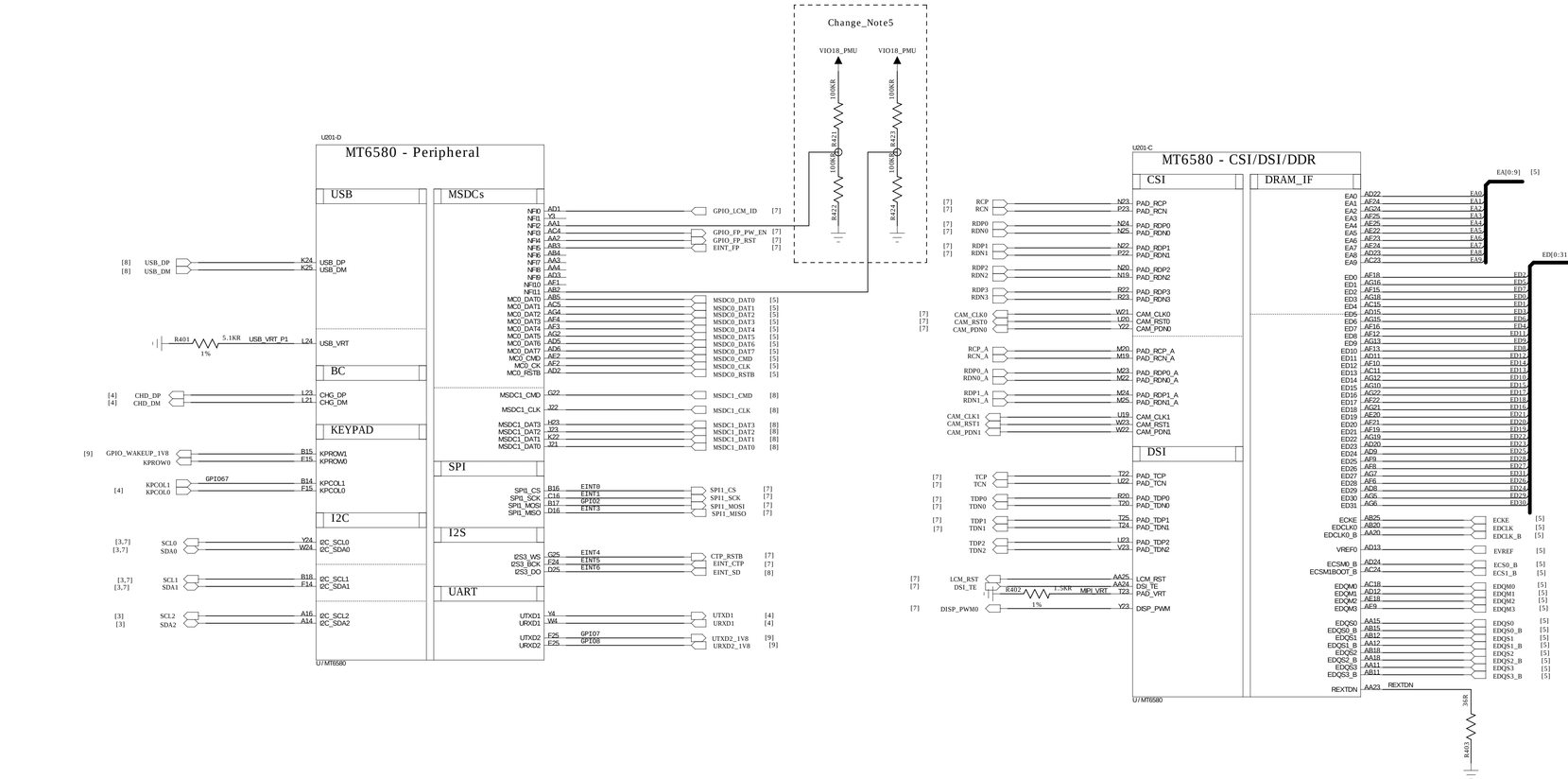

U201-E
MT6580 - Core power
VCCK
DVFS1
VDDQ
FBB
U7/MT6580
VPROC_PMU
R201
0R
VCCK
C201 22uF
C204 1uF
C208 100nF
C209 100nF
C210 100nF
C211 100nF
C212 100nF
VCCK J13 J14 K13 K14 L17 L18 L19 L20 M5 T5 V11 V20 W6 W11 W14 W18
DVDD10_PROC
P7 P8 P9 R6 R7 R8 R9 T6 T7 T8 T9 U6 U7 U8 U9 V6 V7 V8 V9 W7 W8 W9
C215 100nF
C216 100nF
C217 100nF
C218 100nF
C219 100nF
C205 1uF
C203 10uF
C202 22uF
R202
0R
VPROC_PMU
R203
0R
GND_VPROC_FB [4]
R204
0R
VPROC_FB [4]
VCCIO_EMI
C207 4.7uF
C206 1uF
C213 100nF
C214 NC
VCCIO_EMI V13 W13 W16 W17 W15 V13 V16 V17
U201-G
MT6580 - GND
GND
GND_WCN
GND
U7/MT6580
GND G23 J11 J12 K11 K12 L10 L11 L12 L13 L14 L15 L16 L22 M6 M10 M11 M12 M13 M14 M15 M16 M17 N6 N7 N8 N9 N10 N11 N12 N13 N14 N15 N16 N17 P10 P11 P12 P13 P14 P15 P16 P17 P18 R5 R10 R11 R12 R13 R14 R15 R16 R17 R18 T10 T11 T12 T13 T14 T15 T16 T18 T19 U5 U10 U16 V10 V12 V15 V24 V25 W10 W12 W15 W20 Y5 Y6 Y7 Y21 AA6 AA7 AA10 AA13 AA14 AA17 AA21 AA22 AB7 AB10 AB13 AB14 AB17 AB19 AB21 AB22 AB24
AVSS_CONN A25 B22 B23 B24 C19 C20 C21 C22 C23 C24 C25 D18 D19 D20 D21 D22 D23 D24 E18 E19 E20 E22 E23 E24 G17 G18 G19 G20 H16 H17 H18 J15 J16 J17 J18 K15 K16 K18
GND AC9 AC10 AC12 AC13 AC14 AC17 AC19 AC20 AC21 AC22 AD7 AD10 AD14 AD17 AD18 AD19 AD21 AD25 AE5 AE6 AE7 AE10 AE11 AE12 AE13 AE15 AE16 AE17 AE19 AF5 AF7 AF11 AF14 AF17 AF20 AF23 AG1 AG9 AG25 F23

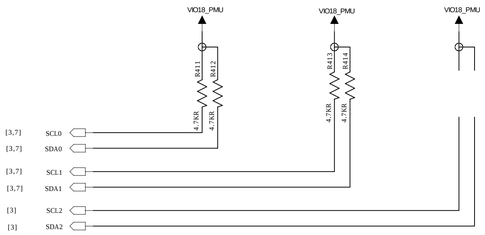






AVDD28_DAC change power source by "VA_PMU".





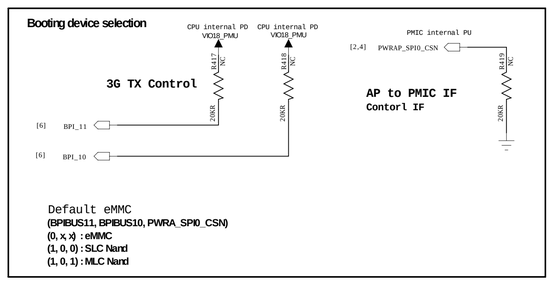
Schematic design notice of "12_BB_2" page.

Note 12-1:

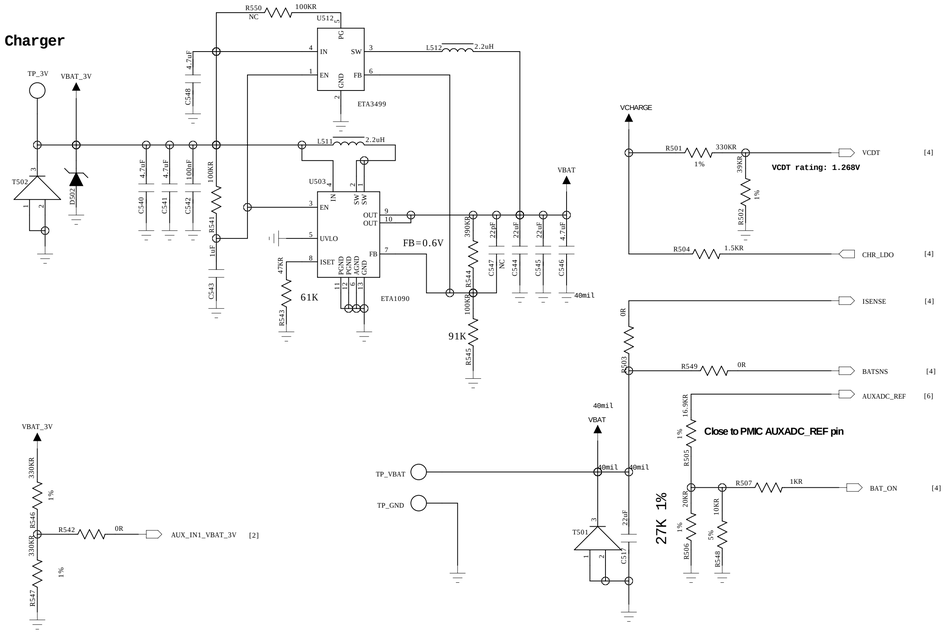
Do not use UART1 as Power solution enable.

Do not use UART2 as power solution enable, if select UART1 as D/L or calibration path,

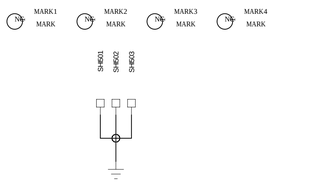
Note: 12-1

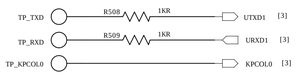


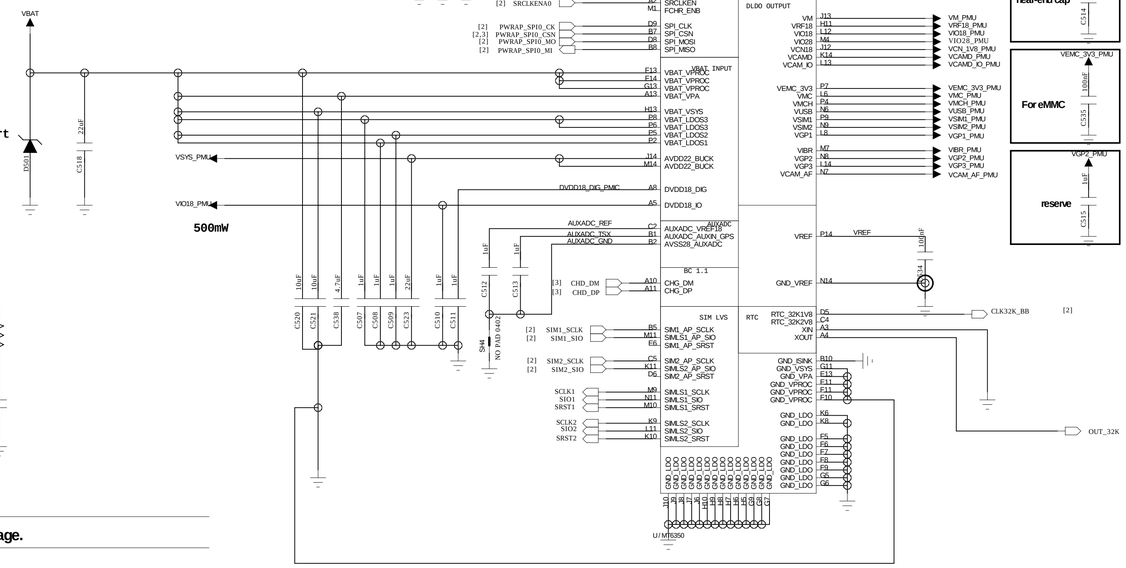
Charger



if battery NTC is 10kohm, R2107=16.9K, R2109=27K
if battery NTC is 47kohm, R2107=61.9K, R2109=100K





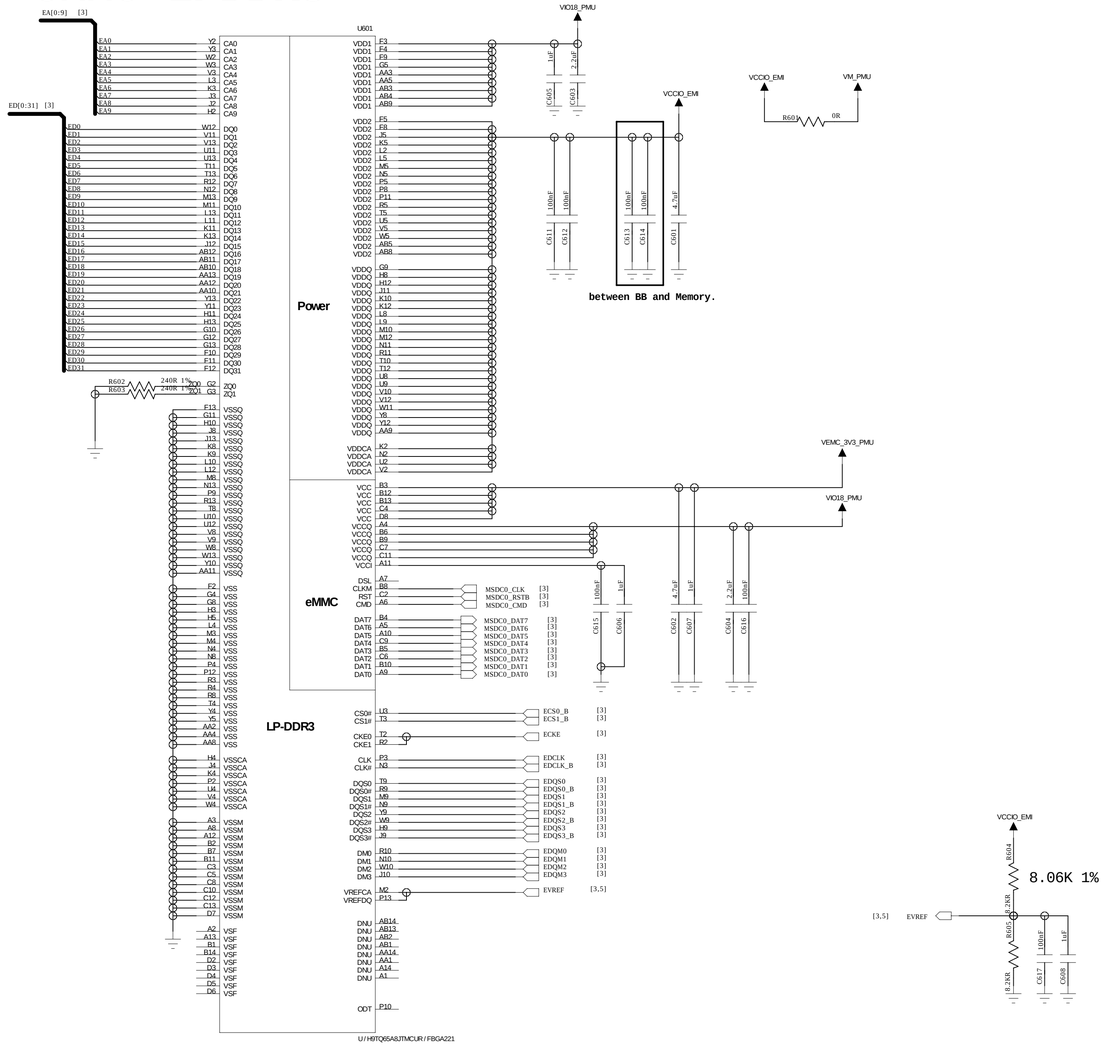


Schematic design notice of "20_Power_MT6350" page.

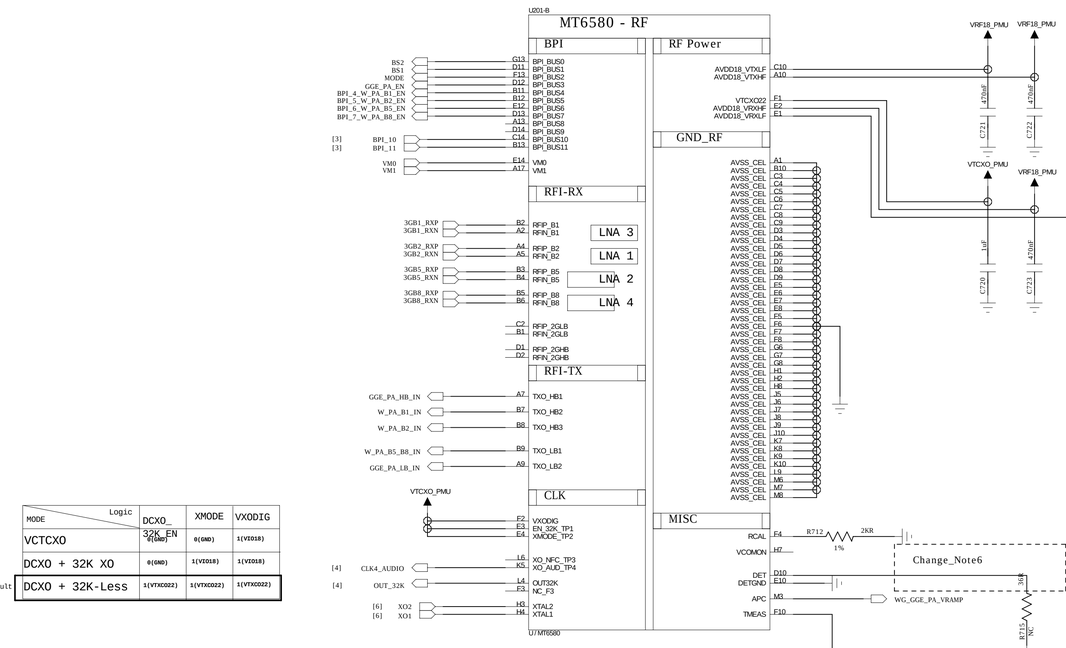
Note 20-1:

Connect TMS GND (Pin2) to PMIC AUXADC_GND (Pin B2) first.
Then connect to main GND by inner layer short pad (i.e., layer 2).

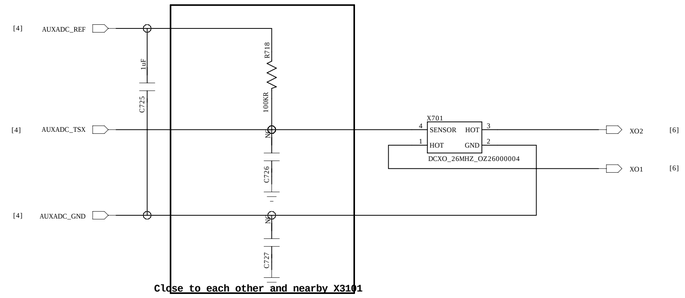
eMMC+LPDDR3



EA[0:9] [3]
ED[0:31] [3]
U601
Power
eMMC
LP-DDR3
VIO18_PMU
VCCIO_EMI
VM_PMU
R601
0R
between BB and Memory.
VEMC_3V3_PMU
R602
R603
240R 1%
MSDC0_CLK [3]
MSDC0_RSTB [3]
MSDC0_CMD [3]
MSDC0_DAT7 [3]
MSDC0_DAT6 [3]
MSDC0_DAT5 [3]
MSDC0_DAT4 [3]
MSDC0_DAT3 [3]
MSDC0_DAT2 [3]
MSDC0_DAT1 [3]
MSDC0_DAT0 [3]
ECS0_B [3]
ECS1_B [3]
ECKE [3]
EDCLK [3]
EDCLK_B [3]
EDQS0 [3]
EDQS0_B [3]
EDQS1 [3]
EDQS1_B [3]
EDQS2 [3]
EDQS2_B [3]
EDQS3 [3]
EDQS3_B [3]
EDQM0 [3]
EDQM1 [3]
EDQM2 [3]
EDQM3 [3]
EVREF [3,5]
8.06K 1%
U / H9TQ65A8JTMCUR / FBGA221



MODE \ Logic	DCXO_32K_EN	XMODE	VXODIG
VCTCXO	0(GND)	0(GND)	1(VIO18)
DCXO + 32K XO	0(GND)	1(VIO18)	1(VIO18)
default DCXO + 32K-Less	1(VTXCO22)	1(VTXCO22)	1(VTXCO22)

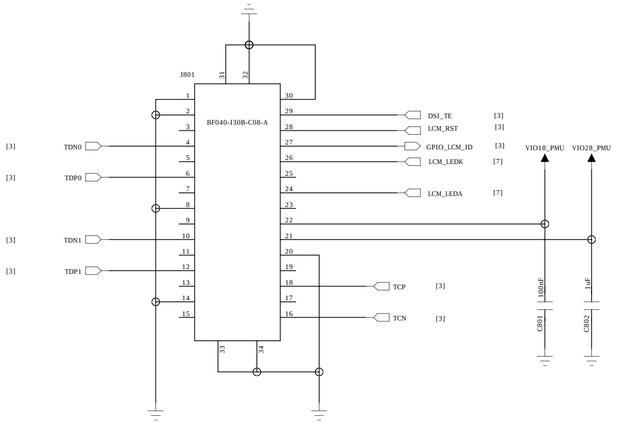


Close to each other and nearby X3101

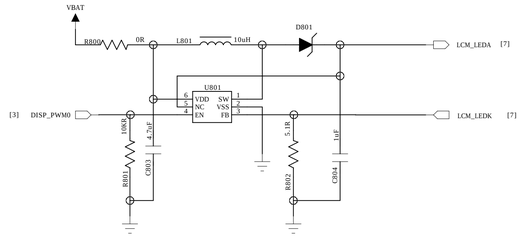
1.Route AUXADC_REF/AUXADC_TSX with 3mil trace width
2.Route AUXADC_REF/AUXADC_TSX as differential trace with well GND shielding
3.Route AUXADC_GND with 15mil trace width under AUXADC_REF/AUXADC_TSX trace to provide return current path

1. Keep the crystal > 10 mm and < 30 mm away from the heat sources (Priority: 2/3G PAs > charger).
2. Keep-out at least the first two inner layers of metal including all crystal circuits.
3. Keep the crystal > 2.5 mm away from MT6580 Co-TMS.
4. Keep-out all crystal components > 0.25 mm away from the surrounding metal.
5. Do not place the TMS directly under the heat sources that on the opposite side (i.e., CPU and PAs).
6. Keep all TMS routing away from high-speed and power traces.

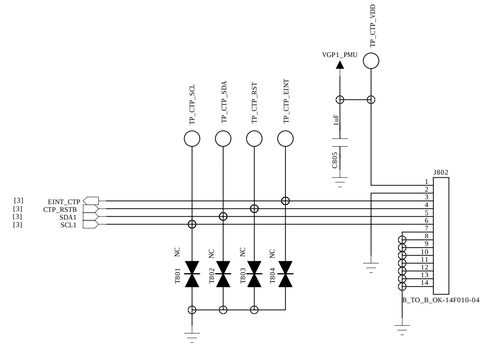
LCD



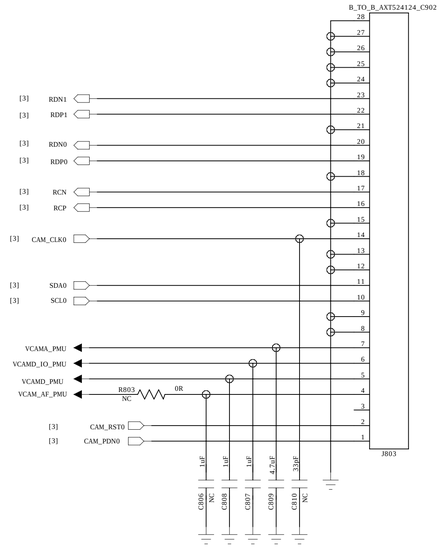
BackLight



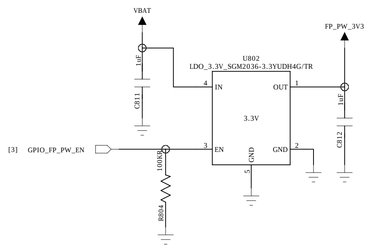
CTP

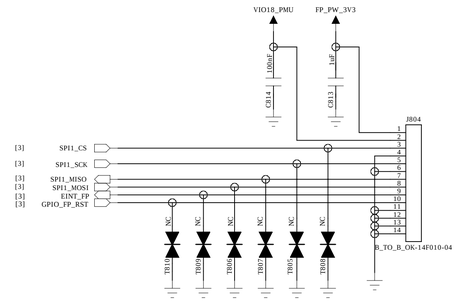


Rear Camera

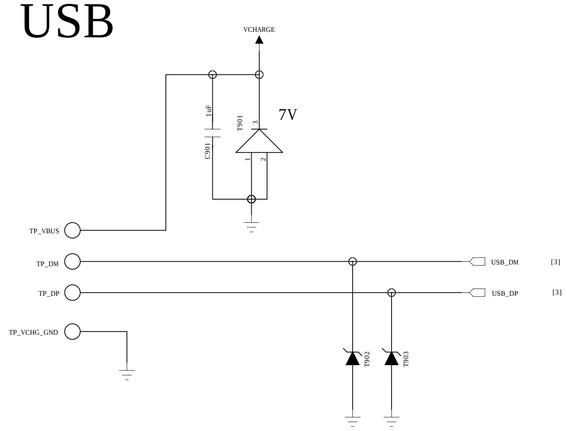


Finger Printor





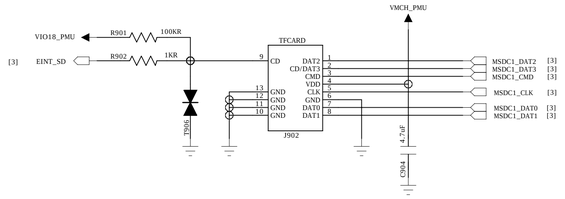
USB



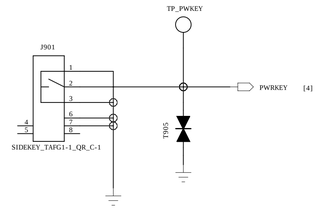
T Card

W/O Card CD=H

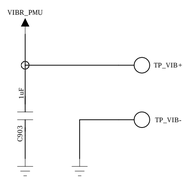
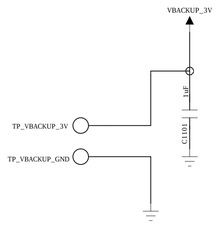
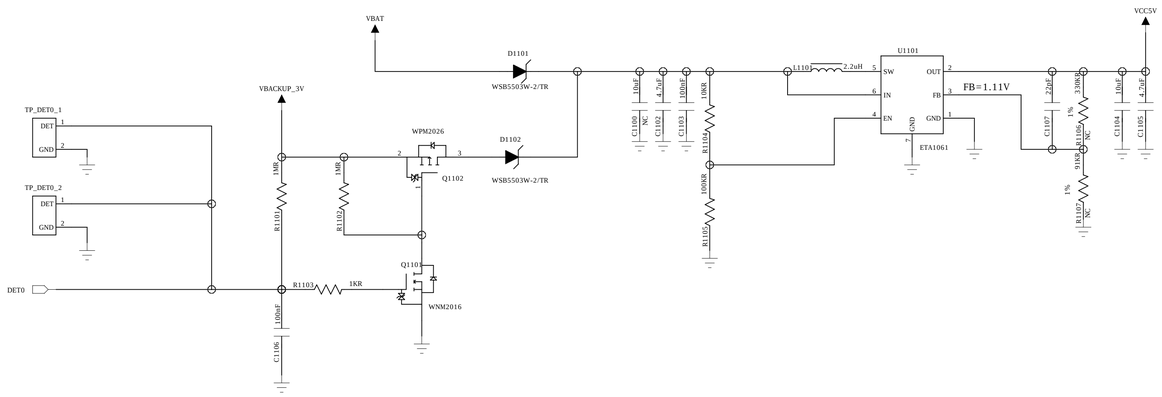
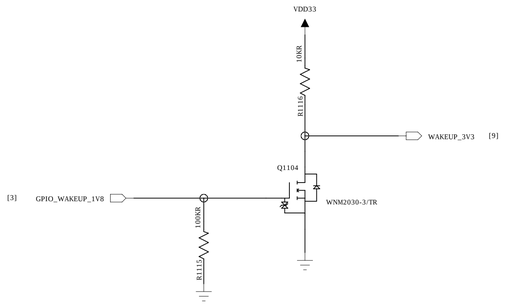
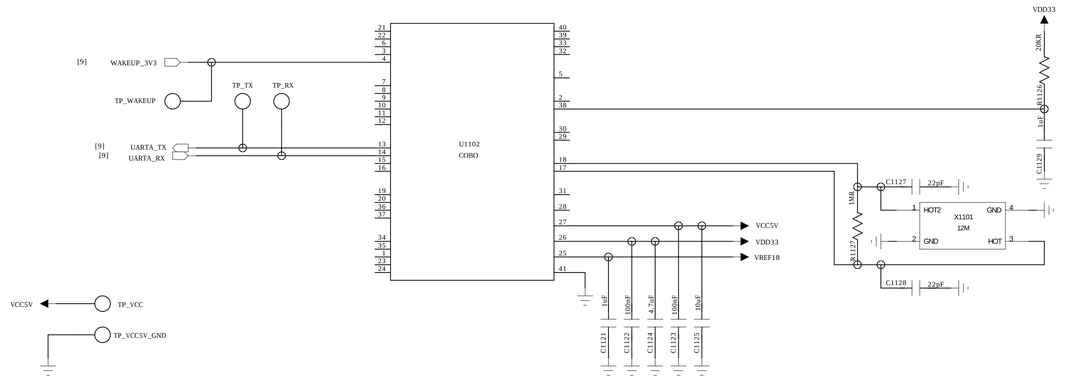
W Card CD=0



KEYS



VIB



BackUp Battery