

ARM Cortex-A7 - Core power

CCK

DVFS1

DDQ

EM

EM

EM

EM

EM

EM

EM

FBB

U7176580

ARM Cortex-A7 - GND

GND

GND_WCN

GND

AC9

AC10

AC13

AC14

AC17

AC19

AC20

AC21

AC22

AD07

AD10

AD14

AD17

AD19

AD19

AD21

AD25

AE5

AE6

AE7

AE10

AE11

AE12

AE13

AE15

AE16

AE17

AE19

AE5

AE7

AE11

AE14

AE17

AE20

AE22

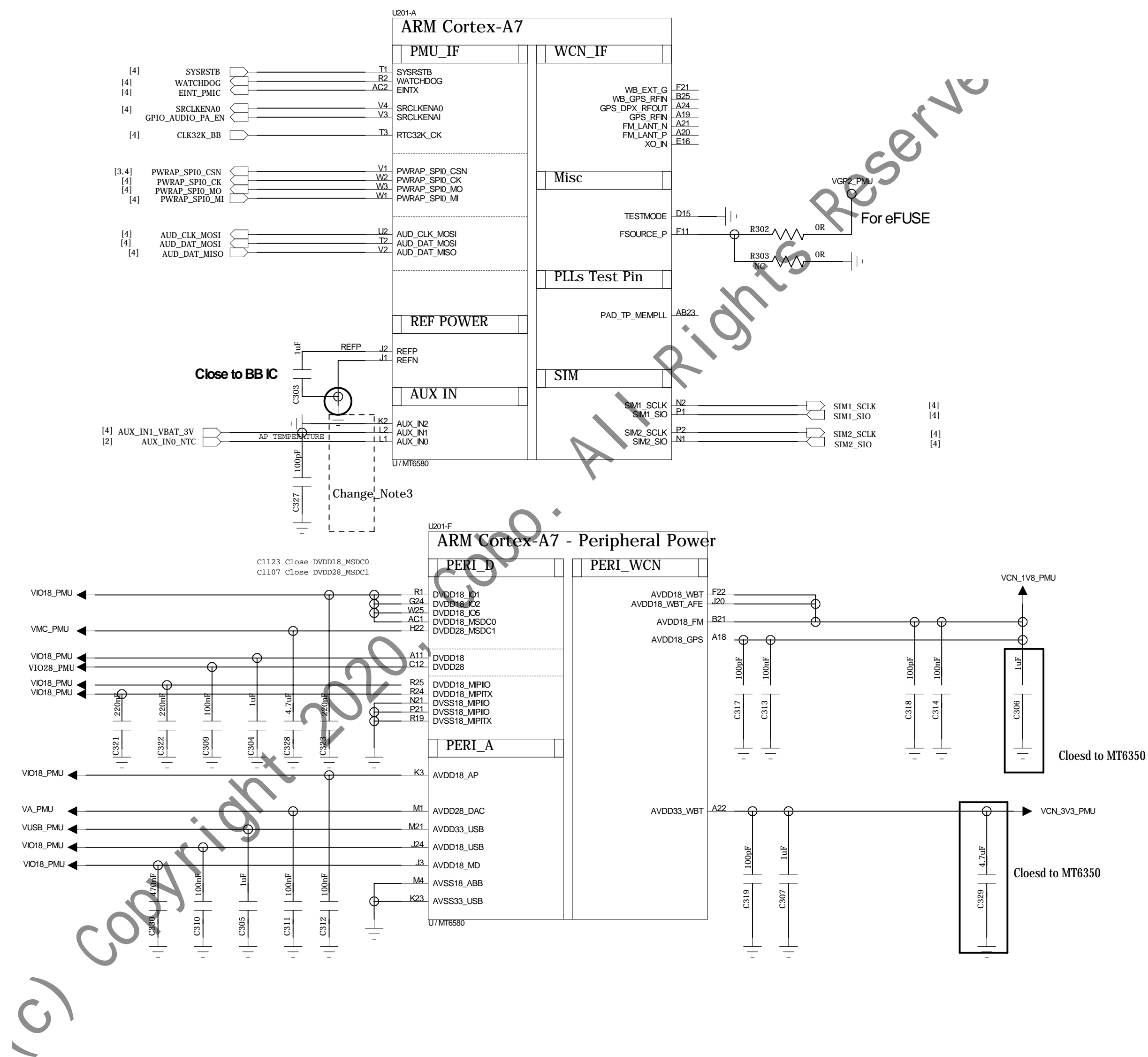
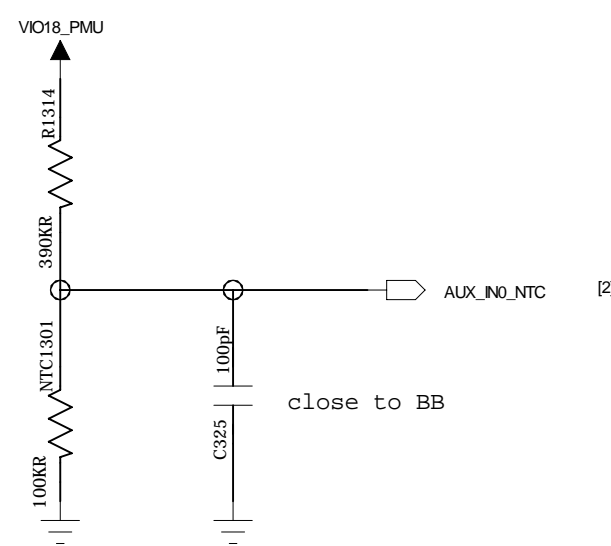
AG1

AG8

AG25

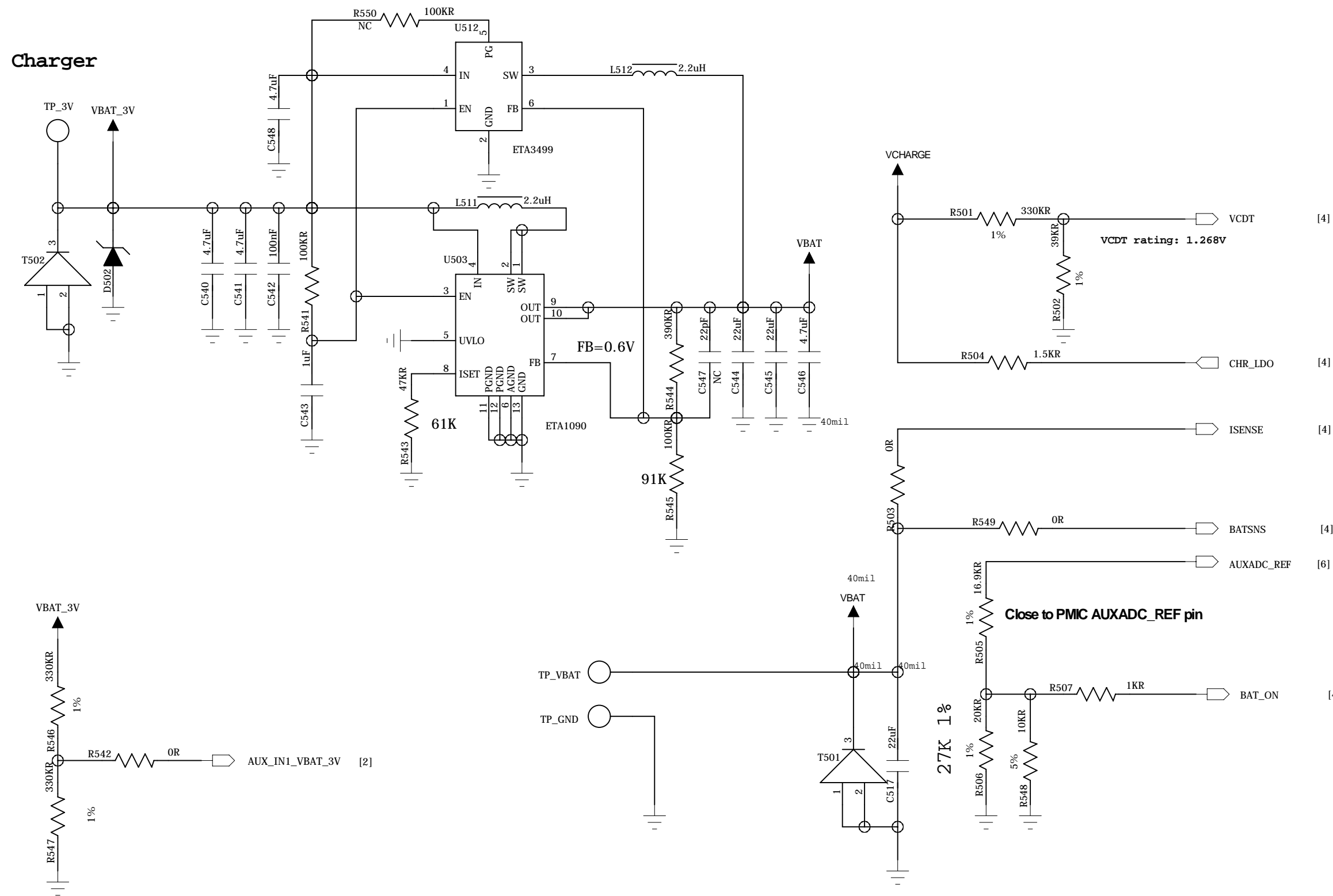
F23

U7176580



AVDD28_DAC change power source by "VA_PMU".

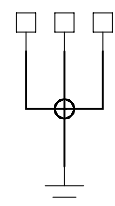
Charger



if battery NTC is 10kohm, R2107-16.9K, R2109-27K
if battery NTC is 47kohm, R2107-61.9K, R2109-100K

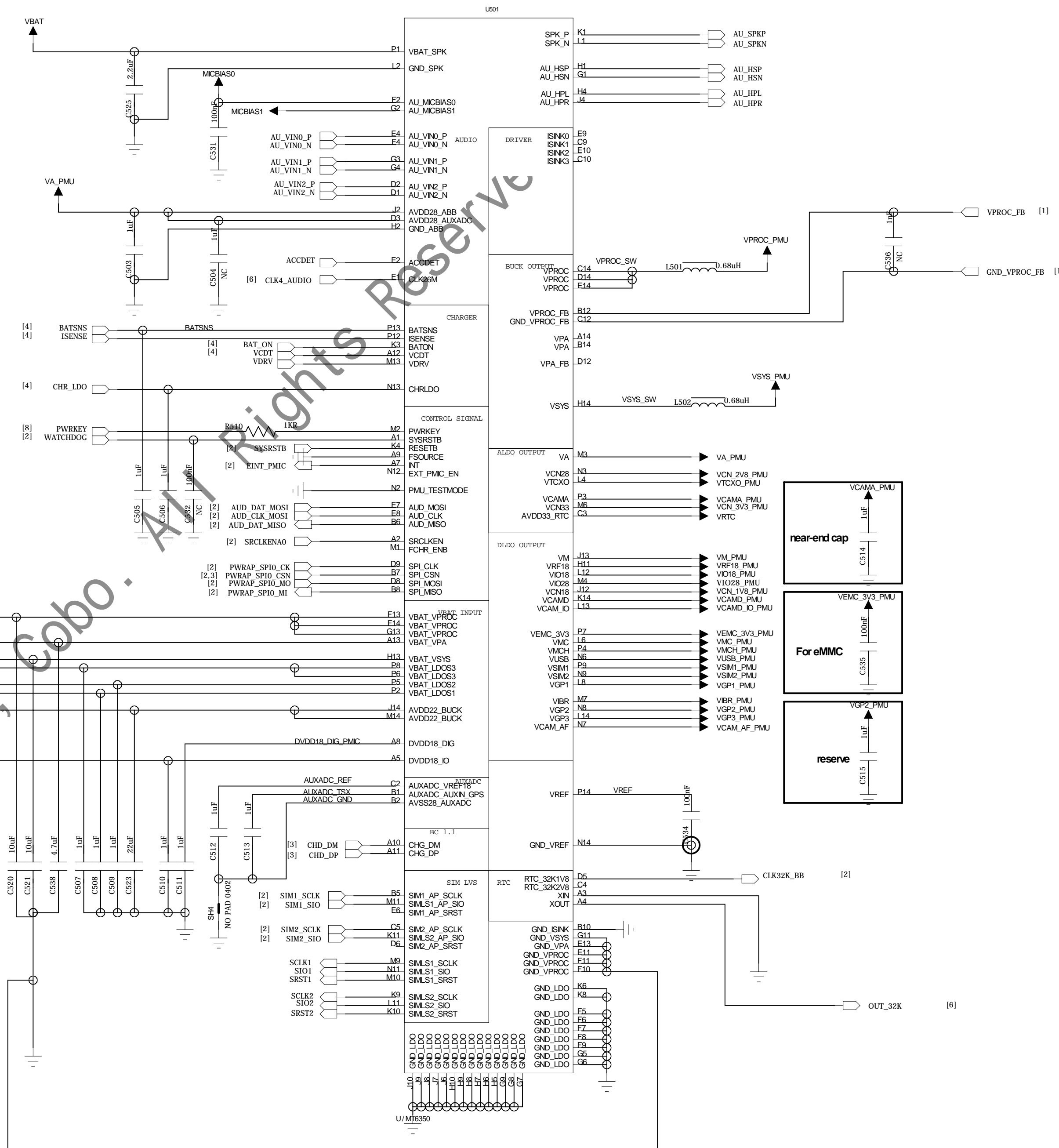
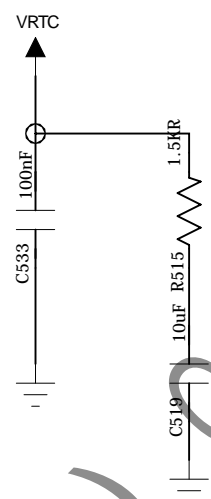
MARK1 MARK2 MARK3 MARK4

SH601 SH602 SH603

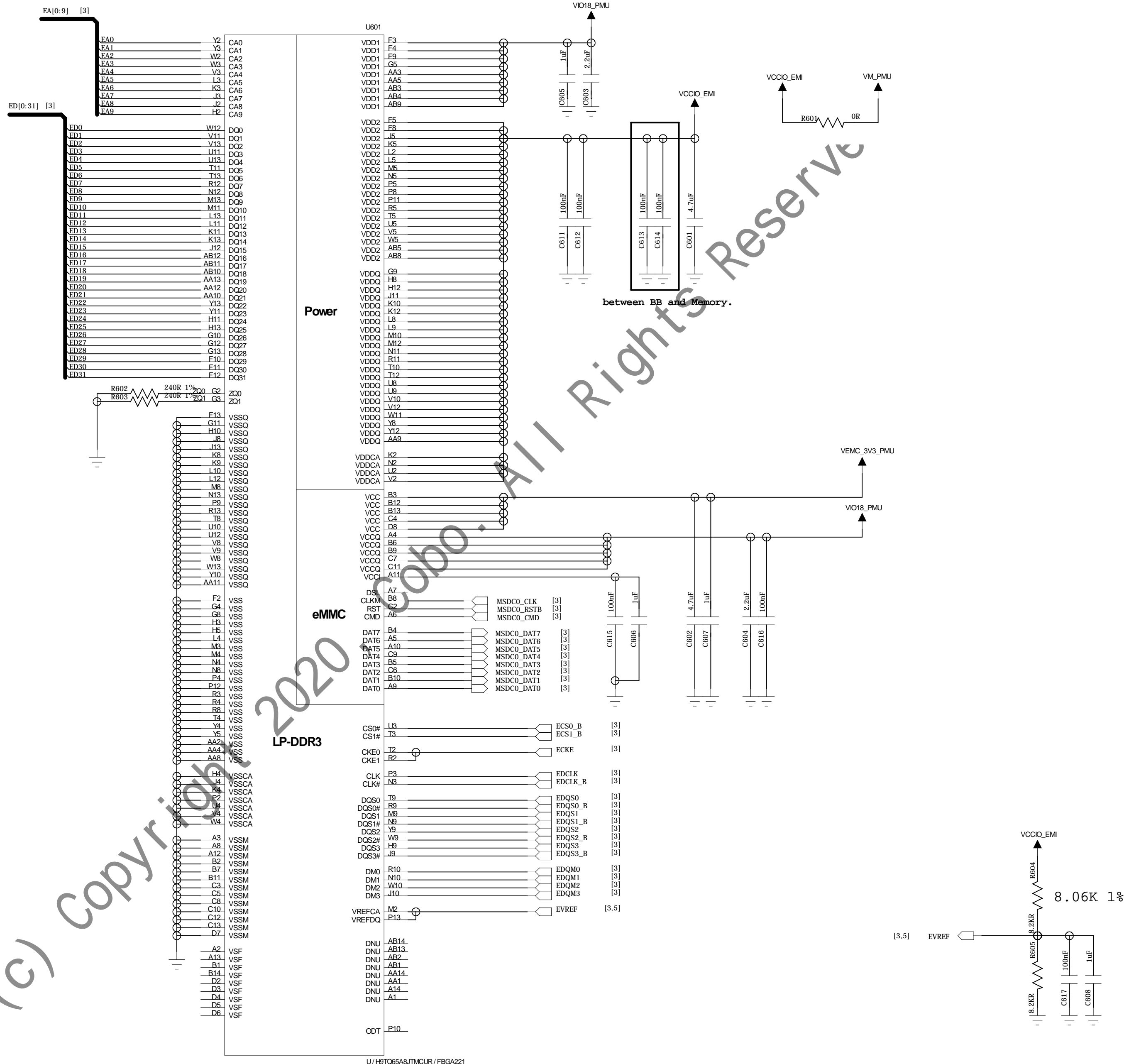


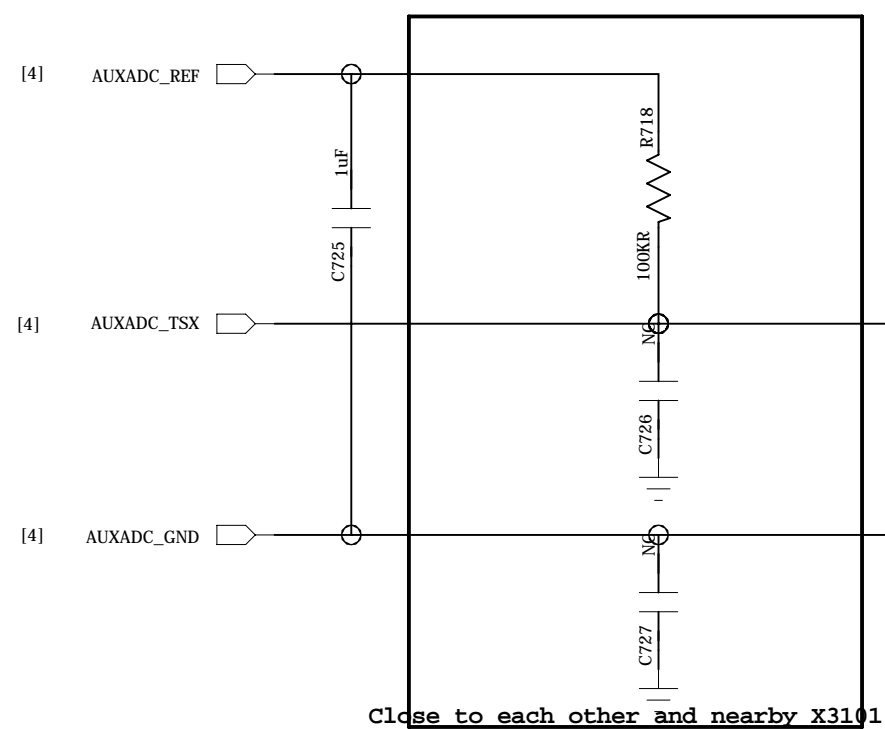
TP_TXD TP_RXD TP_KPCOLO

Between IC and IO port
VF : 4.85V-5.36V



eMMC+LPDDR3

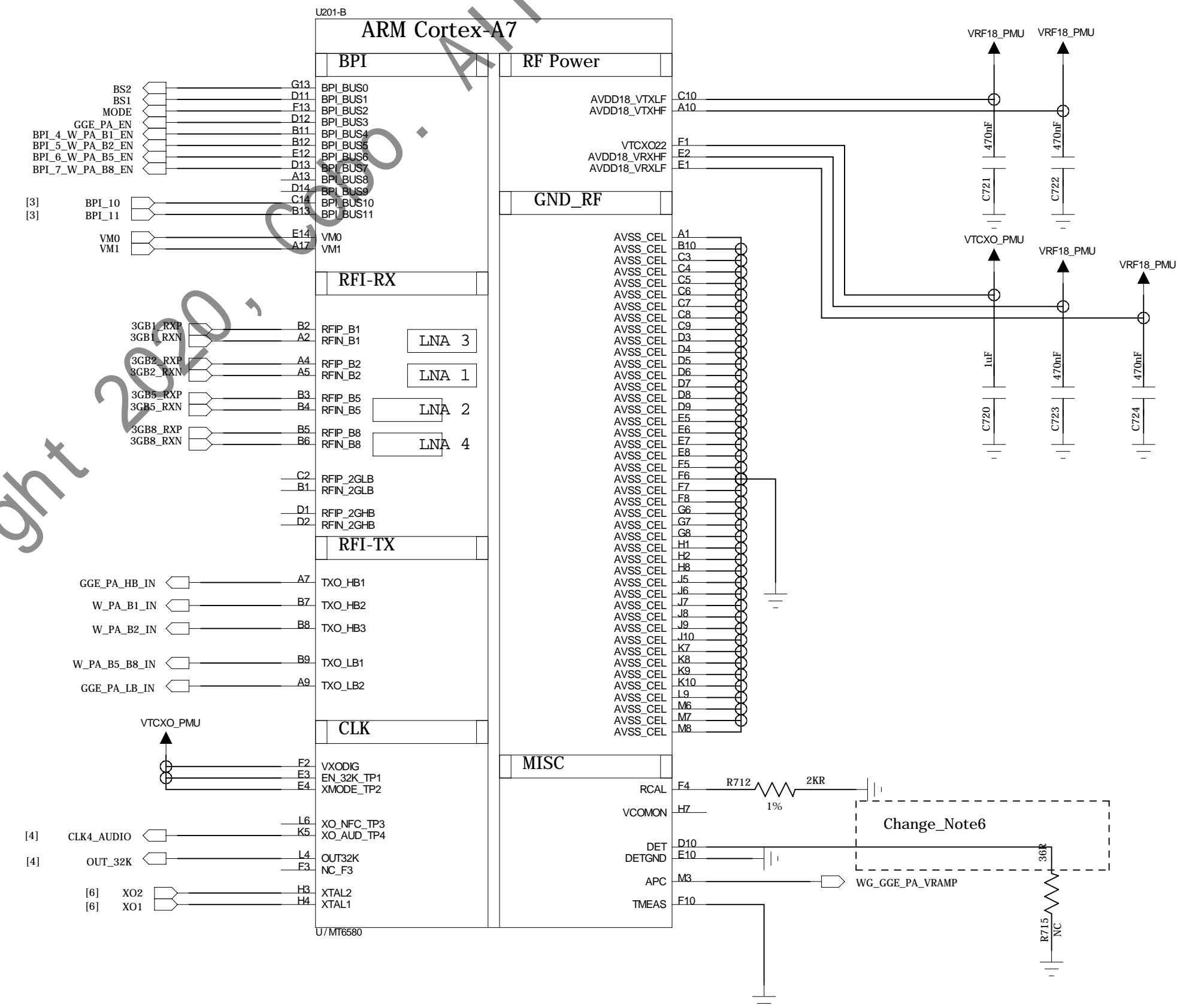




- 1.Route AUXADC_REF/AUXADC_TSX with 3mil trace width
- 2.Route AUXADC_REF/AUXADC_TSX as differential trace with well GND shielding
- 3.Route AUXADC_GND with 15mil trace width under AUXADC_REF/AUXADC_TSX trace to provide return current path

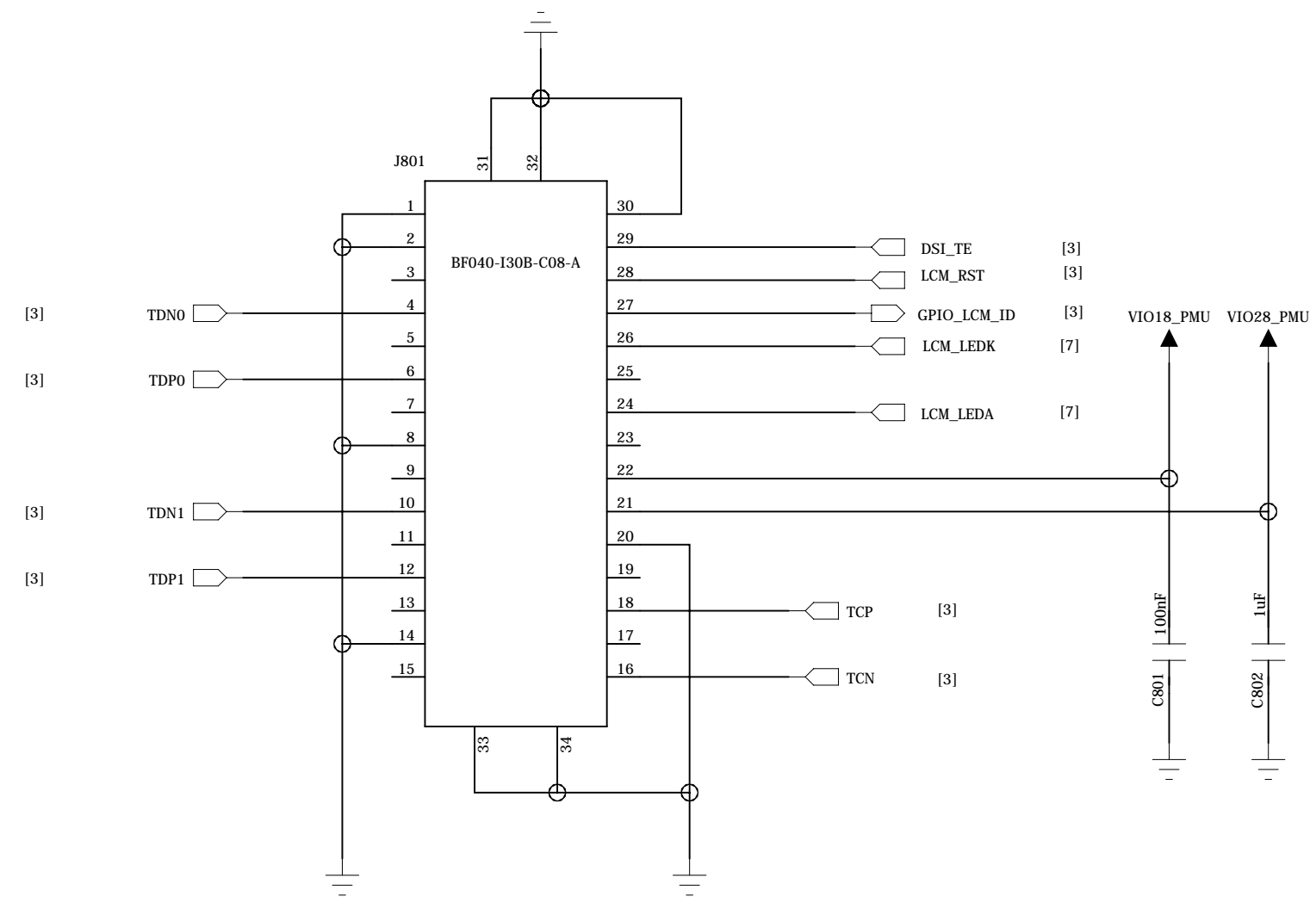
MODE	Logic	DCXO	XMODE	VXODIG
VCTCXO	DCXO + 32K XO	0 (GND)	1 (VIO18)	1 (VIO18)
DCXO + 32K XO	0 (GND)	1 (VIO18)	1 (VIO18)	1 (VIO18)
DCXO + 32K-Less	1 (VIO18)	1 (VIO18)	1 (VIO18)	1 (VIO18)

default

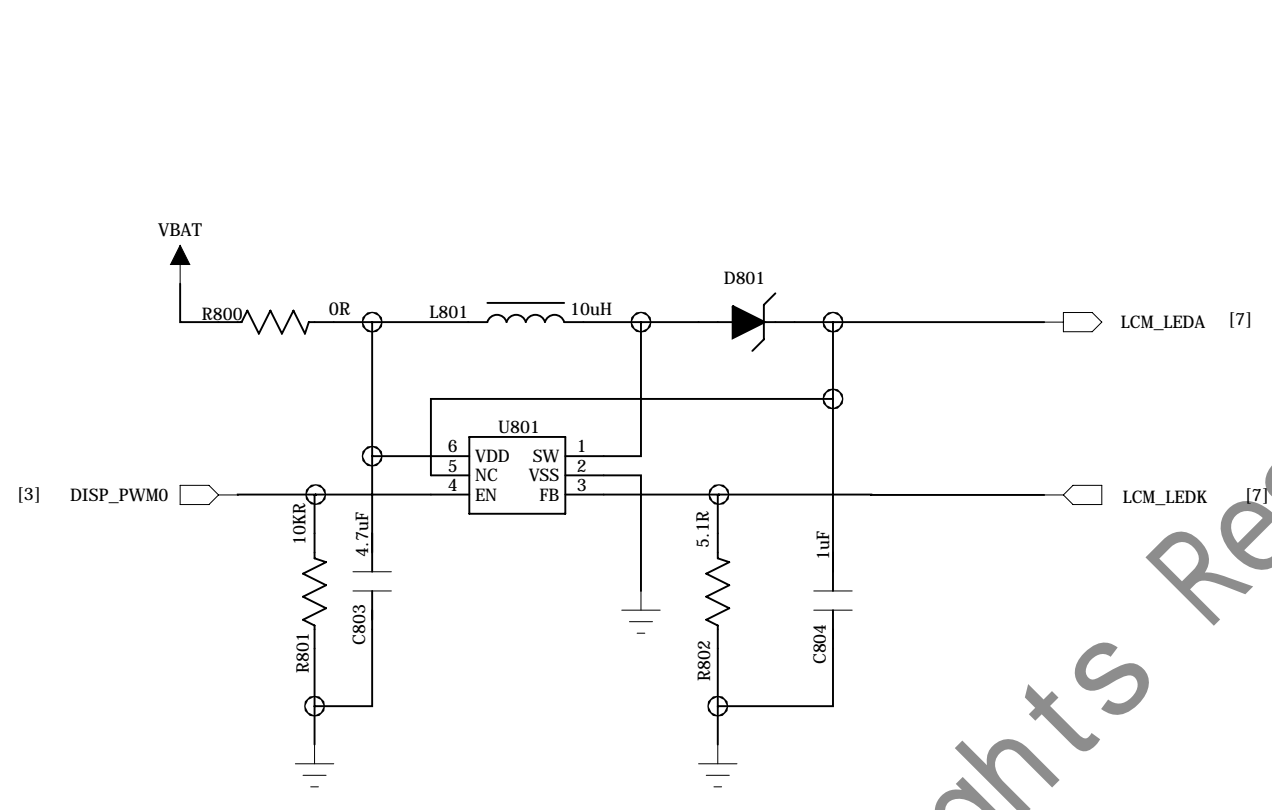


1. Keep the crystal > 10 mm and < 30 mm away from the heat sources (Priority: 2/3G PAs > charger).
2. Keep-out at least the first two inner layers of metal including all crystal circuits.
3. Keep the crystal > 2.5 mm away from M16580 Co-TVS.
4. Keep-out all crystal components > 0.25 mm away from the surrounding metal.
5. Do not place the TVS directly under the heat sources that on the opposite side (i.e., CPU and PAs).
6. Keep all TVS routing away from high-speed and power traces.

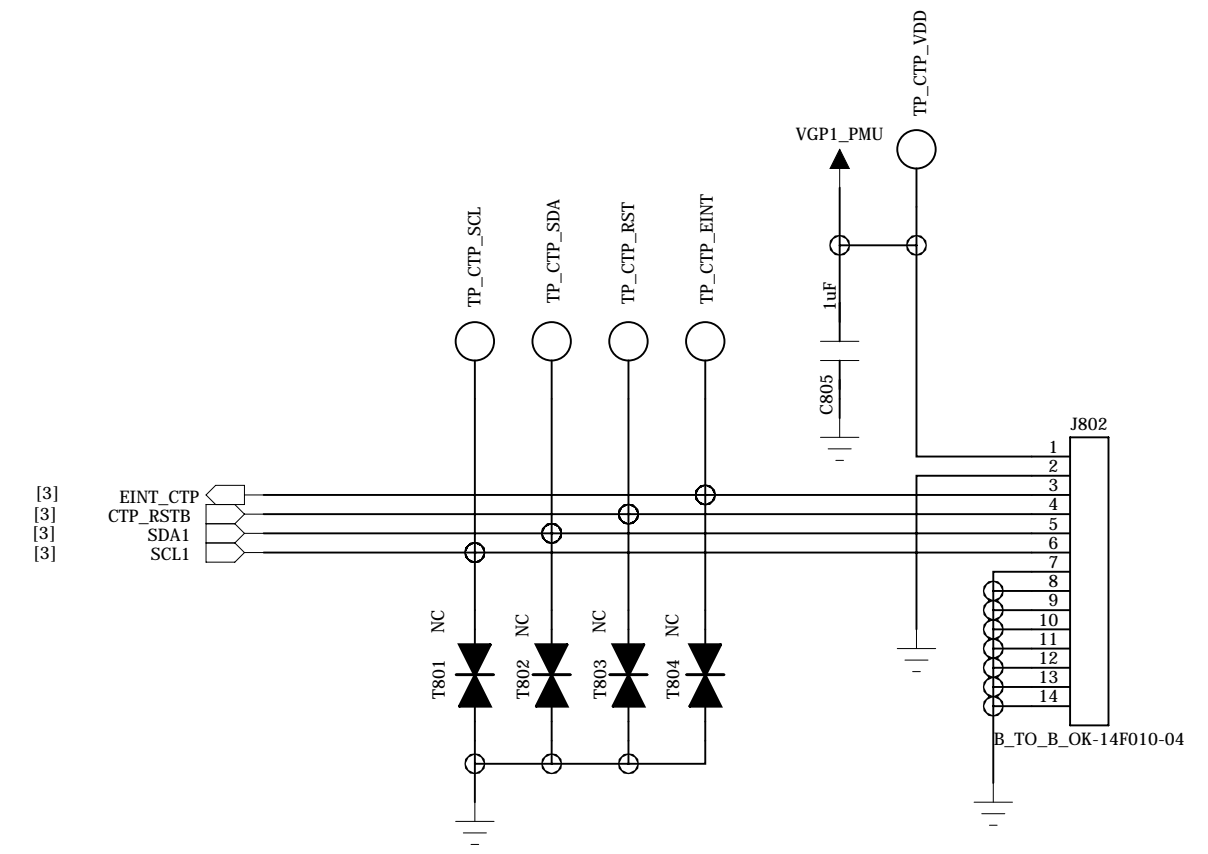
LCD



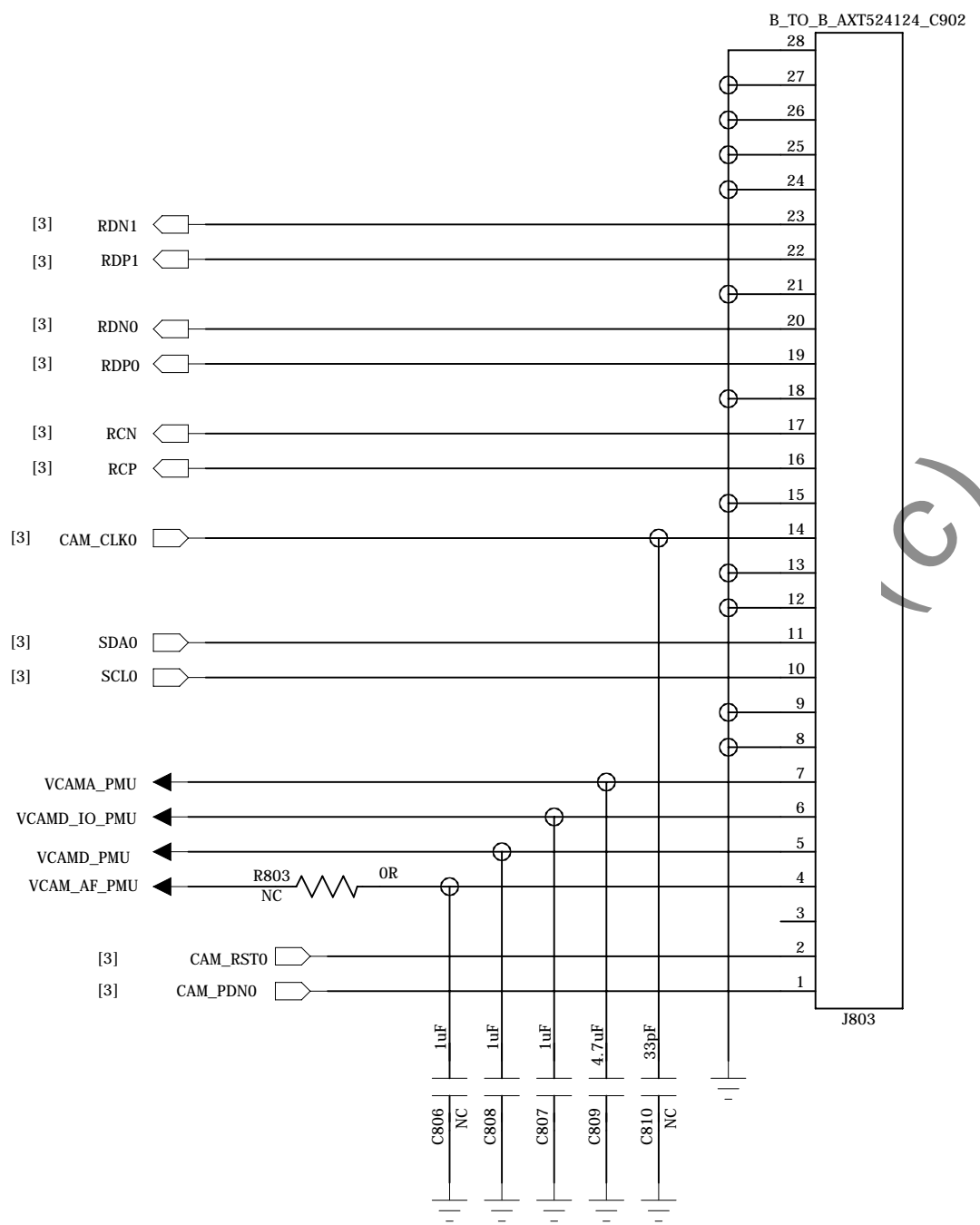
BackLight



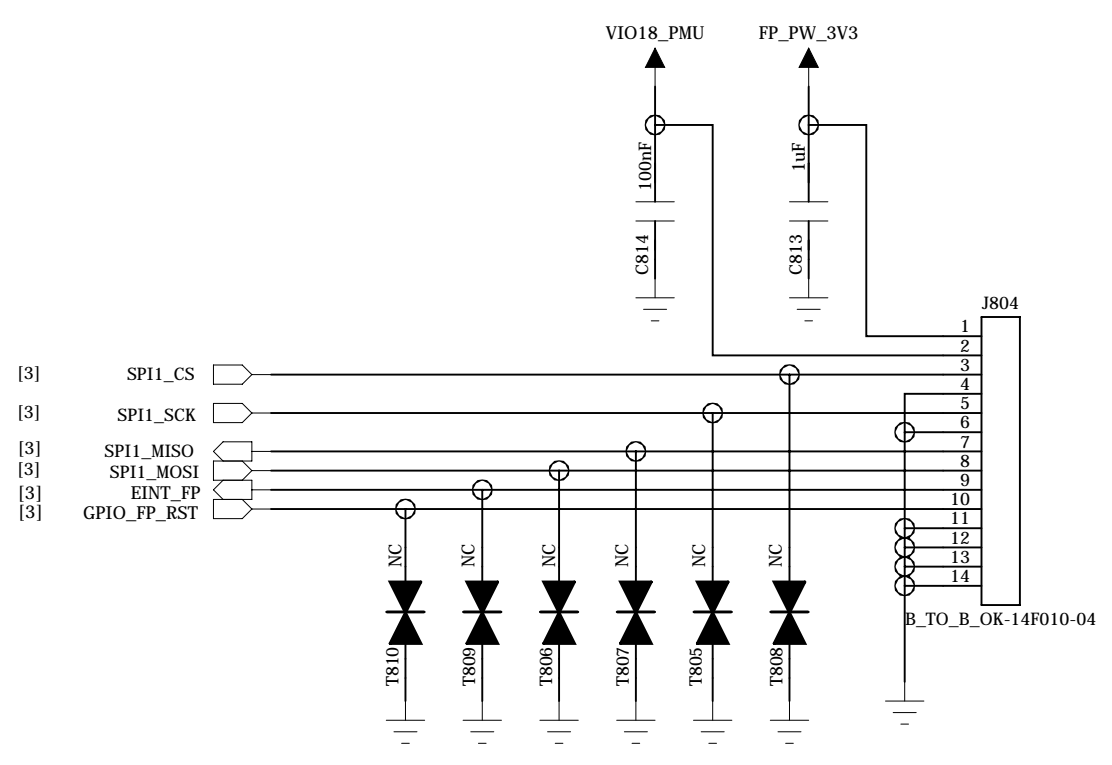
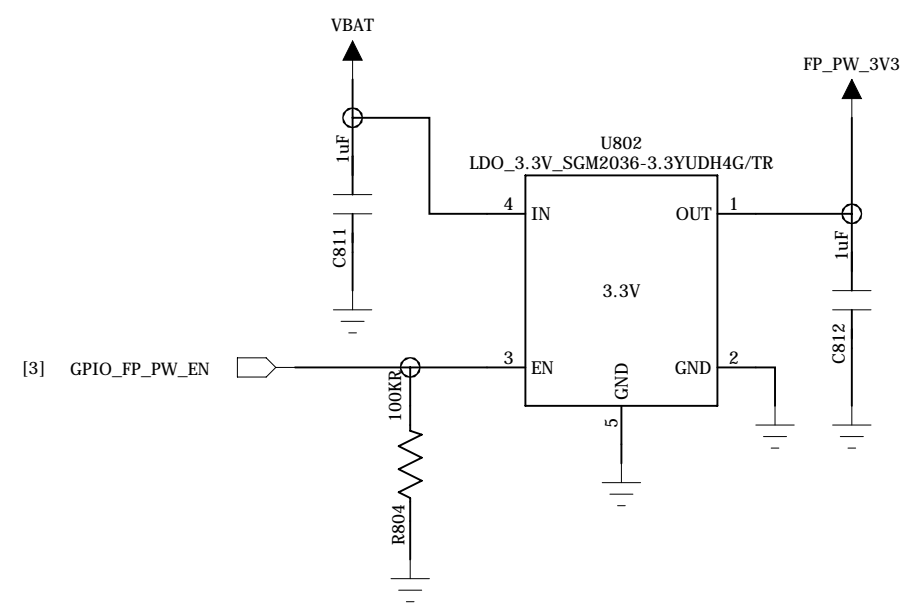
CTP



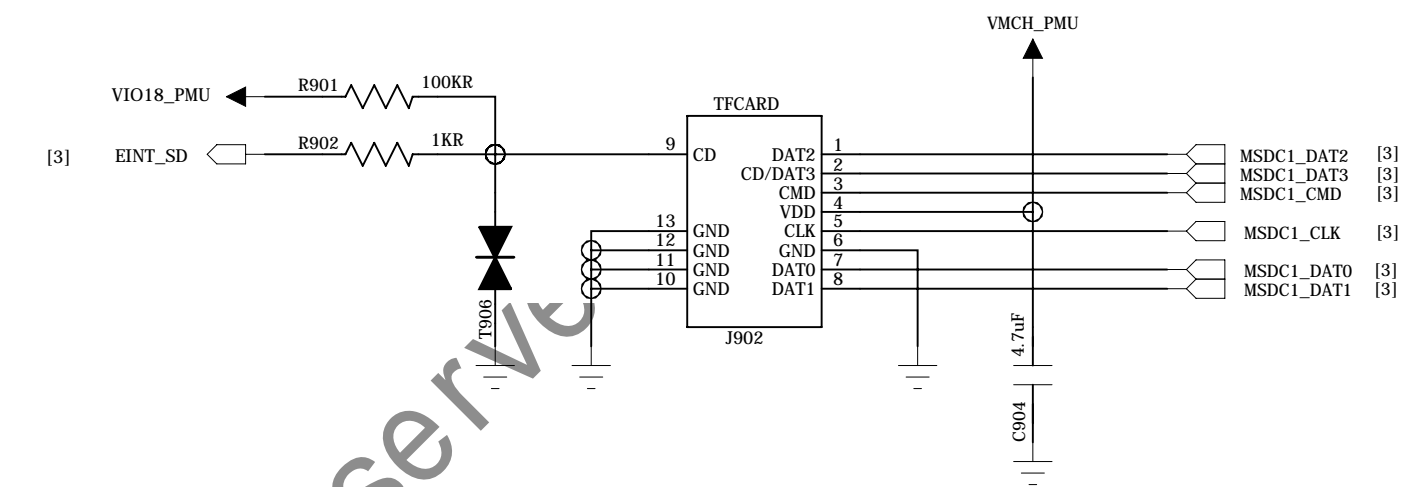
Rear Camera



Finger Printor



W/O Card	CD=H
W Card	CD=0



TP_PWKEY

P001

1

2

3

6

7

8

SIDEKEY_TAFGI-1_QR_C-1

T005

PWRKEY

[4]

