NEC Electronics Inc.

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PRODUCT
INFORMATION

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μPD77C25/
μPD77P25

Digital Signal Processor

Data Sheet

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uPD77C25/77P25
DIGITAL SIGNAL PROCESSOR

Description

The uPD77C25/uPD77P25 signal processing interface (SPI) chips are significant upgrades to the uPD7720 - the original member of NEC's family of digital signal processors. Designated the "SPI PLUS" (SPI+), these chips execute instructions twice as fast as the 7720/77C20. Additional instructions allow the SPI+ to execute common digital filter routines more efficiently and hence at more than twice the speed of a 7720 implementation.

In addition to doubled execution speed, the SPI+ has four times the instruction ROM space and twice the data ROM and RAM space of the 7720. Real savings are now possible especially where one 77C25 can do the work of - and replace two or more 7720s.

The external clock frequency (8.3 MHz maximum) remains the same as for 7720/77C20 while the internal instruction execution speed is doubled. For most applications, the 77C25/77P25 is plug-in compatible with the 7720/77C20/77P20.

The feature that distinguishes digital signal processing (DSP) chips from general-purpose microcomputers is the on-chip multiplier - necessary for high speed signal processing algorithms. The SPI+ multiplier is very sophisticated - especially for a low-cost DSP chip - since both multiplier inputs can be loaded simultaneously from two separate memory areas. These loading operations are only two of nine operations (see 'Features') that can occur during one 122 ns instruction cycle. (On competitive DSP chips such operations require separate instructions). For a typical DSP filter application involving many successive multiplications, the SPI+ provides a new multiplication product for addition to a sum of products every 122 nanoseconds. Additionally, during the same instruction, memory data pointers are manipulated, and even a return from subroutine may be executed.

The uPD77C25 is the mask ROM version, and uPD77P25 is the UVEPROM version. Both versions are CMOS and functionally identical.

See table 1 for detailed comparison of features between 77C25 and 77C20A.

Features

[] Low-power CMOS: approximately 24 mA typical current use (77C25).
[] Fast instruction execution: 122 ns with 8.192 MHz clock.
[] All instructions execute in one instruction cycle
[] Drop-in compatible with uPD7720A/77C20A/77P20
[] 16-bit data word
[] Multi-operation instructions for fast program execution:
  -- Load one multiplier input
  -- Load the other multiplier input
  -- Mulitply (automatic)
  -- Load product to output registers (automatic)
  -- Add product to accumulator
  -- Move RAM column data pointer
  -- Move RAM row pointer
  -- Move data ROM pointer
  -- Return from subrountine

* Any part, any combination, or all 9 of the above operations may constitute one instruction which executes in 122 ns

Features cont

- [] Modified Harvard architecture with three separate memory areas
  - -- Program ROM (2048 x 24 bits)
  - -- Data ROM (1024 x 16 bits)
  - -- Data RAM (256 x 16 bits)
- [] 16- x 16-bit fixed point multiplier; 31-bit product with every instruction
- [] Dual 16-bit accumulators
- [] External maskable interrupt
- [] Four-level stack for subroutines and/or interrupt
- [] Multiple I/O capabilities
  - -- Serial: 8- or 16-bit (244 ns/bit)
  - -- Parallel: 8- or 16-bit
  - -- DMA
- [] Compatible with most uP's, including:
  - -- uPD8080
  - -- uPD8085
  - -- uPD8086
  - -- uPD780 (Z80)
  - -- uPD78xxx family
- [] Single +5 volt power supply

Applications

- [] Portable telecommunications equipment
- [] Digital filtering
- [] High-speed data modems
- [] Fast Fourier transforms (FFT)
- [] Speech synthesis and analysis
- [] Dual-tone multifrequency (DTMF) transmitters/receivers
- [] Equalizers
- [] Adaptive control
- [] Numerical processing

Performance Benchmarks

To be announced.

Table 1. Comparison with uPD77C20A/77P20

	77C25/77P25	77C20A/77P20
Technology	CMOS/CMOS	CMOS/NMOS
Instruction cycle	122 ns	244 ns
Instruction ROM	2048 x 24b	512 x 23b
Data ROM	1024 x 16b	510 x 13b
Data RAM	256 x 16b	128 x 16b
Fixed point multiplier	16b x 16b -> 31b	16b x 16b -> 31b
ALU	16b fixed point	16b fixed point
Accumulator	2 x 16b	2 x 16b
Host CPU Interface	8-bit bus	8-bit bus
Serial Interface	input/output 1channel each 4 MHz	input/output 1 channel each 2 MHz
Temporary Register	Two	One
Additional instructions	JDPLN0 JDPLNF Modification of RAM column data pointer M8 - MF	- - -
DMA Mode	Fully implemented	Partially implemented
Package	28 Pin DIP 44 Pin PLCC	28 Pin DIP 44 Pin PLCC
Power Supply	5 V	5 V
Power Consumption	40 mA (Max)* @ 8.192 MHz	40 mA (Max) @ 8.192 MHz
Power Saving Mode (when idle)	Yes	No

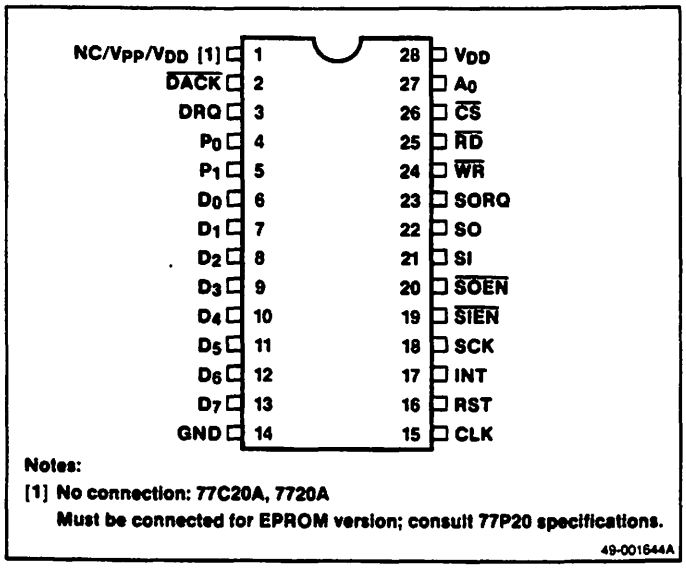
* Not final

Since the 77C25 executes an instruction in one external clock cycle (versus two cycles of the same 8.192 MHz clock for 77C20A), the 77C25 may be substituted for a 77C20A (or 7720A or 77P20) in a circuit without modification of that circuit. Hardware/software which implements data transfers - both serial and parallel - between the SPI+ and other devices in an existing 7720 design should use the handshake protocol described more fully in the 77C25 User's Manual.

Ordering Information

Pin Configurations

28-Pin Dip, Plastic or Ceramic



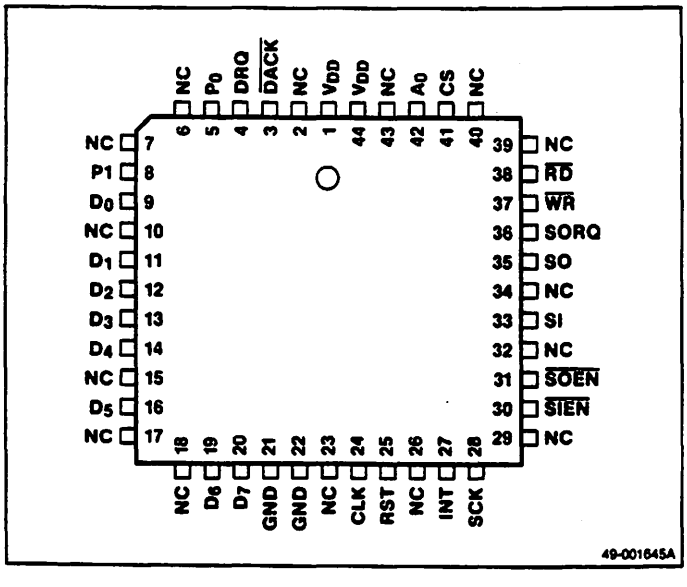
Notes:

[1] No connection: 77C20A, 7720A

Must be connected for EPROM version; consult 77P20 specifications.

49-001644A

44-Pin PLCC



49-001645A

Pin Identification

Symbol	Function
A_0	Status/data register select input
CLK	Single-phase master clock input
$\overline{CS}$	Chip select input
D_0 - D_7	Three-state I/O data bus
$\overline{DACK}$	DMA request acknowledge input
DRQ	DMA request output
$\overline{INT}$	Interrupt input
P_0, P_1	General purpose output control lines
$\overline{RD}$	Read control signal input
$\overline{RST}$	Reset input
SCK	Serial data I/O clock input
SI	Serial data input
$\overline{SIEN}$	Serial input enable input
SO	Three-state serial data output
$\overline{SOEN}$	Serial output enable input
SORQ	Serial data output request
$\overline{WR}$	Write control signal input
GND	Ground
V_{CC}	+5 V power supply
NC/V_{PP}/V_{CC}	No connection on 77C25. Programming power input (+12.5 V) for 77P25; connected to +5 V for normal operation of 77P25

Pin Functions

A_0 [Status Data Register Select]
This input selects data register for read/write (low) or status register for read (high).

CLK

This is the single-phase master clock input.

$\overline{CS}$ [Chip Select]

This input enables data transfer through the data port with RD or WR.

D_0 - D_7 [Data Bus]

This three-state I/O data bus transfers data between the data register or status register and the external data bus.

$\overline{DACK}$ [DMA Request Acknowledge]

This input indicates to the SPI+ that the data bus is ready for a DMA transfer ($\overline{DACK}$ = CS AND A_0 = 0).

DRQ [DMA Request]

This output signals that the SPI+ is requesting a data transfer on the data bus.

INT [Interrupt]

A low-to-high transition on this pin executes a call instruction to location 100H, if interrupts were previously enabled.

P_0 ,P_1
These pins are general-purpose output control lines.

$\overline{RD}$ [Read Control Signal]

This input latches data from the data or status register to the data port where it is read by an external device.

RST [Reset]

This input initializes the SPI+ internal logic and sets the PC to 0.

SCK [Serial data I/O Clock]

When this input is high, a serial data bit is transferred.

SI [Serial Data Input]

This pin inputs 8- or 16-bit serial data words from an external device such as an A/D converter.

$\overline{SIEN}$ [Serial Input Enable]

This input enables the shift clock to the serial input register.

SO [Serial Data Output]

This three-state port outputs 8- or 16-bit data words to an external device such as a D/A converter.

$\overline{\text{SOEN}}$ [Serial Output Enable]

This input enables the shift clock to the serial output register.

SORQ [Serial Data Output Request]

This output specifies to an external device that the serial data register has been loaded and is ready for output. SORQ is reset when the entire 8- or 16-bit word has been transferred.

$\overline{\text{WR}}$ [Write Control Signal]

This input writes data from the data port into the data register.

GND

This is the connection to ground.

V_{CC} [Power Supply]

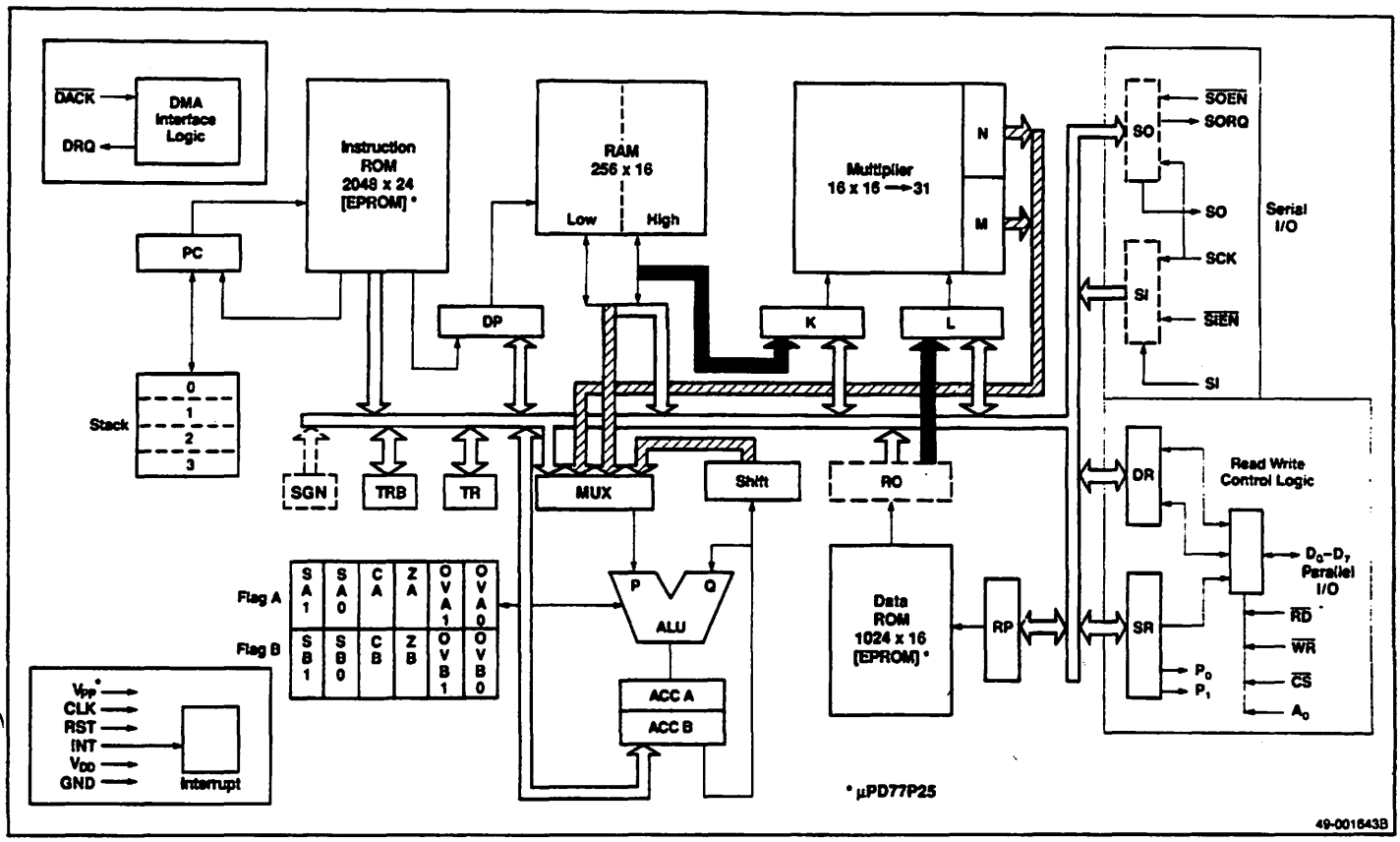
This pin is the +5 volt power supply.

NC/V_{PP}/V_{CC}

This pin is not internally connected in the 77C25. In the 77P25, this pin inputs the programming voltage (V_{PP}) when the part is being programmed.

This pin must be connected to V_{CC} for proper 77P25 operation.

Block Diagram



Functional Description

The primary bus (unshaded in the block diagram) makes a data path between all of the registers (including I/O), memory, and the processing sections. This bus is referred to as the IDB (internal data bus). The multiplier input registers K and L can be loaded not only from the IDB but alternatively via buses (darkened in the block diagram) directly from RAM to the K register and directly from data ROM to the L register. Output from the multiplier in the M and N registers is typically added via buses (shaded in the block diagram) to either accumulator A or B as part of a multi-operation instruction.

Memory

Memory is divided into three types: instruction ROM, data ROM, and data RAM. The 2048 x 24-bit words of instruction ROM are addressed by the 11-bit program counter that can be modified by an external reset, interrupt, call, jump, or return instruction.

The data ROM is organized in 1024 x 16-bit words that are addressed through a 10-bit ROM pointer (RP register). The RP may be modified simultaneously with arithmetic instructions so that the next value is available for the next instruction. The data ROM is ideal for storing the necessary coefficients, conversion tables, and other constants for signal and math processing applications.

The data RAM is 256 x 16-bit words and is addressed through an 8-bit data pointer (DP register). The DP has extensive addressing features that operate simultaneously with arithmetic instruct- ions, eliminating additional time for addressing or address modification.

Arithmetic Capabilities

One of the unique features of the SPI+'s architecture is its arithmetic facilities. With a separate multiplier, ALU, and multiple internal data paths, the SPI+ is capable of carrying out a multiply, an add or other arithmetic operation, and a data move between internal registers in a single instruction cycle.

ALU

The ALU is a 16-bit two's complement unit capable of executing 16 distinct operations on data routed via the P and Q ALU inputs.

Accumulators [ACCA/ACCB]

Associated with the ALU are two 16-bit accumulators, each with its own set of flags, which are updated at the end of each arithmetic instruction (except NOP). Table 2 shows the ACC A/B flag registers. In addition to zero result, sign, carry, and overflow flags, the SPI+ incorporates auxiliary overflow and sign flags (SA1, SB1, OVA1, OVB1). These flags enable the detection of an overflow condition and maintain the correct sign after as many as three successive additions or subtractions.

Table 2. ACC A/B Flag Registers

Flag A	SA1	SA0	CA	ZA	OVA1	OVA0
Flag B	SB1	SB0	CB	ZB	OVB1	OVB0

Sign Register [SGN]

When OVA1 is set, the SA1 bit will hold the corrected sign of the overflow. The SGN register will use SA1 to automatically generate saturation constants 7FFFH(+) or 8000H(-) to permit efficient limiting of a calculated value. The SGN register is not affected by arithmetic operations on accumulator B, but flags SB1, SB0, CB, ZB, OVB1, and OVB0 are affected.

Multiplier

Thirty-one-bit results are developed by a 16 x 16-bit two's complement multiplier in 122 ns. The result is automatically latched to two 16-bit registers, M and N, at the end of each instruction cycle. The sign bit and 15 higher bits are in M and the 16 lower bits are in N; the LSB in N is zero. A new product is available for use after every instruction cycle, providing significant advantages in maximizing processing speed for real-time signal processing.

Stack

The SPI+ contains a four-level program stack for efficient program usage and interrupt handling.

Interrupt

The SPI+ supports a single-level interrupt. Upon sensing a high level on the INT terminal, a subroutine call to location 100H is executed. The EI bit of the status register automatically resets to 0, disabling the interrupt facility until it is reenabled under program control.

Input/Output

General

The SPI+ has three communication ports, as shown in figure 1: two serial and one 8-bit parallel, each with its own control lines for interface handshaking. Parallel port operation is software-configurable to be in either polled mode or DMA mode. A general-purpose, two-line output port rounds out a full complement of interface capability.

Serial I/O

The two shift registers (SI,SO) are software-configurable to single- or double-byte transfers. The shift registers are externally clocked (SCK) to provide a simple interface between the SPI+ and serial peripherals such as A/D and D/A converters, codecs, or other SPI's. Figure 2 shows serial I/O timing.

Figure 1. SPI Communication Ports

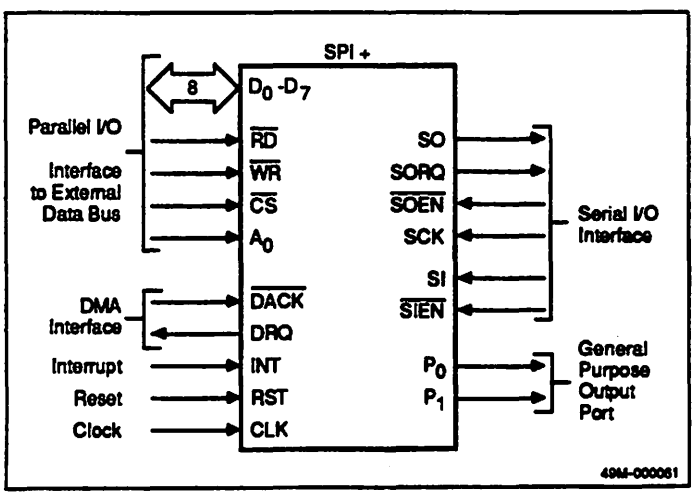
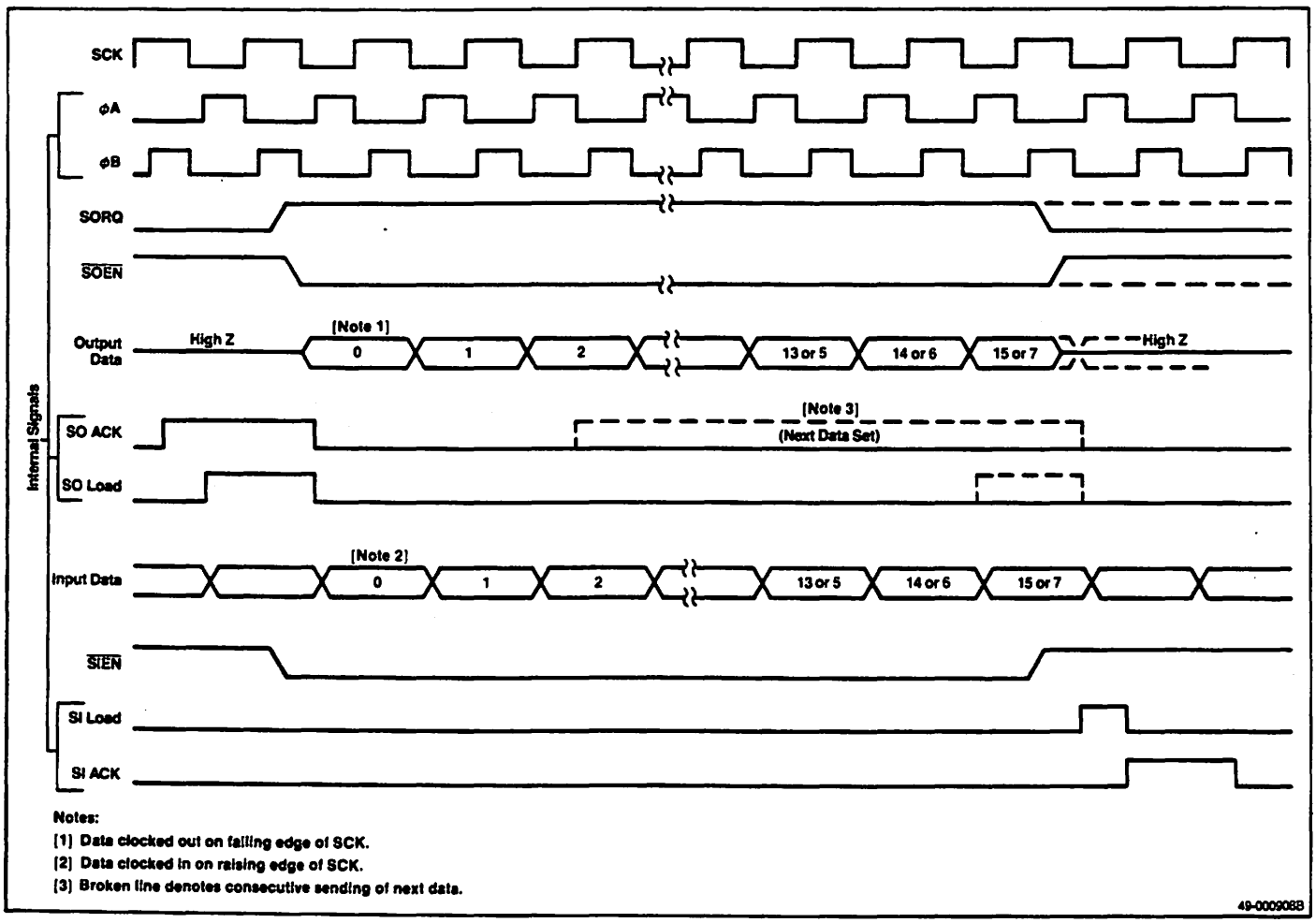


Figure 2. Serial I/O Timing



Parallel I/O

The 8-bit parallel I/O port may be used for transferring data or reading the SPI+'s status, as shown in table 2. Data transfer is handled through a 16-bit data register (DR) that is software configurable for double- or single-byte data transfers. The port is ideally suited for operating with 8080, 8085, and 8086 processor buses and may be used with other processors and computer systems.

Table 3. Parallel R/W Operation

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	Operation
1	X	X	X	No effect on internal operation; D_0-D_7 are at high impedance levels.
X	X	1	1	
0	0	0	1	Data from D_0-D_7 is latched to DR (Note1)
0	0	1	0	Contents of DR ar output to D_0-D_7 (Note1)
0	1	0	1	Illegal (SR is read only)
0	1	1	0	Eight MSBs of SR are output to D_0-D_7
0	X	0	0	Illegal (may not read and write simultaneoulsy)

Note:
(1) Eight MSBs or 8 LSBs of data register (DR) are used, depending on DR status bit (DRS). The condition of DACK = 0 is equivalent to A_0 = CS = 0.

DMA Mode Option

Parallel data transfers may be controlled (optionally) via DMA control lines DRQ and DACK. DMA mode allows high-speed transfers and reduced processor overhead. When in DMA mode, DACK input resets DRQ output when data transfer is completed. DACK also resets the RQM bit of the status register. (Note that the RQM bit is not affected by DACK in 7720).

Status Register

The status register, shown in figure 3, is a 16-bit register in which the eight most significant bits may be read by the system's microprocessor for the latest parallel data I/O status. The RQM and DRS bits can only be affected by parallel data moves. The other bits can be written to (or read) by the SPI+'s load immediate (LDI) or move (MOV) instructions. The EI bit is automatically reset when an interrupt is serviced.

Figure 3. Status Register (SR)

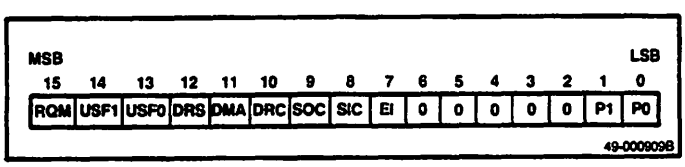


Table 4. Status Register Flags

Flag	Description
RQM (Request for Master)	A read or write form DR to IDB sets RQM = 1, An external read (write) resets RQM = 0.
USF1 and USF0 (User Flags 1 and 0)	General-purpose flags which may be read by an external processor for user-defined signaling
DRS (DR Status)	For 16-bit DR transfers (DRC = 0), DRS = 1 after first 8 bits have been transferred. DRS = 0 after all 16 bits have been transferred.
DMA (DMA Enable)	DMA = 0 (Non-DMA transfer mode) DMA = 1 (DMA transfer mode)
DRC (DR control)	DRC = 0 (16-bit mode) DRC = 1 (8-bit mode)
SOC (SO Control)	SOC = 0 (16-bit mode) SOC = 1 (8-bit mode)
SIC (SI Control)	SIC = 0 (16-bit mode) SIC = 1 (8-bit mdoe)
EI (Enable Interrupt)	EI = 0 (interrupts disabled) EI = 1 (interrupts enabled)
P1, P0 (Ports O and 1)	P0 and P1 directly control the state of output pins P_0 and P_1

Instructions

The SPI+ has three types of instructions: Load Immediate, Branch, and the multifunction OP instruction. Each type takes the form of a 24-bit word and executes in 122 ns.

Temporary Registers

The SPI+ has two 16-bit temproary registers, TR and TRB.

Instruction Timing

To control the execution of instructions, the external 8 MHz clock is divided into phases for internal execution. The various elements of the 24-bit instruction word are executed in a set order. Multiplication automatically begins first. Also, data moves from source to destination before other elements of the instruction. Data being moved on the internal data bus (IDB) is available for use in ALU operations (if P-select of the instruction specifies IDB). However, if the accumulator specified in the ASL field is also specified as the destination of the data move, the ALU operation becomes a NOP, as the data move supersedes the ALU operation.

Pointer modifications occur at the end of the instruction cycle after their values have been used for data moves. The result of multiplication is available at the end of the instruction cycle for possible use in the next instruction. If a return is specified as part of an OP instruction, it is executed last.

An assembly language OP instruction may consist of what looks like one to six lines of assembly code, but all of these lines are assembled together into one 24-bit instruction word. Therefore, the order of the six lines makes no difference in the order of execution described above. However, for understanding the SPI+'s operation and to eliminate confusion, assembly code should be written in the order described; that is: data move, ALU operations, data pointer modifications, and then return.

OP/RT Instruction Field Specification

Figure 4 illustrates the OP/RT instruction field specification. There are two instructions of this type, both of which are capable of executing all ALU functions listed in table 6. The ALU functions operate on the value specified by the P-select field (see table 5).

Besides the arithmetic functions, these instructions can also (1) modify the RAM data pointer DP, (2) modify the data ROM pointer RP, and (3) move data along the on-chip data bus from a source register to a destination register (the possible source and destination registers are listed in tables 10 and 11, respectively). The difference in the two instructions of this type is that RT executes a subroutine or interrupt return at the end of the instruction cycle, but the OP does not. Tables 6,7,8, and 9 show the ASL, DPL, DPH, and RPDCR fields, respectively.

Figure 4. OP/RT Instruction Field

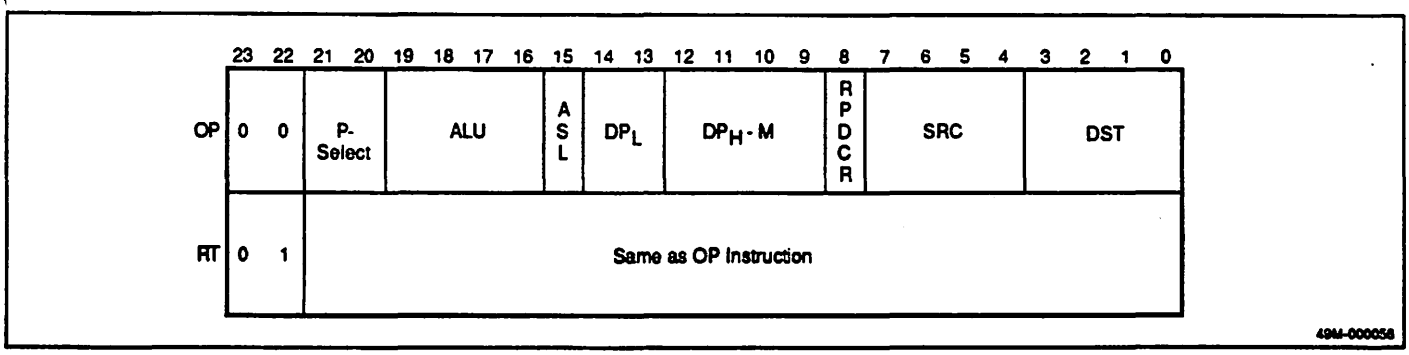


Table 5. P-Select Field

Mnemonic	D_{21}	D_{20}	ALU Input
RAM	0	0	RAM
IDB	0	1	Internal Data Bus (Note 1)
M	1	1	M Register
N	1	1	N Register

Note:
(1) Any value on the on-chip data bus. Value may be selected from any of the registers listed in table 6 source register selections.

Table 6. ALU Field

Mnemonic	D_{19}	D_{18}	D_{17}	D_{16}	ALU Function	SA1 SB1	SA0 SB0	CA CB	ZA AB	OVA1 OVB1	OVA0 OVB0
NOP	0	0	0	0	No operation	-	-	-	-	-	-
OR	0	0	0	1	OR	X	Δ	0	Δ	0	0
AND	0	0	1	0	AND	X	Δ	0	Δ	0	0
XOR	0	0	1	1	Exclusive OR	X	Δ	0	Δ	0	0
SUB	0	1	0	0	Subtract	Δ	Δ	Δ	Δ	Δ	Δ
ADD	0	1	0	1	ADD	Δ	Δ	Δ	Δ	Δ	Δ
SBB	0	1	1	0	Subtract with borrow	Δ	Δ	Δ	Δ	Δ	Δ
ADC	0	1	1	1	Add with carry	Δ	Δ	Δ	Δ	Δ	Δ
DEC	1	0	0	0	Decrement ACC	Δ	Δ	Δ	Δ	Δ	Δ
INC	1	0	0	1	Increment ACC	Δ	Δ	Δ	Δ	Δ	Δ
CMP	1	0	1	0	Complement ACC (one's complement)	X	Δ	0	Δ	0	0
SHR1	1	0	1	1	1-Bit right shift	X	Δ	Δ	Δ	0	0
SHL1	1	1	0	0	1-Bit left shift	X	Δ	Δ	Δ	0	0
SHL2	1	1	0	1	2-Bit left shift	X	Δ	0	Δ	0	0
SHL4	1	1	1	0	4-Bit left shift	X	Δ	0	Δ	0	0
XCHG	1	1	1	1	8-Bit exchange	X	Δ	0	Δ	0	0

Table 7. ASL Field

Mnemonic	D_{15}	ACC Selection
ACCA	0	ACCA
ACCB	1	ACCB

Table 8. DPL Field

Mnemonic	D_{14}	D_{13}	Low DP Modify (DP_3-DP_0)
DPNOP	0	0	No operation
DPINC	0	1	Increment DPL
DPDEC	1	0	Decrement DPL
DPCLR	1	1	Clear DPL

Table 9. DPH Field

Mnemonic	D_{12}	D_{11}	D_{10}	D_9	High DP Modify
M0	0	0	0	0	Exclusive OR of DPH (DP_7 - DP_4) with the mask defined by the three bits (D_{12} - D_9) of the field
M1	0	0	0	1	
M2	0	0	1	0	
M3	0	0	1	1	
M4	0	1	0	0	
M5	0	1	0	1	
M6	0	1	1	0	
M7	0	1	1	1	
M8	1	0	0	0	
M9	1	0	0	1	
MA	1	0	1	0	
MB	1	0	1	1	
MC	1	1	0	0	
MD	1	1	0	1	
ME	1	1	1	0	
MF	1	1	1	1	

Table 10. RPDCR Field

Mnemonics	D8	RP Operation
RPNOP	0	No operation
RPDEC	1	Decrement RP

Table 11. SRC Field

Mnemonic	D_7	D_6	D_5	D_4	Source Register
NON/TRB	0	0	0	0	TRB (Note 1)
A	0	0	0	1	ACCA (Accumulator A)
B	0	0	1	1	ACCB (Accumulator B)
TR	0	0	1	1	TR temporary register
DP	0	1	0	0	DP data pointer
RP	0	1	0	1	RP ROM pointer
RO	0	1	1	0	RO ROM output data
SGN	0	1	1	1	SGN sign register
DR	1	0	0	1	DR data register
DRNF	1	0	0	1	DR no flag (Note 2)
SR	1	0	1	1	SI serial in MSB (Note 2)
SIM	1	0	1	1	SI serial in MSB (Note 3)
SIL	1	1	0	0	SI serial in LSB (Note 4)
K	1	1	0	1	K register
L	1	1	1	0	L register
MEM	1	1	1	1	RAM

Notes:

(1) The contents of the TRB register are also output if NON is specified.
(2) FR to IDB, RQM not set. In DMA not set.
(3) First bit in goes to MSB, last bit to LSB.
(4) First bit goes to LSB, last bit to MSB (bit reversed).

Jump/Call/Branch

Figure 5 shows the JP instruction field specification.

Three types of program counter modifications are accommodated by the SPI+ and are listed in table 12. All the instructions, if unconditional or if the specified condition is true, take their next program execution address from the next address field (NA); otherwise, PC = PC + 1.

Figure 5. JP Instruction Field Specification

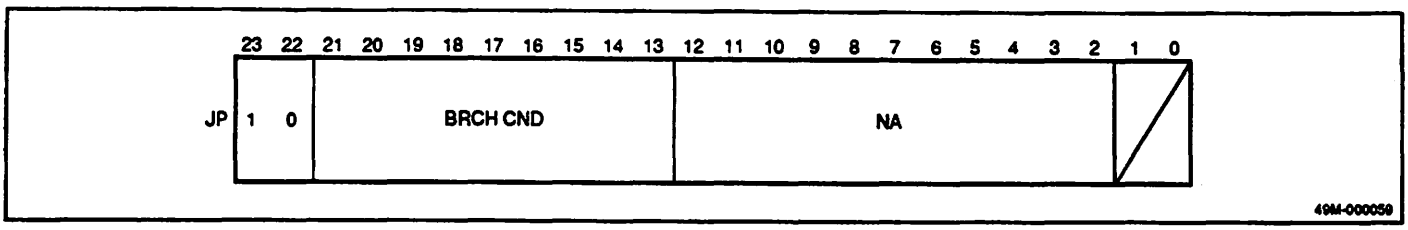


Table 12. BRCH Field

D_{20}	D_{19}	D_{18}	Branch Instruction
1	0	0	Unconditional jump
1	0	1	Subroutine Call
0	1	0	Conditional jump

Load Data [LDI]

Figure 6 shows the LD instruction field specification.

The load data instruction will take the 16-bit value contained in the immediate data field (ID) and place it in the register specified by the destination field (DST) (see table 11).

Figure 6. LD Instruction Field Specification

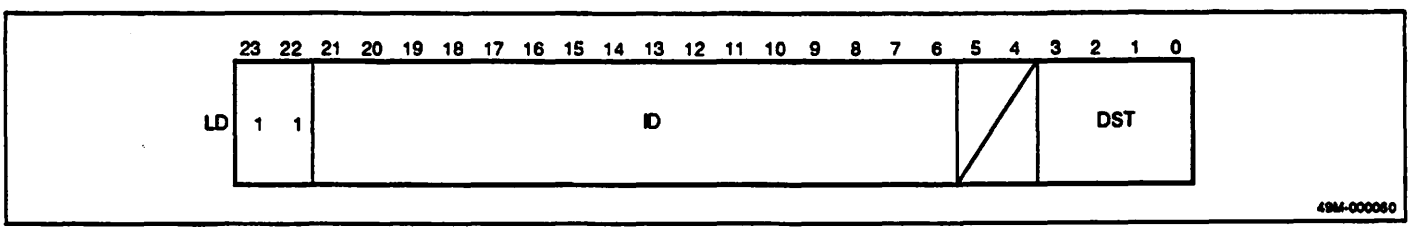


Table 13. DST Field

Mnemonic	D_3	D_2	D_1	D_0	Destination Register
@NON	0	0	0	0	No register
@A	0	0	0	1	ACCA (Accumulator A)
@B	0	0	1	0	ACCB (Accumulator B)
@TR	0	0	1	1	TR temporary register
@DP	0	1	0	0	DP data pointer
@RP	0	1	0	1	RP ROM pointer
@DR	0	1	1	0	DR data register
@SR	0	1	1	1	SR status register
@SOL	1	0	0	0	SO serial out LSB (Note 1)
@SOM	1	0	0	1	SO serial out MSB (Note 2)
@K	1	0	1	0	K (Mult)
@KLR	1	0	1	1	IDB -> K, ROM -> L (Note 3)
@KLM	1	1	0	0	Hi RAM -> K, IDB-> L (Note 4)
@L	1	1	0	1	L Register
@TRB	1	1	1	0	TRB Register
@MEM	1	1	1	1	RAM

Notes:

(1) LSB is first bit out.
(2) MSB is first bit out.
(3) Internal data bus to K, and ROM to L register
(4) Contents of RAM address specified by $DP_6 = 1$, is placed in K register, IDB is placed in L (that is, 1, DP_5, DP_4, DP_3-DP_0).

Table 14. BRCH/CND Fields

Mnemonic	BRCH Field									Condition
	D_{21}	D_{20}	D_{19}	D_{18}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	
JMP	1	0	0	0	0	0	0	0	0	Unconditional jump
CALL	1	0	1	0	0	0	0	0	0	Unconditional call
JNCA	0	1	0	0	0	0	0	0	0	CA = 0
JCA	0	1	0	0	0	0	0	1	0	CA = 1
JNCB	0	1	0	0	0	0	1	0	0	CB = 0
JCB	0	1	0	0	0	0	1	1	0	CB = 1
JNZA	0	1	0	0	0	1	0	0	0	ZA = 0
JZA	0	1	0	0	0	1	0	1	0	ZA = 1
JNZB	0	1	0	0	0	1	1	0	0	ZB = 0
JZB	0	1	0	0	0	1	1	1	0	ZB = 1
JNOVA0	0	1	0	0	1	0	0	0	0	OVA0 = 0
JOVA0	0	1	0	0	1	0	0	1	0	OVA0 = 1
JNOVB0	0	1	0	0	1	0	1	0	0	OVB0 = 0
JOVB0	0	1	0	0	1	0	1	1	0	OVB0 = 1
JNOVA1	0	1	0	0	1	1	0	0	0	OVA1 = 0
JOVA1	0	1	0	0	1	1	0	1	0	OVA1 = 1
JNOVB1	0	1	0	0	1	1	1	0	0	OVB1 = 0
JOVB1	0	1	0	0	1	1	1	1	0	OVB1 = 1
JNSA0	0	1	0	1	0	0	0	0	0	SA0 = 0
JSA0	0	1	0	1	0	0	0	1	0	SA0 = 1
JNSB0	0	1	0	1	0	0	1	0	0	SB0 = 0
JSB0	0	1	0	1	0	0	1	1	0	SB0 = 1
JNSA1	0	1	0	1	0	1	0	0	0	SA1 = 0
JSA1	0	1	0	1	0	1	0	1	0	SA1 = 1
JNSB1	0	1	0	1	0	1	1	0	0	SB1 = 0
JSB1	0	1	0	1	0	1	1	1	0	SB1 = 1
JDPL0	0	1	0	1	1	0	0	0	0	DPL = 0
JDPLN0	0	1	0	1	1	0	0	0	1	DPL ≠ 0
JDPLF	0	1	0	1	1	0	0	1	0	DPL = F (hex)
JDPLNF	0	1	0	1	1	0	0	1	1	DPL ≠ F (hex)
JNSIAK	0	1	0	1	1	0	1	0	0	SI ACK = 0
JSIAK	0	1	0	1	1	0	1	1	0	SI ACK = 1
JNSOAK	0	1	0	1	1	1	0	0	0	SO ACK = 0
JSOAK	0	1	0	1	1	1	0	1	0	SO ACK = 1
JNRQM	0	1	0	1	1	1	1	0	0	RQM = 0
JRQM	0	1	0	1	1	1	1	1	0	RQM = 1

Absolute Maximum Ratings
(T_A = 25°C unless otherwise specified)

ITEM	SYMBOL	RATING	UNIT
Voltage (V_{DD} PIN)	V_{DD}	-0.5 to 7.0 (1)	V
Voltage, Any Input	VI	-0.5 to V_{DD} +0.5 (1)	V
Voltage, Any Output	VO	-0.5 to V_{DD} +0.5 (1)	V
Storage Temperature	Tstg	-65 to 150	°C

Note: (1) With respect to GND

Recomended Operating Conditions

Parameter	Symbol	Limits			Unit	Test Conditions
		MIN	TYP	MAX		
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
Low-Level Input Voltage	V_{IL}	- 0.3		0.8	V	
High-Level Input Voltage	V_{IH}	2.2		V_{DD} +0.3	V	
Low-Level CLK Input Voltage	V_{ILC}	- 0.3		0.5	V	
High-Level CLK Input Voltage	V_{IHC}	3.5		V_{DD} +0.3	V	
Operating Temperature	Tstg	- 40	25	85	°C	Free Air

DC Characterostocs

T_A = 25 + 85°C; V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Limits			Unit	Test Conditions
		MIN	TYP	MAX		
Low-Level Output Voltage	V_{OL}			0.45	V	
High-Level Output Voltage	V_{OH}	0.7 V_{DD}			V	
Low-Level Input Leak Current	V_{LIL}			-10	µA	V_{IN} = 0V
High-Level Input Leak Current	V_{LIH}			10	µA	V_{IN} = V_{DD}
Low-Level Ouput Leak Current	V_{LOL}			-10	µA	V_{OUT} = 0.47 V
High-Level Output Leak Current	V_{LOH}			10	µA	V_{OUT} = V_{DD}
Supply Current *	I_{DD}			40	mA	f_{CLK} = 8.192 MHz

Capacitance

T_A = 25°C; V_{DD} =0 V

Parameter	Symbol	Limits			Unit	Test Conditions
		MIN	TYP	MAX		
CLK, SCK Capacitance	C ϕ			20	pF	fc = 1 MHz
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Clock Timing Requirements

T_A = -40 to +85°C; V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Limits			Unit	Test Conditions
		MIN	TYP	MAX		
CLK Cycle Time	t_{CYC}	120	122	2000	ns	
CLK High Pulse Width	t_{CCL}	40			ns	
CLK Low Pulse Width	t_{CCH}	40			ns	
CLK Rise Time	t_{CR}			20	ns	
CLK Fall Time	t_{CF}			20	ns	
SCK Cycle Time	t_{CYS}	240	244		ns	
SCK High Pulse Width	t_{SSL}	100			ns	
SCK Low Pulse Width	t_{SSR}	100			ns	
SCK Rise Time	t_{SR}			20	ns	
SCK Fall Time	t_{SF}			20	ns	

Figure 7. Input/Output Voltage Reference Levels

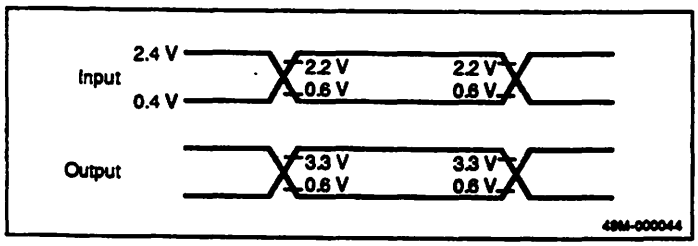
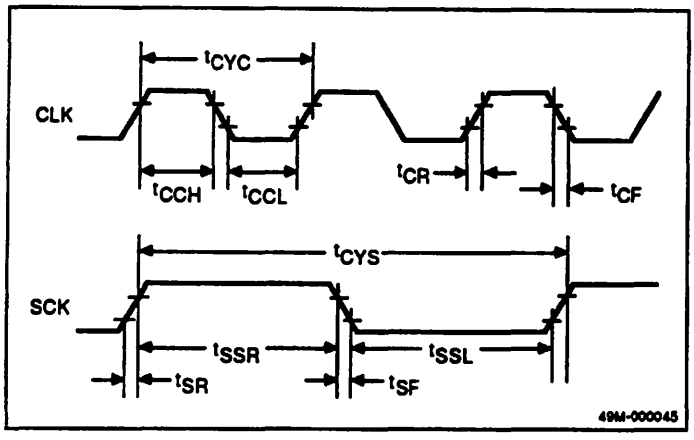


Figure 8. Clock Timing (Clock Input)



Host Interface Timing Requirements

T_A = -40 to +85°C; V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Limits			Unit	Test Conditions
		MIN	TYP	MAX		
AO, $\overline{CS}$, $\overline{DACK}$ Setup time for $\overline{RD}$	t_{SAR}	0			ns	
AO, $\overline{CS}$, $\overline{DACK}$ Hold time for $\overline{RD}$	t_{HAR}	0			ns	
$\overline{RD}$ Pulse Width	t_{WRD}	150			ns	
AO, $\overline{CS}$, $\overline{DACK}$ Setup time for $\overline{WR}$	t_{SAW}	0			ns	
AO, $\overline{CS}$, $\overline{DACK}$ Hold time for $\overline{WR}$	t_{HWA}	0			ns	
$\overline{WR}$ Pulse Width	t_{WWR}	150			ns	
Data Setup Time for $\overline{WR}$	t_{SDW}	100			ns	
Data Hold Time for $\overline{WR}$	t_{HWD}	0			ns	
$\overline{RD}$, $\overline{WR}$ Recovery Time	t_{RV}	100			ns	
$\overline{DACK}$ Hold time for $\overline{DRQ}$	t_{HRQA}	9.5tctk			ns	

Switching Characteristics

T_A = -40 to +85°C; V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Limits			Unit	Test Conditions
		MIN	TYP	MAX		
$\overline{RD}$ ↓ + Data Delay Time	t_{DRD}			100	ns	
$\overline{RD}$ ↑ + Data Float Time	t_{FRD}	10		85	ns	
CLK ↑ + DRQ Delay Time	t_{DARQ}			100	ns	
$\overline{DACK}$ ↓ + DRQ Delay Time	t_{DARQ}			110	ns	
CLK ↑ + P0, P1 Delay Time	t_{DCF}			100	ns	

Figure 9. Host Read Operation

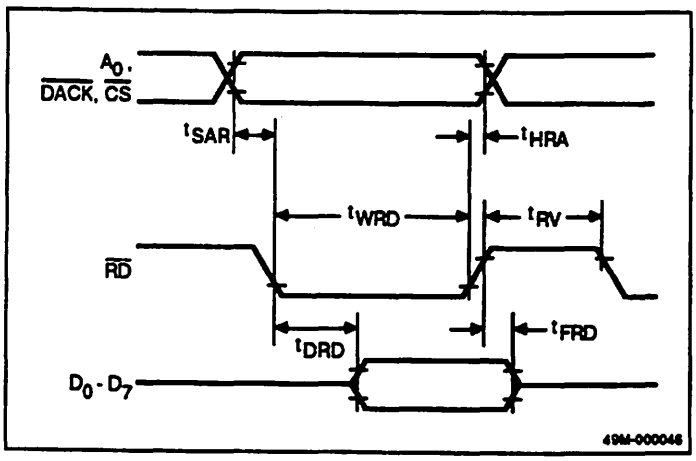


Figure 10. Host Write Operation

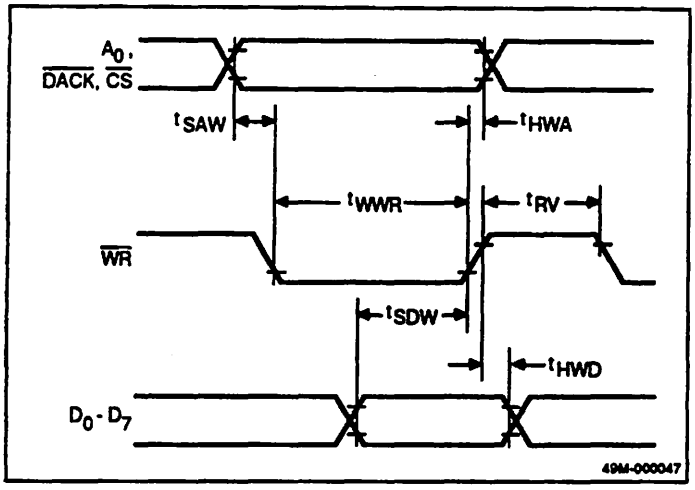


Figure 11. Port Operation

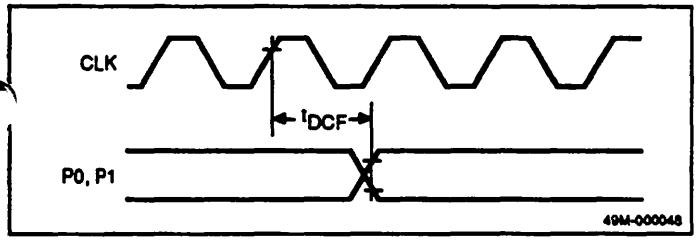


Figure 12. DMA Operation-1 8bit Mode

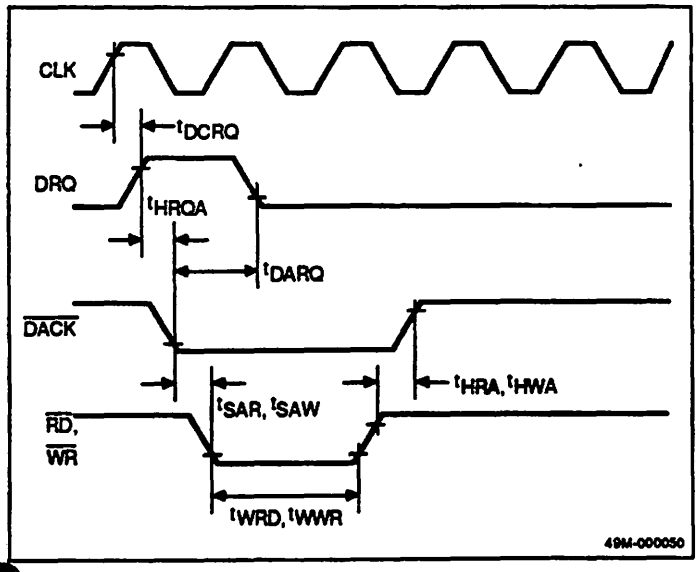


Figure 13. DMA Operation-2 16bit Mode

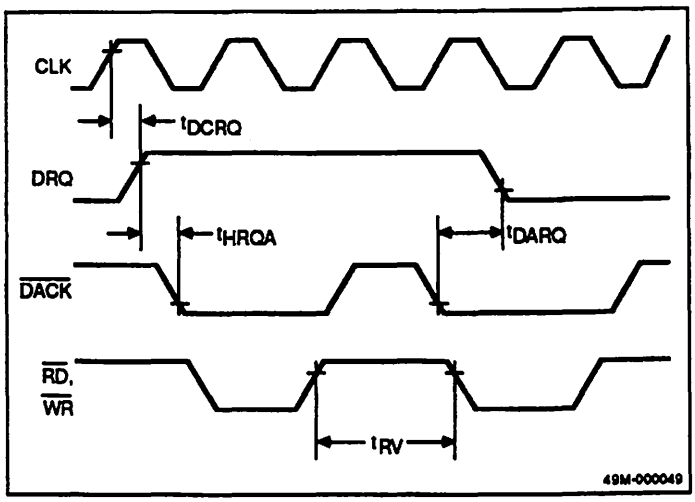
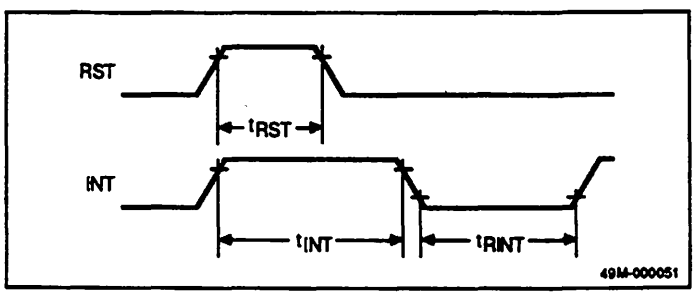


Figure 14. Reset and Interrupt Timing



Interrupt Reset Timing Requirements

T_A = -40 to +85°C; V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Limits			Unit	Test Conditions
		MIN	TYP	MAX		
RST Pulse Width	t_{RST}	$4t_{CYC}$			ns	
INT Pulse Width	t_{INT}	$3t_{CYC}$			ns	
INT Recovery Time	t_{RINT}	$2t_{CYC}$			ns	

Serial Timing

Please refer to the uPD77C20A/7720A/77P20 Data Sheet for a text discussion of serial timing cases.

Serial Interface Timing Requirements

T_A = -40 to +85°C; V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Limits			Unit	Test Conditions
		MIN	TYP	MAX		
$\overline{SIEN}$, SI Setup Time for SCK	t_{SSIS}	55			ns	
$\overline{SIEN}$, SI Hold Time for SCK	t_{HSIS}	30			ns	
$\overline{SOEN}$ Setup Time for SCK	t_{SSES}	50			ns	
$\overline{SOEN}$ Hold Time for SCK	t_{HSSE}	30			ns	
$\overline{SIEN}$, $\overline{SOEN}$ Recovery Time	t_{SRV}	t_{CYS}			ns	

Switching Characteristics

T_A = -40 to +85°C; V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Limits			Unit	Test Conditions
		MIN	TYP	MAX		
SCK ↑ + SORQ Delay Time	t_{DSSQ}	30		150	ns	
$\overline{SOEN}$ ↓ + SO Delay Time	t_{DSESO}			60	ns	
$\overline{SOEN}$ ↑ + SO Float Time	t_{FSESO}	30		150	ns	
SCK ↓ + SO Dealy Time	t_{DSLSO}			60	ns	
SCK ↓ + SO Hold Time	t_{HSLSO}	0			ns	
SCK ↑ + SO Dealy Time	t_{DSHSO}			60	ns	
SCK ↑ + SO Float Time*	t_{FSSO}	70		300	ns	

* Will be changed

Figure 15. Serial Input Operation

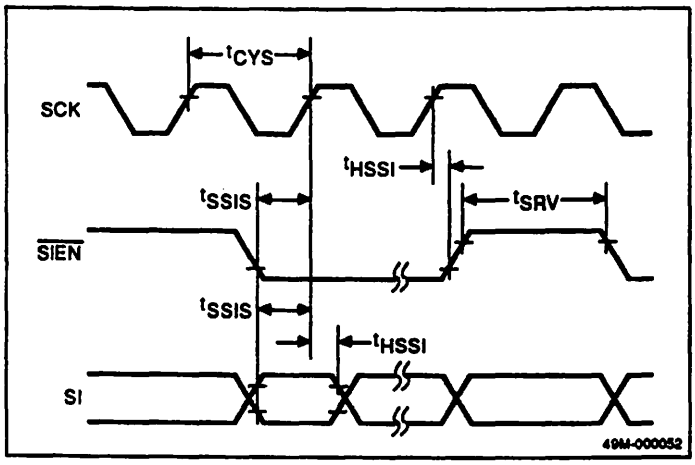


Figure 16. Serial Output Operation (Case #1) $\overline{SOEN}$ asserted in response to SORQ when SCK is low.

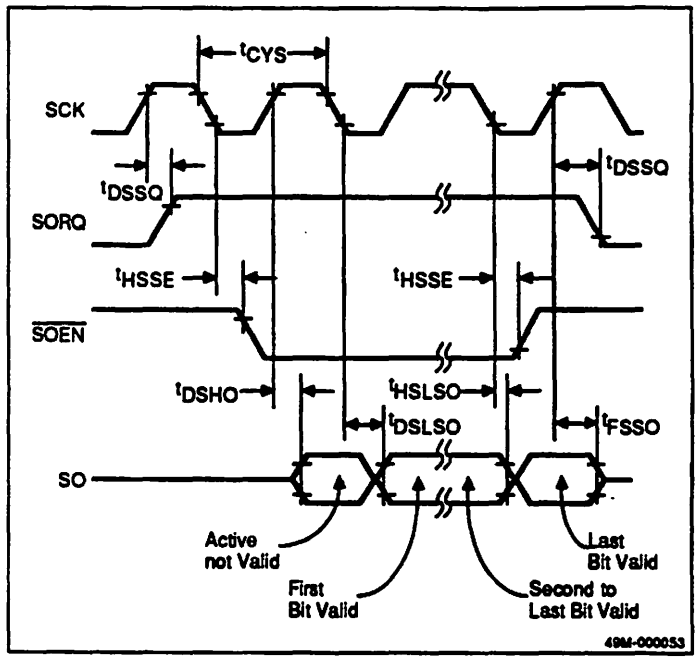


Figure 17. Serial Output Operation (Case #2) $\overline{SOEN}$ asserted in response to SORQ when SCK is high.

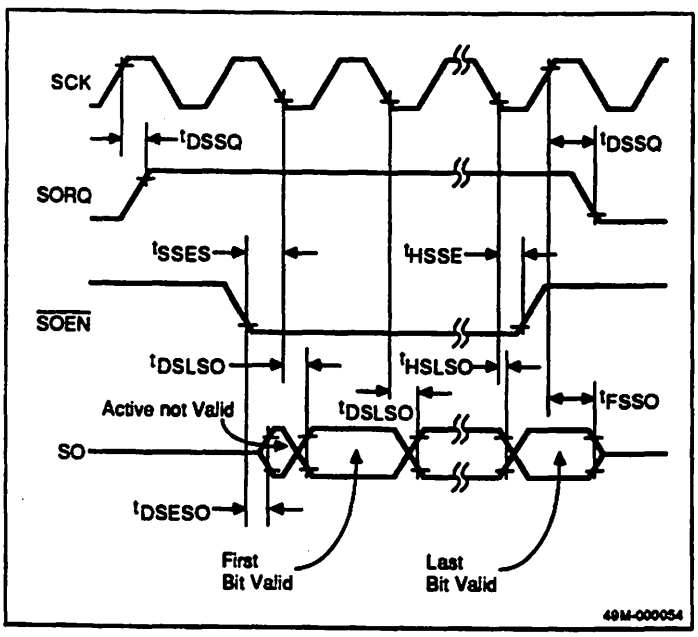


Figure 18. Serial Output Operation (Case #3) $\overline{SOEN}$ active before SORQ high.

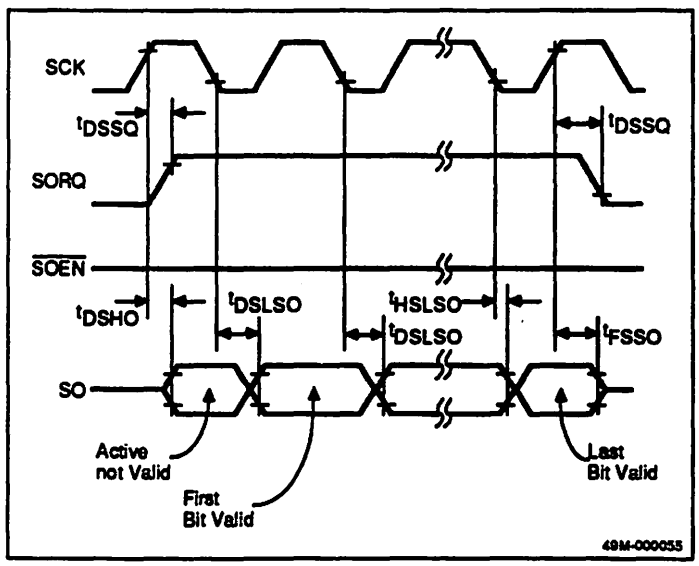


Figure 19. Serial Output Operation (Case #4a) $\overline{SOEN}$ is released in the middle of a transfer during SCK high.

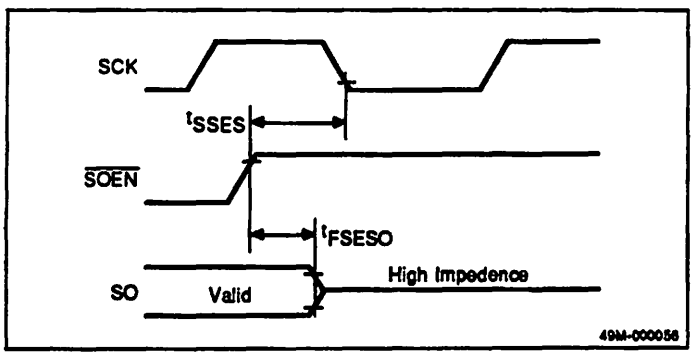
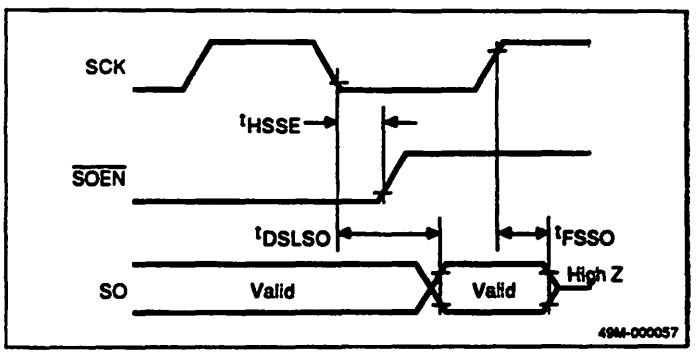


Figure 20. Serial Output Operation (Case #4b) $\overline{SOEN}$ is released in the middle of a transfer during SCK high.



uPD77P25 UV Erasable EPROM Version

During normal operation the 77C25 operates from a single +5 volt power supply and can accordingly be used in any 77C25 masked ROM application.

During programming, however, pin functions are entirely different, as shown in table 14.

Table 15. Pin Functions for Writing/Reading UVEPROM

Pin Name	DIP Pin No.	Pin Name for normal operation	Function
A_0	27	A0	
A_1	24	WR	
A_2	23	SORQ	
A_3	22	SO	
A_4	21	SI	Input address (viewed from external device) for writing/ reading UVEPROM (instruction ROM and data ROM).
A_5	20	SOEN	
A6	19	SIEN	
A_7	18	SCK	
A_8	17	INT	
A_9	15	CLK	
A_{10}	5	P_1	
A_{11}	4	P_0	
A_{12}	3	DRQ	
A_{13}	2	DACK	
D_0 - D_7	6 - 13	D_0 - D_7	Inputs/outputs data for UVEPROM (instruction ROM and data ROM)
$\overline{CE}$	26	$\overline{CS}$	UVEPROM write strobe signal (active low)
$\overline{OE}$	25	$\overline{RD}$	UVEPROM read strobe signal active low)
V_{PP}	1	V_{PP}	Power pin for writing UVEPROM. Apply +12.5V for writing and +5V for reading.
V_{DD}	28	V_{DD}	Power pin. Apply +6V for writing and +5V for reading.
GND	14	GND	Ground pin
-	16	RST	Sets UVEPROM write or read mode. Mode is set when +12.0V is applied.

Development Tools

For software development and assembly into object code, a relocatable assembler (RA77C25) is available. This software is (or will be) available to run on MS/DOS, CCP/M, VAX/VMX, and VAX/UNIX systems. For debugging, a hardware emulator (Evakit-77C25) provides in-circuit real-time emulation of the SPI+++. Some of the features of the Evakit-77C25 include: break/step emulation, symbolic debugging, and on-line assembly/disassembly of code. The Evakit-77C25 connects via a probe to your target system for test and demonstration of your final system design. The Evakit also connects to your host development system via an RS232 port. Using Kermit or NEC's EVA communications program, code can be down-loaded or up-loaded between development system and Evakit.

By connecting to a PROM programmer, the Evakit is also used to prepare uPD77P25 UVEPROMs which are intended for prototyping and small volume applications.

Code submittal for the mask ROM uPD77C25 is accomplished by preparing a 27C256A PROM using the same programming device as for the uPD77P25.

System Configuration

Figures 21, 22, 23, and 24 show typical system applications for the 77C25/77P25.

Figure 21. Spectrum Analysis System

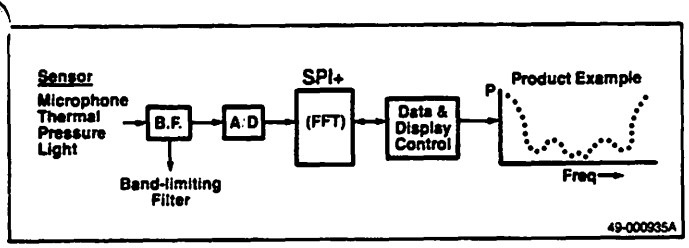


Figure 22. Analog-to-Analog Digital Processing System Using A single SPI+

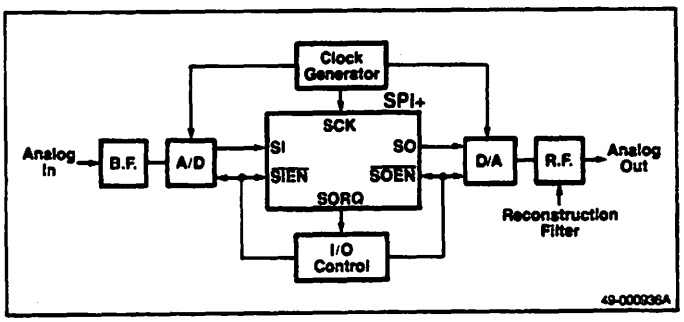


Figure 23. Signal Processing System Using Cascaded SPI+s and Serial Communication

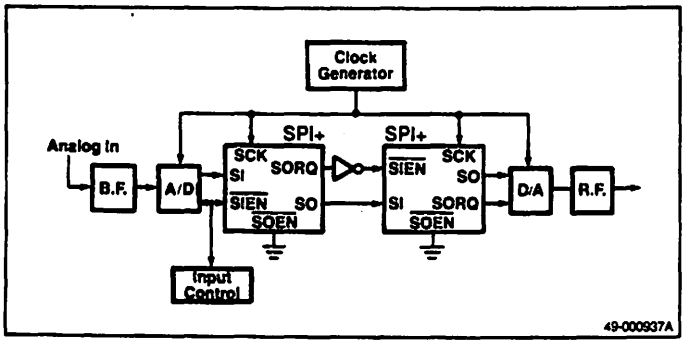
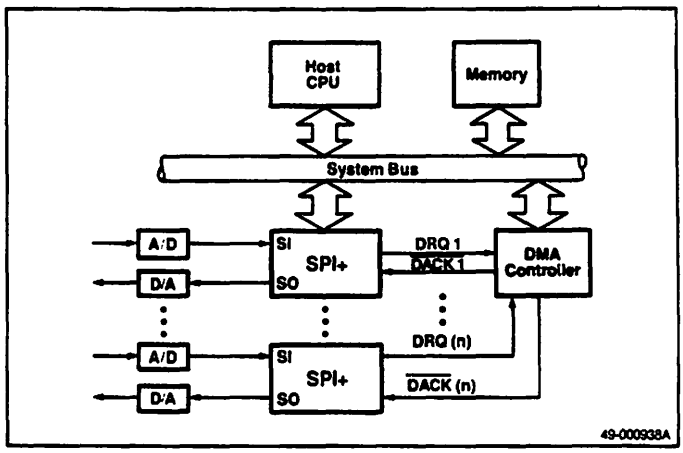
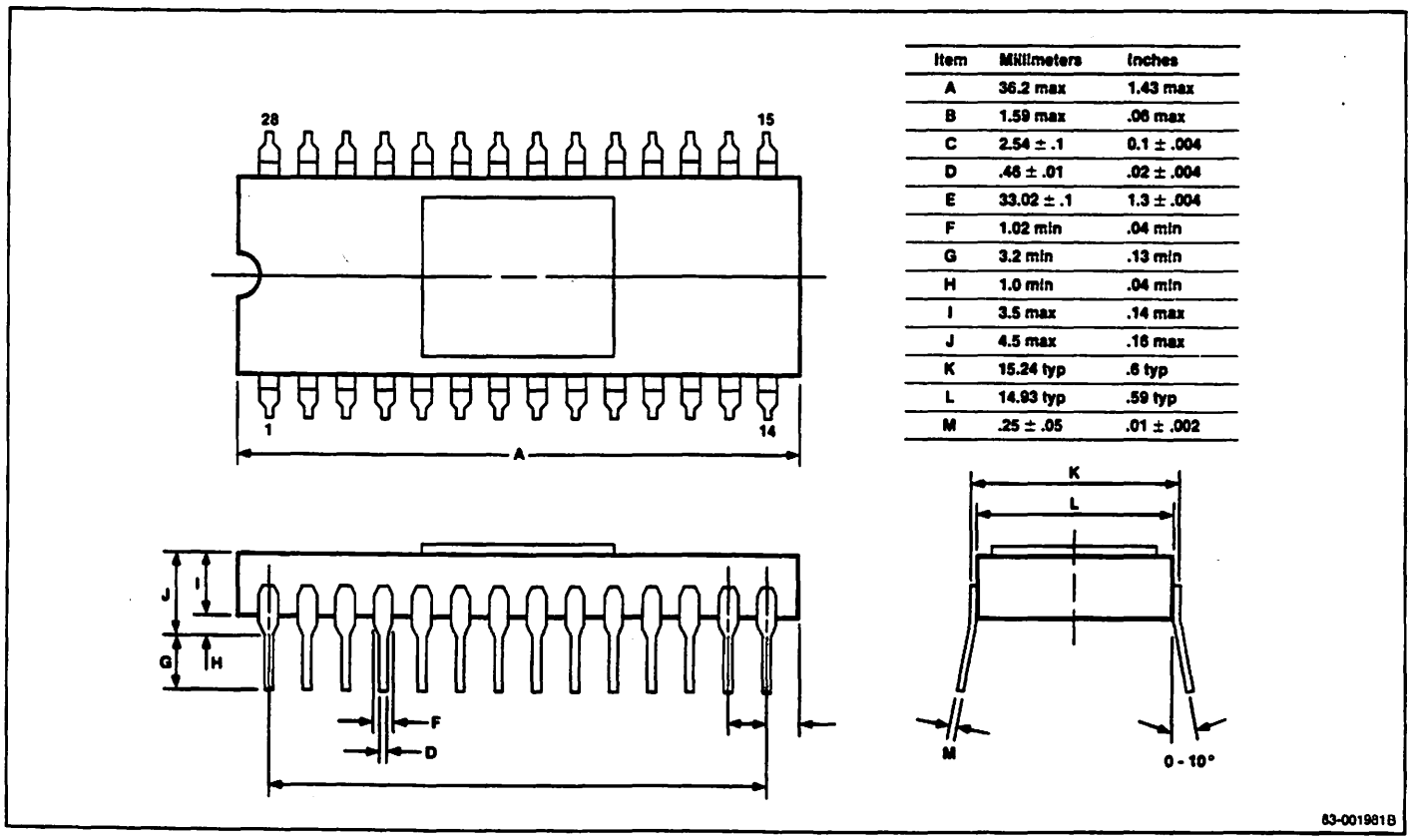


Figure 24 Signal Processing system Using SPI+s as a Complex Computer Peripheral



28-pin Ceramic DIP

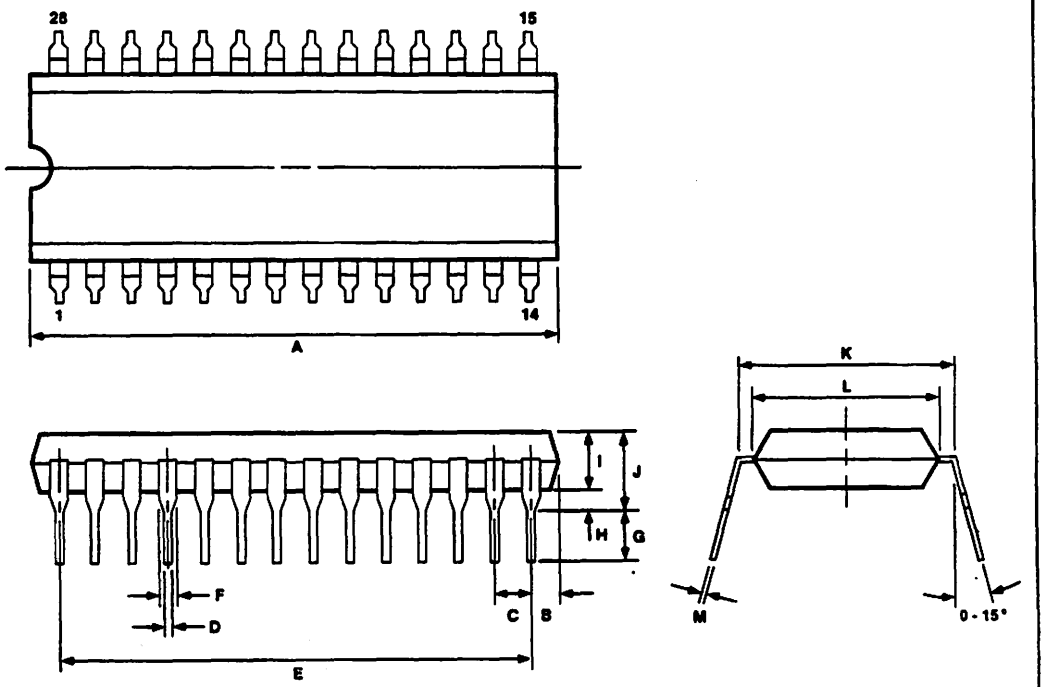


Item	Millimeters	Inches
A	36.2 max	1.43 max
B	1.59 max	.06 max
C	2.54 ± .1	0.1 ± .004
D	.46 ± .01	.02 ± .004
E	33.02 ± .1	1.3 ± .004
F	1.02 min	.04 min
G	3.2 min	.13 min
H	1.0 min	.04 min
I	3.5 max	.14 max
J	4.5 max	.18 max
K	15.24 typ	.6 typ
L	14.93 typ	.59 typ
M	.25 ± .05	.01 ± .002

28-pin Plastic DIP

Item	Millimeters	Inches
A	38.1 max	1.5 max
B	2.54 max	.10 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	33.02	1.3
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.72 max	.226 max
K	15.24 [TP]	.60 [TP]
L	13.2	.52
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.



83-001407B

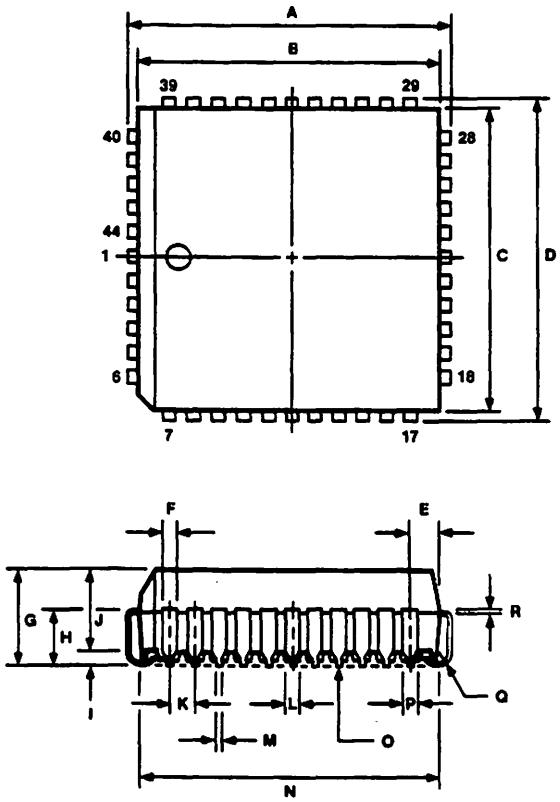
44-pin PLCC (Plastic Leaded Chip Carrier)

Item	Millimeters	Inches
A	17.5 +.2	.689 ±.008
B	16.58	.653
C	16.58	.653
D	17.5 ±.2	.689 ±.008
E	1.94 ±.15	.076 $^{+.007}_{-.006}$
F	.6	.024
G	4.4 ±.2	.173 $^{+.009}_{-.008}$
H	2.8 ± .2	.110 $^{+.009}_{-.008}$
I	.7 min	.028 min
J	3.6	.142
K	1.27 [TP] Note 1	.050 [TP]
L	.7	.028
M	.40 ± .10	.016 $^{+.004}_{-.005}$
N	15.50 ± .20	.610 $^{+.009}_{-.008}$
O	.15 Note 2	.006
P	1.0	.040
Q	R .8	R .031
R	.20 $^{+.10}_{-.05}$	.008 $^{+.004}_{-.002}$

Note:

[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.

[2] Flat within .15 mm [.006 inch] total.



83-003790B

Note: 28-Pin Ceramic DIP with window to be added.

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