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STM32L4P5xx

Ultra-low-power Arm®Cortex®-M4 32-bit MCU+FPU, 150 DMIPS, up to 1-MB Flash memory, 320-KB SRAM, LCD-TFT, ext. SMPS

Datasheet - preliminary data

Features

Ultra-low-power with FlexPowerControl

- 1.71 V to 3.6 V power supply
- -40 °C to 85/125 °C temperature range
- Batch acquisition mode (BAM)
- 305 nA in VBAT mode: supply for RTC and 32x32-bit backup registers
- 33 nA Shutdown mode (5 wakeup pins)
- 125 nA Standby mode (5 wakeup pins)
- 420 nA Standby mode with RTC
- 2.8 µA Stop 2 with RTC
- 110 µA/MHz Run mode (LDO mode)
- 43 µA/MHz Run mode (@ 3.3 V SMPS mode)
- 5 µs wakeup from Stop mode
- Brownout reset (BOR) in all modes except shutdown

Core

- Arm® 32-bit Cortex®-M4 CPU with FPU, adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory, frequency up to 120 MHz, MPU, 150 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions

Memories

- 1-Mbyte Flash, 2 banks read-while-write, proprietary code readout protection
- 320 Kbytes of SRAM including 64 Kbytes with hardware parity check
- External memory interface for static memories supporting SRAM, PSRAM, NOR, NAND and FRAM memories
- 2 x OctoSPI memory interface

General-purpose inputs/outputs

- Up to 136 fast I/Os, most 5 V-tolerant, up to 14 I/Os with independent supply down to 1.08 V

Performance benchmark

- 1.25 DMIPS/MHz (Drystone 2.1)
- 409.20 Coremark® (3.41 Coremark/MHz @120 MHz)

Energy benchmark

- 233 ULPMark™CP score
- 56.5 ULPMark™PP score

Up to 24 capacitive sensing channels

- Support touchkey, linear and rotary touch sensors

Clock management

- 4 to 48 MHz crystal oscillator
- 32 kHz crystal oscillator for RTC (LSE)
- Internal 16 MHz factory-trimmed RC (±1%)
- Internal low-power 32 kHz RC (±5%)
- Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
- Internal 48 MHz with clock recovery
- 3 PLLs for system clock, USB, audio, ADC

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This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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Interconnect matrix

- 1 AHB bus matrix

14-channel DMA controller

23 communication peripherals

- USB OTG 2.0 full-speed, LPM and BCD
- 2x SAIs (serial audio interface)
- 4x I2C FM+(1 Mbit/s), SMBus/PMBus
- 6x USARTs (ISO 7816, LIN, IrDA, modem)
- 3x SPIs (5x SPIs with the dual OctoSPI)
- CAN (2.0B Active) and 2x SDMMC
- 8- to 14-bit camera interface up to 32 MHz (black and white) or 10 MHz (color)
- 8-/16-bit parallel synchronous data input/output slave interface (PSSI)

11 analog peripherals (independent supply)

- 2x 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
- 2x 12-bit DAC, low-power sample and hold
- 2x operational amplifiers with built-in PGA
- 2x ultra-low-power comparators
- 2x digital filters for sigma delta modulator
- 1x temperature sensor

Advanced graphics features

- Chrom-ART Accelerator™ (DMA2D) for enhanced graphic content creation
- LCD-TFT controller

16x timers and watchdog

- 2 x 16-bit advanced motor-control
- 2 x 32-bit general purpose timers
- 5 x 16-bit general purpose timers
- 2x 16-bit basic timers
- 2x low-power 16-bit timers (available in Stop mode)
- 2x watchdogs
- 1x SysTick timer
- RTC with HW calendar, alarms and calibration

True random generator

CRC calculation unit

HASH (SHA-256) hardware accelerator

Debug mode

- Serial wire debug (SWD)
- JTAG
- Embedded Trace Macrocell (ETM)

96-bit unique ID

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Table 1. Device summary

Reference	Part numbers
STM32L4P5xx	STM32L4P5CG, STM32L4P5RG, STM32L4P5VG, STM32L4P5QG, STM32L4P5ZG, STM32L4P5AG, STM32L4P5CE, STM32L4P5RE, STM32L4P5VE, STM32L4P5QE, STM32L4P5ZE, STM32L4P5AE

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Contents

1 Introduction 14

2 Description 15

3 Functional overview 19

3.1 Arm® Cortex®-M4 core with FPU 19

3.2 Adaptive real-time memory accelerator (ART Accelerator™) 19

3.3 Memory protection unit (MPU) 19

3.4 Memories 20

3.4.1 Embedded Flash memory 20

3.4.2 Embedded SRAM 21

3.5 Boot modes 22

3.6 Firewall 22

3.7 Power supply management 23

3.7.1 Power supply schemes 23

3.7.2 Power supply supervisor 26

3.7.3 Voltage regulator 26

3.7.4 Low-power modes 28

3.7.5 Reset mode 36

3.7.6 VBAT operation 36

3.8 Peripheral and interconnect matrix 36

3.9 Reset and clock controller (RCC) 38

3.10 Clock recovery system (CRS) 41

3.11 General-purpose inputs/outputs (GPIOs) 41

3.12 Multi-AHB bus matrix 41

3.13 Direct memory access controller (DMA) 42

3.14 DMA request router (DMAMux) 44

3.15 Chrom-ART Accelerator™ (DMA2D) 44

3.16 Interrupts and events 44

3.16.1 Nested vectored interrupt controller (NVIC) 44

3.16.2 Extended interrupt/event controller (EXTI) 45

3.17 Cyclic redundancy check calculation unit (CRC) 45

ST Restricted DRAFT

ST RESTRICTED – SUBJECT TO NON-DISCLOSURE AGREEMENT – DO NOT COPY

3.18 Flexible static memory controller (FSMC) 45
3.19 Octo-SPI interface (OCTOSPI) 46
3.20 Octo-SPI IO manager (OCTOSPIIOM) 47
3.21 Analog-to-digital converter (ADC) 48
3.21.1 Temperature sensor 48
3.21.2 Internal voltage reference (VREFINT) 49
3.21.3 VBAT battery voltage monitoring 49
3.22 Digital to analog converter (DAC) 49
3.23 Voltage reference buffer (VREFBUF) 50
3.24 Comparators (COMP) 50
3.25 Operational amplifier (OPAMP) 51
3.26 Digital filter for sigma-delta modulators (DFSDM) 51
3.27 Digital camera interface (DCMI) 52
3.28 LCD-TFT controller (LTDC) 53
3.29 Touch sensing controller (TSC) 53
3.30 Random number generator (RNG) 54
3.31 Parallel synchronous slave interface (PSSI) 54
3.32 HASH hardware accelerator (HASH) 54
3.33 Timers and watchdogs 54
3.33.1 Advanced-control timer (TIM1, TIM8) 55
3.33.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17) 56
3.33.3 Basic timers (TIM6 and TIM7) 56
3.33.4 Low-power timer (LPTIM1 and LPTIM2) 56
3.33.5 Independent watchdog (IWDG) 57
3.33.6 Window watchdog (WWDG) 57
3.33.7 SysTick timer 57
3.34 Real-time clock (RTC) and backup registers 58
3.35 Inter-integrated circuit interface (I^2C) 58
3.36 Universal synchronous/asynchronous receiver transmitter (USART) . . . 60
3.37 Low-power universal asynchronous receiver transmitter (LPUART) 61
3.38 Serial peripheral interface (SPI) 61
3.39 Serial audio interfaces (SAI) 61
3.40 Secure digital input/output and MultiMediaCards Interface (SDMMC) . . . 62
3.41 Controller area network (CAN) 63

ST Restricted
DRAFT

ST RESTRICTED – SUBJECT TO NON-DISCLOSURE AGREEMENT – DO NOT COPY

3.42 Universal serial bus on-the-go full-speed (OTG_FS) 64
3.43 Development support 64
3.43.1 Serial wire JTAG debug port (SWJ-DP) 64
3.43.2 Embedded Trace Macrocell™ 65

4 Pinouts and pin description 66

5 Memory mapping 134

6 Electrical characteristics 135
6.1 Parameter conditions 135
6.1.1 Minimum and maximum values 135
6.1.2 Typical values 135
6.1.3 Typical curves 135
6.1.4 Loading capacitor 135
6.1.5 Pin input voltage 135
6.1.6 Power supply scheme 136
6.1.7 Current consumption measurement 137
6.2 Absolute maximum ratings 137
6.3 Operating conditions 139
6.3.1 General operating conditions 139
6.3.2 Operating conditions at power-up / power-down 141
6.3.3 Embedded reset and power control block characteristics 141
6.3.4 Embedded voltage reference 143
6.3.5 Supply current characteristics 145
6.3.6 Wakeup time from low-power modes and voltage scaling transition times 182
6.3.7 External clock source characteristics 185
6.3.8 Internal clock source characteristics 190
6.3.9 PLL characteristics 196
6.3.10 Flash memory characteristics 197
6.3.11 EMC characteristics 198
6.3.12 Electrical sensitivity characteristics 199
6.3.13 I/O current injection characteristics 200
6.3.14 I/O port characteristics 200
6.3.15 NRST pin characteristics 207
6.3.16 Extended interrupt and event controller input (EXTI) characteristics . . 208

ST Restricted
DRAFT

ST RESTRICTED – SUBJECT TO NON-DISCLOSURE AGREEMENT – DO NOT COPY

6.3.17 Analog switches booster . . . 208
6.3.18 Analog-to-digital converter characteristics . . . 209
6.3.19 Digital-to-Analog converter characteristics . . . 222
6.3.20 Voltage reference buffer characteristics . . . 227
6.3.21 Comparator characteristics . . . 229
6.3.22 Operational amplifiers characteristics . . . 230
6.3.23 Temperature sensor characteristics . . . 234
6.3.24 V_{BAT} monitoring characteristics . . . 234
6.3.25 DFSDM characteristics . . . 235
6.3.26 Timer characteristics . . . 236
6.3.27 Communication interfaces characteristics . . . 238
6.3.28 FSMC characteristics . . . 247
6.3.29 OctoSPI characteristics . . . 263
6.3.30 Camera interface (DCMI) timing specifications . . . 271
6.3.31 Parallel slave interface (PSSI) . . . 272
6.3.32 LCD-TFT controller (LTDC) characteristics . . . 273
6.3.33 SD/SDIO/MMC card host interfaces (SDMMC) . . . 273

7 Package information . . . 277
7.1 LQFP48 package information . . . 277
7.2 UFQFPN48 package information . . . 281
7.3 LQFP64 package information . . . 284
7.4 LQFP100 package information . . . 287
7.5 WLCSP100 package information . . . 290
7.6 UFBGA132 package information . . . 294
7.7 LQFP144 package information . . . 297
7.8 UFBGA169 package information . . . 301
7.9 Thermal characteristics . . . 304
7.9.1 Reference document . . . 304
7.9.2 Selecting the product temperature range . . . 304

8 Ordering information . . . 307

9 Revision history . . . 308

ST Restricted
DRAFT

ST RESTRICTED – SUBJECT TO NON-DISCLOSURE AGREEMENT – DO NOT COPY

List of tables

Table 1. Device summary . . . 2
Table 2. STM32L4P5xx features and peripheral counts . . . 16
Table 3. Access status versus readout protection level and execution modes . . . 21
Table 4. STM32L4P5xx modes overview . . . 28
Table 5. Functionalities depending on the working mode . . . 33
Table 6. STM32L4P5xx peripherals interconnect matrix . . . 36
Table 7. DMA implementation . . . 43
Table 8. Temperature sensor calibration values . . . 49
Table 9. Internal voltage reference calibration values . . . 49
Table 10. Timer feature comparison . . . 55
Table 11. I2C implementation . . . 59
Table 12. USART/UART/LPUART features . . . 60
Table 13. SAI implementation . . . 62
Table 14. Legend/abbreviations used in the pinout table . . . 76
Table 15. STM32L4P5xx pin definitions . . . 77
Table 16. Alternate function AF0 to AF7 . . . 116
Table 17. Alternate function AF8 to AF15 . . . 125
Table 18. Voltage characteristics . . . 137
Table 19. Current characteristics . . . 138
Table 20. Thermal characteristics . . . 139
Table 21. General operating conditions . . . 139
Table 22. Operating conditions at power-up / power-down . . . 141
Table 23. Embedded reset and power control block characteristics . . . 141
Table 24. Embedded internal voltage reference . . . 143
Table 25. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF)146
Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS . . . 147
Table 27. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF) . . . 148
Table 28. Consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS . . . 149
Table 29. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable . . . 150
Table 30. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable and power supplied by external SMPS . 151
Table 31. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable . . . 152
Table 32. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable and power supplied by external SMPS . . 153
Table 33. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1 . . . 154
Table 34. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1 and power supplied by external SMPS . . . 155
Table 35. Typical current consumption in Run and Low-power run modes, with different codes

ST Restricted DRAFT

ST RESTRICTED – SUBJECT TO NON-DISCLOSURE AGREEMENT – DO NOT COPY

running from Flash, ART enable (Cache ON Prefetch OFF) 156
Table 36. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS 158
Table 37. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable 160
Table 38. Typical current consumption in Run and Low-power run modes with different codes running from Flash, ART disable and power supplied by external SMPS 161
Table 39. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1 162
Table 40. Typical consumption in Run and Low-power run modes, with different codes running from SRAM1 and power supplied by external SMPS 163
Table 41. Current consumption in Sleep and Low-power sleep mode, Flash ON 164
Table 42. Current consumption in Sleep and Low-power sleep modes, Flash ON and power supplied by external SMPS 165
Table 43. Current consumption in Low-power sleep mode, Flash in power-down 166
Table 44. Current consumption in Stop 2 mode, SRAM3 disabled 167
Table 45. Current consumption in Stop 2 mode, SRAM3 enabled 168
Table 46. Current consumption in Stop 1 mode 169
Table 47. Current consumption in Stop 0 mode 170
Table 48. Current consumption in Standby mode 171
Table 49. Current consumption in Shutdown mode 174
Table 50. Current consumption in VBAT mode 175
Table 51. STM32L4P5xx peripheral current consumption 177
Table 52. Low-power mode wakeup timings 182
Table 53. Regulator modes transition times 184
Table 54. Wakeup time using USART/LPUART 184
Table 55. High-speed external user clock characteristics 185
Table 56. Low-speed external user clock characteristics 186
Table 57. HSE oscillator characteristics 187
Table 58. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) 189
Table 59. HSI16 oscillator characteristics 190
Table 60. MSI oscillator characteristics 192
Table 61. LSI oscillator characteristics 195
Table 62. PLL, PLLSAI1, PLLSAI2 characteristics 196
Table 63. Flash memory characteristics 197
Table 64. Flash memory endurance and data retention 197
Table 65. EMS characteristics 198
Table 66. ESD absolute maximum ratings 199
Table 67. Electrical sensitivities 199
Table 68. I/O current injection susceptibility 200
Table 69. I/O static characteristics 201
Table 70. Output voltage characteristics 204
Table 71. I/O AC characteristics 205
Table 72. NRST pin characteristics 207
Table 73. EXTI input characteristics 208
Table 74. Analog switches booster characteristics 208
Table 75. ADC characteristics 209
Table 76. Maximum ADC RAIN 211
Table 77. ADC accuracy - limited test conditions 1 213
Table 78. ADC accuracy - limited test conditions 2 215
Table 79. ADC accuracy - limited test conditions 3 217

ST Restricted
DRAFT

ST RESTRICTED – SUBJECT TO NON-DISCLOSURE AGREEMENT – DO NOT COPY

Table 80. ADC accuracy - limited test conditions 4 . . . 219
Table 81. DAC characteristics . . . 222
Table 82. DAC accuracy . . . 225
Table 83. VREFBUF characteristics . . . 227
Table 84. COMP characteristics . . . 229
Table 85. OPAMP characteristics . . . 230
Table 86. TS characteristics . . . 234
Table 87. V_{BAT} monitoring characteristics . . . 234
Table 88. V_{BAT} charging characteristics . . . 234
Table 89. DFSDM characteristics . . . 235
Table 90. TIMx characteristics . . . 237
Table 91. IWDG min/max timeout period at 32 kHz (LSI) . . . 237
Table 92. WWDG min/max timeout value at 120 MHz (PCLK) . . . 237
Table 93. I2C analog filter characteristics . . . 238
Table 94. SPI characteristics . . . 239
Table 95. SAI characteristics . . . 243
Table 96. USB electrical characteristics . . . 245
Table 97. USB OTG electrical characteristics . . . 246
Table 98. USB BCD DC electrical characteristics . . . 246
Table 99. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings . . . 249
Table 100. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings . . . 249
Table 101. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings . . . 250
Table 102. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings . . . 251
Table 103. Asynchronous multiplexed PSRAM/NOR read timings . . . 252
Table 104. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings . . . 252
Table 105. Asynchronous multiplexed PSRAM/NOR write timings . . . 253
Table 106. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings . . . 254
Table 107. Synchronous multiplexed NOR/PSRAM read timings . . . 256
Table 108. Synchronous multiplexed PSRAM write timings . . . 258
Table 109. Synchronous non-multiplexed NOR/PSRAM read timings . . . 259
Table 110. Synchronous non-multiplexed PSRAM write timings . . . 261
Table 111. Switching characteristics for NAND Flash read cycles . . . 263
Table 112. Switching characteristics for NAND Flash write cycles . . . 263
Table 113. OctoSPI characteristics in SDR mode . . . 264
Table 114. OctoSPI characteristics in DTR mode (no DQS) . . . 265
Table 115. OctoSPI characteristics in DTR mode (with DQS)/Octal and Hyperbus . . . 266
Table 116. DCMI characteristics . . . 271
Table 117. LTDC characteristics . . . 273
Table 118. Dynamics characteristics: SD / eMMC characteristics at VDD = 2.7 V to 3.6 V . . . 274
Table 119. Dynamics characteristics: eMMC characteristics at VDD = 1.71 V to 1.9 V . . . 274
Table 120. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data . . . 277
Table 121. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data . . . 281
Table 122. LQFP - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data . . . 284
Table 123. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data . . . 287
Table 124. WLCSP – 100 ball, 4.618 x 4.142 mm, 0.4 mm pitch wafer level chip scale package mechanical data . . . 290

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Table 125. WLCSP100 recommended PCB design rules (0.4 mm pitch) 292
Table 126. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data 294
Table 127. UFBGA132 recommended PCB design rules (0.5 mm pitch BGA) 295
Table 128. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data 298
Table 129. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data 301
Table 130. UFBGA169 recommended PCB design rules (0.5 mm pitch BGA) 302
Table 131. Package thermal characteristics 304
Table 132. Document revision history 308

ST Restricted
DRAFT

ST RESTRICTED – SUBJECT TO NON-DISCLOSURE AGREEMENT – DO NOT COPY

List of figures

Figure 1. STM32L4P5xx block diagram . . . 18
Figure 2. STM32L4P5xx power supply overview . . . 24
Figure 3. STM32L4P5xxxP with external SMPS power supply overview . . . 25
Figure 4. Power-up/down sequence . . . 26
Figure 5. Clock tree . . . 40
Figure 6. Multi-AHB bus matrix . . . 42
Figure 7. Voltage reference buffer . . . 50
Figure 8. STM32L4P5Cxxx LQFP48 pinout(1) . . . 66
Figure 9. STM32L4P5CxxxP external SMPS LQFP48 pinout(1) . . . 66
Figure 10. STM32L4P5Cxxx UFQFP48 pinout(1) . . . 67
Figure 11. STM32L4P5CxxxP external SMPS UFQFP48 pinout(1) . . . 67
Figure 12. STM32L4P5Rxxx LQFP64 pinout(1) . . . 68
Figure 13. STM32L4P5RxxxP external SMPS LQFP64 pinout(1) . . . 68
Figure 14. STM32L4P5Vxxx LQFP100 pinout(1) . . . 69
Figure 15. STM32L4P5VxxxP external SMPS LQFP100 pinout(1) . . . 70
Figure 16. STM32L4P5Vxxx WLCSP100 ballout(1) . . . 71
Figure 17. STM32L4P5VxxxP external SMPS WLCSP100 ballout(1) . . . 71
Figure 18. STM32L4P5Qxxx UFBGA132 ballout(1) . . . 72
Figure 19. STM32L4P5QxxxP external SMPS UFBGA132 ballout(1) . . . 72
Figure 20. STM32L4P5Zxxx LQFP144 pinout(1) . . . 73
Figure 21. STM32L4P5ZxxxP external SMPS LQFP144 pinout(1) . . . 74
Figure 22. STM32L4P5Axxx UFBGA169 ballout(1) . . . 75
Figure 23. STM32L4P5AxxxP UFBGA169 external SMPS ballout(1) . . . 75
Figure 24. Pin loading conditions . . . 135
Figure 25. Pin input voltage . . . 135
Figure 26. Power supply scheme . . . 136
Figure 27. Current consumption measurement . . . 137
Figure 28. VREFINT versus temperature . . . 144
Figure 29. High-speed external clock source AC timing diagram . . . 185
Figure 30. Low-speed external clock source AC timing diagram . . . 186
Figure 31. Typical application with an 8 MHz crystal . . . 188
Figure 32. Typical application with a 32.768 kHz crystal . . . 189
Figure 33. HSI16 frequency versus temperature . . . 191
Figure 34. Typical current consumption versus MSI frequency . . . 194
Figure 35. I/O input characteristics . . . 203
Figure 36. I/O AC characteristics definition(1) . . . 207
Figure 37. Recommended NRST pin protection . . . 208
Figure 38. ADC accuracy characteristics . . . 221
Figure 39. Typical connection diagram using the ADC . . . 221
Figure 40. 12-bit buffered / non-buffered DAC . . . 224
Figure 41. SPI timing diagram - slave mode and CPHA = 0 . . . 240
Figure 42. SPI timing diagram - slave mode and CPHA = 1 . . . 241
Figure 43. SPI timing diagram - master mode . . . 241
Figure 44. SAI master timing waveforms . . . 244
Figure 45. SAI slave timing waveforms . . . 244
Figure 46. USB OTG timings – definition of data signal rise and fall time . . . 246
Figure 47. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms . . . 248
Figure 48. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms . . . 250

ST Restricted DRAFT

ST RESTRICTED – SUBJECT TO NON-DISCLOSURE AGREEMENT – DO NOT COPY

Figure 49. Asynchronous multiplexed PSRAM/NOR read waveforms . . . 251
Figure 50. Asynchronous multiplexed PSRAM/NOR write waveforms . . . 253
Figure 51. Synchronous multiplexed NOR/PSRAM read timings . . . 255
Figure 52. Synchronous multiplexed PSRAM write timings . . . 257
Figure 53. Synchronous non-multiplexed NOR/PSRAM read timings . . . 259
Figure 54. Synchronous non-multiplexed PSRAM write timings . . . 260
Figure 55. NAND controller waveforms for read access . . . 262
Figure 56. NAND controller waveforms for write access . . . 262
Figure 57. NAND controller waveforms for common memory read access . . . 262
Figure 58. NAND controller waveforms for common memory write access . . . 263
Figure 59. OctoSPI timing diagram - SDR mode . . . 268
Figure 60. OctoSPI timing diagram - DDR mode . . . 268
Figure 61. OctoSPI Hyperbus clock . . . 268
Figure 62. OctoSPI Hyperbus read . . . 269
Figure 63. OctoSPI Hyperbus read with double latency . . . 269
Figure 64. OctoSPI Hyperbus write . . . 270
Figure 65. DCMI timing diagram . . . 271
Figure 66. SDIO high-speed mode . . . 275
Figure 67. SD default mode . . . 275
Figure 68. DDR mode . . . 276
Figure 69. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline . . . 277
Figure 70. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint . . . 278
Figure 71. LQFP48 marking (package top view) . . . 279
Figure 72. LQFP48, external SMPS device, marking (package top view) . . . 280
Figure 73. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline . . . 281
Figure 74. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint . . . 282
Figure 75. UFQFPN48 marking (package top view) . . . 283
Figure 76. UFQFPN48, external SMPS device, marking (package top view) . . . 283
Figure 77. LQFP - 64-pin, 10 x 10 mm low-profile quad flat package outline . . . 284
Figure 78. LQFP - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint . . . 285
Figure 79. LQFP64 marking (package top view) . . . 286
Figure 80. LQFP64, external SMPS device, marking (package top view) . . . 286
Figure 81. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline . . . 287
Figure 82. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint . . . 288
Figure 83. LQFP100 marking (package top view) . . . 289
Figure 84. WLCSP – 100 ball, 4.618 x 4.142 mm, 0.4 mm pitch wafer level chip scale package outline . . . 290
Figure 85. WLCSP – 100 ball, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package recommended footprint . . . 291
Figure 86. WLCSP100 marking (package top view) . . . 292
Figure 87. WLCSP100, external SMPS device, marking (package top view) . . . 293
Figure 88. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline . . . 294
Figure 89. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package recommended footprint . . . 295
Figure 90. UFBGA132 marking (package top view) . . . 296
Figure 91. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline . . . 297

ST Restricted
DRAFT

ST RESTRICTED – SUBJECT TO NON-DISCLOSURE AGREEMENT – DO NOT COPY

Figure 92. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint . . . 299
Figure 93. LQFP144 marking (package top view) . . . 300
Figure 94. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline . . . 301
Figure 95. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint . . . 302
Figure 96. UFBGA169 marking (package top view) . . . 303
Figure 97. STM32L4P5xx ordering information scheme . . . 307

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1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32L4P5xx microcontrollers.

This document should be read in conjunction with the STM32L4P5xx reference manual (RM0432). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the Arm®[a] Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

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2 Description

STM32L4P5xx designates a family of ultra-low-power microcontroller devices (part of STM32L4+ Series) based on the high-performance Arm® Cortex®-M4 32-bit RISC core. They operate at a frequency of up to 120 MHz.

The Cortex-M4 core features a single-precision floating-point unit (FPU), which supports all the Arm® single-precision data-processing instructions and all the data types. The Cortex-M4 core also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) that enhances the application's security.

These devices embed high-speed memories (up to 1 Mbyte of Flash memory and 320 Kbytes of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), two OctoSPI Flash memory interfaces (for devices with packages of 100 pins or more) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

These devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and a firewall.

These devices offer two fast 12-bit ADCs (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timers, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support two digital filters for external sigma delta modulators (DFSDMs). In addition, up to 24 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces such as:

- Four I2Cs
- Three SPIs
- Three USARTs, two UARTs and one low-power UART
- Two SAIs
- Two SDMMCs
- One CAN
- One USB OTG full-speed
- Camera interface
- Synchronous parallel data interface (PSSI)

The devices operate in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported such as an analog independent supply input for ADC, DAC, OPAMPs and comparators, a 3.3 V dedicated supply input for USB and up to 14 I/Os, which can be supplied independently down to 1.08 V. A VBAT input allows backup of the RTC and the registers. Dedicated VDD12 power supplies can be used to bypass the internal LDO regulator when connected to an external SMPS.

The STM32L4P5xx family offers eight packages from 48-pin to 169-pin.

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Table 2. STM32L4P5xx features and peripheral counts

Peripheral		P5CG/P5CE (48 pins)	P5RG/P5RE (64 pins)	P5VG/P5VE (100 pins)	P5QG/P5QE (132 pins)	P5ZG/P5ZE (144 pins)	P5AG/P5AE (169 pins)
Flash memory		Up to 1 Mbyte					
SRAM	System	320 (128 + 64 + 128) Kbytes					
	Backup	128 bytes					
External memory controller for static memories (FSMC)		No		Yes(1)	Yes		
OCTOSPI		1(2)			2		
Timers	Advanced control	2 (16-bit)					
	General purpose	5 (16-bit) 2 (32-bit)					
	Basic	2 (16-bit)					
	Low-power	2 (16-bit)					
	SysTick timer	1					
	Watchdog timers (independent, window)	2					
Comm. interfaces	SPI	3					
	I^2C	4					
	USART/UART UART LPUART	3 2(3) 1					
	SAI	2					
	CAN	1					
	USB OTG FS	Yes					
	SDMMC	2(4)					
Digital filters for sigma-delta modulators		Yes (2 filters)					
Number of channels		4					
Real time clock (RTC)		Yes					
Tamper pins		3					
Camera interface		Yes(5)					
PSSI		Yes(6)					
Chrom-ART Accelerator™		Yes					
LCD - TFT		Yes					
True random number generator		Yes					

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Table 2. STM32L4P5xx features and peripheral counts (continued)

Peripheral	P5CG/P5CE (48 pins)	P5RG/P5RE (64 pins)	P5VG/P5VE (100 pins)	P5QG/P5QE (132 pins)	P5ZG/P5ZE (144 pins)	P5AG/P5AE (169 pins)
HASH (SHA-256)	Yes					
GPIOs[7] Wakeup pins Nb of I/Os down to 1.08 V	38 3 0	54 4 0	83 5 0	110 5 14	115 5 14	136 5 14
Capacitive sensing Number of channels	9	21		24		
12-bit ADCs Number of channels	2					
	TBD	TBD	TBD	TBD	TBD	TBD
12-bit DAC Number of channels	2 2					
Internal voltage reference buffer	Yes					
Analog comparator	2					
Operational amplifiers	2					
Max. CPU frequency	120 MHz					
Operating voltage (V_{DD})	1.71 to 3.6 V					
Operating voltage (V_{DD12})	1.05 to 1.32 V					
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C					
Packages	UFQFPN48/ LQFP48	LQFP64	LQFP100/ WLCSP100	UFBGA132	LQFP144	UFBGA169

1. For the LQFP100 package, only FMC bank1 and NAND bank are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
2. Two OCTOSPIs are available when Muxed mode is enabled, for further details on Muxed mode refer to the RM0432 reference manual.
3. For 48-pin and 64-pin packages only 1x UART is available.
4. For 48 pins packages only one SDMMC2 with SDIO 4-bits is available. SDMMC1 and SDMMC2 are available for packages starting from 64 pins.
5. DCMI is available on devices with packages starting from 64-pin.
6. PSSI is available on devices with packages starting from 100-pin.
7. When an SMPS package type is used, two GPIOs are replaced by V_{DD12} pins to connect the SMPS power supplies hence the available GPIOs number is reduced by two.

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Figure 1. STM32L4P5xx block diagram

Note: AF: alternate function on I/O pins.

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3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of the MCU implementation, with a reduced pin count and with low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features an exceptional code-efficiency, delivering the expected high-performance from an Arm® core in a memory size usually associated with 8-bit and 16-bit devices.

The processor supports a set of DSP instructions which allows an efficient signal processing and a complex algorithm execution. Its single precision FPU speeds up the software development by using metalanguage development tools to avoid saturation.

With its embedded Arm® core, the family is compatible with all Arm® tools and software.

Figure 1 shows the general block diagram of the family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator that is optimized for the STM32 industry-standard Arm®Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 150 DMIPS performance at 120 MHz, the accelerator implements an instruction prefetch queue and a branch cache, which increases the program's execution speed from the Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from the Flash memory at a CPU frequency of up to 120 MHz.

3.3 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to eight protected areas, which can be divided in up into eight subareas each. The protection area sizes range between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

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3.4 Memories

3.4.1 Embedded Flash memory

The devices feature up to 1 Mbyte of embedded Flash memory which is available for storing programs and data.

The Flash interface features:

- Single or dual bank operating modes
- Read-while-write (RWW) in dual bank mode

This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual-bank boot is also supported. Each bank contains 128 pages of 4 Kbytes. In Single-bank mode the main Flash memory contains 128 pages of 8 Kbytes.

Flexible protections can be configured thanks to the option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels of protection are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection; the Flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected
  - Level 2: chip readout protection; the debug features (Cortex-M4 JTAG and serial wire), the boot in RAM and the bootloader selection are disabled (JTAG fuse). This selection is irreversible.

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Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming:
  - In single bank mode, four areas can be selected with 8-Kbyte granularity.
  - In dual bank mode, two areas per bank can be selected with 4-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only and it can only be reached by the STM32 CPU as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited:
  - In single bank mode, two areas can be selected with 128-bit granularity.
  - In dual bank mode, one area per bank can be selected with 64-bit granularity.

  An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- The address of the ECC fail can be read in the ECC register.

3.4.2 Embedded SRAM

The devices feature 320 Kbytes of embedded SRAM. This SRAM is split into three blocks:

- 128 Kbytes mapped at address 0x2000 0000 (SRAM1).
- 64 Kbytes located at address 0x1000 0000 with hardware parity check (SRAM2). This memory is also mapped at address 0x2002 0000 offering a contiguous address space with the SRAM1.
  This block is accessed through the ICode/DCode buses for maximum performance.

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Either 64 Kbytes or 4 Kbytes of SRAM2 can be retained in Standby mode. The SRAM2 can be write-protected with 1 Kbyte granularity.

- 128 Kbytes mapped at address 0x2003 0000 (SRAM3).

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.5 Boot modes

At startup, a BOOT0 pin and an nBOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty-check mechanism is implemented to force the boot from system Flash if the first Flash memory location is not programmed and if the boot selection is configured to boot from main Flash.

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN or USB OTG FS in device mode through the DFU (device firmware upgrade).

3.6 Firewall

These devices embed a firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The main features of the firewall are the following:

- Three segments can be protected and defined thanks to the firewall registers:
  - Code segment (located in Flash or SRAM1 if defined as executable protected area)
  - Non-volatile data segment (located in Flash)
  - Volatile data segment (located in SRAM1)
- The start address and the length of each segment are configurable:
  - Code segment: up to 1024 Kbytes with granularity of 256 bytes
  - Non-volatile data segment: up to 1024 Kbytes with granularity of 256 bytes
  - Volatile data segment: up to 128 Kbytes of SRAM1 with a granularity of 64 bytes
- Specific mechanism implemented to open the firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

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3.7 Power supply management

3.7.1 Power supply schemes

The STM32L4P5xx devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V

  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.

- V_{DD12} = 1.05 to 1.32 V

  V_{DD12} is the external power supply bypassing the internal regulator when connected to an external SMPS. It is provided externally through VDD12 pins and only available on packages with the external SMPS supply option. VDD12 does not require any external decoupling capacitance and cannot support any external load.

- V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 V (DACs/OPAMPs) to 2.4 V (VREFBUF) to 3.6 V

  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage and should preferably be connected to V_{DD} when these peripherals are not used.

- VDDUSB = 3.0 V to 3.6 V

  VDDUSB is the external independent power supply for USB transceivers. The VDDUSB voltage level is independent from the VDD voltage and should preferably be connected to VDD when the USB is not used.

- VDDIO2 = 1.08 V to 3.6 V

- VDDIO2 is the external power supply for 14 I/Os (port G[15:2]). The VDDIO2 voltage level is independent from the VDD voltage and should preferably be connected to VDD when PG[15:2] are not used.

- V_{BAT} = 1.55 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

- V_{REF-}, V_{REF+}

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  When V_{DDA} < 2 V V_{REF+} must be equal to V_{DDA}.

  When V_{DDA} ≥ 2 V V_{REF+} must be between 2 V and V_{DDA}.

  V_{REF+} can be grounded when ADC and DAC are not active.

  The internal voltage reference buffer supports two output voltages, which are configured with VRS bit in the VREFBUF_CSR register:

  – V_{REF+} around 2.048 V. This requires V_{DDA} equal to or higher than 2.4 V.

  – V_{REF+} around 2.5 V. This requires V_{DDA} equal to or higher than 2.8 V.

  VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.
  When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disable (refer to datasheet for packages pinout description).
  V_{REF-} must always be equal to V_{SSA}.

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An embedded linear voltage-regulator is used to supply the internal digital power V_{CORE}. V_{CORE} is the power supply for digital peripherals, SRAM1, SRAM2 and SRAM3. The Flash is supplied by V_{CORE} and V_{DD}.

Figure 2. STM32L4P5xx power supply overview

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Figure 3. STM32L4P5xxxP with external SMPS power supply overview

During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2} and V_{DDUSB}) must remain below VDD +300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

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Figure 4. Power-up/down sequence

1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDIO2} and V_{DDUSB}.

3.7.2 Power supply supervisor

The STM32L4P5xx devices have an integrated ultra-low-power Brownout reset (BOR) active in all modes (except for Shutdown mode). The BOR ensures proper operation of the devices after power-on and during power-down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold.

An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor which compares the independent supply voltages V_{DDA}, V_{DDUSB}, V_{DDIO2} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.7.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-power run, Low-power sleep, Stop 1 and Stop 2 modes. It is also used to supply the 64 Kbytes SRAM2 in standby with RAM2 retention.
- Both regulators are in power-down while they are in standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

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The ultra-low-power devices support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the main regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

The main regulator operates in the following ranges:

- Range 1 boost mode with the CPU running at up to 120 MHz.
- Range 1 normal mode with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The VCORE can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by the HSI16.

When the MR is in use, the device with the external SMPS option allows to force an external V_{CORE} supply on the VDD12 supply pins.

When V_{DD12} is forced by an external source and that it is higher than the output of the internal LDO, the current is taken from this external supply and the overall power efficiency is significantly improved if using an external step down DC/DC converter.

Note: The USB can only be used when the main regulator is in Range 1 boost mode.

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3.7.4 Low-power modes

The ultra-low-power devices support seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wake-up sources. The table below shows the related STM32L4P5xx modes overview.

Table 4. STM32L4P5xx modes overview

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source
Run	Range 1	Yes	ON[3]	ON	Any	All	N/A
	SMPS range 2 High						
	Range 2					All except OTG_FS, RNG, LCD-TFT	
	SMPS range 2 Low						
LPRun	LPR	Yes	ON[3]	ON	Any except PLL	All except OTG_FS, RNG, LCD-TFT	N/A
Sleep	Range 1	No	ON[3]	ON[4]	Any	All	Any interrupt or event
	SMPS range 2 High						
	Range 2					All except OTG_FS, RNG, LCD-TFT	
	SMPS range 2 Low						
LPSleep	LPR	No	ON[3]	ON[4]	Any except PLL	All except OTG_FS, RNG, LCD-TFT	Any interrupt or event

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Table 4. STM32L4P5xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source
Stop 0[5]	Range 1 Range 2	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) OTG_FS[8]
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) OTG_FS[8]

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Table 4. STM32L4P5xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3[7] LPUART1[6] LPTIM1 *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3[7] LPUART1[6] LPTIMx (x=1,2)
Standby	LPR	Powered Off	Off	SRAM2 ON	LSE LSI	BOR, RTC, IWDG *** All other peripherals are powered off *** I/O configuration can be floating, pull-up or pull-down	Reset pin 5 I/Os (WKUPx)[9] BOR, RTC, IWDG
	OFF			Powered Off			
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals are powered off *** I/O configuration can be floating, pull-up or pull-down[10]	Reset pin 5 I/Os (WKUPx)[9] RTC

1. LPR means Main regulator is OFF and Low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
4. The SRAM1, SRAM2 and SRAM3 clocks can be gated on or off independently.
5. SMPS mode can be used in Stop 0 mode, but no significant power gain can be expected.
6. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. OTG_FS wakeup by resume from suspend and attach detection protocol event.
9. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
10. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

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By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep** mode

  This mode is entered from the Low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the Low-power run mode.

- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wake-up capability can enable the HSI16 RC during Stop mode to detect their wake-up condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop 1 or Stop 2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The Brownout reset (BOR) always remains active in Standby mode.

  The state of each I/O during Standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1, SRAM3 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, the full SRAM2 (or

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only the upper 4 Kbytes) can be retained in Standby mode, supplied by the low-power regulator (standby with RAM2 retention mode).

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2, SRAM3 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

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Table 5. Functionalities depending on the working mode[1]

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (2 Mbytes)	O[2]	O[2]	O[2]	O[2]	-	-	-	-	-	-	-	-	-
SRAM1 (128 Kbytes)	Y	Y[3]	Y	Y[3]	Y	-	Y	-	-	-	-	-	-
SRAM2 (64 Kbytes)	Y	Y[3]	Y	Y[3]	Y	-	Y	-	O[4]	-	-	-	-
SRAM3 (128 Kbytes)	Y	Y[3]	Y	Y[3]	Y	-	Y[3]	-	-	-	-	-	-
FSMC	O	O	O	O	-	-	-	-	-	-	-	-	-
OCTOSPIx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
Backup registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brownout reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral voltage monitor (PVMx; x=1,2,3,4)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
DMA2D	O	O	O	O	-	-	-	-	-	-	-	-	-
High speed internal (HSI16)	O	O	O	O	[5]	-	[5]	-	-	-	-	-	-
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-	-	-	-
High speed external (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low speed internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi speed internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-

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Table 5. Functionalities depending on the working mode[1] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O
Number of RTC Tamper pins	3	3	3	3	3	O	3	O	3	O	3	O	3
Camera interface (DCMI)	O	O	O	O	-	-	-	-	-	-	-	-	-
PSSI	O	O	O	O	-	-	-	-	-	-	-	-	-
LCD-TFT	O	O	-	-	-	-	-	-	-	-	-	-	-
USB OTG FS	O[8]	O[8]	-	-	-	O	-	-	-	-	-	-	-
USARTx (x=1,2,3,4,5)	O	O	O	O	O[6]	O[6]	-	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O[6]	O[6]	O[6]	O[6]	-	-	-	-	-
I2Cx (x=1,2,4)	O	O	O	O	O[7]	O[7]	-	-	-	-	-	-	-
I2C3	O	O	O	O	O[7]	O[7]	O[7]	O[7]	-	-	-	-	-
SPIx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
CAN(x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC2	O	O	O	O	-	-	-	-	-	-	-	-	-
SAIx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DFSDM1	O	O	O	O	-	-	-	-	-	-	-	-	-
ADCx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DACx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMPx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power timer 1 (LPTIM1)	O	O	O	O	O	O	O	O	-	-	-	-	-

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Table 5. Functionalities depending on the working mode[1] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O[8]	O[8]	-	-	-	-	-	-	-	-	-	-	-
HASH hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	[9]	5 pins [10]	[11]	5 pins [10]	-

1. Legend: Y = yes (enable). O = optional (disable by default, can be enabled by software). - = not available.

Gray cells highlight the wakeup capability in each mode.

2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off. In Stop 2 mode, the content of SRAM3 is preserved or not depending on the RRSTP bit in PWR_CR1 register.
4. The upper 4 Kbytes or the full SRAM2 content is preserved depending on RRS[1:0] bits configuration in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from standby/shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

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3.7.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.7.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when there is no external battery and when an external supercapacitor is present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when V_{DD} is not present. An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, neither external interrupts nor RTC alarm/events exit the microcontroller from the VBAT operation.

3.8 Peripheral and interconnect matrix

Several peripherals have direct connections between them, which allow autonomous communication between them and support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power Sleep, Stop 0, Stop 1 and Stop 2 modes. See *Table 6* for more details.

Table 6. STM32L4P5xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADCx DACx DFSDM1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
COMPx	TIM1, 8 TIM2, 3	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y
ADCx	TIM1, 8	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-

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Table 6. STM32L4P5xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y
All clocks sources (internal and external)	TIM2 TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD DFSDM1 (analog watchdog, short circuit detection)	TIM1,8 TIM15,16,17	Timer break	Y	Y	Y	Y	-	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y
	ADC DACx DFSDM1	Conversion external trigger	Y	Y	Y	Y	-	-

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3.9 Reset and clock controller (RCC)

The clock controller (see *Figure 5*) distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4 to 48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device, saving the need of an external high-speed crystal (HSE). The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 120 MHz.
- **RC48 with clock recovery system (HSI48):** internal 48 MHz clock source (HSI48)can be used to drive the USB, the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG, the two SAIs, and LCD-TFT.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

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interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
  - **MCO (microcontroller clock output):** it outputs one of the internal clocks for external use by the application
  - **LSCO (low-speed clock output):** it outputs LSI or LSE in all low-power modes (except VBAT).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 120 MHz.

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Figure 5. Clock tree

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3.10 Clock recovery system (CRS)

The devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.11 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.12 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, DMA2D, SDMMC1, SDMMC2 and LCD-TFT) and the slaves (Flash memory, RAM, FMC, OctoSPI, AHB and APB peripherals). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

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Figure 6. Multi-AHB bus matrix

3.13 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 7: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

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The DMA supports:

- 14 independently configurable channels (requests)
  - Each channel is connected to a dedicated hardware DMA request, a software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are both software programmable (4 levels: very high, high, medium, low) or hardware programmable in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size
- Support for circular buffer management
- 3 event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536

Table 7. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

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3.14 DMA request router (DMAMux)

When a peripheral indicates a request for DMA transfer by setting its DMA request line, the DMA request is pending until it is served and the corresponding DMA request line is reset. The DMA request router allows to route the DMA control lines between the peripherals and the DMA controllers of the product.

An embedded multi-channel DMA request generator can be considered as one of such peripherals. The routing function is ensured by a multi-channel DMA request line multiplexer. Each channel selects a unique set of DMA control lines, unconditionally or synchronously with events on synchronization inputs.

For simplicity, the functional description is limited to DMA request lines. The other DMA control lines are not shown in figures or described in the text. The DMA request generator produces DMA requests following events on DMA request trigger inputs.

3.15 Chrom-ART Accelerator™ (DMA2D)

Chrom-ART Accelerator™ (DMA2D) is a graphic accelerator that offers an advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4 bpp color mode up to 32 bpp direct color. It embeds a dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

3.16 Interrupts and events

3.16.1 Nested vectored interrupt controller (NVIC)

The STM32L4P5xx devices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and to handle up to 95 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

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The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.16.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 36 edge detector lines used to generate interrupt/event requests and to wake-up the system from the Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently.

A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 114 GPIOs can be connected to the 16 external interrupt lines.

3.17 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the Flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and which can be stored at a given memory location.

3.18 Flexible static memory controller (FSMC)

The flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (four memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
  - Ferroelectric RAM (FRAM)
- 8-,16- bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- The Maximum FMC_CLK frequency for synchronous accesses is HCLK/2.

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LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

3.19 Octo-SPI interface (OCTOSPI)

The OctoSPI is a specialized communication interface targetting single, dual, quad or octal SPI memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the OctoSPI registers
- Status polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external memory is memory mapped and is seen by the system as if it were an internal memory supporting read and write operation

The OctoSPI supports two frame formats:

- Classical frame format with command, address, alternate byte, dummy cycles and data phase over 1, 2, 4 or 8 data pins
- Hyperbus™ frame format

The OctoSPI offers the following features:

- Three functional modes: indirect, status-polling, and memory-mapped
- Read and write support in memory-mapped mode
- Supports for single, dual, quad and octal communication
- Dual-quad mode, where 8 bits can be sent/received simultaneously by accessing two quad memories in parallel.
- SDR and DTR support
- Data strobe support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the five following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Hyperbus™ support
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations

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- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

3.20 Octo-SPI IO manager (OCTOSPIIOM)

The OctoSPI IO Manager is a low level interface allowing:

- Efficient OctoSPI pin assignment with a full IO Matrix (before alternate function map)
- Multiplexing single/dual/quad/octal SPI interface over the same bus

The OctoSPI IO Manager has the following features:

- Support up to two single/dual/quad/octal SPI Interface
- Support up to eight ports for pin assignment
- Fully programmable IO matrix for pin assignment by function (data/control/clock)
- Muxer for Single/Dual/Quad/Octal SPI interface multiplexing over the same bus

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3.21 Analog-to-digital converter (ADC)

The device embeds two successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 16 external channels
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into a data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

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3.21.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN17 input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

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Table 8. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.21.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and the comparators. The VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 9. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.21.3 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN18. As the V_{BAT} voltage may be higher than the VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third of the V_{BAT} voltage.

3.22 Digital to analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation

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- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.23 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 7. Voltage reference buffer

3.24 Comparators (COMP)

The devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can also be combined into a window comparator.

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3.25 Operational amplifier (OPAMP)

The devices embed two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.26 Digital filter for sigma-delta modulators (DFSDM)

The STM32L4P5xx devices embed one DFSDM with two digital filters modules and four external input serial channels (transceivers) or alternately four internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to the microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs).

The DFSDM can also interface the PDM (pulse density modulation) microphones and perform PDM to PCM conversion and filtering in hardware. The DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

The DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators) and the DFSDM digital filter modules perform digital processing according to the user's selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 4 multiplexed input digital serial channels:
  - Configurable SPI interface to connect various SD modulator(s)
  - Configurable Manchester coded 1 wire interface support
  - PDM (pulse density modulation) microphone input support
  - Maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - Clock output for SD modulator(s): 0..20 MHz
- Alternative inputs from 8 internal digital parallel channels (up to 16-bit input resolution):
  - Internal sources: device memory data streams (DMA)
- 2 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - Integrator: oversampling ratio (1..256)
- Up to 24-bit output data resolution, signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion triggered by:
  - Software trigger
  - Internal timers

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  - External events
  - Start-of-conversion synchronously with first digital filter module (DFSDM0)
- Analog watchdog feature:
  - Low value and high-value data threshold registers
  - Dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - Input from final output data or from selected input digital serial channels
  - Continuous monitoring independently from standard conversion
- Short circuit detector to detect saturated analog input values (bottom and top range):
  - Up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - Monitoring continuously each input serial channel
- Break signal generation on analog watchdog event or on short circuit detector event
- Extremes detector:
  - Storage of minimum and maximum values of final conversion data
  - Refreshed by software
- DMA capability to read the final conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- "Regular" or "injected" conversions:
  - "Regular" conversions can be requested at any time or even in continuous mode without having any impact on the timing of "injected" conversions
  - "Injected" conversions for precise timing and with high conversion priority

3.27 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with any camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface in order to receive video data.

The camera interface can sustain a data transfer rate up to 54 Mbytes/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication of 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image.

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3.28 LCD-TFT controller (LTDC)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (red, green, blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels with the following features:

- One display layer with dedicated FIFO (64 x 32-bit)
- Color look-up table (CLUT) up to 256 colors (256 x 24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to four programmable interrupt events

3.29 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution to add capacitive sensing functionality to any application. A capacitive sensing technology is able to detect finger presence near an electrode that is protected from direct touch by a dielectric (glass, plastic or other). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 24 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

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3.30 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.31 Parallel synchronous slave interface (PSSI)

The PSSI is a generic synchronous 8-/16-bit parallel data input/output slave interface. It allows the transmitter to send a data valid signal to indicate when the data is valid, and the receiver to output a flow control signal to indicate when it is ready to sample the data.

The PSSI main features are:

- The PSSI shares most of the circuitry with the digital camera interface (DCMI). It thus cannot be used simultaneously with the DCMI.
- Slave mode operation
- 8- or 16-bit parallel data input or output
- 4-word (16-byte) FIFO
- Data enable (DE) alternate function input and Ready (RDY) alternate function output. When enabled, these signals can either allow the transmitter to indicate when the data is valid or the receiver to indicate when it is ready to sample the data, or both.

3.32 HASH hardware accelerator (HASH)

The hash processor is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-224, SHA-256), the MD5 (message-digest algorithm 5) hash algorithm and the HMAC (keyed-hash message authentication code) algorithm suitable for a variety of applications.

It computes a message digest (160 bits for the SHA-1 algorithm, 256 bits for the SHA-256 algorithm and 224 bits for the SHA-224 algorithm,128 bits for the MD5 algorithm) for messages of up to (264 - 1) bits, while the HMAC algorithms provide a way of authenticating messages by means of hash functions. The HMAC algorithms consist in calling the SHA-1, SHA-224, SHA-256 or MD5 hash function twice.

3.33 Timers and watchdogs

The devices include two advanced control timers, up to nine general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer.

The *Table 10* below compares the features of the advanced control, general-purpose and basic timers.

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Table 10. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.33.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.33.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

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3.33.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

There are up to seven synchronizable general-purpose timers embedded in the devices (see *Table 10* for differences).
Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, TIM4 and TIM5

  They are full-featured general-purpose timers:

  – TIM2 and TIM5 have a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and TIM4 have 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  They are general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has two channels and one complementary channel

  – TIM16 and TIM17 have one channel and one complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.33.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.33.4 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 and LPTIM2 can be active in Stop 0, Stop 1 and Stop 2 modes.

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This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)
- Repetition counter.

3.33.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.33.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.33.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

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3.34 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Three anti-tamper detection pins with programmable filter
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, or when the device wakes up from standby or Shutdown mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (alarm, wake-up timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.35 Inter-integrated circuit interface (I2C)

The device embeds four I2C. Refer to *Table 11: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

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The I2C peripheral supports:

- I²C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 5: Clock tree*
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 11. I2C implementation

I2C features[1]	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wakeup from Stop 0, Stop 1 mode on address match	X	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X	-

1. X: supported

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3.36 Universal synchronous/asynchronous receiver transmitter (USART)

The devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, UART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN master/slave capability. They provide hardware management of the CTS and RTS signals, and RS485 driver enable. They are able to communicate at speeds of up to 10 Mbit/s.

The USART1, USART2 and USART3 also provide a Smartcard mode (ISO 7816 compliant) and an SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode using baudrates up to 200 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 12. USART/UART/LPUART features

USART modes/features[1]	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain	X	X	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	-	-	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection	X (4 modes)					-
Driver enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

1. X = supported.

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3.37 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

3.38 Serial peripheral interface (SPI)

Three SPI interfaces allow communication up to slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives eight master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and hardware CRC calculation.

All SPI interfaces can be served by the DMA controller.

3.39 Serial audio interfaces (SAI)

The devices embed two SAI. Refer to *Table 13: SAI implementation* for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.

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- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
  - Overrun and underrun detection.
  - Anticipated frame synchronization signal detection in slave mode.
  - Late frame synchronization signal detection in slave mode.
  - Codec not ready for the AC'97 mode in reception.
- Interruption sources when enabled:
  - Errors.
  - FIFO requests.
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

Table 13. SAI implementation

SAI features[1]	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
Mute mode	X	X
Stereo/Mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO size	X (8 Word)	X (8 Word)
SPDIF	X	X
PDM	X	-

1. X: supported

3.40 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The STM32L4P5xx devices embed two SDMMC host interfaces. Each SDMMC host interface embeds a dedicated DMA controller allowing high-speed transfers between the interface and the other AHB slaves.

The SD/SDIO, MultiMediaCard (MMC) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards and MMC devices.

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The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.51. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (backward compatibility)
- Full compliance with SD Memory Card Specifications Version 4.1. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Full compliance with SDIO Card Specification Version 4.0: card support for two different databus modes: 1-bit (default) and 4-bit. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Data transfer up to 104 Mbyte/s for the 8-bit mode (depending maximum allowed IO speed)
- Data and command output enable signals to control external bidirectional drivers.

3.41 Controller area network (CAN)

The CAN is compliant with the 2.0A and B (active) specifications with a bit rate of up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. The CAN has three transmit mailboxes, two receive FIFOS with three stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated.

The CAN peripheral supports:

- CAN protocol version 2.0 A, B Active
- Bit rates of up to 1 Mbit/s
- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - Scalable filter banks: 28 filter banks
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

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3.42 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume.

The USB OTG controller requires a dedicated 48 MHz clock that can be provided by the internal multispeed oscillator (MSI) automatically trimmed by 32.768 kHz external oscillator (LSE).This allows to use the USB device without external high speed crystal (HSE).

The major features are:

- Combined Rx and Tx FIFO size of 1.25 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- One bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- Eight host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- Software configurable to OTG 1.3 and OTG 2.0 modes of operation
- OTG 2.0 Supports ADP (Attach detection Protocol)
- USB 2.0 LPM (Link Power Management) support
- Battery charging specification revision 1.2 support
- Internal FS OTG PHY support

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected.

The synchronization for this oscillator can also be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.43 Development support

3.43.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins could be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

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3.43.2 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

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4 Pinouts and pin description

Figure 8. STM32L4P5Cxxx LQFP48 pinout(1)

1. The above figure shows the package top view.

Figure 9. STM32L4P5CxxxP external SMPS LQFP48 pinout(1)

1. The above figure shows the package top view.

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Figure 10. STM32L4P5Cxxx UFQFP48 pinout(1)

1. The above figure shows the package top view.

Figure 11. STM32L4P5CxxxP external SMPS UFQFP48 pinout(1)

1. The above figure shows the package top view.

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Figure 12. STM32L4P5Rxxx LQFP64 pinout(1)

1. The above figure shows the package top view.

Figure 13. STM32L4P5RxxxP external SMPS LQFP64 pinout(1)

1. The above figure shows the package top view.

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Figure 14. STM32L4P5Vxxx LQFP100 pinout(1)

1. The above figure shows the package top view.

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Figure 15. STM32L4P5VxxxP external SMPS LQFP100 pinout(1)

1. The above figure shows the package top view.

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Figure 16. STM32L4P5Vxxx WLCSP100 ballout(1)

	1	2	3	4	5	6	7	8	9	10
A	VDDUSB	PA15	PD1	VDD	PG10	VDDIO2	PB6	PB9	VSS	VDD
B	VSS	PA14	PD0	PD4	PG9	PG12	PB5	PB8	PE2	PE3
C	PA12	PA13	PC11	PC12	PD7	PB3	PB4	PE4	PC13	VBAT
D	PA11	PA10	PA9	PC10	PD6	PG11	PB7	PE5	VSS	PC14-OSC32_IN
E	PC8	PC9	PA8	PD2	PD5	PH3-BOOT0	PE6	NRST	VDD	PC15-OSC32_OUT
F	VDD	PC6	PC7	PD15	PB2	PA4	PC3	PC1	PC0	PH0-OSC_IN
G	PD10	PD9	PD14	PE13	PE12	PA5	VREF+	VREF-	PA0	PH1-OSC_OUT
H	PB15	PB14	PD8	PE15	PE10	PC4	PA2	PA1	VSSA	PC2
J	PB12	PB13	PB11	PE14	PE9	PB0	PA7	VDD	PA3	VDDA
K	VDD	VSS	PB10	PE11	PE8	PE7	PB1	PC5	PA6	VSS

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1. The above figure shows the package top view.

Figure 17. STM32L4P5VxxxP external SMPS WLCSP100 ballout(1)

	1	2	3	4	5	6	7	8	9	10
A	VDDUSB	PA15	PD1	VDD	PG10	VDDIO2	PB6	PB9	VDD12	VDD
B	VSS	PA14	PD0	PD5	PD6	PG12	PB7	PB8	VSS	PE3
C	PA12	PA13	PC10	PC12	PD4	PD7	PB5	PE2	PC13	VBAT
D	PA11	PA10	PA9	PC11	PD2	PG9	PH3-BOOT0	PE6	PC15-OSC32_OUT	PC14-OSC32_IN
E	PC8	PC9	PA8	PC7	PG11	PB4	PE4	PE5	VDD	VSS
F	VDD	PD15	PD14	PC6	PB3	PC3	PC1	NRST	PH1-OSC_OUT	PH0-OSC_IN
G	PD10	PD9	PD8	PE14	PE13	PA7	PA1	PA0	PC2	PC0
H	PB14	PB13	PB15	PE15	PE10	PB0	PA4	PA2	VSSA/VREF-	VREF+
J	PB12	VDD	PB11	PE12	PE9	PB2	PA5	VDD	PA3	VDDA
K	VDD12	VSS	PB10	PE11	PE8	PE7	PB1	PC4	PA6	VSS

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1. The above figure shows the package top view.

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Figure 18. STM32L4P5Qxxx UFBGA132 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	PH3-BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD	PB5	PG14	PG13	PD2	PD0	PC11	VDDUSB	PA10
D	PC14-OSC32_IN	PE6	VSS	PF2	PF1	PF0	PG12	PG10	PG9	PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS	PF3					PG5	PC8	PC7	PC6
F	PH0-OSC_IN	VSS	PF4	PF5		VSS	VSS		PG3	PG4	VSS	VSS
G	PH1-OSC_OUT	VDD	PG11	PG6		VDD	VDDIO2		PG1	PG2	VDD	VDD
H	PC0	NRST	VDD	PG7					PG0	PD15	PD14	PD13
J	VSSA/VREF-	PC1	PC2	PA4	PA7	PG8	PF12	PF14	PF15	PD12	PD11	PD10
K	PG15	PC3	PA2	PA5	PC4	PF11	PF13	PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	PB11	PB12
M	VDDA	PA1	OPAMP1_VINM	OPAMP2_VINM	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

MSv62904V1

1. The above figure shows the package top view.

Figure 19. STM32L4P5QxxxP external SMPS UFBGA132 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	PH3-BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD	PB5	VDD12	PG13	PD2	PD0	PC11	VDDUSB	PA10
D	PC14-OSC32_IN	PE6	VSS	PF2	PF1	PF0	PG12	PG10	PG9	PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS	PF3					PG5	PC8	PC7	PC6
F	PH0-OSC_IN	VSS	PF4	PF5		VSS	VSS		PG3	PG4	VSS	VSS
G	PH1-OSC_OUT	VDD	PG11	PG6		VDD	VDDIO2		PG1	PG2	VDD	VDD
H	PC0	NRST	VDD	PG7					PG0	PD15	PD14	PD13
J	VSSA/VREF-	PC1	PC2	PA4	PA7	PG8	PF12	PF14	PF15	PD12	PD11	PD10
K	PG15	PC3	PA2	PA5	PC4	PF11	PF13	PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	VDD12	PB12
M	VDDA	PA1	OPAMP1_VINM	OPAMP2_VINM	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

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1. The above figure shows the package top view.

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Figure 20. STM32L4P5Zxxx LQFP144 pinout(1)

1. The above figure shows the package top view.

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Figure 21. STM32L4P5ZxxxP external SMPS LQFP144 pinout(1)

1. The above figure shows the package top view.

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Figure 22. STM32L4P5Axxx UFBGA169 ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	PG15	PD4	PD1	PH13	PI3	PI8	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PH9	PH7	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PH6	VDDUSB	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PA10	PA9	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG14	PG13	PA8	PC9	PC8	PG6	PC7	VDD
H	PH0-OSC_IN	VSS	NRST	PF10	PC4	PG1	PE10	PB11	PG8	PG7	PD15	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PC5	PG0	PE9	PE15	PG5	PG4	PG3	PG2	PD10
K	PC3	VSSA/VREF-	PA0	PA5	PB0	PF15	PE8	PE14	PH4	PD14	PD12	PD11	PD13
L	VREF+	VDDA	PA4	PA7	PB1	PF14	PE7	PE13	PH5	PD9	PD8	VDD	VSS
M	OPAMP1_VINM	PA3	VSS	PA6	PF11	PF13	VSS	PE12	PH10	PH11	VSS	PB15	PB14
N	PA2	PA1	VDD	OPAMP2_VINM	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

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1. The above figure shows the package top view.

Figure 23. STM32L4P5AxxxP UFBGA169 external SMPS ballout(1)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	VDD12	PD4	PD1	PH13	PI3	PI8	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PH9	PH7	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PH6	VDDUSB	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PA10	PA9	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG14	PG13	PA8	PC9	PC8	PG6	PC7	VDD
H	PH0-OSC_IN	VSS	NRST	PF10	PC4	PG1	PE10	PB11	PG8	PG7	PD15	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PC5	PG0	PE9	PE15	PG5	PG4	PG3	PG2	PD10
K	PC3	VSSA/VREF-	PA0	PA5	PB0	PF15	PE8	PE14	PH4	PD14	PD12	PD11	PD13
L	VREF+	VDDA	PA4	PA7	PB1	PF14	PE7	PE13	PH5	PD9	PD8	VDD	VSS
M	OPAMP1_VINM	PA3	VSS	PA6	PF11	PF13	VSS	PE12	PH10	VDD12	VSS	PB15	PB14
N	PA2	PA1	VDD	OPAMP2_VINM	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

MSv62901V1

1. The above figure shows the package top view.

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Table 14. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os	
		_f (1)	I/O, Fm+ capable
		_u (2)	I/O, with USB function supplied by V_{DDUSB}
		_a (3)	I/O, with Analog switch function supplied by V_{DDA}
		_s (4)	I/O supplied only by V_{DDIO2}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures are: FT_f, FT_fa, FT_fl, FT_fla.
2. The related I/O structures are: FT_u, FT_lu.
3. The related I/O structures are: FT_a, FT_la, FT_fa, FT_fla, TT_a, TT_la.
4. The related I/O structures are: FT_s, FT_fs.

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Table 15. STM32L4P5xx pin definitions

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	D3	D3	-	-	M11	M11	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	C4	C4	-	-	C1	C1	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	C3	C3	PI11	I/O	FT	-	OCTOSPIM_P2_IO0, PSSI_D15, EVENTOUT	-
-	-	-	-	-	-	C8	B9	1	1	B2	B2	1	1	D3	D3	PE2	I/O	FT_I	-	TRACECK, TIM3_ETR, SAI1_CK1, TSC_G7_IO1, LCD_R7, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	B10	B10	2	2	A1	A1	2	2	D2	D2	PE3	I/O	FT_I	-	TRACED0, TIM3_CH1, OCTOSPIM_P1_DQS, TSC_G7_IO2, LCD_R6, FMC_A19, SAI1_SD_B, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	E7	C8	3	3	B1	B1	3	3	D1	D1	PE4	I/O	FT	-	TRACED1, TIM3_CH2, SAI1_D2, DFSDM1_DATIN3, TSC_G7_IO3, DCMI_D4/PSSI_D4, LCD_B7, FMC_A20, SAI1_FS_A, EVENTOUT	-
-	-	-	-	-	-	E8	D8	4	4	C2	C2	4	4	E4	E4	PE5	I/O	FT	-	TRACED2, TIM3_CH3, SAI1_CK2, DFSDM1_CKIN3, TSC_G7_IO4, DCMI_D6/PSSI_D6, LCD_G7, FMC_A21, SAI1_SCK_A, EVENTOUT	-
-	-	-	-	-	-	D8	E7	5	5	D2	D2	5	5	E3	E3	PE6	I/O	FT	-	TRACED3, TIM3_CH4, SAI1_D1, DCMI_D7/PSSI_D7, LCD_G6, FMC_A22, SAI1_SD_A, EVENTOUT	RTC_TAMP3,WKUP3
1	1	1	1	1	1	C10	C10	6	6	E2	E2	6	6	E2	E2	VBAT	S	-	-	-	-
2	2	2	2	2	2	C9	C9	7	7	C1	C1	7	7	E1	E1	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_TAMP1/RTC_TS/RTC_OUT,WKUP2

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
3	3	3	3	3	3	D10	D10	8	8	D1	D1	8	8	F1	F1	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
4	4	4	4	4	4	D9	E10	9	9	E1	E1	9	9	G1	G1	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	-	-	-	-	D6	D6	10	10	F5	F5	PF0	I/O	FT_f	-	I2C2_SDA, OCTOSPIM_P2_IO0, FMC_A0, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	D5	D5	11	11	F4	F4	PF1	I/O	FT_f	-	I2C2_SCL, OCTOSPIM_P2_IO1, FMC_A1, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	D4	D4	12	12	F3	F3	PF2	I/O	FT	-	I2C2_SMBA, OCTOSPIM_P2_IO2, FMC_A2, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	E4	E4	13	13	G3	G3	PF3	I/O	FT	-	OCTOSPIM_P2_IO3, FMC_A3, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	F3	F3	14	14	G4	G4	PF4	I/O	FT	-	OCTOSPIM_P2_CLK, FMC_A4, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	F4	F4	15	15	G5	G5	PF5	I/O	FT	-	OCTOSPIM_P2_NCLK, FMC_A5, EVENTOUT	-
-	-	-	-	-	-	E10	D9	10	10	F2	F2	16	16	F2	F2	VSS	S	-	-	-	-
-	-	-	-	-	-	E9	E9	11	11	G2	G2	17	17	G2	G2	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	18	18	-	-	PF6	I/O	FT	-	TIM5_ETR, TIM5_CH1, OCTOSPIM_P1_IO3, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	19	19	-	-	PF7	I/O	FT	-	TIM5_CH2, OCTOSPIM_P1_IO2, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	20	20	-	-	PF8	I/O	FT	-	TIM5_CH3, OCTOSPIM_P1_IO0, SAI1_SCK_B, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	21	21	-	-	PF9	I/O	FT	-	TIM5_CH4, OCTOSPIM_P1_IO1, SAI1_FS_B, TIM15_CH1, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	-	-	22	22	H4	H4	PF10	I/O	FT	-	OCTOSPIM_P1_CLK, PSSI_D15, DFSDM1_CKOUT, DCMI_D11/PSSI_D11, SAI1_D3, TIM15_CH2, EVENTOUT	-
5	5	5	5	5	5	F10	F10	12	12	F1	F1	23	23	H1	H1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
6	6	6	6	6	6	F9	G10	13	13	G1	G1	24	24	J1	J1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
7	7	7	7	7	7	F8	E8	14	14	H2	H2	25	25	H3	H3	NRST	I-O	RST	-	-	-
-	-	-	-	8	8	G10	F9	15	15	H1	H1	26	26	J2	J2	PC0	I/O	FT_fla	-	LPTIM1_IN1, I2C3_SCL, SDMMC2_CKIN, LPUART1_RX, LCD_DE, SDMMC1_CMD, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	ADC12_IN1

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	9	9	F7	F8	16	16	J2	J2	27	27	J3	J3	PC1	I/O	FT_fla	-	TRACED0, LPTIM1_OUT, SPI2_MOSI, I2C3_SDA, LPUART1_TX, OCTOSPIM_P1_IO4, SAI1_SD_A, EVENTOUT	ADC12_IN2
-	-	-	-	10	10	G9	H10	17	17	J3	J3	28	28	J4	J4	PC2	I/O	FT_la	-	LPTIM1_IN2, SPI2_MISO, DFSDM1_CKOUT, OCTOSPIM_P1_IO5, LCD_HSYNC, EVENTOUT	ADC12_IN3
-	-	-	-	11	11	F6	F7	18	18	K2	K2	29	29	K1	K1	PC3	I/O	FT_a	-	LPTIM1_ETR, SAI1_D1, SPI2_MOSI, OCTOSPIM_P1_IO6, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC12_IN4
-	-	-	-	-	-	-	H9	19	19	-	-	30	30	-	-	VSSA	S	-	-	-	-
-	-	-	-	-	-	-	G8	20	20	-	-	31	31	-	-	VREF-	S	-	-	-	-
8	8	8	8	12	12	H9	-	-	-	J1	J1	-	-	K2	K2	VSSA/VREF-	S	-	-	-	-
-	-	-	-	-	-	H10	G7	21	21	L1	L1	32	32	L1	L1	VREF+	S	-	-	-	VREFBUF_OUT

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	J10	J10	22	22	M1	M1	33	33	L2	L2	VDDA	S	-	-	-	-
9	9	9	9	13	13	-	-	-	-	-	-	-	-	-	-	VDDA/VREF+	S	-	-	-	-
10	10	10	10	14	14	G8	G9	23	23	L2	L2	34	34	K3	K3	PA0	I/O	FT_a	-	TIM2_CH1, TIM5_CH1, TIM8_ETR, USART2_CTS_NSS, UART4_TX, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, ADC12_IN5, RTC_TAMP2,WKUP1
-	-	-	-	-	-	-	-	-	-	M3	M3	-	-	M1	M1	OPAMP1_VINM	I	TT	-	-	-
11	11	11	11	15	15	G7	H8	24	24	M2	M2	35	35	N2	N2	PA1	I/O	FT_la	-	TIM2_CH2, TIM5_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS_DE, UART4_RX, OCTOSPIM_P1_DQS, SDMMC2_CMD, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, ADC12_IN6

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
12	12	12	12	16	16	H8	H7	25	25	K3	K3	36	36	N1	N1	PA2	I/O	FT_la	-	TIM2_CH3, TIM5_CH3, USART2_TX, LPUART1_TX, OCTOSPIM_P1_NCS, SAI2_EXTCLK, TIM15_CH1, EVENTOUT	ADC12_IN7, WKUP4/LSCO
13	13	13	13	17	17	J9	J9	26	26	L3	L3	37	37	M2	M2	PA3	I/O	TT_a	-	TIM2_CH4, TIM5_CH4, SAI1_CK1, USART2_RX, LPUART1_RX, OCTOSPIM_P1_CLK, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, ADC12_IN8
-	-	-	-	18	18	K10	K10	27	27	E3	E3	38	38	H2	H2	VSS	S	-	-	-	-
-	-	-	-	19	19	J8	J8	28	28	H3	H3	39	39	N3	N3	VDD	S	-	-	-	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
14	14	14	14	20	20	H7	F6	29	29	J4	J4	40	40	L3	L3	PA4	I/O	TT_a	-	OCTOSPIM_P1_NCS, SPI1_NSS, SPI3_NSS, USART2_CK, DCMI_HSYNC/PSSI_DE, LCD_CLK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	ADC12_IN9, DAC1_OUT1
15	15	15	15	21	21	J7	G6	30	30	K4	K4	41	41	K4	K4	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, TIM8_CH1N, PSSI_D14, SPI1_SCK, LCD_R7, LPTIM2_ETR, EVENTOUT	ADC12_IN10, DAC1_OUT2
16	16	16	16	22	22	K9	K9	31	31	L4	L4	42	42	M4	M4	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, DCMI_PIXCLK/PSSI_PDCK, SPI1_MISO, USART3_CTS_NSS, LPUART1_CTS, OCTOSPIM_P1_IO3, TIM16_CH1, EVENTOUT	OPAMP2_VINP, ADC12_IN11
-	-	-	-	-	-	-	-	-	-	M4	M4	-	-	N4	N4	OPAMP2_VINM	I	TT	-	-	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
17	17	17	17	23	23	G6	J7	32	32	J5	J5	43	43	L4	L4	PA7	I/O	FT_fla	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, I2C3_SCL, SPI1_MOSI, OCTOSPIM_P1_IO2, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC12_IN12
-	-	-	-	24	24	K8	H6	33	33	K5	K5	44	44	H5	H5	PC4	I/O	FT_a	-	OCTOSPIM_P2_NCS, USART3_TX, OCTOSPIM_P1_IO7, EVENTOUT	COMP1_INM, ADC12_IN13
-	-	-	-	NC	25	-	K8	34	34	L5	L5	45	45	J5	J5	PC5	I/O	FT_a	(3)	SAI1_D3, PSSI_D15, USART3_RX, LCD_CLK, EVENTOUT	COMP1_INP, ADC12_IN14, WKUP5
18	18	18	18	25	26	H6	J6	35	35	M5	M5	46	46	K5	K5	PB0	I/O	TT_la	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI1_NSS, USART3_CK, OCTOSPIM_P1_IO1, LCD_B6, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	OPAMP2_VOUT, ADC12_IN15

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
19	19	19	19	26	27	K7	K7	36	36	M6	M6	47	47	L5	L5	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN0, USART3_RTS_DE, LPUART1_RTS_DE, OCTOSPIM_P1_IO0, LCD_G6, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC12_IN16
20	20	20	20	27	28	J6	F5	37	37	L6	L6	48	48	N5	N5	PB2	I/O	FT_a	-	RTC_OUT2, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, OCTOSPIM_P1_DQS, EVENTOUT	COMP1_INP
-	-	-	-	-	-	-	-	-	-	K6	K6	49	49	M5	M5	PF11	I/O	FT	-	OCTOSPIM_P1_NCLK, LCD_DE, DCMI_D12/PSSI_D12, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	J7	J7	50	50	N6	N6	PF12	I/O	FT	-	OCTOSPIM_P2_DQS, LCD_B0, FMC_A6, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	E3	E3	51	51	H2	H2	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	H3	H3	52	52	N7	N7	VDD	S	-	-	-	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	K7	K7	53	53	M6	M6	PF13	I/O	FT	-	I2C4_SMBA, LCD_B1, FMC_A7, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	J8	J8	54	54	L6	L6	PF14	I/O	FT_f	-	I2C4_SCL, TSC_G8_IO1, LCD_G0, FMC_A8, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	J9	J9	55	55	K6	K6	PF15	I/O	FT_f	-	I2C4_SDA, TSC_G8_IO2, LCD_G1, FMC_A9, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	H9	H9	56	56	J6	J6	PG0	I/O	FT	-	OCTOSPIM_P2_IO4, TSC_G8_IO3, FMC_A10, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	G9	G9	57	57	H6	H6	PG1	I/O	FT	-	OCTOSPIM_P2_IO5, TSC_G8_IO4, FMC_A11, EVENTOUT	-
-	-	-	-	-	-	K6	K6	38	38	M7	M7	58	58	L7	L7	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, LCD_B6, FMC_D4, SAI1_SD_B, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	K5	K5	39	39	L7	L7	59	59	K7	K7	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, LCD_B7, FMC_D5, SAI1_SCK_B, EVENTOUT	-
-	-	-	-	-	-	J5	J5	40	40	M8	M8	60	60	J7	J7	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, OCTOSPIM_P1_NCLK, LCD_G2, FMC_D6, SAI1_FS_B, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	F6	F6	61	61	M7	M7	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	G6	G6	62	62	N7	N7	VDD	S	-	-	-	-
-	-	-	-	-	-	H5	H5	41	41	L8	L8	63	63	H7	H7	PE10	I/O	FT	-	TIM1_CH2N, TSC_G5_IO1, OCTOSPIM_P1_CLK, LCD_G3, FMC_D7, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	K4	K4	42	42	M9	M9	64	64	N8	N8	PE11	I/O	FT	-	TIM1_CH2, TSC_G5_IO2, OCTOSPIM_P1_NCS, LCD_G4, FMC_D8, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	J4	G5	43	43	L9	L9	65	65	M8	M8	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, TSC_G5_IO3, OCTOSPIM_P1_IO0, LCD_G5, FMC_D9, EVENTOUT	-
-	-	-	-	-	-	G5	G4	44	44	M10	M10	66	66	L8	L8	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, TSC_G5_IO4, OCTOSPIM_P1_IO1, LCD_G6, FMC_D10, EVENTOUT	-
-	-	-	-	-	-	G4	J4	45	45	M11	M11	67	67	K8	K8	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, OCTOSPIM_P1_IO2, LCD_G7, FMC_D11, EVENTOUT	-
-	-	-	-	-	-	H4	H4	46	46	M12	M12	68	68	J8	J8	PE15	I/O	FT	-	TIM1_BKIN, SPI1_MOSI, OCTOSPIM_P1_IO3, LCD_R2, FMC_D12, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
21	21	21	21	28	29	K3	K3	47	47	L10	L10	69	69	N9	N9	PB10	I/O	FT_fl	-	TIM2_CH3, I2C4_SCL, I2C2_SCL, SPI2_SCK, OCTOSPIM_P1_IO3, USART3_TX, LPUART1_RX, TSC_SYNC, OCTOSPIM_P1_CLK, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-
NC	22	NC	22	29	30	J3	J3	NC	48	NC	L11	NC	70	H8	H8	PB11	I/O	FT_fl	(3)	TIM2_CH4, I2C4_SDA, I2C2_SDA, USART3_RX, LPUART1_TX, OCTOSPIM_P1_NCS, LCD_VSYNC, COMP2_OUT, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	K9	K9	PH4	I/O	FT_f	-	I2C2_SCL, OCTOSPIM_P2_DQS, PSSI_D14, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	L9	L9	PH5	I/O	FT_f	-	I2C2_SDA, DCMI_PIXCLK/PSSI_PDCK, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	-	-	-	-	N10	N10	PH8	I/O	FT_f	-	I2C3_SDA, OCTOSPIM_P2_IO3, DCMI_HSYNC/PSSI_DE, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	M9	M9	PH10	I/O	FT	-	TIM5_CH1, OCTOSPIM_P2_IO5, DCMI_D1/PSSI_D1, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	NC	M10	PH11	I/O	FT	(3)	TIM5_CH2, OCTOSPIM_P2_IO6, DCMI_D2/PSSI_D2, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	F6	F6	-	-	C2	C2	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	G6	G6	-	-	L12	L12	VDD	S	-	-	-	-
22	-	22	-	30	-	K1	-	48	-	L11	-	70	-	M10	-	VDD12	S	-	-	-	-
23	23	23	23	31	31	K2	K2	49	49	F12	F12	71	71	A7	A7	VSS	S	-	-	-	-
24	24	24	24	32	32	J2	K1	50	50	G12	G12	72	72	N11	N11	VDD	S	-	-	-	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
25	25	25	25	33	33	J1	J1	51	51	L12	L12	73	73	N12	N12	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS, DFSDM1_DATIN1, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, OCTOSPIM_P1_NCLK, SDMMC2_CK, SAI2_FS_A, TIM15_BKIN, EVENTOUT	-
26	26	26	26	34	34	H2	J2	52	52	K12	K12	74	74	N13	N13	PB13	I/O	FT_fl	-	TIM1_CH1N, I2C2_SCL, SPI2_SCK, DFSDM1_CKIN1, USART3_CTS_NSS, LPUART1_CTS, TSC_G1_IO2, OCTOSPIM_P1_IO1, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
27	27	27	27	35	35	H1	H2	53	53	K11	K11	75	75	M13	M13	PB14	I/O	FT_fl	-	TIM1_CH2N, TIM8_CH2N, I2C2_SDA, SPI2_MISO, DFSDM1_DATIN2, USART3_RTS_DE, TSC_G1_IO3, OCTOSPIM_P1_IO6, SDMMC2_D0, SAI2_MCLK_A, TIM15_CH1, EVENTOUT	-
28	28	28	28	36	36	H3	H1	54	54	K10	K10	76	76	M12	M12	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM1_CKIN2, TSC_G1_IO4, OCTOSPIM_P1_IO7, SDMMC2_D1, SAI2_SD_A, TIM15_CH2, EVENTOUT	-
-	-	-	-	-	-	G3	H3	55	55	K9	K9	77	77	L11	L11	PD8	I/O	FT	-	USART3_TX, DCMI_HSYNC/PSSI_DE, LCD_R3, FMC_D13, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	G2	G2	56	56	K8	K8	78	78	L10	L10	PD9	I/O	FT	-	USART3_RX, DCMI_PIXCLK/PSSI_PDCK, LCD_R4, FMC_D14, SAI2_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	G1	G1	57	57	J12	J12	79	79	J13	J13	PD10	I/O	FT	-	USART3_CK, TSC_G6_IO1, LCD_R5, FMC_D15, SAI2_SCK_A, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	F11	F11	-	-	L13	L13	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	H3	H3	-	-	H13	H13	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	58	58	J11	J11	80	80	K12	K12	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS_NSS, TSC_G6_IO2, LCD_R6, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	59	59	J10	J10	81	81	K11	K11	PD12	I/O	FT_fl	-	TIM4_CH1, I2C4_SCL, USART3_RTS_DE, TSC_G6_IO3, LCD_R7, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	-
-	-	-	-	-	-	-	-	60	60	H12	H12	82	82	K13	K13	PD13	I/O	FT_fl	-	TIM4_CH2, I2C4_SDA, TSC_G6_IO4, FMC_A18, LPTIM2_OUT, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	F11	F11	83	83	H12	H12	VSS	S	-	-	-	-
-	-	-	-	-	-	F1	F1	-	-	H3	H3	84	84	G13	G13	VDD	S	-	-	-	-
-	-	-	-	-	-	F3	G3	61	61	H11	H11	85	85	K10	K10	PD14	I/O	FT	-	TIM4_CH3, LCD_B2, FMC_D0, EVENTOUT	-
-	-	-	-	-	-	F2	F4	62	62	H10	H10	86	86	H11	H11	PD15	I/O	FT	-	TIM4_CH4, LCD_B3, FMC_D1, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	G10	G10	87	87	J12	J12	PG2	I/O	FT_s	-	SPI1_SCK, SDMMC2_D4, FMC_A12, SAI2_SCK_B, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	F9	F9	88	88	J11	J11	PG3	I/O	FT_s	-	SPI1_MISO, SDMMC2_D5, FMC_A13, SAI2_FS_B, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	F10	F10	89	89	J10	J10	PG4	I/O	FT_s	-	SPI1_MOSI, SDMMC2_D6, FMC_A14, SAI2_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	E9	E9	90	90	J9	J9	PG5	I/O	FT_s	-	SPI1_NSS, LPUART1_CTS, SDMMC2_D7, FMC_A15, SAI2_SD_B, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	G4	G4	91	91	G11	G11	PG6	I/O	FT_s	-	OCTOSPIM_P1_DQS, I2C3_SMBA, LPUART1_RTS_DE, LCD_R1, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	H4	H4	92	92	H10	H10	PG7	I/O	FT_fs	-	SAI1_CK1, I2C3_SCL, OCTOSPIM_P2_DQS, DFSDM1_CKOUT, LPUART1_TX, FMC_INT, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	J6	J6	93	93	H9	H9	PG8	I/O	FT_fs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	F7	F7	94	94	F13	F13	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	G7	G7	95	95	F12	F12	VDDIO2	S	-	-	-	-
-	-	-	-	37	37	F4	F2	63	63	E12	E12	96	96	F11	F11	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, SDMMC2_D6, SDMMC1_D0DIR, TSC_G4_IO1, DCMI_D0/PSSI_D0, LCD_G7, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	38	38	E4	F3	64	64	E11	E11	97	97	G12	G12	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, SDMMC2_D7, SDMMC1_D123DIR, TSC_G4_IO2, DCMI_D1/PSSI_D1, LCD_B6, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT	-
-	-	-	-	39	39	E1	E1	65	65	E10	E10	98	98	G10	G10	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, TSC_G4_IO3, DCMI_D2/PSSI_D2, SDMMC1_D0, EVENTOUT	-
-	-	-	-	40	40	E2	E2	66	66	D12	D12	99	99	G9	G9	PC9	I/O	FT _fl	-	TRACED0, TIM8_BKIN2, TIM3_CH4, TIM8_CH4, DCMI_D3/PSSI_D3, I2C3_SDA, TSC_G4_IO4, OTG_FS_NOE, SDMMC1_D1, SAI2_EXTCLK, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
29	29	29	29	41	41	E3	E3	67	67	D11	D11	100	100	G8	G8	PA8	I/O	FT_f	-	MCO, TIM1_CH1, SAI1_CK2, USART1_CK, OTG_FS_SOF, LCD_B7, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
30	30	30	30	42	42	D3	D3	68	68	D10	D10	101	101	F10	F10	PA9	I/O	FT_fu	-	TIM1_CH2, SPI2_SCK, DCMI_D0/PSSI_D0, USART1_TX, LCD_G7, SAI1_FS_A, TIM15_BKIN, EVENTOUT	OTG_FS_VBUS
31	31	31	31	43	43	D2	D2	69	69	C12	C12	102	102	F9	F9	PA10	I/O	FT_fu	-	TIM1_CH3, SAI1_D1, DCMI_D1/PSSI_D1, USART1_RX, OTG_FS_ID, LCD_G6, SAI1_SD_A, TIM17_BKIN, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
32	32	32	32	44	44	D1	D1	70	70	B12	B12	103	103	E13	E13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS_NSS, CAN1_RX, OTG_FS_DM, LCD_DE, EVENTOUT	-
33	33	33	33	45	45	C1	C1	71	71	A12	A12	104	104	D13	D13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, OCTOSPIM_P2_NCS, USART1_RTS_DE, CAN1_TX, OTG_FS_DP, LCD_VSYNC, EVENTOUT	-
34	34	34	34	46	46	C2	C2	72	72	A11	A11	105	105	A11	A11	PA13 (JTMS/SWDIO)	I/O	FT	(4)	JTMS/SWDIO, IR_OUT, OTG_FS_NOE, SAI1_SD_B, EVENTOUT	-
35	35	35	35	47	47	B1	B1	-	-	F11	F11	-	-	C12	C12	VSS	S	-	-	-	-
36	36	36	36	48	48	A1	A1	73	73	C11	C11	106	106	E12	E12	VDDUSB	S	-	-	-	-
-	-	-	-	-	-	B1	B1	74	74	F11	F11	107	107	C12	C12	VSS	S	-	-	-	-
-	-	-	-	-	-	F1	F1	75	75	G11	G11	108	108	C13	C13	VDD	S	-	-	-	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	-	-	-	-	E11	E11	PH6	I/O	FT	-	I2C2_SMBA, OCTOSPIM_P2_CLK, DCMI_D8/PSSI_D8, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	D12	D12	PH7	I/O	FT_f	-	I2C3_SCL, OCTOSPIM_P2_NCLK, DCMI_D9/PSSI_D9, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	D11	D11	PH9	I/O	FT	-	I2C3_SMBA, OCTOSPIM_P2_IO4, DCMI_D0/PSSI_D0, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	B13	B13	PH12	I/O	FT	-	TIM5_CH3, OCTOSPIM_P2_IO7, DCMI_D3/PSSI_D3, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	A13	A13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4/PSSI_D4, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	B12	B12	PH15	I/O	FT	-	TIM8_CH3N, OCTOSPIM_P2_IO6, DCMI_D11/PSSI_D11, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	-	-	-	-	A12	A12	PI0	I/O	FT	-	TIM5_CH4, OCTOSPIM_P1_IO5, SPI2_NSS, DCMI_D13/PSSI_D13, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	C11	C11	PI8	I/O	FT	-	OCTOSPIM_P2_NCS, DCMI_D12/PSSI_D12, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	B11	B11	PI1	I/O	FT	-	SPI2_SCK, DCMI_D8/PSSI_D8, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	B10	B10	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, DCMI_D9/PSSI_D9, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	C10	C10	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI, DCMI_D10/PSSI_D10, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	D10	D10	PI4	I/O	FT	-	TIM8_BKIN, DCMI_D5/PSSI_D5, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	-	-	-	-	E10	E10	PI5	I/O	FT	-	TIM8_CH1, OCTOSPIM_P2_NCS, DCMI_VSYNC/PSSI_RDY, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	C9	C9	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	B9	B9	PI6	I/O	FT	-	TIM8_CH2, OCTOSPIM_P2_CLK, DCMI_D6/PSSI_D6, EVENTOUT	-
37	37	37	37	49	49	B2	B2	76	76	A10	A10	109	109	A10	A10	PA14 (JTCK/SWCLK)	I/O	FT	(4)	JTCK/SWCLK, LPTIM1_OUT, I2C1_SMBA, I2C4_SMBA, OTG_FS_SOF, SAI1_FS_B, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
38	38	38	38	50	50	A2	A2	77	77	A9	A9	110	110	A9	A9	PA15 (JTDI)	I/O	FT	(4)	JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS_DE, UART4_RTS_DE, TSC_G3_IO1, LCD_HSYNC, SAI2_FS_B, EVENTOUT	-
-	-	-	-	51	51	C3	D4	78	78	B11	B11	111	111	D9	D9	PC10	I/O	FT	-	TRACED1, DCMI_VSYNC/PSSI_RDY, SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, DCMI_D8/PSSI_D8, SDMMC1_D2, SAI2_SCK_B, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	52	52	D4	C3	79	79	C10	C10	112	112	E9	E9	PC11	I/O	FT	-	DCMI_D2/PSSI_D2, OCTOSPIM_P1_NCS, SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, DCMI_D4/PSSI_D4, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT	-
-	-	-	-	53	53	C4	C4	80	80	B10	B10	113	113	F8	F8	PC12	I/O	FT	-	TRACED3, SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, DCMI_D9/PSSI_D9, LCD_R6, SDMMC1_CK, SAI2_SD_B, EVENTOUT	-
-	-	-	-	-	-	B3	B3	81	81	C9	C9	114	114	B8	B8	PD0	I/O	FT	-	SPI2_NSS, CAN1_RX, LCD_B4, FMC_D2, EVENTOUT	-
-	-	-	-	-	-	A3	A3	82	82	B9	B9	115	115	C8	C8	PD1	I/O	FT	-	SPI2_SCK, CAN1_TX, LCD_B5, FMC_D3, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	NC	54	D5	E4	83	83	C8	C8	116	116	D8	D8	PD2	I/O	FT	(3)	TRACED2, TIM3_ETR, USART3_RTS_DE, UART5_RX, TSC_SYNC, DCMI_D11/PSSI_D11, SDMMC1_CMD, EVENTOUT	-
-	-	-	-	-	-	-	-	84	84	B8	B8	117	117	E8	E8	PD3	I/O	FT	-	SPI2_SCK, DCMI_D5/PSSI_D5, SPI2_MISO, DFSDM1_DATIN0, USART2_CTS_NSS, OCTOSPIM_P2_NCS, LCD_CLK, FMC_CLK, EVENTOUT	-
-	-	-	-	-	-	C5	B4	85	85	B7	B7	118	118	C7	C7	PD4	I/O	FT	-	SPI2_MOSI, DFSDM1_CKIN0, USART2_RTS_DE, SDMMC2_CKIN, OCTOSPIM_P1_IO4, FMC_NOE, EVENTOUT	-
-	-	-	-	-	-	B4	E5	86	86	A6	A6	119	119	D7	D7	PD5	I/O	FT	-	USART2_TX, OCTOSPIM_P1_IO5, FMC_NWE, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	F11	F11	120	120	M3	M3	VSS	S	-	-	-	-
-	-	-	-	-	-	A4	A4	-	-	G11	G11	121	121	A8	A8	VDD	S	-	-	-	-
-	-	-	-	-	-	B5	D5	87	87	B6	B6	122	122	E7	E7	PD6	I/O	FT	-	SAI1_D1, DCMI_D10/PSSI_D10, SPI3_MOSI, DFSDM1_DATIN1, USART2_RX, SDMMC2_CK, OCTOSPIM_P1_IO6, LCD_DE, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
-	-	-	-	-	-	C6	C5	88	88	A5	A5	123	123	F7	F7	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, SDMMC2_CMD, OCTOSPIM_P1_IO7, FMC_NCE/FMC_NE1, EVENTOUT	-
-	-	-	-	-	-	D6	B5	-	-	D9	D9	124	124	B7	B7	PG9	I/O	FT_s	-	OCTOSPIM_P2_IO6, SPI3_SCK, USART1_TX, SDMMC2_D0, FMC_NCE/FMC_NE2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	A5	A5	-	-	D8	D8	125	125	D6	D6	PG10	I/O	FT_s	-	LPTIM1_IN1, OCTOSPIM_P2_IO7, SPI3_MISO, USART1_RX, SDMMC2_D1, FMC_NE3, SAI2_FS_A, TIM15_CH1, EVENTOUT	-
-	-	-	-	-	-	E5	D6	-	-	G3	G3	126	126	E6	E6	PG11	I/O	FT_s	-	LPTIM1_IN2, OCTOSPIM_P1_IO5, SPI3_MOSI, USART1_CTS_NSS, SDMMC2_D2, SAI2_MCLK_A, TIM15_CH2, EVENTOUT	-
-	-	-	-	-	-	B6	B6	-	-	D7	D7	127	127	F6	F6	PG12	I/O	FT_s	-	LPTIM1_ETR, OCTOSPIM_P2_NCS, SPI3_NSS, USART1_RTS_DE, SDMMC2_D3, FMC_NE4, SAI2_SD_A, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	C7	C7	128	128	G7	G7	PG13	I/O	FT_fs	-	I2C1_SDA, USART1_CK, LCD_R0, FMC_A24, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	NC	C6	129	129	G6	G6	PG14	I/O	FT_fs	(3)	I2C1_SCL, LCD_R1, FMC_A25, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	F7	F7	130	130	A7	A7	VSS	S	-	-	-	-
-	-	-	-	-	-	A6	A6	-	-	G7	G7	131	131	B6	B6	VDDIO2	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	K1	K1	NC	132	NC	C6	PG15	I/O	FT_s	(3)	LPTIM1_OUT, I2C1_SMBA, OCTOSPIM_P2_DQS, DCMI_D13/PSSI_D13, EVENTOUT	-
39	39	39	39	54	55	F5	C6	89	89	A8	A8	132	133	A6	A6	PB3 (JTDO/TRACESWO)	I/O	FT_la	-	JTDO/TRACESWO, TIM2_CH2, OCTOSPIM_P1_IO4, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, OTG_FS_CRS_SYNC, SDMMC2_D2, SAI1_SCK_B, EVENTOUT	COMP2_INM

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
40	40	40	40	55	56	E6	C7	90	90	A7	A7	133	134	A5	A5	PB4 (NJTRST)	I/O	FT_fa	(4)	NJTRST, TIM3_CH1, OCTOSPIM_P1_IO5, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS_NSS, UART5_RTS_DE, TSC_G2_IO1, DCMI_D12/PSSI_D12, SDMMC2_D3, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT	COMP2_INP
41	41	41	41	56	57	C7	B7	91	91	C5	C5	134	135	B5	B5	PB5	I/O	FT_la	-	LPTIM1_IN1, TIM3_CH2, OCTOSPIM_P1_IO0, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, UART5_CTS, TSC_G2_IO2, DCMI_D10/PSSI_D10, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
42	42	42	42	57	58	A7	A7	92	92	B5	B5	135	136	C5	C5	PB6	I/O	FT_fa	-	LPTIM1_ETR, TIM4_CH1, TIM8_BKIN2, I2C1_SCL, I2C4_SCL, USART1_TX, TSC_G2_IO3, DCMI_D5/PSSI_D5, LCD_R6, SAI1_FS_B, TIM16_CH1N, EVENTOUT	COMP2_INP
43	43	43	43	58	59	B7	D7	93	93	B4	B4	136	137	D5	D5	PB7	I/O	FT_fla	-	LPTIM1_IN2, TIM4_CH2, TIM8_BKIN, I2C1_SDA, I2C4_SDA, USART1_RX, UART4_CTS, TSC_G2_IO4, DCMI_VSYNC/PSSI_RDY, LCD_VSYNC, FMC_NL, TIM17_CH1N, EVENTOUT	COMP2_INM, PVD_IN
44	44	44	44	59	60	D7	E6	94	94	A4	A4	137	138	E5	E5	PH3-BOOT0	I/O	FT	-	EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
NC	45	NC	45	60	61	B8	B8	95	95	A3	A3	138	139	C4	C4	PB8	I/O	FT_fl	(3)	TIM4_CH3, SAI1_CK1, I2C1_SCL, DFSDM1_CKOUT, SDMMC2_D4, SDMMC1_CKIN, CAN1_RX, DCMI_D6/PSSI_D6, LCD_DE, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	-
45	46	45	46	61	62	A8	A8	96	96	B3	B3	139	140	D4	D4	PB9	I/O	FT_fl	-	IR_OUT, TIM4_CH4, SAI1_D2, I2C1_SDA, SPI2_NSS, SDMMC2_D5, SDMMC1_CDIR, CAN1_TX, DCMI_D7/PSSI_D7, SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	97	97	C3	C3	140	141	A4	A4	PE0	I/O	FT	-	TIM4_ETR, DCMI_D2/PSSI_D2, LCD_HSYNC, FMC_NBL0, TIM16_CH1, EVENTOUT	-
-	-	-	-	-	-	-	-	NC	98	A2	A2	141	142	B4	B4	PE1	I/O	FT	(3)	DCMI_D3/PSSI_D3, LCD_VSYNC, FMC_NBL1, TIM17_CH1, EVENTOUT	-
46	-	46	-	62	-	A9	-	98	-	C6	-	142	-	C6	-	VDD12	-	-	-	-	-
47	47	47	47	63	63	B9	A9	99	99	D3	D3	143	143	B3	B3	VSS	S	-	-	-	-
48	48	48	48	64	64	A10	A10	100	100	C4	C4	144	144	A3	A3	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	C4	C4	-	-	A3	A3	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	D3	D3	-	-	B3	B3	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	A2	A2	PH2	I/O	FT	-	OCTOSPIM_P1_IO4, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	B2	B2	PI7	I/O	FT	-	TIM8_CH3, OCTOSPIM_P2_NCLK, DCMI_D7/PSSI_D7, EVENTOUT	-

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Table 15. STM32L4P5xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48 + Ext SMPS	UFQFPN48	LQFP48 + Ext SMPS	LQFP48	LQFP64 + Ext SMPS	LQFP64	WLCSP100 + Ext SMPS	WLCSP100	LQFP100 + Ext SMPS	LQFP100	UFBGA132 + Ext SMPS	UFBGA132	LQFP144 + Ext SMSP	LQFP144	UFBGA169 + ext SMPS	UFBGA169						
-	-	-	-	-	-	-	-	-	-	-	-	-	-	B1	B1	PI9	I/O	FT	-	OCTOSPIM_P2_IO2, CAN1_RX, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	A1	A1	PI10	I/O	FT	-	OCTOSPIM_P2_IO1, PSSI_D14, EVENTOUT	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (for example to drive a LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0432 reference manual.
3. NC (not-connected) balls must be left unconnected. However, PF8 and PF9 NC' IOs are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra current consumption in low-power modes.
4. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

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Table 16. Alternate function AF0 to AF7[1]

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/CAN2/OTG_FS/TIM1/8/OCTOSPIM_P1/QUADSPI	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2/QUADSPI	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P1/2/QUADSPI	USART1/2/3/SDMMC2
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS_NSS
	PA1	-	TIM2_CH2	TIM5_CH2	-	I2C1_SMBA	SPI1_SCK	-	USART2_RTS_DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	SAI1_CK1	-	-	-	USART2_RX
	PA4	-	-	-	OCTOSPIM_P1_NCS	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	PSSI_D14	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	DCMI_PIXCLK/PSSI_PDCK	SPI1_MISO	-	USART3_CTS_NSS
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	SAI1_CK2	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	SPI2_SCK	-	DCMI_D0/PSSI_D0	-	USART1_TX
	PA10	-	TIM1_CH3	-	SAI1_D1	-	DCMI_D1/PSSI_D1	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	USART1_CTS_NSS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	OCTOSPIM_P2_NCS	USART1_RTS_DE
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	I2C4_SMBA	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_RTS_DE

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Table 16. Alternate function AF0 to AF7[1]

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/CAN2/OTG_FS/TIM1/8/OCTOSPIM_P1/QUADSPI	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2/QUADSPI	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P1/2/QUADSPI	USART1/2/3/SDMMC2
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_DATIN0	USART3_RTS_DE
	PB2	RTC_OUT2	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM1_CKIN0	-
	PB3	JTDO/TRACESWO	TIM2_CH2	-	OCTOSPIM_P1_IO4	-	SPI1_SCK	SPI3_SCK	USART1_RTS_DE
	PB4	NJTRST	-	TIM3_CH1	OCTOSPIM_P1_IO5	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS_NSS
	PB5	-	LPTIM1_IN1	TIM3_CH2	OCTOSPIM_P1_IO0	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	I2C4_SCL	-	USART1_TX
	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	I2C4_SDA	-	USART1_RX
	PB8	-	-	TIM4_CH3	SAI1_CK1	I2C1_SCL	DFSDM1_CKOUT	-	SDMMC2_D4
	PB9	-	IR_OUT	TIM4_CH4	SAI1_D2	I2C1_SDA	SPI2_NSS	-	SDMMC2_D5
	PB10	-	TIM2_CH3	-	I2C4_SCL	I2C2_SCL	SPI2_SCK	OCTOSPIM_P1_IO3	USART3_TX
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-	-	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C2_SMBA	SPI2_NSS	DFSDM1_DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	DFSDM1_CKIN1	USART3_CTS_NSS
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2C2_SDA	SPI2_MISO	DFSDM1_DATIN2	USART3_RTS_DE
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI	DFSDM1_CKIN2	-

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Table 16. Alternate function AF0 to AF7[(1)]

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/CAN2/OTG_FS/TIM1/8/OCTOSPIM_P1/QUADSPI	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2/QUADSPI	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P1/2/QUADSPI	USART1/2/3/SDMMC2
Port C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	-	SDMMC2_CKIN
	PC1	TRACED0	LPTIM1_OUT	-	SPI2_MOSI	I2C3_SDA	-	-	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	DFSDM1_CKOUT	-
	PC3	-	LPTIM1_ETR	-	SAI1_D1	-	SPI2_MOSI	-	-
	PC4	-	-	-	-	-	OCTOSPIM_P2_NCS	-	USART3_TX
	PC5	-	-	-	SAI1_D3	PSSI_D15	-	-	USART3_RX
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	-	DFSDM1_CKIN3	SDMMC2_D6
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	DFSDM1_DATIN3	SDMMC2_D7
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-
	PC9	TRACED0	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	DCMI_D3/PSSI_D3	-	I2C3_SDA	-
	PC10	TRACED1	-	-	-	DCMI_VSYNC/PSSI_RDY	-	SPI3_SCK	USART3_TX
	PC11	-	-	-	-	DCMI_D2/PSSI_D2	OCTOSPIM_P1_NCS	SPI3_MISO	USART3_RX
	PC12	TRACED3	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

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Table 16. Alternate function AF0 to AF7[(1)]

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/CAN2/OTG_FS/TIM1/8/OCTOSPIM_P1/QUADSPI	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2/QUADSPI	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P1/2/QUADSPI	USART1/2/3/SDMMC2
Port D	PD0	-	-	-	-	-	SPI2_NSS	-	-
	PD1	-	-	-	-	-	SPI2_SCK	-	-
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	USART3_RTS_DE
	PD3	-	-	-	SPI2_SCK	DCMI_D5/PSSI_D5	SPI2_MISO	DFSDM1_DATIN0	USART2_CTS_NSS
	PD4	-	-	-	-	-	SPI2_MOSI	DFSDM1_CKIN0	USART2_RTS_DE
	PD5	-	-	-	-	-	-	-	USART2_TX
	PD6	-	-	-	SAI1_D1	DCMI_D10/PSSI_D10	SPI3_MOSI	DFSDM1_DATIN1	USART2_RX
	PD7	-	-	-	-	-	-	DFSDM1_CKIN1	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	-	-	-	-	-	-	-	USART3_CK
	PD11	-	-	-	-	I2C4_SMBA	-	-	USART3_CTS_NSS
	PD12	-	-	TIM4_CH1	-	I2C4_SCL	-	-	USART3_RTS_DE
	PD13	-	-	TIM4_CH2	-	I2C4_SDA	-	-	-
	PD14	-	-	TIM4_CH3	-	-	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	-	-

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Table 16. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/CAN2/OTG_FS/TIM1/8/OCTOSPIM_P1/QUADSPI	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2/QUADSPI	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P1/2/QUADSPI	USART1/2/3/SDMMC2
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	SAI1_CK1	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	OCTOSPIM_P1_DQS	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	SAI1_D2	-	-	DFSDM1_DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	SAI1_CK2	-	-	DFSDM1_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	SAI1_D1	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	-	-
	PE11	-	TIM1_CH2	-	-	-	-	-	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	-	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	-	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN	-	SPI1_MOSI	-	-

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Table 16. Alternate function AF0 to AF7[(1)]

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/CAN2/OTG_FS/TIM1/8/OCTOSPIM_P1/QUADSPI	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2/QUADSPI	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P1/2/QUADSPI	USART1/2/3/SDMMC2
Port F	PF0	-	-	-	-	I2C2_SDA	OCTOSPIM_P2_IO0	-	-
	PF1	-	-	-	-	I2C2_SCL	OCTOSPIM_P2_IO1	-	-
	PF2	-	-	-	-	I2C2_SMBA	OCTOSPIM_P2_IO2	-	-
	PF3	-	-	-	-	-	OCTOSPIM_P2_IO3	-	-
	PF4	-	-	-	-	-	OCTOSPIM_P2_CLK	-	-
	PF5	-	-	-	-	-	OCTOSPIM_P2_NCLK	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-	-	-
	PF10	-	-	-	OCTOSPIM_P1_CLK	PSSI_D15	-	DFSDM1_CKOUT	-
	PF11	-	-	-	OCTOSPIM_P1_NCLK	-	-	-	-
	PF12	-	-	-	-	-	OCTOSPIM_P2_DQS	-	-
	PF13	-	-	-	-	I2C4_SMBA	-	-	-
	PF14	-	-	-	-	I2C4_SCL	-	-	-
	PF15	-	-	-	-	I2C4_SDA	-	-	-

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Table 16. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/CAN2/OTG_FS/TIM1/8/OCTOSPIM_P1/QUADSPI	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2/QUADSPI	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P1/2/QUADSPI	USART1/2/3/SDMMC2
Port G	PG0	-	-	-	-	-	OCTOSPIM_P2_IO4	-	-
	PG1	-	-	-	-	-	OCTOSPIM_P2_IO5	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	OCTOSPIM_P1_DQS	I2C3_SMBA	-	-	-
	PG7	-	-	-	SAI1_CK1	I2C3_SCL	OCTOSPIM_P2_DQS	DFSDM1_CKOUT	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	OCTOSPIM_P2_IO6	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	OCTOSPIM_P2_IO7	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	OCTOSPIM_P1_IO5	-	-	SPI3_MOSI	USART1_CTS_NSS
	PG12	-	LPTIM1_ETR	-	-	-	OCTOSPIM_P2_NCS	SPI3_NSS	USART1_RTS_DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	OCTOSPIM_P2_DQS	-	-

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Table 16. Alternate function AF0 to AF7[1]

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/CAN2/OTG_FS/TIM1/8/OCTOSPIM_P1/QUADSPI	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2/QUADSPI	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P1/2/QUADSPI	USART1/2/3/SDMMC2
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH2	-	-	-	OCTOSPIM_P1_IO4	-	-	-	-
	PH3	-	-	-	-	-	-	-	-
	PH4	-	-	-	-	I2C2_SCL	OCTOSPIM_P2_DQS	-	-
	PH5	-	-	-	-	I2C2_SDA	-	-	-
	PH6	-	-	-	-	I2C2_SMBA	OCTOSPIM_P2_CLK	-	-
	PH7	-	-	-	-	I2C3_SCL	OCTOSPIM_P2_NCLK	-	-
	PH8	-	-	-	-	I2C3_SDA	OCTOSPIM_P2_IO3	-	-
	PH9	-	-	-	-	I2C3_SMBA	OCTOSPIM_P2_IO4	-	-
	PH10	-	-	TIM5_CH1	-	-	OCTOSPIM_P2_IO5	-	-
	PH11	-	-	TIM5_CH2	-	-	OCTOSPIM_P2_IO6	-	-
	PH12	-	-	TIM5_CH3	-	-	OCTOSPIM_P2_IO7	-	-
	PH13	-	-	-	TIM8_CH1N	-	-	-	-
	PH14	-	-	-	TIM8_CH2N	-	-	-	-
	PH15	-	-	-	TIM8_CH3N	-	OCTOSPIM_P2_IO6	-	-

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Table 16. Alternate function AF0 to AF7[1]

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/CAN2/OTG_FS/TIM1/8/OCTOSPIM_P1/QUADSPI	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2/QUADSPI	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P1/2/QUADSPI	USART1/2/3/SDMMC2
Port I	PI0	-	-	TIM5_CH4	OCTOSPIM_P1_IO5	-	SPI2_NSS	-	-
	PI1	-	-	-	-	-	SPI2_SCK	-	-
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	-	-
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI	-	-
	PI4	-	-	-	TIM8_BKIN	-	-	-	-
	PI5	-	-	-	TIM8_CH1	-	OCTOSPIM_P2_NCS	-	-
	PI6	-	-	-	TIM8_CH2	-	OCTOSPIM_P2_CLK	-	-
	PI7	-	-	-	TIM8_CH3	-	OCTOSPIM_P2_NCLK	-	-
	PI8	-	-	-	-	-	OCTOSPIM_P2_NCS	-	-
	PI9	-	-	-	-	-	OCTOSPIM_P2_IO2	-	-
	PI10	-	-	-	-	-	OCTOSPIM_P2_IO1	-	-
	PI11	-	-	-	-	-	OCTOSPIM_P2_IO0	-	-

1. Refer to next table for AF8 to AF15.

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Table 17. Alternate function AF8 to AF15[(1)]

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/CAN2/SDMMC1/2	CAN1/TSC/LCD	CAN2/OTG_FS/DCMI/OCTOSPIM_P1/2/QUADSPI	SDMMC2/LCD/DSI/LCD	SDMMC1/2/COMP1/2/TIM1/8/FMC/SWPMI1	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENOUT
Port A	PA0	UART4_TX	-	-	-	-	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	OCTOSPIM_P1_DQS	-	SDMMC2_CMD	-	TIM15_CH1N	EVENTOUT
	PA2	LPUART1_TX	-	OCTOSPIM_P1_NCS	-	-	SAI2_EXTCLK	TIM15_CH1	EVENTOUT
	PA3	LPUART1_RX	-	OCTOSPIM_P1_CLK	-	-	SAI1_MCLK_A	TIM15_CH2	EVENTOUT
	PA4	-	-	DCMI_HSYNC/PSSI_DE	LCD_CLK	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	LCD_R7	-	-	LPTIM2_ETR	EVENTOUT
	PA6	LPUART1_CTS	-	OCTOSPIM_P1_IO3	-	TIM1_BKIN	TIM8_BKIN	TIM16_CH1	EVENTOUT
	PA7	-	-	OCTOSPIM_P1_IO2	-	-	-	TIM17_CH1	EVENTOUT
	PA8	-	-	OTG_FS_SOF	LCD_B7	-	SAI1_SCK_A	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-	LCD_G7	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PA10	-	-	OTG_FS_ID	LCD_G6	-	SAI1_SD_A	TIM17_BKIN	EVENTOUT
	PA11	-	CAN1_RX	OTG_FS_DM	LCD_DE	TIM1_BKIN2	-	-	EVENTOUT
	PA12	-	CAN1_TX	OTG_FS_DP	LCD_VSYNC	-	-	-	EVENTOUT
	PA13	-	-	OTG_FS_NOE	-	-	SAI1_SD_B	-	EVENTOUT
	PA14	-	-	OTG_FS_SOF	-	-	SAI1_FS_B	-	EVENTOUT
	PA15	UART4_RTS_DE	TSC_G3_IO1	-	LCD_HSYNC	-	SAI2_FS_B	-	EVENTOUT

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Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/CAN2/SDMMC1/2	CAN1/TSC/LCD	CAN2/OTG_FS/DCMI/OCTOSPIM_P1/2/QUADSPI	SDMMC2/LCD/DSI/LCD	SDMMC1/2/COMP1/2/TIM1/8/FMC/SWPMI1	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENOUT
Port B	PB0	-	-	OCTOSPIM_P1_IO1	LCD_B6	COMP1_OUT	SAI1_EXTCLK	-	EVENTOUT
	PB1	LPUART1_RTS_DE	-	OCTOSPIM_P1_IO0	LCD_G6	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	OCTOSPIM_P1_DQS	-	-	-	-	EVENTOUT
	PB3	-	-	OTG_FS_CRS_SYNC	-	SDMMC2_D2	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_RTS_DE	TSC_G2_IO1	DCMI_D12/PSSI_D12	-	SDMMC2_D3	SAI1_MCLK_B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS	TSC_G2_IO2	DCMI_D10/PSSI_D10	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	DCMI_D5/PSSI_D5	LCD_R6	TIM8_BKIN2	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	DCMI_VSYNC/PSSI_RDY	LCD_VSYNC	FMC_NL	TIM8_BKIN	TIM17_CH1N	EVENTOUT
	PB8	SDMMC1_CKIN	CAN1_RX	DCMI_D6/PSSI_D6	LCD_DE	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	SDMMC1_CDIR	CAN1_TX	DCMI_D7/PSSI_D7	-	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_RX	TSC_SYNC	OCTOSPIM_P1_CLK	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	OCTOSPIM_P1_NCS	LCD_VSYNC	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RTS_DE	TSC_G1_IO1	OCTOSPIM_P1_NCLK	-	SDMMC2_CK	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CTS	TSC_G1_IO2	OCTOSPIM_P1_IO1	-	-	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	OCTOSPIM_P1_IO6	SDMMC2_D0	-	SAI2_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	OCTOSPIM_P1_IO7	SDMMC2_D1	-	SAI2_SD_A	TIM15_CH2	EVENTOUT

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Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/CAN2/SDMMC1/2	CAN1/TSC/LCD	CAN2/OTG_FS/DCMI/OCTOSPIM_P1/2/QUADSPI	SDMMC2/LCD/DSI/LCD	SDMMC1/2/COMP1/2/TIM1/8/FMC/SWPMI1	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENOUT
Port C	PC0	LPUART1_RX	-	-	LCD_DE	SDMMC1_CMD	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	OCTOSPIM_P1_IO4	-	-	SAI1_SD_A	-	EVENTOUT
	PC2	-	-	OCTOSPIM_P1_IO5	LCD_HSYNC	-	-	-	EVENTOUT
	PC3	-	-	OCTOSPIM_P1_IO6	-	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	OCTOSPIM_P1_IO7	-	-	-	-	EVENTOUT
	PC5	-	-	-	LCD_CLK	-	-	-	EVENTOUT
	PC6	SDMMC1_D0DIR	TSC_G4_IO1	DCMI_D0/PSSI_D0	LCD_G7	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	SDMMC1_D123DIR	TSC_G4_IO2	DCMI_D1/PSSI_D1	LCD_B6	SDMMC1_D7	SAI2_MCLK_B	-	EVENTOUT
	PC8	-	TSC_G4_IO3	DCMI_D2/PSSI_D2	-	SDMMC1_D0	-	-	EVENTOUT
	PC9	-	TSC_G4_IO4	OTG_FS_NOE	-	SDMMC1_D1	SAI2_EXTCLK	TIM8_BKIN2	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	DCMI_D8/PSSI_D8	-	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	DCMI_D4/PSSI_D4	-	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	DCMI_D9/PSSI_D9	LCD_R6	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

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Table 17. Alternate function AF8 to AF15[(1)] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/CAN2/SDMMC1/2	CAN1/TSC/LCD	CAN2/OTG_FS/DCMI/OCTOSPIM_P1/2/QUADSPI	SDMMC2/LCD/DSI/LCD	SDMMC1/2/COMP1/2/TIM1/8/FMC/SWPMI1	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENOUT
Port D	PD0	-	CAN1_RX	-	LCD_B4	FMC_D2	-	-	EVENTOUT
	PD1	-	CAN1_TX	-	LCD_B5	FMC_D3	-	-	EVENTOUT
	PD2	UART5_RX	TSC_SYNC	DCMI_D11/PSSI_D11	-	SDMMC1_CMD	-	-	EVENTOUT
	PD3	-	-	OCTOSPIM_P2_NCS	LCD_CLK	FMC_CLK	-	-	EVENTOUT
	PD4	SDMMC2_CKIN	-	OCTOSPIM_P1_IO4	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	OCTOSPIM_P1_IO5	-	FMC_NWE	-	-	EVENTOUT
	PD6	SDMMC2_CK	-	OCTOSPIM_P1_IO6	LCD_DE	FMC_NWAIT	SAI1_SD_A	-	EVENTOUT
	PD7	SDMMC2_CMD	-	OCTOSPIM_P1_IO7	-	FMC_NCE/FMC_NE1	-	-	EVENTOUT
	PD8	-	-	DCMI_HSYNC/PSSI_DE	LCD_R3	FMC_D13	-	-	EVENTOUT
	PD9	-	-	DCMI_PIXCLK/PSSI_PDCK	LCD_R4	FMC_D14	SAI2_MCLK_A	-	EVENTOUT
	PD10	-	TSC_G6_IO1	-	LCD_R5	FMC_D15	SAI2_SCK_A	-	EVENTOUT
	PD11	-	TSC_G6_IO2	-	LCD_R6	FMC_A16	SAI2_SD_A	LPTIM2_ETR	EVENTOUT
	PD12	-	TSC_G6_IO3	-	LCD_R7	FMC_A17	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PD13	-	TSC_G6_IO4	-	-	FMC_A18	-	LPTIM2_OUT	EVENTOUT
	PD14	-	-	-	LCD_B2	FMC_D0	-	-	EVENTOUT
	PD15	-	-	-	LCD_B3	FMC_D1	-	-	EVENTOUT

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Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/CAN2/SDMMC1/2	CAN1/TSC/LCD	CAN2/OTG_FS/DCMI/OCTOSPIM_P1/2/QUADSPI	SDMMC2/LCD/DSI/LCD	SDMMC1/2/COMP1/2/TIM1/8/FMC/SWPMI1	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENOUT
Port E	PE0	-	-	DCMI_D2/PSSI_D2	LCD_HSYNC	FMC_NBL0	-	TIM16_CH1	EVENTOUT
	PE1	-	-	DCMI_D3/PSSI_D3	LCD_VSYNC	FMC_NBL1	-	TIM17_CH1	EVENTOUT
	PE2	-	TSC_G7_IO1	-	LCD_R7	FMC_A23	SAI1_MCLK_A	-	EVENTOUT
	PE3	-	TSC_G7_IO2	-	LCD_R6	FMC_A19	SAI1_SD_B	-	EVENTOUT
	PE4	-	TSC_G7_IO3	DCMI_D4/PSSI_D4	LCD_B7	FMC_A20	SAI1_FS_A	-	EVENTOUT
	PE5	-	TSC_G7_IO4	DCMI_D6/PSSI_D6	LCD_G7	FMC_A21	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	DCMI_D7/PSSI_D7	LCD_G6	FMC_A22	SAI1_SD_A	-	EVENTOUT
	PE7	-	-	-	LCD_B6	FMC_D4	SAI1_SD_B	-	EVENTOUT
	PE8	-	-	-	LCD_B7	FMC_D5	SAI1_SCK_B	-	EVENTOUT
	PE9	-	-	OCTOSPIM_P1_NCLK	LCD_G2	FMC_D6	SAI1_FS_B	-	EVENTOUT
	PE10	-	TSC_G5_IO1	OCTOSPIM_P1_CLK	LCD_G3	FMC_D7	SAI1_MCLK_B	-	EVENTOUT
	PE11	-	TSC_G5_IO2	OCTOSPIM_P1_NCS	LCD_G4	FMC_D8	-	-	EVENTOUT
	PE12	-	TSC_G5_IO3	OCTOSPIM_P1_IO0	LCD_G5	FMC_D9	-	-	EVENTOUT
	PE13	-	TSC_G5_IO4	OCTOSPIM_P1_IO1	LCD_G6	FMC_D10	-	-	EVENTOUT
	PE14	-	-	OCTOSPIM_P1_IO2	LCD_G7	FMC_D11	-	-	EVENTOUT
	PE15	-	-	OCTOSPIM_P1_IO3	LCD_R2	FMC_D12	-	-	EVENTOUT

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Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/CAN2/SDMMC1/2	CAN1/TSC/LCD	CAN2/OTG_FS/DCMI/OCTOSPIM_P1/2/QUADSPI	SDMMC2/LCD/DSI/LCD	SDMMC1/2/COMP1/2/TIM1/8/FMC/SWPMI1	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENOUT
Port F	PF0	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	OCTOSPIM_P1_IO3	-	-	SAI1_SD_B	-	EVENTOUT
	PF7	-	-	OCTOSPIM_P1_IO2	-	-	SAI1_MCLK_B	-	EVENTOUT
	PF8	-	-	OCTOSPIM_P1_IO0	-	-	SAI1_SCK_B	-	EVENTOUT
	PF9	-	-	OCTOSPIM_P1_IO1	-	-	SAI1_FS_B	TIM15_CH1	EVENTOUT
	PF10	-	-	DCMI_D11/PSSI_D11	-	-	SAI1_D3	TIM15_CH2	EVENTOUT
	PF11	-	LCD_DE	DCMI_D12/PSSI_D12	-	-	-	-	EVENTOUT
	PF12	-	-	-	LCD_B0	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	LCD_B1	FMC_A7	-	-	EVENTOUT
	PF14	-	TSC_G8_IO1	-	LCD_G0	FMC_A8	-	-	EVENTOUT
	PF15	-	TSC_G8_IO2	-	LCD_G1	FMC_A9	-	-	EVENTOUT

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Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/CAN2/SDMMC1/2	CAN1/TSC/LCD	CAN2/OTG_FS/DCMI/OCTOSPIM_P1/2/QUADSPI	SDMMC2/LCD/DSI/LCD	SDMMC1/2/COMP1/2/TIM1/8/FMC/SWPMI1	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENOUT
Port G	PG0	-	TSC_G8_IO3	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	TSC_G8_IO4	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	SDMMC2_D4	FMC_A12	SAI2_SCK_B	-	EVENTOUT
	PG3	-	-	-	SDMMC2_D5	FMC_A13	SAI2_FS_B	-	EVENTOUT
	PG4	-	-	-	SDMMC2_D6	FMC_A14	SAI2_MCLK_B	-	EVENTOUT
	PG5	LPUART1_CTS	-	-	SDMMC2_D7	FMC_A15	SAI2_SD_B	-	EVENTOUT
	PG6	LPUART1_RTS_DE	LCD_R1	-	-	-	-	-	EVENTOUT
	PG7	LPUART1_TX	-	-	-	FMC_INT	SAI1_MCLK_A	-	EVENTOUT
	PG8	LPUART1_RX	-	-	-	-	-	-	EVENTOUT
	PG9	-	-	-	SDMMC2_D0	FMC_NCE/FMC_NE2	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PG10	-	-	-	SDMMC2_D1	FMC_NE3	SAI2_FS_A	TIM15_CH1	EVENTOUT
	PG11	-	-	-	SDMMC2_D2	-	SAI2_MCLK_A	TIM15_CH2	EVENTOUT
	PG12	-	-	-	SDMMC2_D3	FMC_NE4	SAI2_SD_A	-	EVENTOUT
	PG13	-	-	-	LCD_R0	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	LCD_R1	FMC_A25	-	-	EVENTOUT
	PG15	-	-	DCMI_D13/PSSI_D13	-	-	-	-	EVENTOUT

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Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/CAN2/SDMMC1/2	CAN1/TSC/LCD	CAN2/OTG_FS/DCMI/OCTOSPIM_P1/2/QUADSPI	SDMMC2/LCD/DSI/LCD	SDMMC1/2/COMP1/2/TIM1/8/FMC/SWPMI1	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	EVENTOUT
	PH4	-	-	PSSI_D14	-	-	-	-	EVENTOUT
	PH5	-	-	DCMI_PIXCLK/PSSI_PDCK	-	-	-	-	EVENTOUT
	PH6	-	-	DCMI_D8/PSSI_D8	-	-	-	-	EVENTOUT
	PH7	-	-	DCMI_D9/PSSI_D9	-	-	-	-	EVENTOUT
	PH8	-	-	DCMI_HSYNC/PSSI_DE	-	-	-	-	EVENTOUT
	PH9	-	-	DCMI_D0/PSSI_D0	-	-	-	-	EVENTOUT
	PH10	-	-	DCMI_D1/PSSI_D1	-	-	-	-	EVENTOUT
	PH11	-	-	DCMI_D2/PSSI_D2	-	-	-	-	EVENTOUT
	PH12	-	-	DCMI_D3/PSSI_D3	-	-	-	-	EVENTOUT
	PH13	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PH14	-	-	DCMI_D4/PSSI_D4	-	-	-	-	EVENTOUT
	PH15	-	-	DCMI_D11/PSSI_D11	-	-	-	-	EVENTOUT

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Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/CAN2/SDMMC1/2	CAN1/TSC/LCD	CAN2/OTG_FS/DCMI/OCTOSPIM_P1/2/QUADSPI	SDMMC2/LCD/DSI/LCD	SDMMC1/2/COMP1/2/TIM1/8/FMC/SWPMI1	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENOUT
Port I	PI0	-	-	DCMI_D13/PSSI_D13	-	-	-	-	EVENTOUT
	PI1	-	-	DCMI_D8/PSSI_D8	-	-	-	-	EVENTOUT
	PI2	-	-	DCMI_D9/PSSI_D9	-	-	-	-	EVENTOUT
	PI3	-	-	DCMI_D10/PSSI_D10	-	-	-	-	EVENTOUT
	PI4	-	-	DCMI_D5/PSSI_D5	-	-	-	-	EVENTOUT
	PI5	-	-	DCMI_VSYNC/PSSI_RDY	-	-	-	-	EVENTOUT
	PI6	-	-	DCMI_D6/PSSI_D6	-	-	-	-	EVENTOUT
	PI7	-	-	DCMI_D7/PSSI_D7	-	-	-	-	EVENTOUT
	PI8	-	-	DCMI_D12/PSSI_D12	-	-	-	-	EVENTOUT
	PI9	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-	PSSI_D14	-	-	-	-	EVENTOUT
	PI11	-	-	PSSI_D15	-	-	-	-	EVENTOUT

1. Refer to previous table for AF0 to AF7.

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5 Memory mapping

For memory map and peripheral register boundary addresses refer to the corresponding section of reference manual RM0432.

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6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 24*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 25*.

Figure 24. Pin loading conditions

Figure 25. Pin input voltage

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6.1.6 Power supply scheme

Figure 26. Power supply scheme

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

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6.1.7 Current consumption measurement

The I_{DD_ALL} parameters given in *Table 25* to *Table 39* represent the total MCU consumption including the current supplying V_{DD}, V_{DDIO2}, V_{DDA}, V_{DDUSB} and V_{BAT}.

Figure 27. Current consumption measurement

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18: Voltage characteristics*, *Table 19: Current characteristics* and *Table 20: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 18. Voltage characteristics(1)

Symbol	Ratings		Min	Max	Unit
$V_{DDX} - V_{SS}$	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{BAT})		-0.3	4.0	V
$V_{DD12} - V_{SS}$	External SMPS supply voltage	Range 1	-0.3	1.4	V
		Range 2	-0.3		

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Table 18. Voltage characteristics(1) (continued)

Symbol	Ratings	Min	Max	Unit
V_{IN}(2)	Input voltage on FT_xxx pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}) + 4.0(3)(4)	
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	
	Input voltage on BOOT0 pin	V_{SS}	9.0	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins(5)	-	50	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 19: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 19. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1) (2)	200	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1) (2)	200	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(3)	100	
	Total output current sourced by sum of all I/Os and control pins(3)	100	
$I_{INJ(PIN)}$(4)	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0(5)	
	Injected current on PA4, PA5	-5/0	
$\Sigma\|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)(6)	25	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. Valid also for V_{DD12} on SMPS package.
3. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
4. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

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5. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 18: Voltage characteristics* for the minimum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	120	
f_{PCLK2}	Internal APB2 clock frequency	-	0	120	
V_{DD}	Standard operating voltage	-	1.71(1)	3.6	V
V_{DD12}	Standard operating voltage	Up to 120 MHz	1.14	1.32	V
		Up to 80 MHz	1.08		
		Up to 26 MHz	1.05(2)		
V_{DDIO2}	PG[15:2] I/Os supply voltage	At least one I/O in PG[15:2] used	1.08	3.6	V
		PG[15:2] not used	0	3.6	
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	
V_{DDUSB}	USB supply voltage	USB used	3.0	3.6	V
		USB not used	0	3.6	

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Table 21. General operating conditions (continued)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{IN}	I/O input voltage	TT_xx I/O		-0.3	V_{DDIOx}+0.3	V
		BOOT0		0	9	
		All I/O except BOOT0 and TT_xx		-0.3	MIN(MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD})+3.6 V, 5.5 V)(3)(4)	
P_D	Power dissipation at T_A = 85 °C for suffix 6(5)	LQFP144	-	-	TBD	mW
		LQFP100	-	-	TBD	
		UFBGA169	-	-	TBD	
		UFBGA132	-	-	TBD	
		WLCSP100	-	-	TBD	
		LQFP48	-	-	TBD	
		LQFP64	-	-	TBD	
		UFQFPN48	-	-	TBD	
P_D	Power dissipation at T_A = 125 °C for suffix 3(5)	LQFP144	-	-	TBD	mW
		LQFP100	-	-	TBD	
		UFBGA169	-	-	TBD	
		UFBGA132	-	-	TBD	
		WLCSP100	-	-	TBD	
		LQFP48	-	-	TBD	
		LGFP64	-	-	TBD	
		UFQFPN48	-	-	TBD	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation		–40	85	°C
		Low-power dissipation(6)		–40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation		–40	125	
		Low-power dissipation(6)		–40	130	
T_J	Junction temperature range	Suffix 6 version		–40	105	°C
		Suffix 3 version		–40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. For Flash erase and program operation, V_{DD12} min must be 1.08 V.
3. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB})+3.6 V and 5.5V.
4. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
5. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).
6. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).

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6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 22* are derived from tests performed under the ambient temperature condition summarized in *Table 21*.

Table 22. Operating conditions at power-up / power-down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	TBD	TBD	µs/V
	V_{DD} fall time rate		TBD	TBD	
t_{VDDA}	V_{DDA} rise time rate	-	TBD	TBD	µs/V
	V_{DDA} fall time rate		TBD	TBD	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	TBD	TBD	µs/V
	V_{DDUSB} fall time rate		TBD	TBD	
t_{VDDIO2}	V_{DDIO2} rise time rate	-	TBD	TBD	µs/V
	V_{DDIO2} fall time rate		TBD	TBD	

1. At power-up, the V_{DD12} voltage should not be forced externally.

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature conditions summarized in *Table 21: General operating conditions*.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	TBD	TBD	TBD	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD1}	PVD threshold 1	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	

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Table 23. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVD2}	PVD threshold 2	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD3}	PVD threshold 3	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD4}	PVD threshold 4	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD5}	PVD threshold 5	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVD6}	PVD threshold 6	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	TBD	TBD	TBD	mV
		Hysteresis in other mode	TBD	TBD	TBD	
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	TBD	TBD	TBD	mV
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	TBD	TBD	TBD	µA
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	TBD	TBD	TBD	V
		Falling edge	TBD	TBD	TBD	
V_{hyst_PVM3}	PVM3 hysteresis	-	TBD	TBD	TBD	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	TBD	TBD	TBD	mV
I_{DD} (PVM1/PVM2) (2)	PVM1 and PVM2 consumption from V_{DD}	-	TBD	TBD	TBD	µA
I_{DD} (PVM3/PVM4) (2)	PVM3 and PVM4 consumption from V_{DD}	-	TBD	TBD	TBD	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

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6.3.4 Embedded voltage reference

The parameters given in *Table 24* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 24. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	TBD	TBD	TBD	µs
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	TBD	TBD	TBD	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	TBD	TBD	TBD	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	TBD	TBD	TBD	mV
T_{Coeff}	Average temperature coefficient	–40°C < T_A < +130°C	TBD	TBD	TBD	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	TBD	TBD	TBD	ppm
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	TBD	TBD	TBD	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	TBD	TBD	TBD	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		TBD	TBD	TBD	
V_{REFINT_DIV3}	3/4 reference voltage		TBD	TBD	TBD	

1. The shortest sampling time can be determined in the application by multiple iterations.

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Figure 28. V_{REFINT} versus temperature

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6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code

The current consumption is measured as described in .

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0432 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- The voltage scaling Range 1 is adjusted to f_{HCLK} frequency as follows:
  - Voltage Range 1 Boost mode for 80 MHz < f_{HCLK} <= 120 MHz
  - Voltage Range 1 Normal mode for 26 MHz < f_{HCLK} <= 80 MHz

The parameters given in *Table 25* to *Table 39* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

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Table 25. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost Mode	120 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Normal Mode	80 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				24 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable		2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				400 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS

Symbol	Parameter	Conditions[1]			TYP					Unit
		-	VDD12	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	120 MHz	TBD	TBD	TBD	TBD	TBD	mA
			VDD12=1.10V	80 MHz	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	
				26 MHz	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

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Table 27. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost Mode	120 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Normal Mode	80 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				24 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable		2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				400 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 28. Consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS

Symbol	Parameter	Conditions[1]			TYP					Unit
		-	VDD12	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	120 MHz	TBD	TBD	TBD	TBD	TBD	mA
			VDD12=1.10V	80 MHz	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	
				26 MHz	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

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Table 29. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost Mode	120 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Normal Mode	80 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				24 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable		2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				400 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 30. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable and power supplied by external SMPS

Symbol	Parameter	Conditions[1]			TYP					Unit
		-	VDD12	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	120 MHz	TBD	TBD	TBD	TBD	TBD	mA
			VDD12=1.10V	80 MHz	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	
				26 MHz	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

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Table 31. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost Mode	120 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Normal Mode	80 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				24 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				400 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 32. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable and power supplied by external SMPS

Symbol	Parameter	Conditions[1]			TYP					Unit
		-	VDD12	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	120 MHz	TBD	TBD	TBD	TBD	TBD	mA
			VDD12=1.10V	80 MHz	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	
				26 MHz	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

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Table 33. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost Mode	120 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Normal Mode	80 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				24 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD} (LPRun)	Supply current in Low-power run mode	f_{HCLK} = f_{MSI} all peripherals disable FLASH in power-down		2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				400 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 34. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1 and power supplied by external SMPS

Symbol	Parameter	Conditions[1]			TYP					Unit
		-	VDD12	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	120 MHz	TBD	TBD	TBD	TBD	TBD	mA
			VDD12=1.10V	80 MHz	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	
				26 MHz	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

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Table 35. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26MHz	Reduced code(1)	TBD	TBD	mA	TBD	TBD	µA/MHz
				Coremark	TBD	TBD		TBD	TBD	
				Dhrystone2.1	TBD	TBD		TBD	TBD	
				Fibonacci	TBD	TBD		TBD	TBD	
				While(1)	TBD	TBD		TBD	TBD	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	TBD	TBD	mA	TBD	TBD	µA/MHz
				Coremark	TBD	TBD		TBD	TBD	
				Dhrystone2.1	TBD	TBD		TBD	TBD	
				Fibonacci	TBD	TBD		TBD	TBD	
				While(1)	TBD	TBD		TBD	TBD	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	TBD	TBD	mA	TBD	TBD	µA/MHz
				Coremark	TBD	TBD		TBD	TBD	
				Dhrystone2.1	TBD	TBD		TBD	TBD	
				Fibonacci	TBD	TBD		TBD	TBD	
				While(1)	TBD	TBD		TBD	TBD	

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Table 35. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) (continued)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all pripherals disable		Reduced code(1)	TBD	TBD	µA	TBD	TBD	µA/MHz
				Coremark	TBD	TBD		TBD	TBD	
				Dhrystone2.1	TBD	TBD		TBD	TBD	
				Fibonacci	TBD	TBD		TBD	TBD	
				While(1)	TBD	TBD		TBD	TBD	

1. Reduced code used for characterization results provided in *Table 25*, *Table 29*, *Table 33*.

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Table 36. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS

Symbol	Parameter	Conditions[1]				TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	VDD12	f_{HCLK}	Code	25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK}=f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.05V	f_{HCLK}= 26 MHz	Reduced code	TBD	TBD	mA	TBD	TBD	µA/MHz
					Coremark	TBD	TBD		TBD	TBD	
					Dhrystone2.1	TBD	TBD		TBD	TBD	
					Fibonacci	TBD	TBD		TBD	TBD	
					While(1)	TBD	TBD		TBD	TBD	
			VDD12=1.10V	f_{HCLK}= 26 MHz	Reduced code	TBD	TBD	mA	TBD	TBD	µA/MHz
					Coremark	TBD	TBD		TBD	TBD	
					Dhrystone2.1	TBD	TBD		TBD	TBD	
					Fibonacci	TBD	TBD		TBD	TBD	
					While(1)	TBD	TBD		TBD	TBD	
				f_{HCLK}= 80 MHz	Reduced code	TBD	TBD	mA	TBD	TBD	µA/MHz
					Coremark	TBD	TBD		TBD	TBD	
					Dhrystone2.1	TBD	TBD		TBD	TBD	
					Fibonacci	TBD	TBD		TBD	TBD	
					While(1)	TBD	TBD		TBD	TBD	

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Table 36. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) and power supplied by external SMPS (continued)

Symbol	Parameter	Conditions(1)				TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	VDD12	f_{HCLK}	Code	25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK}=f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	f_{HCLK}= 120 MHz	Reduced code	TBD	TBD	mA	TBD	TBD	µA/MHz
					Coremark	TBD	TBD		TBD	TBD	
					Dhrystone2.1	TBD	TBD		TBD	TBD	
					Fibonacci	TBD	TBD		TBD	TBD	
					While(1)	TBD	TBD		TBD	TBD	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

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Table 37. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 MHz	Reduced code(1)	TBD	TBD	mA	TBD	TBD	µA/MHz
				Coremark	TBD	TBD		TBD	TBD	
				Dhrystone2.1	TBD	TBD		TBD	TBD	
				Fibonacci	TBD	TBD		TBD	TBD	
				While(1)	TBD	TBD		TBD	TBD	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	TBD	TBD	mA	TBD	TBD	µA/MHz
				Coremark	TBD	TBD		TBD	TBD	
				Dhrystone2.1	TBD	TBD		TBD	TBD	
				Fibonacci	TBD	TBD		TBD	TBD	
				While(1)	TBD	TBD		TBD	TBD	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	TBD	TBD	mA	TBD	TBD	µA/MHz
				Coremark	TBD	TBD		TBD	TBD	
				Dhrystone2.1	TBD	TBD		TBD	TBD	
				Fibonacci	TBD	TBD		TBD	TBD	
				While(1)	TBD	TBD		TBD	TBD	
I_{DD} (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all pripherals disable		Reduced code(1)	TBD	TBD	µA	TBD	TBD	µA/MHz
				Coremark	TBD	TBD		TBD	TBD	
				Dhrystone2.1	TBD	TBD		TBD	TBD	
				Fibonacci	TBD	TBD		TBD	TBD	
				While(1)	TBD	TBD		TBD	TBD	

1. Reduced code used for characterization results provided in *Table 25*, *Table 29*, *Table 33*.

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Table 38. Typical current consumption in Run and Low-power run modes with different codes running from Flash, ART disable and power supplied by external SMPS

Symbol	Parameter	Conditions[1]				TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	VDD12	f_{HCLK}	Code	25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK}=f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12= 1.05V	f_{HCLK}= 26 MHz	Reduced code	TBD	TBD	mA	TBD	TBD	µA/MHz
					Coremark	TBD	TBD		TBD	TBD	
					Dhrystone2.1	TBD	TBD		TBD	TBD	
					Fibonacci	TBD	TBD		TBD	TBD	
					While(1)	TBD	TBD		TBD	TBD	
			VDD12= 1.10V	f_{HCLK}= 26 MHz	Reduced code	TBD	TBD	mA	TBD	TBD	µA/MHz
					Coremark	TBD	TBD		TBD	TBD	
					Dhrystone2.1	TBD	TBD		TBD	TBD	
					Fibonacci	TBD	TBD		TBD	TBD	
					While(1)	TBD	TBD		TBD	TBD	
				f_{HCLK}= 80 MHz	Reduced code	TBD	TBD	mA	TBD	TBD	µA/MHz
					Coremark	TBD	TBD		TBD	TBD	
					Dhrystone2.1	TBD	TBD		TBD	TBD	
					Fibonacci	TBD	TBD		TBD	TBD	
					While(1)	TBD	TBD		TBD	TBD	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK}=f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12= 1.20V	f_{HCLK}= 120 MHz	Reduced code	TBD	TBD	mA	TBD	TBD	µA/MHz
					Coremark	TBD	TBD		TBD	TBD	
					Dhrystone 2.1	TBD	TBD		TBD	TBD	
					Fibonacci	TBD	TBD		TBD	TBD	
					While(1)	TBD	TBD		TBD	TBD	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, VDD12 = 1.10 V.

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Table 39. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions		Code	TYP	Unit	TYP	Unit
		-	Voltage scaling		25°C		25°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK}=f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 MHz	Reduced code(1)	TBD	mA	TBD	µA/MHz
				Coremark	TBD		TBD	
				Dhrystone2.1	TBD		TBD	
				Fibonacci	TBD		TBD	
				While(1)	TBD		TBD	
			Range 1 Normal Mode f_{HCLK}= 80 MHz	Reduced code(1)	TBD	mA	TBD	µA/MHz
				Coremark	TBD		TBD	
				Dhrystone2.1	TBD		TBD	
				Fibonacci	TBD		TBD	
				While(1)	TBD		TBD	
			Range 1 Boost Mode f_{HCLK}= 120 MHz	Reduced code(1)	TBD	mA	TBD	µA/MHz
				Coremark	TBD		TBD	
				Dhrystone2.1	TBD		TBD	
				Fibonacci	TBD		TBD	
				While(1)	TBD		TBD	
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all pripherals disable		Reduced code(1)	TBD	µA	TBD	µA/MHz
				Coremark	TBD		TBD	
				Dhrystone2.1	TBD		TBD	
				Fibonacci	TBD		TBD	
				While(1)	TBD		TBD	

1. Reduced code used for characterization results provided in *Table 25*, *Table 29*, *Table 33*.

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Table 40. Typical consumption in Run and Low-power run modes, with different codes running from SRAM1 and power supplied by external SMPS

Symbol	Parameter	Conditions[1]				TYP	Unit	TYP	Unit
		-	VDD12	f_{HCLK}	Code	25°C		25°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK}=f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.05 V	f_{HCLK}= 26 MHz	Reduced code	TBD	mA	TBD	µA/MHz
					Coremark	TBD		TBD	
					Dhrystone2.1	TBD		TBD	
					Fibonacci	TBD		TBD	
					While(1)	TBD		TBD	
			VDD12=1.10V	f_{HCLK}= 26 MHz	Reduced code	TBD	mA	TBD	µA/MHz
					Coremark	TBD		TBD	
					Dhrystone2.1	TBD		TBD	
					Fibonacci	TBD		TBD	
					While(1)	TBD		TBD	
				f_{HCLK}= 80 MHz	Reduced code	TBD	mA	TBD	µA/MHz
					Coremark	TBD		TBD	
					Dhrystone2.1	TBD		TBD	
					Fibonacci	TBD		TBD	
					While(1)	TBD		TBD	
			VDD12=1.20V	f_{HCLK}= 120 MHz	Reduced code	TBD	mA	TBD	µA/MHz
					Coremark	TBD		TBD	
					Dhrystone2.1	TBD		TBD	
					Fibonacci	TBD		TBD	
					While(1)	TBD		TBD	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

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Table 41. Current consumption in Sleep and Low-power sleep mode, Flash ON

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	-
I_{DD} (Sleep)	Supply current in Sleep mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Boost Mode	120 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			Range 1 Normal Mode	80 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				24 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD} (LPSleep)	Supply current in Low-power sleep mode	f_{HCLK} = f_{MSI} all peripherals disable		2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				400 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 42. Current consumption in Sleep and Low-power sleep modes, Flash ON and power supplied by external SMPS

Symbol	Parameter	Conditions[1]			TYP					Unit
		-	VDD12	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Sleep)	Supply current in Sleep mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	120 MHz	TBD	TBD	TBD	TBD	TBD	mA
			VDD12=1.10V	80 MHz	TBD	TBD	TBD	TBD	TBD	
				72 MHz	TBD	TBD	TBD	TBD	TBD	
				64 MHz	TBD	TBD	TBD	TBD	TBD	
				48 MHz	TBD	TBD	TBD	TBD	TBD	
				32 MHz	TBD	TBD	TBD	TBD	TBD	
				26 MHz	TBD	TBD	TBD	TBD	TBD	
				16 MHz	TBD	TBD	TBD	TBD	TBD	
				8 MHz	TBD	TBD	TBD	TBD	TBD	
				4 MHz	TBD	TBD	TBD	TBD	TBD	
				2 MHz	TBD	TBD	TBD	TBD	TBD	
				1 MHz	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

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Table 43. Current consumption in Low-power sleep mode, Flash in power-down

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (LPSleep)	Supply current in Low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				1 MHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				400 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
				100 KHz	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 44. Current consumption in Stop 2 mode, SRAM3 disabled

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD}(Stop 2 with RTC)	Supply current in STOP 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE quartz in low drive mode	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD}(wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(2)	3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(2)	3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(2)	3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.
2. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 52: Low-power mode wakeup timings*.

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Table 45. Current consumption in Stop 2 mode, SRAM3 enabled

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	VDD	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(Stop 2)	Supply current in Stop 2 mode, RTC disabled	-	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
IDD(Stop 2 with RTC)	Supply current in STOP 2 mode, RTC enabled	RTC clocked by LSI	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE quartz in low drive mode	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
IDD(wakeup from Stop 2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(2)	3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(2)	3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(2)	3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.
2. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 52: Low-power mode wakeup timings*.

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Table 46. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	VDD	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
IDD (Stop 1 with RTC)	Supply current in STOP 1 mode, RTC enabled	RTC clocked by LSI	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE quartz(2) in low drive mode	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
IDD (wakeup from Stop 1)	Supply current during wakeup from Stop 1 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1(3)	3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2(3)	3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		Wakeup clock is HSI = 16 MHz, voltage Range 1(3)	3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 52: Low-power mode wakeup timings*

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Table 47. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Stop 0)	Supply current in Stop 0 mode, RTC disabled	-	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 48. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	No independent watchdog	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		With independent watchdog	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

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Table 48. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSI, with independent watchdog	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE quartz(2) in low drive mode	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD} (SRAM2)(3)	Supply current to be added in Standby mode when the full 64 Kbytes of SRAM2 are retained	-	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

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Table 48. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (SRAM2)(3)	Supply current to be added in Standby mode when 4 Kbytes of SRAM2 are retained	-	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is MSI = 4 MHz(4)	3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. The supply current in Standby with SRAM2 mode is: I_{DD_ALL}(Standby) + I_{DD_ALL}(SRAM2). The supply current in Standby with RTC with SRAM2 mode is: I_{DD_ALL}(Standby + RTC) + I_{DD_ALL}(SRAM2).
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 52: Low-power mode wakeup timings*.

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Table 49. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC clocked by LSE quartz(2) in low drive mode	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{DD}(wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz(3)	3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 52: Low-power mode wakeup timings*.

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Table 50. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{BAT}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(VBAT)	Backup domain supply current	RTC disabled	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	nA
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
		RTC enabled and clocked by LSE quartz(2)	1.8 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
			3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

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I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 69: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

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On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 52*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 18: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 52*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 51. STM32L4P5xx peripheral current consumption

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
AHB	Bus matrix	TBD	TBD	TBD	TBD	µA/MHz
	ADC independent clock domain	TBD	TBD	TBD	TBD	
	ADC AHB clock domain	TBD	TBD	TBD	TBD	
	CRC	TBD	TBD	TBD	TBD	
	DCMI	TBD	TBD	TBD	TBD	
	PSSI	TBD	TBD	TBD	TBD	
	DMA1	TBD	TBD	TBD	TBD	
	DMA2	TBD	TBD	TBD	TBD	
	DMA2D	TBD	TBD	TBD	TBD	
	DMAMUX	TBD	TBD	TBD	TBD	
	FLASH	TBD	TBD	TBD	TBD	
	FMC	TBD	TBD	TBD	TBD	
	GPIOA	TBD	TBD	TBD	TBD	
	GPIOB	TBD	TBD	TBD	TBD	
	GPIOC	TBD	TBD	TBD	TBD	
	GPIOD	TBD	TBD	TBD	TBD	
	GPIOE	TBD	TBD	TBD	TBD	
	GPIOF	TBD	TBD	TBD	TBD	
	GPIOG	TBD	TBD	TBD	TBD	

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Table 51. STM32L4P5xx peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
AHB (Cont.)	GPIOH	TBD	TBD	TBD	TBD	µA/MHz
	GPIOI	TBD	TBD	TBD	TBD	
	HASH1	TBD	TBD	TBD	TBD	
	OTG_FS independent clock domain	TBD	TBD	TBD	TBD	
	OTG_FS AHB clock domain	TBD	TBD	TBD	TBD	
	OSPIM independent clock domain	TBD	TBD	TBD	TBD	
	OSPIM AHB clock domain	TBD	TBD	TBD	TBD	
	OSPI1 independent clock domain	TBD	TBD	TBD	TBD	
	OSPI1 AHB clock domain	TBD	TBD	TBD	TBD	
	OSPI2 independent clock domain	TBD	TBD	TBD	TBD	
	OSPI2 AHB clock domain	TBD	TBD	TBD	TBD	
	RNG independent clock domain	TBD	TBD	TBD	TBD	
	RNG AHB clock domain	TBD	TBD	TBD	TBD	
	SDMMC1 independent clock domain	TBD	TBD	TBD	TBD	
	SDMMC1 AHB clock domain	TBD	TBD	TBD	TBD	
	SDMMC2 independent clock domain	TBD	TBD	TBD	TBD	
	SDMMC2 AHB clock domain	TBD	TBD	TBD	TBD	
	SRAM1	TBD	TBD	TBD	TBD	
	SRAM2	TBD	TBD	TBD	TBD	
	SRAM3	TBD	TBD	TBD	TBD	
	TSC	TBD	TBD	TBD	TBD	
	All AHB Peripherals	TBD	TBD	TBD	TBD	

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Table 51. STM32L4P5xx peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB1	AHB to APB1 bridge	TBD	TBD	TBD	TBD	µA/MHz
	CAN1	TBD	TBD	TBD	TBD	
	CRS	TBD	TBD	TBD	TBD	
	DAC1	TBD	TBD	TBD	TBD	
	I2C1 independent clock domain	TBD	TBD	TBD	TBD	
	I2C1 APB clock domain	TBD	TBD	TBD	TBD	
	I2C2 independent clock domain	TBD	TBD	TBD	TBD	
	I2C2 APB clock domain	TBD	TBD	TBD	TBD	
	I2C3 independent clock domain	TBD	TBD	TBD	TBD	
	I2C3 APB clock domain	TBD	TBD	TBD	TBD	
	I2C4 independent clock domain	TBD	TBD	TBD	TBD	
	I2C4 APB clock domain	TBD	TBD	TBD	TBD	
	LPUART1 independent clock domain	TBD	TBD	TBD	TBD	
	LPUART1 APB clock domain	TBD	TBD	TBD	TBD	
	LPTIM1 independent clock domain	TBD	TBD	TBD	TBD	
	LPTIM1 APB clock domain	TBD	TBD	TBD	TBD	
	LPTIM2 independent clock domain	TBD	TBD	TBD	TBD	
	LPTIM2 APB clock domain	TBD	TBD	TBD	TBD	
	OPAMP	TBD	TBD	TBD	TBD	
	PWR	TBD	TBD	TBD	TBD	
	RTCAPB	TBD	TBD	TBD	TBD	
	SPI2	TBD	TBD	TBD	TBD	

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Table 51. STM32L4P5xx peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB1 (Cont.)	SPI3	TBD	TBD	TBD	TBD	µA/MHz
	TIM2	TBD	TBD	TBD	TBD	
	TIM3	TBD	TBD	TBD	TBD	
	TIM4	TBD	TBD	TBD	TBD	
	TIM5	TBD	TBD	TBD	TBD	
	TIM6	TBD	TBD	TBD	TBD	
	TIM7	TBD	TBD	TBD	TBD	
	USART2 independent clock domain	TBD	TBD	TBD	TBD	
	USART2 APB clock domain	TBD	TBD	TBD	TBD	
	USART3 independent clock domain	TBD	TBD	TBD	TBD	
	USART3 APB clock domain	TBD	TBD	TBD	TBD	
	UART4 independent clock domain	TBD	TBD	TBD	TBD	
	UART4 APB clock domain	TBD	TBD	TBD	TBD	
	UART5 independent clock domain	TBD	TBD	TBD	TBD	
	UART5 APB clock domain	TBD	TBD	TBD	TBD	
	WWDG	TBD	TBD	TBD	TBD	
	All APB1 on	TBD	TBD	TBD	TBD	

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Table 51. STM32L4P5xx peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB2	AHB to APB2 bridge	TBD	TBD	TBD	TBD	µA/MHz
	DFSDM	TBD	TBD	TBD	TBD	
	FW	TBD	TBD	TBD	TBD	
	LTDC independent clock domain	TBD	TBD	TBD	TBD	
	LTDC APB clock domain	TBD	TBD	TBD	TBD	
	SAI1 independent clock domain	TBD	TBD	TBD	TBD	
	SAI1 APB clock domain	TBD	TBD	TBD	TBD	
	SAI2 independent clock domain	TBD	TBD	TBD	TBD	
	SAI2 APB clock domain	TBD	TBD	TBD	TBD	
	SPI1	TBD	TBD	TBD	TBD	
	SYSCFG/VREFBUF/COMP	TBD	TBD	TBD	TBD	
	TIM1	TBD	TBD	TBD	TBD	
	TIM8	TBD	TBD	TBD	TBD	
	TIM15	TBD	TBD	TBD	TBD	
	TIM16	TBD	TBD	TBD	TBD	
	TIM17	TBD	TBD	TBD	TBD	
	USART1 independent clock domain	TBD	TBD	TBD	TBD	
	USART1 APB clock domain	TBD	TBD	TBD	TBD	
	All APB2 on	TBD	TBD	TBD	TBD	
ALL		TBD	TBD	TBD	TBD	

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6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 52* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (wait for event) instruction.

Table 52. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		TBD	TBD	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in Flash with Flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		TBD	TBD	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	TBD	TBD	µs
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
		Range 2	Wakeup clock MSI = 24 MHz	TBD	TBD	
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
			Wakeup clock MSI = 4 MHz	TBD	TBD	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	TBD	TBD	
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
		Range 2	Wakeup clock MSI = 24 MHz	TBD	TBD	
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
			Wakeup clock MSI = 4 MHz	TBD	TBD	

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Table 52. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash	Range 1	Wakeup clock MSI = 48 MHz	TBD	TBD	µs
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
		Range 2	Wakeup clock MSI = 24 MHz	TBD	TBD	
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
			Wakeup clock MSI = 4 MHz	TBD	TBD	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	TBD	TBD	
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
		Range 2	Wakeup clock MSI = 24 MHz	TBD	TBD	
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
			Wakeup clock MSI = 4 MHz	TBD	TBD	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	TBD	TBD	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			TBD	TBD	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in Flash	Range 1	Wakeup clock MSI = 48 MHz	TBD	TBD	µs
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
		Range 2	Wakeup clock MSI = 24 MHz	TBD	TBD	
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
			Wakeup clock MSI = 4 MHz	TBD	TBD	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	TBD	TBD	
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
		Range 2	Wakeup clock MSI = 24 MHz	TBD	TBD	
			Wakeup clock HSI16 = 16 MHz	TBD	TBD	
			Wakeup clock MSI = 4 MHz	TBD	TBD	

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Table 52. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	TBD	TBD	µs
			Wakeup clock MSI = 4 MHz	TBD	TBD	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	TBD	TBD	
			Wakeup clock MSI = 4 MHz	TBD	TBD	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	TBD	TBD	

1. Guaranteed by characterization results.

Table 53. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low- power run mode to Run mode(2)	Code run with MSI 2 MHz	TBD	TBD	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with MSI 24 MHz	TBD	TBD	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

Table 54. Wakeup time using USART/LPUART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI	Stop mode 0	TBD	TBD	µs
		Stop mode 1/2	TBD	TBD	

1. Guaranteed by characterization results.

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6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 29: High-speed external clock source AC timing diagram*.

Table 55. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	TBD	TBD	TBD	MHz
		Voltage scaling Range 2	TBD	TBD	TBD	
V_{HSEH}	OSC_IN input pin high level voltage	-	TBD	TBD	TBD	V
V_{HSEL}	OSC_IN input pin low level voltage	-	TBD	TBD	TBD	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	TBD	TBD	TBD	ns
		Voltage scaling Range 2	TBD	TBD	TBD	

1. Guaranteed by design.

Figure 29. High-speed external clock source AC timing diagram

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Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 30*.

Table 56. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	TBD	TBD	TBD	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	TBD	TBD	TBD	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	TBD	TBD	TBD	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	TBD	TBD	TBD	ns

1. Guaranteed by design.

Figure 30. Low-speed external clock source AC timing diagram

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High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 57*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 57. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	TBD	TBD	TBD	MHz
R_F	Feedback resistor	-	TBD	TBD	TBD	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	TBD	TBD	TBD	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	TBD	TBD	TBD	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	TBD	TBD	TBD	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	TBD	TBD	TBD	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	TBD	TBD	TBD	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	TBD	TBD	TBD	
G_m	Maximum critical crystal transconductance	Startup	TBD	TBD	TBD	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	TBD	TBD	TBD	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 31*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

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Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 31. Typical application with an 8 MHz crystal

1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 58*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

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Table 58. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	TBD	TBD	TBD	nA
		LSEDRV[1:0] = 01 Medium low drive capability	TBD	TBD	TBD	
		LSEDRV[1:0] = 10 Medium high drive capability	TBD	TBD	TBD	
		LSEDRV[1:0] = 11 High drive capability	TBD	TBD	TBD	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	TBD	TBD	TBD	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	TBD	TBD	TBD	
		LSEDRV[1:0] = 10 Medium high drive capability	TBD	TBD	TBD	
		LSEDRV[1:0] = 11 High drive capability	TBD	TBD	TBD	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	TBD	TBD	TBD	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 32. Typical application with a 32.768 kHz crystal

Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

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6.3.8 Internal clock source characteristics

The parameters given in *Table 59* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 59. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	TBD	TBD	TBD	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	TBD	TBD	TBD	%
		Trimming code is a multiple of 64	TBD	TBD	TBD	
DuCy(HSI16)(2)	Duty Cycle	-	TBD	TBD	TBD	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	TBD	TBD	TBD	%
		T_A= -40 to 125 °C	TBD	TBD	TBD	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	TBD	TBD	TBD	%
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	TBD	TBD	TBD	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	TBD	TBD	TBD	µs
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	TBD	TBD	TBD	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

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Figure 33. HSI16 frequency versus temperature

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Multi-speed internal (MSI) RC oscillator

Table 60. MSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD}=3 V and T_A=30 °C	MSI mode	Range 0	TBD	TBD	TBD	kHz
			Range 1	TBD	TBD	TBD	
			Range 2	TBD	TBD	TBD	
			Range 3	TBD	TBD	TBD	
			Range 4	TBD	TBD	TBD	MHz
			Range 5	TBD	TBD	TBD	
			Range 6	TBD	TBD	TBD	
			Range 7	TBD	TBD	TBD	
			Range 8	TBD	TBD	TBD	
			Range 9	TBD	TBD	TBD	
			Range 10	TBD	TBD	TBD	
			Range 11	TBD	TBD	TBD	
		PLL mode XTAL= 32.768 kHz	Range 0	TBD	TBD	TBD	kHz
			Range 1	TBD	TBD	TBD	
			Range 2	TBD	TBD	TBD	
			Range 3	TBD	TBD	TBD	
			Range 4	TBD	TBD	TBD	MHz
			Range 5	TBD	TBD	TBD	
			Range 6	TBD	TBD	TBD	
			Range 7	TBD	TBD	TBD	
			Range 8	TBD	TBD	TBD	
			Range 9	TBD	TBD	TBD	
			Range 10	TBD	TBD	TBD	
			Range 11	TBD	TBD	TBD	
$\Delta_{TEMP}(MSI)$(2)	MSI oscillator frequency drift over temperature	MSI mode	T_A= -0 to 85 °C	TBD	TBD	TBD	%
			T_A= -40 to 125 °C	TBD	TBD	TBD	

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Table 60. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$\Delta_{VDD}(MSI)$(2)	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD}=1.62 V to 3.6 V	TBD	TBD	TBD	%
				V_{DD}=2.4 V to 3.6 V	TBD	TBD	TBD	
			Range 4 to 7	V_{DD}=1.62 V to 3.6 V	TBD	TBD	TBD	
				V_{DD}=2.4 V to 3.6 V	TBD	TBD	TBD	
			Range 8 to 11	V_{DD}=1.62 V to 3.6 V	TBD	TBD	TBD	
				V_{DD}=2.4 V to 3.6 V	TBD	TBD	TBD	
$\Delta F_{SAMPLING}$ (MSI)(2)(4)	Frequency variation in sampling mode(3)	MSI mode	T_A= -40 to 85 °C		TBD	TBD	TBD	%
			T_A= -40 to 125 °C		TBD	TBD	TBD	
CC jitter(MSI)(4)	RMS cycle-to-cycle jitter	PLL mode Range 11		-	TBD	TBD	TBD	ps
P jitter(MSI)(4)	RMS Period jitter	PLL mode Range 11		-	TBD	TBD	TBD	ps
t_{SU}(MSI)(4)	MSI oscillator start-up time	Range 0		-	TBD	TBD	TBD	us
		Range 1		-	TBD	TBD	TBD	
		Range 2		-	TBD	TBD	TBD	
		Range 3		-	TBD	TBD	TBD	
		Range 4 to 7		-	TBD	TBD	TBD	
		Range 8 to 11		-	TBD	TBD	TBD	
t_{STAB}(MSI)(4)	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	TBD	TBD	TBD	ms
			5 % of final frequency	-	TBD	TBD	TBD	
			1 % of final frequency	-	TBD	TBD	TBD	

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Table 60. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$I_{DD}(MSI)^{(4)}$	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	TBD	TBD	TBD	µA
			Range 1	-	TBD	TBD	TBD	
			Range 2	-	TBD	TBD	TBD	
			Range 3	-	TBD	TBD	TBD	
			Range 4	-	TBD	TBD	TBD	
			Range 5	-	TBD	TBD	TBD	
			Range 6	-	TBD	TBD	TBD	
			Range 7	-	TBD	TBD	TBD	
			Range 8	-	TBD	TBD	TBD	
			Range 9	-	TBD	TBD	TBD	
			Range 10	-	TBD	TBD	TBD	
			Range 11	-	TBD	TBD	TBD	

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Guaranteed by design.

Figure 34. Typical current consumption versus MSI frequency

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Low-speed internal (LSI) RC oscillator

Table 61. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	TBD	TBD	TBD	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	TBD	TBD	TBD	
$t_{SU}(LSI)$(2)	LSI oscillator start-up time	-	TBD	TBD	TBD	µs
$t_{STAB}(LSI)$(2)	LSI oscillator stabilization time	5% of final frequency	TBD	TBD	TBD	µs
$I_{DD}(LSI)$(2)	LSI oscillator power consumption	-	TBD	TBD	TBD	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

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6.3.9 PLL characteristics

The parameters given in *Table 62* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 62. PLL, PLLSAI1, PLLSAI2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	TBD	TBD	TBD	MHz
	PLL input clock duty cycle	-	TBD	TBD	TBD	%
$f_{PLL_P_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1 Normal mode	TBD	TBD	TBD	MHz
		Voltage scaling Range 1 Boost mode	TBD	TBD	TBD	
		Voltage scaling Range 2	TBD	TBD	TBD	
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1 Normal mode	TBD	TBD	TBD	
		Voltage scaling Range 1 Boost mode	TBD	TBD	TBD	
		Voltage scaling Range 2	TBD	TBD	TBD	
$f_{PLL_R_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1 Normal mode	TBD	TBD	TBD	
		Voltage scaling Range 1 Boost mode	TBD	TBD	TBD	
		Voltage scaling Range 2	TBD	TBD	TBD	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	TBD	TBD	TBD	
		Voltage scaling Range 2	TBD	TBD	TBD	
t_{LOCK}	PLL lock time	-	TBD	TBD	TBD	µs
Jitter	RMS cycle-to-cycle jitter	System clock 80 MHz	TBD	TBD	TBD	±ps
	RMS period jitter		TBD	TBD	TBD	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 64 MHz	TBD	TBD	TBD	µA
		VCO freq = 96 MHz	TBD	TBD	TBD	
		VCO freq = 192 MHz	TBD	TBD	TBD	
		VCO freq = 344 MHz	TBD	TBD	TBD	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 3 PLLs.

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6.3.10 Flash memory characteristics

Table 63. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	TBD	TBD	µs
t_{prog_row}	One row (64 double word) programming time	Normal programming	TBD	TBD	ms
		Fast programming	TBD	TBD	
t_{prog_page}	One page (4 Kbytes) programming time	Normal programming	TBD	TBD	
		Fast programming	TBD	TBD	
t_{ERASE}	Page (4 Kbytes) erase time	-	TBD	TBD	
t_{prog_bank}	One bank (1 Mbyte) programming time	Normal programming	TBD	TBD	s
		Fast programming	TBD	TBD	
t_{ME}	Mass erase time (one or two banks)	-	TBD	TBD	ms
I_{DD}	Average consumption from V_{DD}	Write mode	TBD	TBD	mA
		Erase mode	TBD	TBD	
	Maximum current (peak)	Write mode	TBD	TBD	
		Erase mode	TBD	TBD	

1. Guaranteed by design.

Table 64. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	TBD	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	TBD	Years
		1 kcycle(2) at T_A = 105 °C	TBD	
		1 kcycle(2) at T_A = 125 °C	TBD	
		10 kcycles(2) at T_A = 55 °C	TBD	
		10 kcycles(2) at T_A = 85 °C	TBD	
		10 kcycles(2) at T_A = 105 °C	TBD	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

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6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 65*. They are based on the EMS levels and classes defined in application note AN1709.

Table 65. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 120 MHz, conforming to IEC 61000-4-2	TBD
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 120 MHz, conforming to IEC 61000-4-4	TBD

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

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Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 66. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	TBD	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	C3	TBD	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 67. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A(1)

1. Negative injection is limited to -30 mA for PF0, PF1, PG6, PG7, PG8, PG12, PG13, PG14.

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6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 68*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 68. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}(1)	Injected current on all pins except PA4, PA5, PB0, PF13, PE15, PC8, PA13, PH3-BOOT0, PB8, PE0, OPAMP1_V1NM, OPAMP2_V1NM	TBD	TBD	mA
	Injected current on pins PF13, PE15, PC8, PA13, PH3-BOOT0, PB8, PE0	TBD	TBD	
	Injected current on pins OPAMP1_V1NM, OPAMP2_V1NM	TBD	TBD	
	Injected current on PA4, PA5, PB0 pins	TBD	TBD	

1. Guaranteed by characterization.

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 69* are derived from tests performed under the conditions summarized in *Table 21: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

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Table 69. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL} (1)	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	TBD(2)	V
	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	TBD(3)	
	I/O input low level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	-	-	TBD(3)	
	BOOT0 I/O input low level voltage	1.62 V<V_{DDIOx}<3.6 V	-	-	TBD(3)	
V_{IH} (1)	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	TBD(2)	-	-	V
	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	TBD(3)	-	-	
	I/O input high level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	TBD(3)	-	-	
	BOOT0 I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	TBD(3)	-	-	
V_{hys} (3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	TBD	-	mV
	FT_sx	1.08 V<V_{DDIOx}<1.62 V	-	TBD	-	
	BOOT0 I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	TBD	-	

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Table 69. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	FT_xx input leakage current(3)	$V_{IN} \leq Max(V_{DDXXX})$(4)	-	-	TBD	nA
		$Max(V_{DDXXX}) \leq V_{IN} \leq Max(V_{DDXXX})+1$ V(4)(5)	-	-	TBD(3)(6)	
		$Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(3)(5)	-	-	TBD(6)	
	FT_lu, FT_u, PB2 and PC3 IO	$V_{IN} \leq Max(V_{DDXXX})$ (4)	-	-	TBD	
		$Max(V_{DDXXX}) \leq V_{IN} \leq Max(V_{DDXXX})+1$ V(4)	-	-	TBD	
		$Max(V_{DDXXX})+1$ V < VIN ≤ 5.5 V(4)(5)(7)	-	-	TBD(7)	
	TT_xx input leakage current	$V_{IN} \leq Max(V_{DDXXX})$(6)	-	-	TBD	
		$Max(V_{DDXXX}) \leq V_{IN}$ < 3.6 V(6)	-	-	TBD(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current	-	-	-	(8)	
R_{PU}	Weak pull-up equivalent resistor (9)	$V_{IN} = V_{SS}$	TBD	TBD	TBD	kΩ
R_{PD}	Weak pull-down equivalent resistor(9)	$V_{IN} = V_{DDIOx}$	TBD	TBD	TBD	kΩ
C_{IO}	I/O pin capacitance	-	-	TBD	-	pF

1. Refer to *Figure 35: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. $Max(V_{DDXXX})$ is the maximum value of all the I/O supplies. Refer to *Table: Legend/Abbreviations used in the pinout table*.
5. All TX_xx IO except FT_lu, FT_u, PB2 and PC3.
6. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula: $I_{Total_Ileak_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x I_{lkg}(Max).
7. To sustain a voltage higher than $MIN(V_{DD}, V_{DDA})$ +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Refer to I_{bias} in *Table 85: OPAMP characteristics* for the values of the OPAMP dedicated input leakage current.
9. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

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All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 35* for standard I/Os, and in *Figure 35* for 5 V tolerant I/Os.

Figure 35. I/O input characteristics

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 18: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 18: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

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Table 70. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	TBD	V
V_{OH}	Output high level voltage for an I/O pin		TBD	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	TBD	
V_{OH}(3)	Output high level voltage for an I/O pin		TBD	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	TBD	
V_{OH}(3)	Output high level voltage for an I/O pin		TBD	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA $V_{DDIOx} \geq 1.62$ V	-	TBD	
V_{OH}(3)	Output high level voltage for an I/O pin		TBD	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	TBD	
V_{OH}(3)	Output high level voltage for an I/O pin		TBD	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	TBD	
		$\|I_{IO}\|$ = 10 mA $V_{DDIOx} \geq 1.62$ V	-	TBD	
		$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	TBD	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 18: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

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Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 36* and *Table 71*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

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Table 71. I/O AC characteristics(1)(2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	

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Table 71. I/O AC characteristics(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD(3)	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	TBD	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	TBD	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	TBD	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V≤V_{DDIOx}≤3.6 V	-	TBD	MHz
	Tf	Output fall time(4)		-	TBD	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0351 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.

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Figure 36. I/O AC characteristics definition(1)

Maximum frequency is achieved if ($t_r + t_f$) ≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 71: I/O AC characteristics*.

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 72. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	TBD	TBD	TBD	TBD	V
$V_{IH(NRST)}$	NRST input high level voltage	TBD	TBD	TBD	TBD	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	TBD	TBD	TBD	TBD	mV
R_{PU}	Weak pull-up equivalent resistor(2)	TBD	TBD	TBD	TBD	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	TBD	TBD	TBD	TBD	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	TBD	TBD	TBD	TBD	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

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Figure 37. Recommended NRST pin protection

1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 72: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

6.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 73. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	TBD	TBD	TBD	ns

1. Guaranteed by design.

6.3.17 Analog switches booster

Table 74. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	TBD	TBD	TBD	V
$t_{SU(BOOST)}$	Booster startup time	TBD	TBD	TBD	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	TBD	TBD	TBD	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	TBD	TBD	TBD	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	TBD	TBD	TBD	

1. Guaranteed by design.

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6.3.18 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in *Table 75* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 21: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 75. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	TBD	TBD	TBD	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	TBD	TBD	TBD	V
		$V_{DDA} < 2$ V	TBD	TBD	TBD	V
V_{REF-}	Negative reference voltage	-	TBD	TBD	TBD	V
f_{ADC}	ADC clock frequency	Range 1	TBD	TBD	TBD	MHz
		Range 2	TBD	TBD	TBD	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	TBD	TBD	TBD	Msps
		Resolution = 10 bits	TBD	TBD	TBD	
		Resolution = 8 bits	TBD	TBD	TBD	
		Resolution = 6 bits	TBD	TBD	TBD	
	Sampling rate for SLOW channels	Resolution = 12 bits	TBD	TBD	TBD	
		Resolution = 10 bits	TBD	TBD	TBD	
		Resolution = 8 bits	TBD	TBD	TBD	
		Resolution = 6 bits	TBD	TBD	TBD	
f_{TRIG}	External trigger frequency	f_{ADC} = 80 MHz Resolution = 12 bits	TBD	TBD	TBD	MHz
		Resolution = 12 bits	TBD	TBD	TBD	$1/f_{ADC}$
V_{AIN} (3)	Conversion voltage range(2)	-	TBD	TBD	TBD	V
R_{AIN}	External input impedance	-	TBD	TBD	TBD	kΩ
C_{ADC}	Internal sample and hold capacitor	-	TBD	TBD	TBD	pF
t_{STAB}	Power-up time	-	TBD	TBD	TBD	conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 80 MHz	TBD	TBD	TBD	µs
		-	TBD	TBD	TBD	$1/f_{ADC}$

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Table 75. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	TBD	TBD	TBD	$1/f_{ADC}$
		CKMODE = 01	TBD	TBD	TBD	
		CKMODE = 10	TBD	TBD	TBD	
		CKMODE = 11	TBD	TBD	TBD	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	TBD	TBD	TBD	$1/f_{ADC}$
		CKMODE = 01	TBD	TBD	TBD	
		CKMODE = 10	TBD	TBD	TBD	
		CKMODE = 11	TBD	TBD	TBD	
t_s	Sampling time	f_{ADC} = 80 MHz	TBD	TBD	TBD	µs
		-	TBD	TBD	TBD	$1/f_{ADC}$
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	TBD	TBD	TBD	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	TBD	TBD	TBD	µs
		Resolution = 12 bits	TBD	TBD	TBD	$1/f_{ADC}$
$I_{DDA}(ADC)$	ADC consumption from the V_{DDA} supply	fs = 5 Msps	TBD	TBD	TBD	µA
		fs = 1 Msps	TBD	TBD	TBD	
		fs = 10 ksps	TBD	TBD	TBD	
$I_{DDV_S}(ADC)$	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	TBD	TBD	TBD	µA
		fs = 1 Msps	TBD	TBD	TBD	
		fs = 10 ksps	TBD	TBD	TBD	
$I_{DDV_D}(ADC)$	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	TBD	TBD	TBD	µA
		fs = 1 Msps	TBD	TBD	TBD	
		fs = 10 ksps	TBD	TBD	TBD	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package.
Refer to *Section 4: Pinouts and pin description* for further details.

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The maximum value of R_{AIN} can be found in *Table 76: Maximum ADC RAIN*.

Table 76. Maximum ADC R_{AIN}(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	R_{AIN} max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
10 bits	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
8 bits	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
6 bits	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD
	TBD	TBD	TBD	TBD

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1. Guaranteed by design.
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0.
4. Slow channels are: all ADC inputs except the fast channels.

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Table 77. ADC accuracy - limited test conditions 1(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	TBD	TBD	TBD	LSB
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EO	Offset error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EG	Gain error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
ED	Differential linearity error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EL	Integral linearity error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	TBD	TBD	TBD	bits
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	TBD	TBD	TBD	dB
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	

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Table 77. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C	Single ended	Fast channel (max speed)	TBD	TBD	TBD	dB
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

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Table 78. ADC accuracy - limited test conditions 2(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	TBD	TBD	TBD	LSB
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EO	Offset error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EG	Gain error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
ED	Differential linearity error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EL	Integral linearity error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	TBD	TBD	TBD	bits
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	TBD	TBD	TBD	dB
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	

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Table 78. ADC accuracy - limited test conditions 2(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	TBD	TBD	TBD	dB
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

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Table 79. ADC accuracy - limited test conditions 3(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	TBD	TBD	TBD	LSB
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EO	Offset error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EG	Gain error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
ED	Differential linearity error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EL	Integral linearity error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	TBD	TBD	TBD	bits
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	TBD	TBD	TBD	dB
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	

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Table 79. ADC accuracy - limited test conditions 3(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	TBD	TBD	TBD	dB
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

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Table 80. ADC accuracy - limited test conditions 4(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	TBD	TBD	TBD	LSB
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EO	Offset error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EG	Gain error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
ED	Differential linearity error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
EL	Integral linearity error		Single ended	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	TBD	TBD	TBD	bits
				Slow channel (max speed)	10.2	10.5	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	63	65	-	dB
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	65	-	
				Slow channel (max speed)	64	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

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Table 80. ADC accuracy - limited test conditions 4(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	TBD	TBD	TBD	dB
				Slow channel (max speed)	TBD	TBD	TBD	
			Differential	Fast channel (max speed)	TBD	TBD	TBD	
				Slow channel (max speed)	TBD	TBD	TBD	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

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Figure 38. ADC accuracy characteristics

Figure 39. Typical connection diagram using the ADC

1. Refer to *Table 75: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 69: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 69: I/O static characteristics* for the values of I_{lkg}.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 26: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

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6.3.19 Digital-to-Analog converter characteristics

Table 81. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		TBD	TBD	3.6	V
		Other modes		TBD	TBD		
V_{REF+}	Positive reference voltage	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		TBD	TBD	V_{DDA}	
		Other modes		TBD	TBD		
V_{REF-}	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	TBD	TBD	TBD	kΩ
			connected to V_{DDA}	TBD	TBD	TBD	
R_O	Output Impedance	DAC output buffer OFF		TBD	TBD	TBD	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		TBD	TBD	TBD	kΩ
		V_{DD} = 2.0 V		TBD	TBD	TBD	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		TBD	TBD	TBD	kΩ
		V_{DD} = 2.0 V		TBD	TBD	TBD	
C_L	Capacitive load	DAC output buffer ON		TBD	TBD	TBD	pF
C_{SH}		Sample and hold mode		TBD	TBD	TBD	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		TBD	TBD	TBD	V
		DAC output buffer OFF		TBD	TBD	TBD	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	TBD	TBD	TBD	µs
			±1 LSB	TBD	TBD	TBD	
			±2 LSB	TBD	TBD	TBD	
			±4 LSB	TBD	TBD	TBD	
			±8 LSB	TBD	TBD	TBD	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		TBD	TBD	TBD	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	TBD	TBD	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		TBD	TBD	TBD	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		TBD	TBD	TBD	dB

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Table 81. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W_to_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB) DAC_MCR:MODEx[2:0] = 000 or 001 DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 50 pF, RL ≥ 5 kΩ CL ≤ 10 pF		TBD	TBD	TBD	µs
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	TBD	TBD	TBD	ms
			DAC output buffer OFF, C_{SH} = 100 nF	TBD	TBD	TBD	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	TBD	TBD	TBD	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		TBD	TBD	TBD	nA
CI_{int}	Internal sample and hold capacitor	-		TBD	TBD	TBD	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		TBD	TBD	TBD	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		TBD	TBD	TBD	µV
		V_{REF+} = 1.8 V		TBD	TBD	TBD	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	TBD	TBD	TBD	µA
			No load, worst code (0xF1C)	TBD	TBD	TBD	
		DAC output buffer OFF	No load, middle code (0x800)	TBD	TBD	TBD	
		Sample and hold mode, C_{SH} = 100 nF		TBD	TBD	TBD	

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Table 81. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	TBD	TBD	TBD	µA
			No load, worst code (0xF1C)	TBD	TBD	TBD	
		DAC output buffer OFF	No load, middle code (0x800)	TBD	TBD	TBD	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		TBD	TBD	TBD	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		TBD	TBD	TBD	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 40. 12-bit buffered / non-buffered DAC

1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

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Table 82. DAC accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		TBD	TBD	TBD	LSB
		DAC output buffer OFF		TBD	TBD	TBD	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	TBD	TBD	
		DAC output buffer OFF CL ≤ 50 pF, no RL		TBD	TBD	TBD	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	TBD	TBD	TBD	
			V_{REF+} = 1.8 V	TBD	TBD	TBD	
		DAC output buffer OFF CL ≤ 50 pF, no RL		TBD	TBD	TBD	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF CL ≤ 50 pF, no RL		TBD	TBD	TBD	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	TBD	TBD	TBD	
			V_{REF+} = 1.8 V	TBD	TBD	TBD	
Gain	Gain error(5)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	TBD	TBD	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		TBD	TBD	TBD	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	TBD	TBD	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		TBD	TBD	TBD	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	TBD	TBD	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		TBD	TBD	TBD	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		TBD	TBD	TBD	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		TBD	TBD	TBD	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		TBD	TBD	TBD	

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Table 82. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	TBD	TBD	TBD	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	TBD	TBD	TBD	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	TBD	TBD	TBD	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	TBD	TBD	TBD	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} – 0.2) V when buffer is ON.

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6.3.20 Voltage reference buffer characteristics

Table 83. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	TBD	TBD	TBD	V
			V_{RS} = 1	TBD	TBD	TBD	
		Degraded mode(2)	V_{RS} = 0	TBD	TBD	TBD	
			V_{RS} = 1	TBD	TBD	TBD	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	V_{RS} = 0	TBD	TBD	TBD	
			V_{RS} = 1	TBD	TBD	TBD	
		Degraded mode(2)	V_{RS} = 0	TBD	TBD	TBD	
			V_{RS} = 1	TBD	TBD	TBD	
TRIM	Trim step resolution	-	-	TBD	TBD	TBD	%
CL	Load capacitor	-	-	TBD	TBD	TBD	µF
esr	Equivalent Serial Resistor of Cload	-	-	TBD	TBD	TBD	Ω
I_{load}	Static load current	-	-	TBD	TBD	TBD	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	TBD	TBD	TBD	ppm/V
			I_{load} = 4 mA	TBD	TBD	TBD	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	TBD	TBD	TBD	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < TJ < +125 °C		TBD	TBD	TBD	ppm/ °C
		0 °C < TJ < +50 °C		TBD	TBD	TBD	
PSRR	Power supply rejection	DC		TBD	TBD	TBD	dB
		100 kHz		TBD	TBD	TBD	
t_{START}	Start-up time	CL = 0.5 µF(3)		TBD	TBD	TBD	µs
		CL = 1.1 µF(3)		TBD	TBD	TBD	
		CL = 1.5 µF(3)		TBD	TBD	TBD	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (4)	-	-	TBD	TBD	TBD	mA
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA		TBD	TBD	TBD	µA
		I_{load} = 500 µA		TBD	TBD	TBD	
		I_{load} = 4 mA		TBD	TBD	TBD	

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1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
4. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

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6.3.21 Comparator characteristics

Table 84. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			V
V_{SC}	Scaler offset voltage	-		TBD	TBD	TBD	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		TBD	TBD	TBD	nA
		BRG_EN=1 (bridge enable)		TBD	TBD	TBD	µA
t_{START_SCALER}	Scaler startup time	-		TBD	TBD	TBD	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	TBD	TBD	TBD	µs
			$V_{DDA} < 2.7$ V	TBD	TBD	TBD	
		Medium mode	$V_{DDA} \geq 2.7$ V	TBD	TBD	TBD	
			$V_{DDA} < 2.7$ V	TBD	TBD	TBD	
		Ultra-low-power mode		TBD	TBD	TBD	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	TBD	TBD	TBD	ns
			$V_{DDA} < 2.7$ V	TBD	TBD	TBD	
		Medium mode	$V_{DDA} \geq 2.7$ V	TBD	TBD	TBD	µs
			$V_{DDA} < 2.7$ V	TBD	TBD	TBD	
		Ultra-low-power mode		TBD	TBD	TBD	
V_{offset}	Comparator offset error	Full common mode range	-	TBD	TBD	TBD	mV
V_{hys}	Comparator hysteresis	No hysteresis		TBD	TBD	TBD	mV
		Low hysteresis		TBD	TBD	TBD	
		Medium hysteresis		TBD	TBD	TBD	
		High hysteresis		TBD	TBD	TBD	

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Table 84. COMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	TBD	TBD	TBD	nA
			With 50 kHz ±100 mV overdrive square signal	TBD	TBD	TBD	
		Medium mode	Static	TBD	TBD	TBD	µA
			With 50 kHz ±100 mV overdrive square signal	TBD	TBD	TBD	
		High-speed mode	Static	TBD	TBD	TBD	
			With 50 kHz ±100 mV overdrive square signal	TBD	TBD	TBD	
I_{bias}	Comparator input bias current	-		TBD	TBD	TBD	nA

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 24: Embedded internal voltage reference*.
3. Guaranteed by characterization results.

6.3.22 Operational amplifiers characteristics

Table 85. OPAMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	TBD	TBD	TBD	V
CMIR	Common mode input range	-	TBD	TBD	TBD	V
VI_{OFFSET}	Input offset voltage	25 °C, No Load on output.	TBD	TBD	TBD	mV
		All voltage/Temp.	TBD	TBD	TBD	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode	TBD	TBD	TBD	µV/°C
		Low-power mode	TBD	TBD	TBD	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 x V_{DDA})	-	TBD	TBD	TBD	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 x V_{DDA})	-	TBD	TBD	TBD	

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Table 85. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	TBD	TBD	TBD	µA
		Low-power mode		TBD	TBD	TBD	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	TBD	TBD	TBD	
		Low-power mode		TBD	TBD	TBD	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	TBD	TBD	TBD	kΩ
		Low-power mode		TBD	TBD	TBD	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	TBD	TBD	TBD	
		Low-power mode		TBD	TBD	TBD	
C_{LOAD}	Capacitive load	-		TBD	TBD	TBD	pF
CMRR	Common mode rejection ratio	Normal mode		TBD	TBD	TBD	dB
		Low-power mode		TBD	TBD	TBD	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	TBD	TBD	TBD	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	TBD	TBD	TBD	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	TBD	TBD	TBD	kHz
		Low-power mode		TBD	TBD	TBD	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	TBD	TBD	TBD	
		Low-power mode		TBD	TBD	TBD	
SR(2)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	TBD	TBD	TBD	V/ms
		Low-power mode		TBD	TBD	TBD	
		Normal mode	$V_{DDA} < 2.4$ V	TBD	TBD	TBD	
		Low-power mode		TBD	TBD	TBD	
AO	Open loop gain	Normal mode		TBD	TBD	TBD	dB
		Low-power mode		TBD	TBD	TBD	
V_{OHSAT}(2)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	TBD	TBD	TBD	mV
		Low-power mode		TBD	TBD	TBD	
V_{OLSAT}(2)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	TBD	TBD	TBD	
		Low-power mode		TBD	TBD	TBD	
φ_m	Phase margin	Normal mode		TBD	TBD	TBD	°
		Low-power mode		TBD	TBD	TBD	

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Table 85. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
GM	Gain margin	Normal mode		TBD	TBD	TBD	dB
		Low-power mode		TBD	TBD	TBD	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ follower configuration	TBD	TBD	TBD	µs
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ follower configuration	TBD	TBD	TBD	
I_{bias}	OPAMP input bias current	General purpose input (all packages except UFBGA132 and UFBGA169 only)		TBD	TBD	TBD	nA
		Dedicated input (UFBGA132 and UFBGA169 only)	$T_J \leq 75$ °C	TBD	TBD	TBD	
			$T_J \leq 85$ °C	TBD	TBD	TBD	
			$T_J \leq 105$ °C	TBD	TBD	TBD	
			$T_J \leq 125$ °C	TBD	TBD	TBD	
PGA gain(2)	Non inverting gain value	-		TBD	TBD	TBD	-
				TBD	TBD	TBD	
				TBD	TBD	TBD	
				TBD	TBD	TBD	
$R_{network}$	R2/R1 internal resistance values in PGA mode(3)	PGA Gain = 2		TBD	TBD	TBD	kΩ/kΩ
		PGA Gain = 4		TBD	TBD	TBD	
		PGA Gain = 8		TBD	TBD	TBD	
		PGA Gain = 16		TBD	TBD	TBD	
Delta R	Resistance variation (R1 or R2)	-		TBD	TBD	TBD	%
PGA gain error	PGA gain error	-		TBD	TBD	TBD	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	TBD	TBD	TBD	MHz
		Gain = 4	-	TBD	TBD	TBD	
		Gain = 8	-	TBD	TBD	TBD	
		Gain = 16	-	TBD	TBD	TBD	

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Table 85. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
en	Voltage noise density	Normal mode	at 1 kHz, Output loaded with 4 kΩ	TBD	TBD	TBD	nV/√Hz
		Low-power mode	at 1 kHz, Output loaded with 20 kΩ	TBD	TBD	TBD	
		Normal mode	at 10 kHz, Output loaded with 4 kΩ	TBD	TBD	TBD	
		Low-power mode	at 10 kHz, Output loaded with 20 kΩ	TBD	TBD	TBD	
I_{DDA}(OPAMP)(2)	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode	TBD	TBD	TBD	µA
		Low-power mode		TBD	TBD	TBD	

1. Guaranteed by design, unless otherwise specified.
2. Guaranteed by characterization results.
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain =1+R2/R1

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6.3.23 Temperature sensor characteristics

Table 86. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	TBD	TBD	TBD	°C
Avg_Slope(2)	Average slope	TBD	TBD	TBD	mV/°C
V_{30}	Voltage at 30°C (±5 °C)(3)	TBD	TBD	TBD	V
t_{START} (TS_BUF)(1)	Sensor Buffer Start-up time in continuous mode(4)	TBD	TBD	TBD	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	TBD	TBD	TBD	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	TBD	TBD	TBD	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	TBD	TBD	TBD	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 8: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.24 V_{BAT} monitoring characteristics

Table 87. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	TBD	TBD	TBD	kΩ
Q	Ratio on V_{BAT} measurement	TBD	TBD	TBD	-
Er(1)	Error on Q	TBD	TBD	TBD	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	TBD	TBD	TBD	µs

1. Guaranteed by design.

Table 88. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	TBD	TBD	TBD	kΩ
		VBRS = 1	TBD	TBD	TBD	

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6.3.25 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 89* for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in *Table 21: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM1_CKINy, DFSDM1_DATINy, DFSDM1_CKOUT for DFSDM).

Table 89. DFSDM characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	-	TBD	TBD	TBD	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0] = 01)	TBD	TBD	TBD	
f_{CKOUT}	Output clock frequency	-	TBD	TBD	TBD	MHz
$DuCy_{CKOUT}$	Output clock frequency duty cycle	-	TBD	TBD	TBD	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0)	TBD	TBD	TBD	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	TBD	TBD	TBD	
t_h	Data input hold time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0)	TBD	TBD	TBD	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0)	TBD	TBD	TBD	

1. Data based on characterization results, not tested in production.

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Figure 16: DFSDM timing diagram

6.3.26 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

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Table 90. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	TBD	TBD	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	TBD	TBD	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	TBD	TBD	MHz
		$f_{TIMxCLK}$ = 120 MHz	TBD	TBD	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	TBD	TBD	bit
		TIM2 and TIM5	TBD	TBD	
$t_{COUNTER}$	16-bit counter clock period	-	TBD	TBD	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	TBD	TBD	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	TBD	TBD	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 120 MHz	TBD	TBD	s

1. TIMx is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 91. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	TBD	TBD	ms
/8	1	TBD	TBD	
/16	2	TBD	TBD	
/32	3	TBD	TBD	
/64	4	TBD	TBD	
/128	5	TBD	TBD	
/256	6 or 7	TBD	TBD	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 92. WWDG min/max timeout value at 120 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	TBD	TBD	ms
2	1	TBD	TBD	
4	2	TBD	TBD	
8	3	TBD	TBD	

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6.3.27 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0351 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to *Table 93* below for the analog filter characteristics:

Table 93. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	TBD	TBD	ns

1. Guaranteed by design.

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SPI characteristics

Unless otherwise specified, the parameters given in *Table 94* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 21: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 94. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7 V < V_{DD} < 3.6 V Voltage Range V1	-	-	TBD	MHz
		Master mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			TBD	
		Master transmitter mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			TBD	
		Slave receiver mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			TBD	
		Slave mode transmitter/full duplex 2.7 V < V_{DD} < 3.6 V Voltage Range V1			TBD	
		Slave mode transmitter/full duplex 1.71 V < V_{DD} < 3.6 V Voltage Range V1			TBD	
		1.71 V < V_{DD} < 3.6 V Voltage Range V2			TBD	
		1.08 V < V_{DD} < 1.32 V(3)			12	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	TBD	TBD	TBD	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	TBD	TBD	TBD	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	TBD	TBD	TBD	ns
$t_{su(MI)}$	Data input setup time	Master mode	TBD	TBD	TBD	ns
$t_{su(SI)}$		Slave mode	TBD	TBD	TBD	
$t_{h(MI)}$	Data input hold time	Master mode	TBD	TBD	TBD	ns
$t_{h(SI)}$		Slave mode	TBD	TBD	TBD	
$t_{a(SO)}$	Data output access time	Slave mode	TBD	TBD	TBD	ns

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Table 94. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
$t_{dis(SO)}$	Data output disable time	Slave mode	TBD	TBD	TBD	ns
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < V_{DD} < 3.6 V Voltage Range V1	TBD	TBD	TBD	ns
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1	TBD	TBD	TBD	
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range V2	TBD	TBD	TBD	
		Slave mode 1.08 V < V_{DD} < 1.32 V(3)	TBD	TBD	TBD	
$t_{v(MO)}$		Master mode	TBD	TBD	TBD	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	TBD	TBD	TBD	
		Slave mode 1.08 < V_{DD} < 1.32 V(3)	TBD	TBD	TBD	
$t_{h(MO)}$		Master mode	TBD	TBD	TBD	

1. Guaranteed by characterization results.
2. The maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high-phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.
3. SPI mapped on Port G.

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Figure 41. SPI timing diagram - slave mode and CPHA = 0

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Figure 42. SPI timing diagram - slave mode and CPHA = 1

1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 43. SPI timing diagram - master mode

1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

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SAI characteristics

Unless otherwise specified, the parameters given in *Table 95* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in*Table 21: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

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Table 95. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	TBD	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	TBD	MHz
		Master transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	TBD	
		Master receiver Voltage Range 1	-	TBD	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	TBD	
		Slave transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	TBD	
		Slave receiver Voltage Range 1	-	TBD	
		Voltage Range 2	-	TBD	
		1.08 V ≤ V_{DD} ≤ 1.32 V	-	TBD	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	TBD	ns
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V	-	TBD	
$t_{h(FS)}$	FS hold time	Master mode	TBD	TBD	ns
$t_{su(FS)}$	FS setup time	Slave mode	TBD	TBD	ns
$t_{h(FS)}$	FS hold time	Slave mode	TBD	TBD	ns
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	TBD	TBD	ns
$t_{su(SD_B_SR)}$		Slave receiver	TBD	TBD	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	TBD	TBD	ns
$t_{h(SD_B_SR)}$		Slave receiver	TBD	TBD	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	TBD	TBD	ns
		Slave transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	TBD	TBD	
		Slave transmitter (after enable edge) 1.08 V < V_{DD} <1.32 V	TBD	TBD	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	TBD	TBD	ns

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Table 95. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	TBD	TBD	ns
		Master transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	TBD	TBD	
		Master transmitter (after enable edge) 1.08 V ≤ V_{DD} ≤ 1.32 V	TBD	TBD	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	TBD	TBD	ns

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 44. SAI master timing waveforms

Figure 45. SAI slave timing waveforms

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USB OTG full speed (FS) characteristics

The device's USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 96. USB electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDUSB}	USB OTG full speed transceiver operating voltage	-	TBD	TBD	TBD	V
V_{DI}(2)	Differential input sensitivity	Over VCM range	TBD	TBD	TBD	
V_{CM}(2)	Differential input common mode range	Includes V_{DI} range	TBD	TBD	TBD	
V_{SE}(2)	Single ended receiver input threshold	-	TBD	TBD	TBD	
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(3)	TBD	TBD	TBD	
V_{OH}	Static output level high	R_L of 15 kΩ to 3.6 V(3)	TBD	TBD	TBD	
R_{PD}(2)	Pull down resistor on PA11, PA12 (USB_FS_DP/DM)	$V_{IN} = V_{DD}$	TBD	TBD	TBD	kΩ
R_{PU}(2)	Pull Up Resistor on PA12 (USB_FS_DP)	$V_{IN} = V_{SS}$ during idle	TBD	TBD	TBD	
	Pull Up Resistor on PA12 (USB_FS_DP)	$V_{IN} = V_{SS}$ during reception	TBD	TBD	TBD	
	Pull Up Resistor on PA10 (OTG_FS_ID)	-	TBD	TBD	TBD	

1. All the voltages are measured from the local ground potential.
2. Guaranteed by design.
3. R_L is the load connected on the USB OTG full speed drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at its default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

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Figure 46. USB OTG timings – definition of data signal rise and fall time

Table 97. USB OTG electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rLS}	Rise time in LS(2)	C_L = 200 to 600 pF	TBD	TBD	ns
t_{fLS}	Fall time in LS(2)				
t_{rfmLS}	Rise/ fall time matching in LS	t_r / t_f	TBD	TBD	%
t_{rFS}	Rise time in FS(2)	C_L = 50 pF	TBD	TBD	ns
t_{fFS}	Fall time in FS(2)	C_L = 50 pF	TBD	TBD	
t_{rfmFS}	Rise/ fall time matching in FS	t_r / t_f	TBD	TBD	%
V_{CRS}	Output signal crossover voltage (LS/FS)	-	TBD	TBD	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	TBD	TBD	Ω

1. Guaranteed by design
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

Table 98. USB BCD DC electrical characteristics(1)

Driver characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
$I_{DD(USBBCD)}$	Primary detection mode consumption	-	TBD	TBD	TBD	µA
	Secondary detection mode consumption	-	TBD	TBD	TBD	
RDAT_LKG	Data line leakage resistance	-	TBD	TBD	TBD	kΩ
VDAT_LKG	Data line leakage voltage	-	TBD	TBD	TBD	V
RDCP_DAT	Dedicated charging port resistance across D+/D-	-	TBD	TBD	TBD	Ω
VLGC_HI	Logic high	-	TBD	TBD	TBD	V
VLGC_LOW	Logic low	-	TBD	TBD	TBD	V

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Table 98. USB BCD DC electrical characteristics(1) (continued)

Driver characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
VLGC	Logic threshold	-	TBD	TBD	TBD	V
VDAT_REF	Data detect voltage	-	TBD	TBD	TBD	V
VDP_SRC	D+ source voltage	-	TBD	TBD	TBD	V
VDM_SRC	D- source voltage	-	TBD	TBD	TBD	V
IDP_SINK	D+ sink current	-	TBD	TBD	TBD	µA
IDM_SINK	D- sink current	-	TBD	TBD	TBD	µA

1. Guaranteed by design

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.28 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 99* to *Table 112* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 21*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 47 through *Figure 50* represent asynchronous waveforms and *Table 99* through *Table 106* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataHoldTime = 0x1
- ByteLaneSetup = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the THCLK is the HCLK clock period.

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Figure 47. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

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Table 99. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	TBD	TBD	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	TBD	TBD	
$t_{w(NOE)}$	FMC_NOE low time	TBD	TBD	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	TBD	TBD	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	TBD	TBD	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	TBD	TBD	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	TBD	TBD	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	TBD	TBD	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	TBD	TBD	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	TBD	TBD	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	TBD	TBD	
$t_{w(NADV)}$	FMC_NADV low time	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 100. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	TBD	TBD	ns
$t_{w(NOE)}$	FMC_NWE low time	TBD	TBD	
$t_{w(NWAIT)}$	FMC_NWAIT low time	TBD	TBD	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	TBD	TBD	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.

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Figure 48. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

Table 101. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	TBD	TBD	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	TBD	TBD	
$t_{w(NWE)}$	FMC_NWE low time	TBD	TBD	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	TBD	TBD	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	TBD	TBD	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	TBD	TBD	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	TBD	TBD	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	TBD	TBD	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	TBD	TBD	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	TBD	TBD	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	TBD	TBD	
$t_{w(NADV)}$	FMC_NADV low time	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.

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Table 102. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	TBD	TBD	ns
$t_{w(NWE)}$	FMC_NWE low time	TBD	TBD	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	TBD	TBD	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 49. Asynchronous multiplexed PSRAM/NOR read waveforms

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Table 103. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	TBD	TBD	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	TBD	TBD	
$t_{w(NOE)}$	FMC_NOE low time	TBD	TBD	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	TBD	TBD	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	TBD	TBD	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	TBD	TBD	
$t_{w(NADV)}$	FMC_NADV low time	TBD	TBD	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	TBD	TBD	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	TBD	TBD	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	TBD	TBD	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	TBD	TBD	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	TBD	TBD	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 104. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	TBD	TBD	ns
$t_{w(NOE)}$	FMC_NWE low time	TBD	TBD	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	TBD	TBD	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.

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Figure 50. Asynchronous multiplexed PSRAM/NOR write waveforms

Table 105. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	TBD	TBD	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	TBD	TBD	
$t_{w(NWE)}$	FMC_NWE low time	TBD	TBD	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	TBD	TBD	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	TBD	TBD	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	TBD	TBD	
$t_{w(NADV)}$	FMC_NADV low time	TBD	TBD	
$t_{h(AD_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high	TBD	TBD	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	TBD	TBD	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	TBD	TBD	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	TBD	TBD	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	TBD	TBD	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	TBD	TBD	

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1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 106. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	TBD	TBD	ns
$t_{w(NWE)}$	FMC_NWE low time	TBD	TBD	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	TBD	TBD	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 51 through *Figure 54* represent synchronous waveforms and *Table 107* through *Table 110* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For 2.7 V ≤ V_{DD} ≤ 3.6 V, maximum FMC_CLK = 60 MHz for CLKDIV = 0x1 and 54 MHz for CLKDIV = 0x0 at CL = 30 pF (on FMC_CLK).
- For 1.71 V ≤ V_{DD} ≤ 2.7 V, maximum FMC_CLK = 60 MHz for CLKDIV = 0x1 and 32 MHz for CLKDIV = 0x0 at CL= 20 pF (on FMC_CLK).

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Figure 51. Synchronous multiplexed NOR/PSRAM read timings

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Table 107. Synchronous multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	TBD	TBD	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	TBD	TBD	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	TBD	TBD	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	TBD	TBD	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	TBD	TBD	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	TBD	TBD	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	TBD	TBD	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	TBD	TBD	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	TBD	TBD	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	TBD	TBD	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	TBD	TBD	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	TBD	TBD	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	TBD	TBD	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	TBD	TBD	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

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Figure 52. Synchronous multiplexed PSRAM write timings

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Table 108. Synchronous multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	TBD	TBD	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	TBD	TBD	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	TBD	TBD	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	TBD	TBD	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	TBD	TBD	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	TBD	TBD	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	TBD	TBD	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	TBD	TBD	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	TBD	TBD	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	TBD	TBD	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	TBD	TBD	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	TBD	TBD	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	TBD	TBD	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	TBD	TBD	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	TBD	TBD	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

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Figure 53. Synchronous non-multiplexed NOR/PSRAM read timings

Table 109. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	TBD	TBD	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	TBD	TBD	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	TBD	TBD	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	TBD	TBD	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	TBD	TBD	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	TBD	TBD	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	TBD	TBD	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	TBD	TBD	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	TBD	TBD	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	TBD	TBD	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	TBD	TBD	

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Table 109. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	TBD	TBD	ns
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

Figure 54. Synchronous non-multiplexed PSRAM write timings

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Table 110. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	TBD	TBD	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	TBD	TBD	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	TBD	TBD	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	TBD	TBD	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	TBD	TBD	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	TBD	TBD	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	TBD	TBD	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	TBD	TBD	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	TBD	TBD	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	TBD	TBD	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	TBD	TBD	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	TBD	TBD	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	TBD	TBD	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

NAND controller waveforms and timings

Figure 55 through *Figure 58* represent synchronous waveforms, and *Table 111* and *Table 112* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

In all timing tables, the T_{HCLK} is the HCLK clock period.

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Figure 55. NAND controller waveforms for read access

Figure 56. NAND controller waveforms for write access

Figure 57. NAND controller waveforms for common memory read access

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Figure 58. NAND controller waveforms for common memory write access

Table 111. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(N0E)}$	FMC_NOE low width	TBD	TBD	ns
$T_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	TBD	TBD	
$T_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	TBD	TBD	
$T_{d(NCE-NOE)}$	FMC_NCE valid before FMC_NOE low	TBD	TBD	
$T_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 112. Switching characteristics for NAND Flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(NWE)}$	FMC_NWE low width	TBD	TBD	ns
$T_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	TBD	TBD	
$T_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	TBD	TBD	
$T_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	TBD	TBD	
$T_{d(NCE_NWE)}$	FMC_NCE valid before FMC_NWE low	TBD	TBD	
$T_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	TBD	TBD	

1. CL = 30 pF.
2. Guaranteed by characterization results.

6.3.29 OctoSPI characteristics

Unless otherwise specified, the parameters given in *Table 113*, *Table 114* and *Table 115* for OctoSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency

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and V_{DD} supply voltage conditions summarized in *Table 21: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 113. OctoSPI(1) characteristics in SDR mode(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F(QCK)	OctoSPI clock frequency	1.71 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 20 pF	TBD	-	TBD	MHz
		2.7 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 20 pF	TBD	TBD	TBD	
		1.71 V < V_{DD}< 3.6 V Voltage Range 1 C_{LOAD} = 15 pF	TBD	TBD	TBD	
		1.71 V < V_{DD}< 3.6 V Voltage Range 2 C_{LOAD} = 20 pF	TBD	TBD	TBD	
$t_{w(CKH)}$	OctoSPI clock high and low time	Prescaler = 0	TBD	TBD	TBD	ns
$t_{w(CKL)}$			TBD	TBD	TBD	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	TBD	TBD	TBD	
		Voltage Range 2	TBD	TBD	TBD	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	TBD	TBD	TBD	
		Voltage Range 2	TBD	TBD	TBD	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	TBD	TBD	TBD	
		Voltage Range 2	TBD	TBD	TBD	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	TBD	TBD	TBD	
		Voltage Range 2	TBD	TBD	TBD	

1. Values in the table applies to Octal and Quad SPI mode.
2. Guaranteed by characterization results.

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Table 114. OctoSPI[1] characteristics in DTR mode (no DQS)[2]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	OctoSPI clock frequency	1.71 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 20 pF		TBD	TBD	TBD	MHz
		2.7 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 20 pF		TBD	TBD	TBD	
		1.71 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 15 pF		TBD	TBD	TBD	
		1.71 V < V_{DD} < 3.6 V Voltage Range 2 C_{LOAD} = 20 pF		TBD	TBD	TBD	
$t_{w(CKH)}$	OctoSPI clock high and low time	-		TBD	TBD	TBD	ns
$t_{w(CKL)}$				TBD	TBD	TBD	
$t_{sf(IN)}$ $t_{sr(IN)}$	Data input setup time	Voltage Range 1		TBD	TBD	TBD	
		Voltage Range 2		TBD	TBD	TBD	
$t_{hf(IN)}$ $t_{hr(IN)}$	Data input hold time	Voltage Range 1		TBD	TBD	TBD	
		Voltage Range 2		TBD	TBD	TBD	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	Voltage Range 1	DHQC = 0	TBD	TBD	TBD	
			DHQC = 1 Pres=1,2 ...	TBD	TBD	TBD	
		Voltage Range 2	DHQC = 0	TBD	TBD	TBD	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	Voltage Range 1	DHQC = 0	TBD	TBD	TBD	
			DHQC = 1 Pres=1,2 ...	TBD	TBD	TBD	
		Voltage Range 2	DHQC = 0	TBD	TBD	TBD	

1. Values in the table applies to Octal and Quad SPI mode.
2. Guaranteed by characterization results.

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Table 115. OctoSPI characteristics in DTR mode (with DQS)(1)/Octal and Hyperbus

Symbol	Parameter	Conditions		Min	Typ	Max(2)	Unit
F_{CK} $1/t_{(CK)}$	OctoSPI clock frequency (fixed latency)	1.71 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 20 pF		TBD	TBD	TBD	MHz
		2.7 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 20 pF		TBD	TBD	TBD	
		1.71 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 15 pF		TBD	TBD	TBD	
		1.71 V < V_{DD} < 3.6 V Voltage Range 2 C_{LOAD} = 20 pF		TBD	TBD	TBD	
	OctoSPI clock frequency (additional latency)	1.71 < V_{DD} < 3.6 V Voltage Range V1 C_{LOAD} = 20 pF t_{CKDS} = 9ns	Prescaler = 0,1,3,5...	TBD	TBD	TBD	
			Prescaler = 2,4,6...	TBD	TBD	TBD	
		2.7 < V_{DD} < 3.6 V Voltage Range V1 C_{LOAD} = 20 pF t_{CKDS} = 9ns	Prescaler = 0,1,3,5...	TBD	TBD	TBD	
			Prescaler = 2,4,6...	TBD	TBD	TBD	
		1.71 < V_{DD} < 3.6 V Voltage Range V2 C_{LOAD} = 20 pF t_{CKDS} = 9ns	-	TBD	TBD	TBD	

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Table 115. OctoSPI characteristics in DTR mode (with DQS)(1)/Octal and Hyperbus (continued)

Symbol	Parameter	Conditions		Min	Typ	Max(2)	Unit
$t_{w(CKH)}$	OctoSPI clock high and low time	-		TBD	TBD	TBD	ns
$t_{w(CKL)}$				TBD	TBD	TBD	
$t_{v(CK)}$	Clock valid time	-		TBD	TBD	TBD	
$t_{h(CK)}$	Clock hold time	-		TBD	TBD	TBD	
$t_{w(CS)}$	Chip select high time	-		TBD	TBD	TBD	
$t_{v(DQ)}$	Data input vallid time	-		TBD	TBD	TBD	
$t_{v(DS)}$	Data storbe input valid time	-		TBD	TBD	TBD	
$t_{h(DS)}$	Data storbe input hold time	-		TBD	TBD	TBD	
$t_{v(RWDS)}$	Data storbe output valid time	-		TBD	TBD	TBD	
$t_{sr(IN)}$ $t_{sf(IN)}$	Data input setup time	Voltage Range 1		TBD	TBD	TBD	
		Voltage Range 2		TBD	TBD	TBD	
$t_{hr(IN)}$ $t_{hf(IN)}$	Data input hold time	Voltage Range 1		TBD	TBD	TBD	
		Voltage Range 2		TBD	TBD	TBD	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	Voltage Range 1	DHQC = 0	TBD	TBD	TBD	ns
			DHQC = 1 Pres=1,2 ...	TBD	TBD	TBD	
		Voltage Range 2	DHQC = 0	TBD	TBD	TBD	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	Voltage Range 1	DHQC = 0	TBD	TBD	TBD	
			DHQC = 1 Pres=1,2 ...	TBD	TBD	TBD	
		Voltage Range 2	DHQC = 0	TBD	TBD	TBD	

1. Guaranteed by characterization results.
2. Maximum frequency values are given for a RWDS to DQ skew of maximum +/-1.0 ns.

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Figure 59. OctoSPI timing diagram - SDR mode

Figure 60. OctoSPI timing diagram - DDR mode

Figure 61. OctoSPI Hyperbus clock

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Figure 62. OctoSPI Hyperbus read

Figure 63. OctoSPI Hyperbus read with double latency

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Figure 64. OctoSPI Hyperbus write

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6.3.30 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 116* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 20*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data format: 14 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Figure 65. DCMI timing diagram

Table 116. DCMI characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	TBD	TBD	-
DCMI_PIXCLK	Pixel clock input	1.71 < VDD < 3.6 Voltage range V1	TBD	TBD	MHz
		1.71 < VDD < 3.6 Voltage range V2	TBD	TBD	
D_{pixel}	Pixel clock input duty cycle	-	TBD	TBD	%

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Table 116. DCMI characteristics[1] (continued)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{su(DATA)}$	Data input setup time	1.71 < VDD < 3.6 Voltage range V1	TBD	TBD	ns
		1.71 < VDD < 3.6 Voltage range V2	TBD	TBD	
$t_{h(DATA)}$	Data hold time	1.71 < VDD < 3.6 Voltage range V1	TBD	TBD	
		1.71 < VDD < 3.6 Voltage range V2	TBD	TBD	
$t_{su(HSYNC)}$, $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	1.71 < VDD < 3.6 Voltage range V1	TBD	TBD	
		1.71 < VDD < 3.6 Voltage range V2	TBD	TBD	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	1.71 < VDD < 3.6 Voltage range V1	TBD	TBD	
		1.71 < VDD < 3.6 Voltage range V2	TBD	TBD	

1. Data based on characterization results, not tested in production.

6.3.31 Parallel slave interface (PSSI)

Unless otherwise specified, the parameters given in Table 112 for PSSI are derived from tests performed under the ambient temperature, fHCLK frequency and VDD supply voltage summarized in *Table 21*, with the following configuration:

- PSSI_PDCK polarity: falling
- PSSI_RDY and PSSI_DE polarity: high
- Data format: 16 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

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6.3.32 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 117* for LCD-TFT are derived from tests performed under the ambient temperature, fHCLK frequency and VDD supply voltage summarized in *Table 21*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 117. LTDC characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CLK} D_{CLK}	LTDC clock output frequency	2.7 V < V_{DD} < 3.6 V	TBD	TBD	MHz
		1.71 V < V_{DD} < 3.6 V	TBD	TBD	
	LTDC clock output duty cycle	-	TBD	TBD	%
tw(CLKH) tw(CLKL)	Clock high time Clock low time	-	TBD	TBD	-
t_v(DATA)	Data output valid time	-	TBD	TBD	
t_h(DATA)	Data output hold time	-	TBD	TBD	
t_v(HSYNC) t_v(VSYNC) t_v(DE)	HSYNC/VSYNC/DE output valid time	-	TBD	TBD	
t_h(HSYNC) t_h(VSYNC) t_h(DE)	HSYNC/VSYNC/DE output hold time	-	TBD	TBD	

1. Guaranteed by characterization results.

6.3.33 SD/SDIO/MMC card host interfaces (SDMMC)

Unless otherwise specified, the parameters given in Table xx for SDIO are derived from tests performed under the ambient temperature, fPCLKx frequency and VDD supply voltage conditions summarized in *Table 21: General operating conditions* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD} Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

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Table 118. Dynamics characteristics: SD / eMMC characteristics at VDD = 2.7 V to 3.6 V [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fPP	Clock frequency in data transfer mode	-	TBD	TBD	TBD	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	TBD	TBD	TBD	-
tW(CKL)	Clock low time	fpp = 52 MHz	TBD	TBD	TBD	ns
tW(CKH)	Clock high time	fpp = 52 MHz	TBD	TBD	TBD	
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR[2]/DDR[2] mode						
tISU	Input setup time HS	-	TBD	TBD	TBD	ns
tIHD	Input hold time HS	-	TBD	TBD	TBD	
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR[2]/DDR[2] mode						
tOV	Output valid time HS	-	TBD	TBD	TBD	ns
tOH	Output hold time HS	-	TBD	TBD	TBD	
CMD, D inputs (referenced to CK) in SD default mode						
tISUD	Input setup time SD	-	1.5	-	-	ns
tIHD	Input hold time SD	-	2	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
tOVD	Output valid default time SD	-	-	1	2.5	ns
tOHD	Output hold default time SD	-	0	-	-	

1. Guaranteed by characterization results.
2. For SD 1.8 V support, an external voltage converter is needed.

Table 119. Dynamics characteristics: eMMC characteristics at VDD = 1.71 V to 1.9 V[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fPP	Clock frequency in data transfer mode	-	TBD	TBD	TBD	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	TBD	TBD	TBD	-
tW(CKL)	Clock low time	fpp = 52 MHz	TBD	TBD	TBD	ns
tW(CKH)	Clock high time	fpp = 52 MHz	TBD	TBD	TBD	
CMD, D inputs (referenced to CK) in eMMC mode						
tISU	Input setup time HS	-	TBD	TBD	TBD	ns
tIH	Input hold time HS	-	TBD	TBD	TBD	
CMD, D outputs (referenced to CK) in eMMC mode						

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Table 119. Dynamics characteristics: eMMC characteristics at VDD = 1.71 V to 1.9 V(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tOV	Output valid time HS	-	TBD	TBD	TBD	ns
tOH	Output hold time HS	-	TBD	TBD	TBD	

1. Guaranteed by characterization results.
2. Cload = 20 pF.

See the different SDMMC diagrams in *Figure 66*, *Figure 67* and *Figure 68* below.

Figure 66. SDIO high-speed mode

Figure 67. SD default mode

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Figure 68. DDR mode

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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP48 package information

Figure 69. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline

1. Drawing is not to scale.

Table 120. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

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Table 120. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 70. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

1. Dimensions are expressed in millimeters.

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LQFP48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 71. LQFP48 marking (package top view)

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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Figure 72. LQFP48, external SMPS device, marking (package top view)

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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7.2 UFQFPN48 package information

Figure 73. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline

1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 121. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244

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Table 121. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 74. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

Dimensions are expressed in millimeters.

UFQFPN48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

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Figure 75. UFQFPN48 marking (package top view)

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 76. UFQFPN48, external SMPS device, marking (package top view)

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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7.3 LQFP64 package information

Figure 77. LQFP - 64-pin, 10 x 10 mm low-profile quad flat package outline

1. Drawing is not to scale.

Table 122. LQFP - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-

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Table 122. LQFP - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 78. LQFP - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint

1. Dimensions are expressed in millimeters.

LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

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Figure 79. LQFP64 marking (package top view)

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 80. LQFP64, external SMPS device, marking (package top view)

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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7.4 LQFP100 package information

Figure 81. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline

1. Drawing is not to scale.

Table 123. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

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Table 123. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 82. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

1. Dimensions are expressed in millimeters.

LQFP100 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

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Figure 83. LQFP100 marking (package top view)

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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7.5 WLCSP100 package information

Figure 84. WLCSP – 100 ball, 4.618 x 4.142 mm, 0.4 mm pitch wafer level chip scale package outline

1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 124. WLCSP – 100 ball, 4.618 x 4.142 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-

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Table 124. WLCSP – 100 ball, 4.618 x 4.142 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
Ø b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	4.583	4.618	4.653	0.1804	0.1818	0.1832
E	4.107	4.142	4.177	0.1617	0.1631	0.1644
e	-	0.400	-	-	0.0157	-
e1	-	3.600	-	-	0.1417	-
e2	-	3.600	-	-	0.1417	-
F	-	0.509	-	-	0.0200	-
G	-	0.271	-	-	0.0107	-
aaa	-	0.100	-	-	0.0039	-
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

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Figure 85. WLCSP – 100 ball, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package recommended footprint

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Table 125. WLCSP100 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm
Stencil thickness	0.1 mm

Figure 86. WLCSP100 marking (package top view)

1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

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Figure 87. WLCSP100, external SMPS device, marking (package top view)

1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

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7.6 UFBGA132 package information

Figure 88. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline

1. Drawing is not to scale.

Table 126. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-

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Table 126. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-
ddd	-	0.080	-	-	0.0031	-
eee	-	0.150	-	-	0.0059	-
fff	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 89. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package recommended footprint

Table 127. UFBGA132 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm
Ball diameter	0.280 mm

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UFBGA132 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 90. UFBGA132 marking (package top view)

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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7.7 LQFP144 package information

Figure 91. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline

1. Drawing is not to scale.

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Table 128. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

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Figure 92. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint

1. Dimensions are expressed in millimeters.

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LQFP144 device marking

The following figures gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 93. LQFP144 marking (package top view)

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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7.8 UFBGA169 package information

Figure 94. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline

1. Drawing is not to scale.

Table 129. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-

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Table 129. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
F	0.450	0.500	0.550	0.0177	0.0197	0.0217
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 95. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint

Table 130. UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non-solder mask defined (NSMD) pads are recommended.

Note: 4 to 6 mils solder paste screen printing process.

UFBGA169 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

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Figure 96. UFBGA169 marking (package top view)

1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

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7.9 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 131. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP100 - 14 × 14mm	42	°C/W
	Thermal resistance junction-ambient UFBGA132 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm	32	
	Thermal resistance junction-ambient UFBGA144 -10 x 10 mm	53	
	Thermal resistance junction-ambient UFBGA169 - 7 × 7 mm	52	
	Thermal resistance junction-ambient WLCSP144	30.1	

7.9.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.9.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

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The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 131* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 82 °C + (42 °C/W × 447 mW) = 82 °C + 18.774 °C = 100.774 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 8: Ordering information*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 105-18.774 = 86.226 °C

Suffix 3: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 130-18.774 = 111.226 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 131* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 100 °C + (42 °C/W × 134 mW) = 100 °C + 5.628 °C = 105.628 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

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In this case, parts must be ordered at least with the temperature range suffix 3 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

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8 Ordering information

Figure 97. STM32L4P5xx ordering information scheme(1)

Example: STM32 L 4P5 V G T 6 P TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

L = ultra-low-power

Device subfamily

4P5 = STM32L4P5xx

Pin count

C = 48 pins
R = 64 pins
V = 100 pins/balls
Q = 132 balls
Z = 144 pins
A = 169 balls

Flash memory size

G = 1 Mbyte of Flash memory
E = 512 Kbytes of Flash memory

Package

I = UFBGA (7 x 7 mm)
J = UFBGA (10 x 10 mm)
T = LQFP
U = QFPN
Y = WLCSP

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

3 = Industrial temperature range, -40 to 125 °C (130°C junction)

SMPS

P = Dedicated pinout supporting external SMPS

Packing

TR = tape and reel

xxx = programmed parts

1. For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

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9 Revision history

Table 132. Document revision history

Date	Revision	Changes
xx-May-2019	0	Internal release

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