NUC976
NAND Booting Achievement

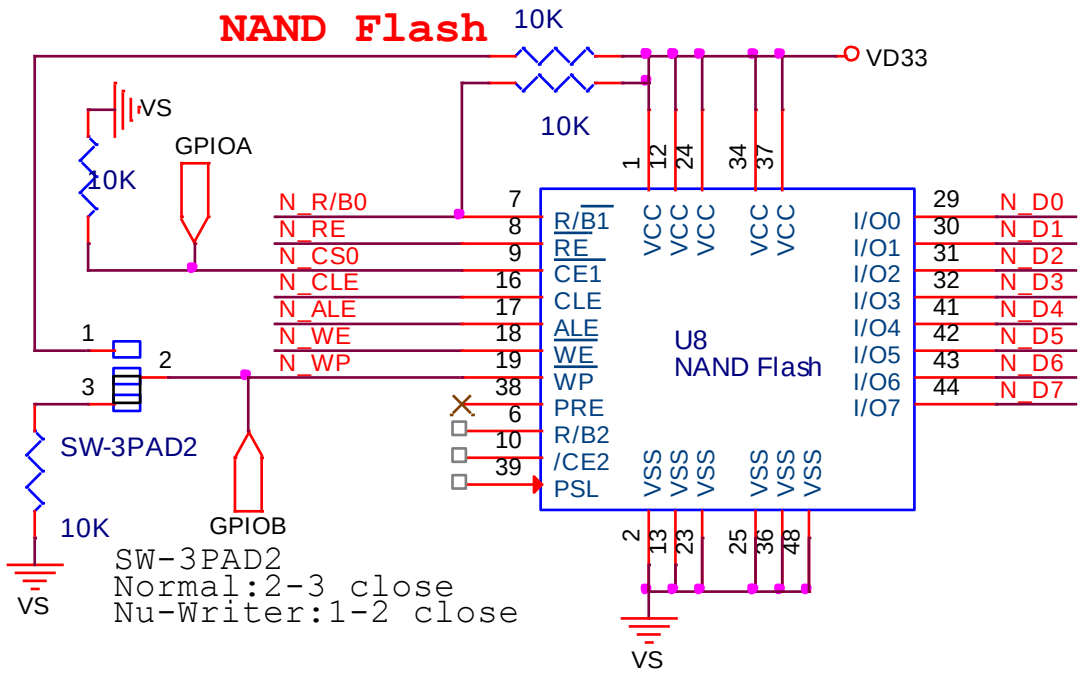
Nuvoton Technology Corp.

Original Limitation

- NUC976 by pin out limitation, it doesn't provide the NAND_CS# signal to PKG as the following table shown on. Thus, NUC976 doesn't support NAND booting directly.
- For this issue, user can use the reference CKT to overcome this limitation.(see the next pages)

PKG pin#	Pin name (DEFAULT)	2nd function	
47	Core_VDD		
48	GPI3	VCAP_CLKO	NAND_ALE
49	GPI4	VCAP_PCLK	NAND_CLE
50	GPI5	VCAP_HSYNC	NAND_nWE
51	GPI6	VCAP_VSYNC	NAND_nRE
52	GPI7	VCAP_FIELD	NAND_RDY0
53	GPI8	VCAP_DATA0	NAND_DATA0
54	GPI9	VCAP_DATA1	NAND_DATA1
55	GPI10	VCAP_DATA2	NAND_DATA2
56	GPI11	VCAP_DATA3	NAND_DATA3
57	GPI12	VCAP_DATA4	NAND_DATA4
58	GPI13	VCAP_DATA5	NAND_DATA5
59	GPI14	VCAP_DATA6	NAND_DATA6
60	GPI15	VCAP_DATA7	NAND_DATA7
61	IO_VDD		

Reference CKT



Connection mapping:

N_D0 == GPI8 ; N_R/B0 == GPI7 ; N_CS0 ➔ GPIOA (TBD)
N_D1 == GPI9 ; N_RE == GPI6 ; N_WP ➔ GPIOB (TBD)
N_D2 == GPI10 ; N_WE == GPI5
N_D3 == GPI11 ; N_CLS == GPI4
N_D4 == GPI12 ; N_ALE == GPI3
N_D5 == GPI13
N_D6 == GPI14
N_D7 == GPI15

Note. TBD, i.e. to be define, it is a option by user consideration, it can select free GPIO to implement.

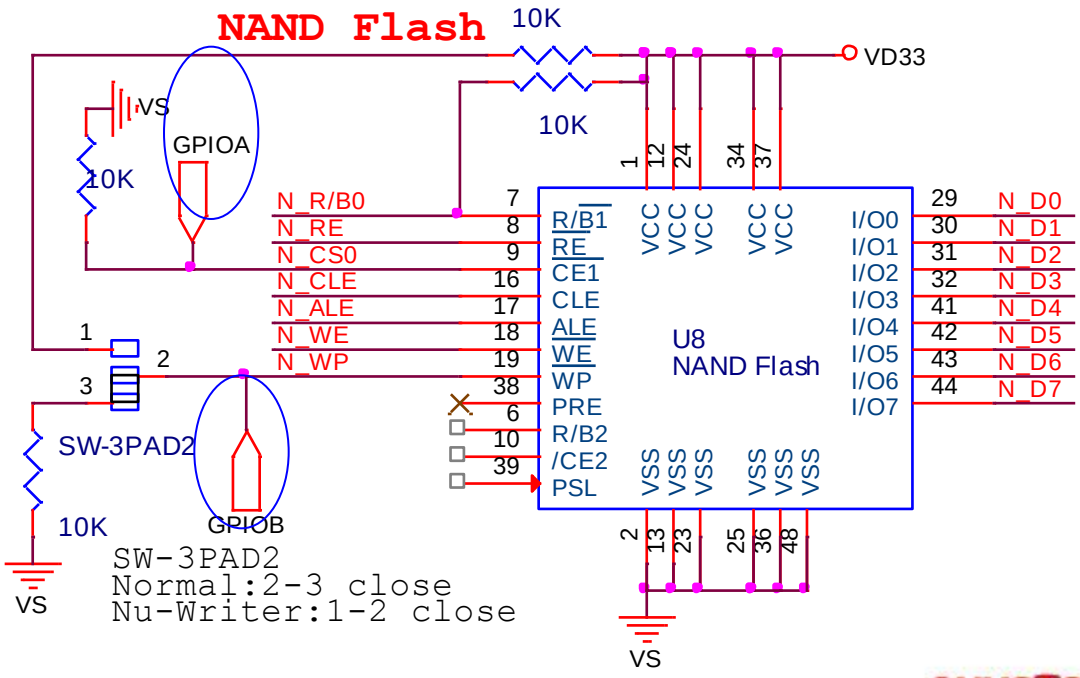
Implement Description

1. Tie a R@10K at N_CS0 to GND, it can get NAND booting for NUC976, if user want to obtain power saving advantage, then use GPIOA to push N_CS0 be high for saving power consumption when NAND entered the idle state.

2. Furthermore, as the CKT indication, close SW-3PAD2's 2-3 location which N_WP pull down with a R@10K, it can prevent un-expectation or out of control operation to get that robustness while power-on or power-off states.

3. If NAND needed to do data writing operation, user have to use GPIOB to set N_WP to be high for disabling NAND write protection.

4. For USB booting mode with Nu-Writer operation, please close the SW-3PAD's location to be 1-2, then NAND writer protection will be disable and NAND is available for programming or erasing by Nu-Writer command.



CKT simplify

If users don't have power saving and robustness concerns, then for NUC976 NAND booting CKT can be simplified as the following.