

# NUC970 VPOST H/W Application Note

April 29, 2015

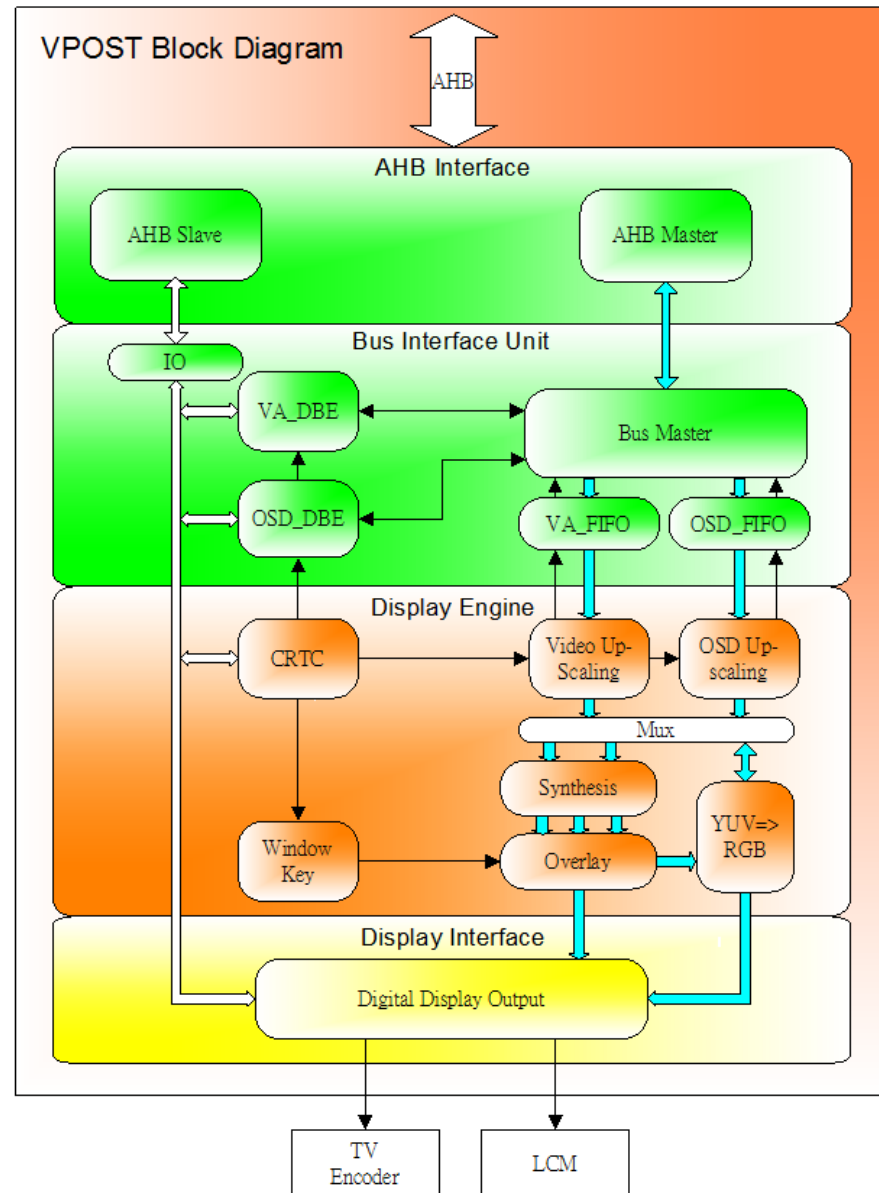
Nuvoton Technology Corp.



# Display Interface Controller (VPOST)

- Input maximum size 1024 \* 768
- The main purpose of VPOST Controller is used to display the video/image data to LCD
- The LCD controller supports both sync-type and MPU-type
- MPU supports the 8/9/16/18/24-bit data output to connect with 80/68 series MPU type LCM module

# VPOST Controller Block Diagram



# LCD interface

## SYNC & MPU mapping table

| Pad Name         | VD [23:0]           | HSYNC           | VSYNC               | VDEN             | VOCLK               |
|------------------|---------------------|-----------------|---------------------|------------------|---------------------|
| <b>Sync mode</b> | Video data bus(O)   | HSYNC(O)        | VSYNC(O)            | Data enable(O)   | Clock out (O)       |
| <b>MPU80</b>     | Video data bus(I/O) | Write (WR) (O)  | Read (RD) (O)       | MPU-LCD (RS) (O) | Chip select(CS) (O) |
| <b>MPU68</b>     | Video data bus(I/O) | Enable (EN) (O) | Read/Write (RW) (O) | MPU-LCD (RS) (O) | Chip select(CS) (O) |

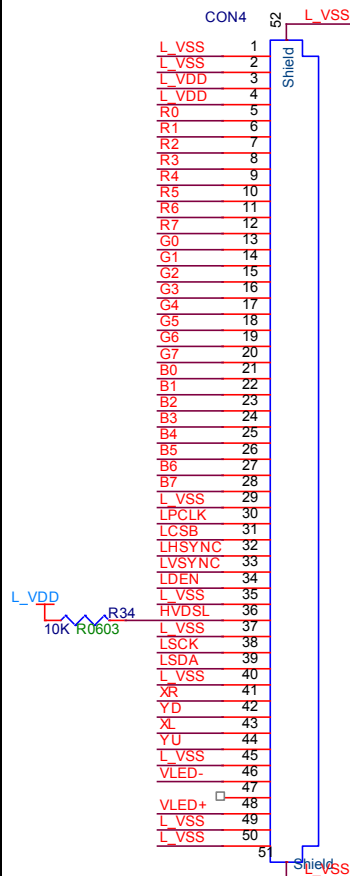
### 5.30.5.4 Display Pin Assignment

| Pad Name           | VD [23:0]           | HSYNC           | VSYNC               | VDEN             | VICLK        | VOCLK               |
|--------------------|---------------------|-----------------|---------------------|------------------|--------------|---------------------|
| <b>Sync mode</b>   | Video data bus(O)   | HSYNC(O)        | VSYNC(O)            | Data enable(O)   | Clock in (I) | Clock out (O)       |
| <b>MPU80</b>       | Video data bus(I/O) | Write (WR) (O)  | Read (RD) (O)       | MPU-LCD (RS) (O) | Non used     | Chip select(CS) (O) |
| <b>MPU80+VSync</b> | Video data bus(I/O) | Write (WR) (O)  | Read (RD) (O)       | MPU-LCD (RS) (O) | Vsync (O)    | Chip select(CS) (O) |
| <b>MPU80+FMARK</b> | Video data bus(I/O) | Write (WR) (O)  | Read (RD) (O)       | MPU-LCD (RS) (O) | FMARK (I)    | Chip select(CS) (O) |
| <b>MPU68</b>       | Video data bus(I/O) | Enable (EN) (O) | Read/Write (RW) (O) | MPU-LCD (RS) (O) | Non used     | Chip select(CS) (O) |
| <b>MPU68+VSync</b> | Video data bus(I/O) | Enable (EN) (O) | Read/Write (RW) (O) | MPU-LCD (RS) (O) | Vsync (O)    | Chip select(CS) (O) |
| <b>MPU68+FMARK</b> | Video data bus(I/O) | Enable (EN) (O) | Read/Write (RW) (O) | MPU-LCD (RS) (O) | FMARK (I)    | Chip select(CS) (O) |

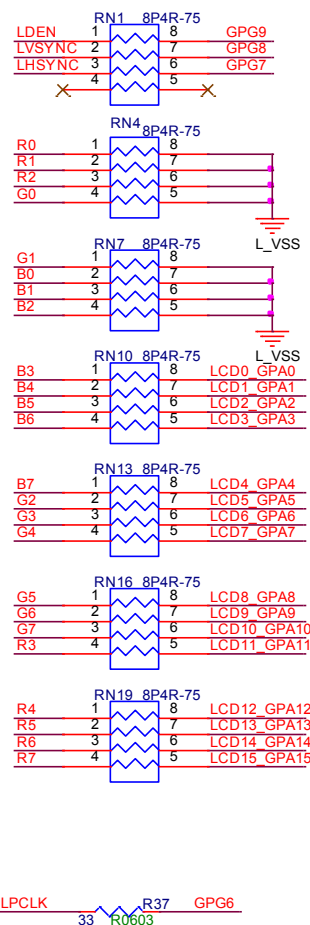
# RGB 565/ RGB666/ RGB888 option for LCD

## DIGITLA RGB 565/666/888 INTERFACE OPTION

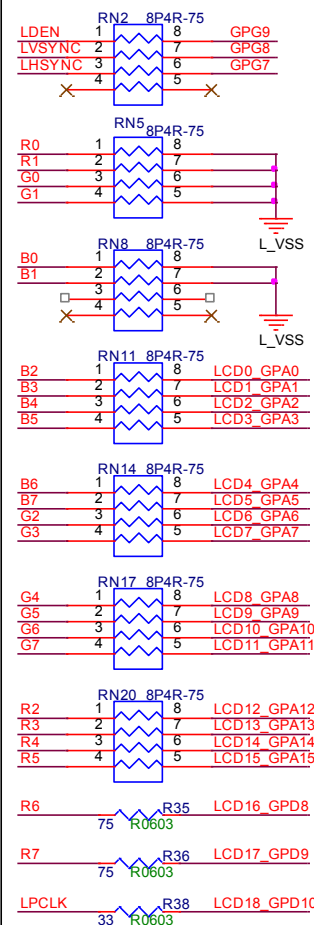
### TFT\_LCD 24-bit FPC CON



### RGB 5/6/5



### RGB 6/6/6



### RGB 8/8/8

