Power Consumption Report

Part No.	**NUC972DF62Y**
IC Version	**(HAD008B)**
Function	**ARM926EJ-S Based 32-bit Micro Processor**
Report Date	**4/02/2015**

Revision History

Revision	Date	Comments
Rev. 1.0	04/02/2015	1st version
Rev. 1.1	07/13/2015	Updated USB core power

Outline:

一、 Product general description

二、 Overview

三、 Electrical characteristics

四、 Power Consumption Measurement

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Table of Contents-

1. PRODUCT GENERAL DESCRIPTION

NUC970 series provides four power management scenarios, including Power-down, Deep standby mode, CPU standby mode and Normal Operating modes, to manage the power consumption. The peripheral clocks can be enabled / disabled individually by controlling the corresponding bit in CLKSEL control register. User can turn-off the unused modules' clock for power saving.

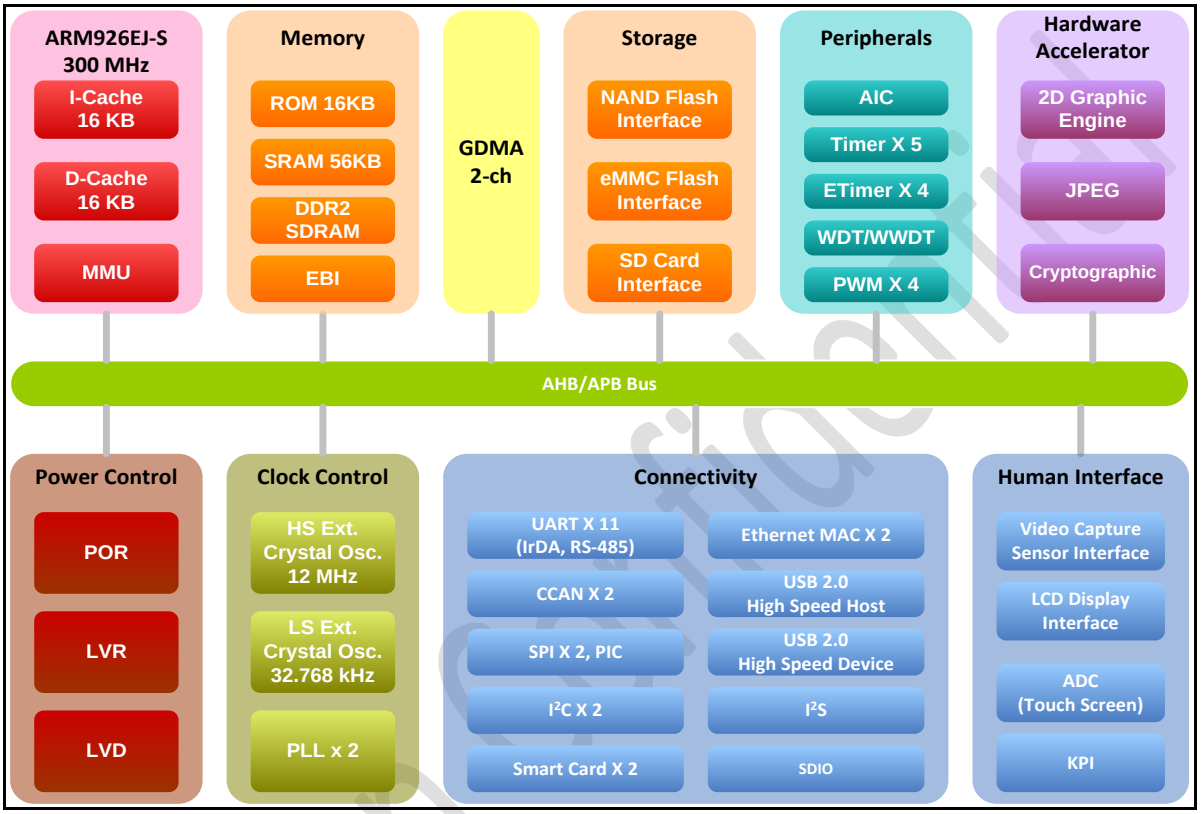
- Normal Operating mode, CPU run normally and all clocks on
  - In this mode, CPU run normally and clocks of all functionalities are on. The clock frequency of CPU, DRAM, AHB peripherals and APB peripherals are 300 MHz, 150 MHz, 150 MHz and 75 MHz, respectively.
- CPU Standby Mode, CPU clock stop, and all other clocks on.
  - When CPU is not busy, user can put ARM926EJ-S processor into a low-power state by the wait for interrupt instruction.This instruction switches the ARM926EJ-S processor into a low-power state until either an interrupt (IRQ or FIQ) or a debug request occurs.
  - In this mode, the clocks of all functionalities are on. The clock frequency of DRAM, AHB peripherals and APB peripherals are 150 MHz, 150 MHz and 75 MHz.
- Deep Standby Mode, all clocks stop, except LXT, with SRAM retention and DRAM entered self-refresh mode.
  - To reduce power consumption further, user could put the chip into deep standby mode. In this mode, all clocks stop, (except LXT Crystal 32.768 kHz) with SRAM retention.
  - The mechanisms shown below could wake chip up from Power-down mode:
    - EINT, External Interrupt, pin toggled.
    - UART 1/2/4/6/8/10 CTS toggled.
    - EMAC 0 or EMAC 1 received a Magic Packet.
    - USB device controller detected a VBUS valid event.
    - USB host controller detected connect/dis-connect/remote-wakeup event.
    - Touch screen touching or Keypad pressing detected by ADC controller.
    - Key pressing or releasing detected by KPI, Keypad Interface.
    - RTC alarm or relative alarm interrupt is generated.
    - Enhanced Timer interrupt is active.
    - WDT time-out wake-up.
- Power-down mode, all powers are off except RTC_VDD (3.3V).
  - To extremely reduce the power consumption, user could put the chip inot Power-down mode without SRAM retention by turning off power supply to all power pin except RTC_VDD.
  - In this mode, only RTC circuit and LXT Crystal 32.768 kHz keep active.

2. OVERVIEW

2.1 Chip features configuration:

Items	**NUC972DF62Y**
CPU	ARM926EJ-S
Speed(MHZ)	300MHZ@1.2V;
SPI	2
PWM	4
I2C	2
UART	11
12-bit SARADC	2 (AIN, BAT_DET, 4-W/5-W Touch)
EMMC	1
GPIO	146
SD/SDIO	2
NAND interface	1
USB Device	1 (USB 2.0)
USB Host	2 (USB 2.0)
LCD BUS	RGB 24/18/16/8-bit
Video in	CMOS sensr interface x1
RTC	external 32K crystal
Ethernet MAC (RMII)	2
I2S BUS	1
CAN BUS	2
JTAG	1
ISO-7816-3 (SIM security)	2
EBI BUS	Support
KPI	Support
PKG type	LQFP216

2.2 NUC970 Internal Block Diagram



3. ELECTRICAL CHARACTERISTICS

3.1 Test conditions

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Core Operation voltage	V_{CORE_VDD}	1.14	1.2	1.26	V	
I/O Operation Voltage	V_{IO_VDD}	2.97	3.3	3.63	V	
DDR I/O Operation Voltage	V_{DDR_VDD}	1.70	1.8	1.90	V	
Power Ground	V_{SS} AV_{SS}	-0.3			V	
Analog Operating Voltage	AV_{DD}	2.97	3.3	3.63	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Current Consumption of Normal Operating Mode 1	I_{CORE_VDD1}		185		mA	Frequency of CPUCLK/DDR_CLK is 300/150 MHz. The functionalities enabled are GE2D, LCD, JPEG, Cryptographic Engine, EMAC, USBD, USBH and UART.
	I_{DDR_VDD1}		50		mA	
	I_{USBPLL_VDD1}		15		mA	
	I_{USB0_VDD1}		35		mA	
	I_{USB1_VDD1}		35		mA	
	I_{RTC_VDD1}		100		uA	
Current Consumption of Normal Operating Mode 2	I_{CORE_VDD2}		165		mA	Frequency of CPUCLK/DDR_CLK is 264/132 MHz. The functionalities enabled are GE2D, LCD, JPEG, Cryptographic Engine, EMAC, USBD, USBH and UART.
	I_{DDR_VDD2}		45		mA	
	I_{USBPLL_VDD2}		15		mA	
	I_{USB0_VDD2}		35		mA	
	I_{USB1_VDD2}		35		mA	
	I_{RTC_VDD2}		100		uA	

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Current Idle Mode	$I_{IDLE\_CORE\_VDD1}$		TBD		mA	Frequency of CPUCLK/DDR_CLK is 300/150 MHz. Clock of all functionalities are ON, and CPU is in idle mode.
	$I_{IDLE\_DDR\_VDD1}$		6		mA	
	$I_{IDLE\_IO\_VDD1}$		3.5		mA	
	$I_{IDLE\_CORE\_VDD2}$		6		mA	Frequency of CPUCLK/DDR_CLK is 300/150 MHz. Clock of all functionalities are OFF, and CPU is in idle mode.
	$I_{IDLE\_DDR\_VDD2}$		6		mA	
	$I_{IDLE\_IO\_VDD2}$		3.5		mA	
Standby Current Power Down Mode	I_{PWD1}		3		mA	V_{CORE_VDD} = 1.2V
	I_{PWD2}		6		mA	V_{DDR_VDD} = 1.8V
	I_{PWD3}		5		µA	V_{IO_VDD} = 3.3V
	I_{PWD4}		0		µA	V_{USB0_VDD} = 3.3V
	I_{PWD5}		0		µA	V_{USB1_VDD} = 3.3V
	I_{PWD6}		5		µA	$V_{USBPLL0\_VDD}$ = 1.2V
	I_{PWD7}		5		µA	$V_{USBPLL1\_VDD}$ = 1.2V
	I_{PWD8}		25		µA	V_{AVDD} = 3.3V
	I_{PWD9}		10		µA	V_{RTC_VDD} = 3.3V
Input Leakage Current PA, PB, PC, PD, PE, PF, PF, PH, PI, PJ	I_{LK1}	-10	-	10	µA	V_{IO_VDD} = 3.63V 0V < V_{IN} < 3.6V
Input Leakage Current with Pull-Down Resistor on PA, PB, PC, PD, PE, PF, PF, PH, PI, PJ	I_{LK2}	40	-	160	µA	V_{IN} = V_{IO_VDD}
Input Leakage Current with Pull-Up Resistor on PA, PB, PC, PD, PE, PF, PF, PH, PI, PJ	I_{LK3}	-160	-	40	µA	V_{IN} = 0
Input Low Voltage PA, PB, PC, PD, PE, PF, PF, PH, PI, PJ (TTL input)	V_{IL1}	-	-	0.8	V	
Input High Voltage PA, PB, PC, PD, PE, PF, PF, PH, PI, PJ (TTL input)	V_{IH1}	2.0	-	-	V	

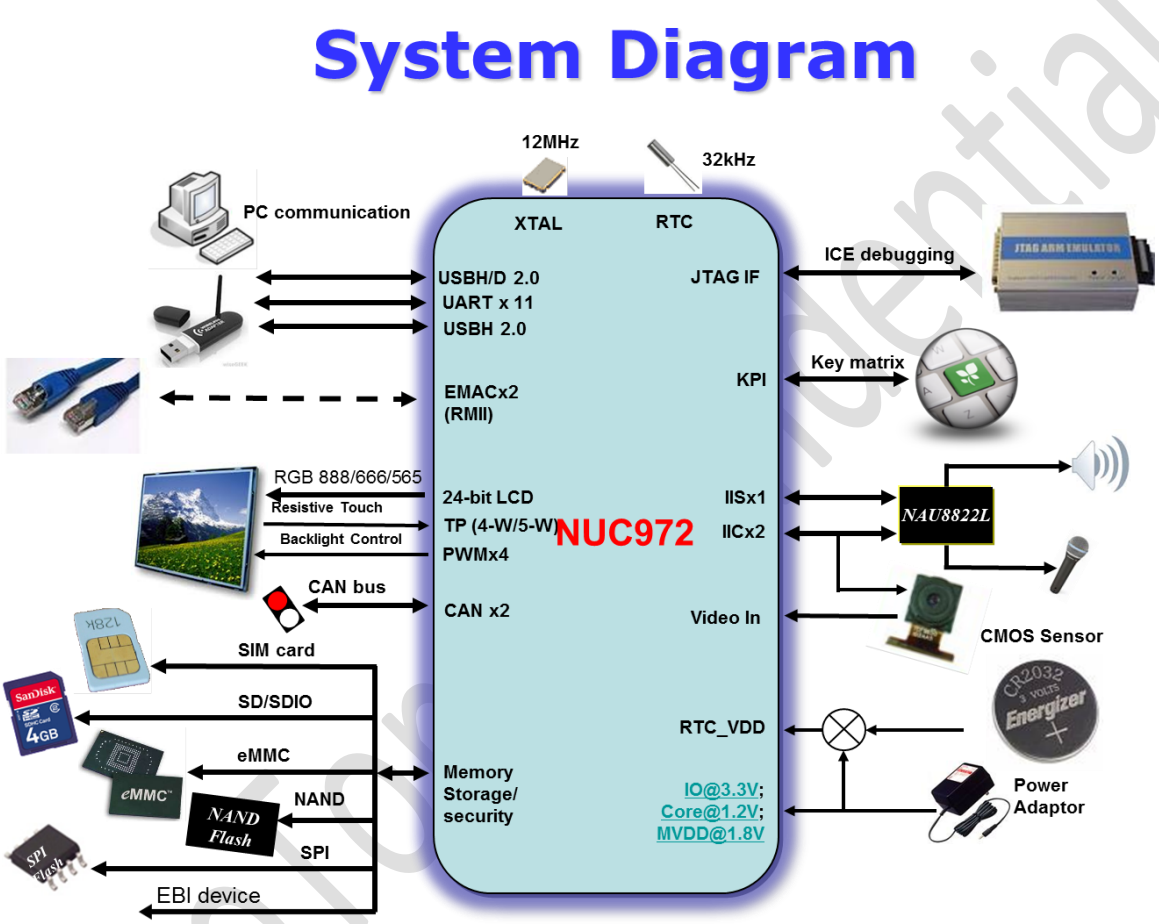
PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Low Voltage PA, PB, PC, PD, PE, PF, PF, PH, PI, PJ (Schmitt input)	V_{IL2}	0.9	1.05	1.2	V	
Input High Voltage PA, PB, PC, PD, PE, PF, PF, PH, PI, PJ (Schmitt input)	V_{IH2}	1.65	1.9	2.1	V	
Hysteresis voltage PA, PB, PC, PD, PE, PF, PF, PH, PI, PJ (Schmitt input)	V_{HY}	0.75	0.85	0.9	V	
Negative going threshold (Schmitt input), nRESET	V_{ILS}	0.75	-	0.9	V	
Positive going threshold (Schmitt input), nRESET	V_{IHS}	1.65	-	2.1	V	
Source Current PA, PB, PC, PD, PE, PF, PH, PI, PJ (Push-pull Mode)	I_{SR21}	8	-	28	mA	
Sink Current PA, PB, PC, PD, PE (Push-pull Mode)	I_{SK1}	8	-	18	mA	
Input Pull-up Resistance PA, PB, PC, PD, PE, PF, PF, PH, PI, PJ	R_{PU}	45	53	82	kΩ	V_{IN} = 0
Input Pull-down Resistance PA, PB, PC, PD, PE, PF, PF, PH, PI, PJ	R_{PD}	37	49	91	kΩ	V_{IN} = V_{IO_VDD}
Input Pull-up Resistance nRESET	R_{RST}	45	53	85	kΩ	

Note:

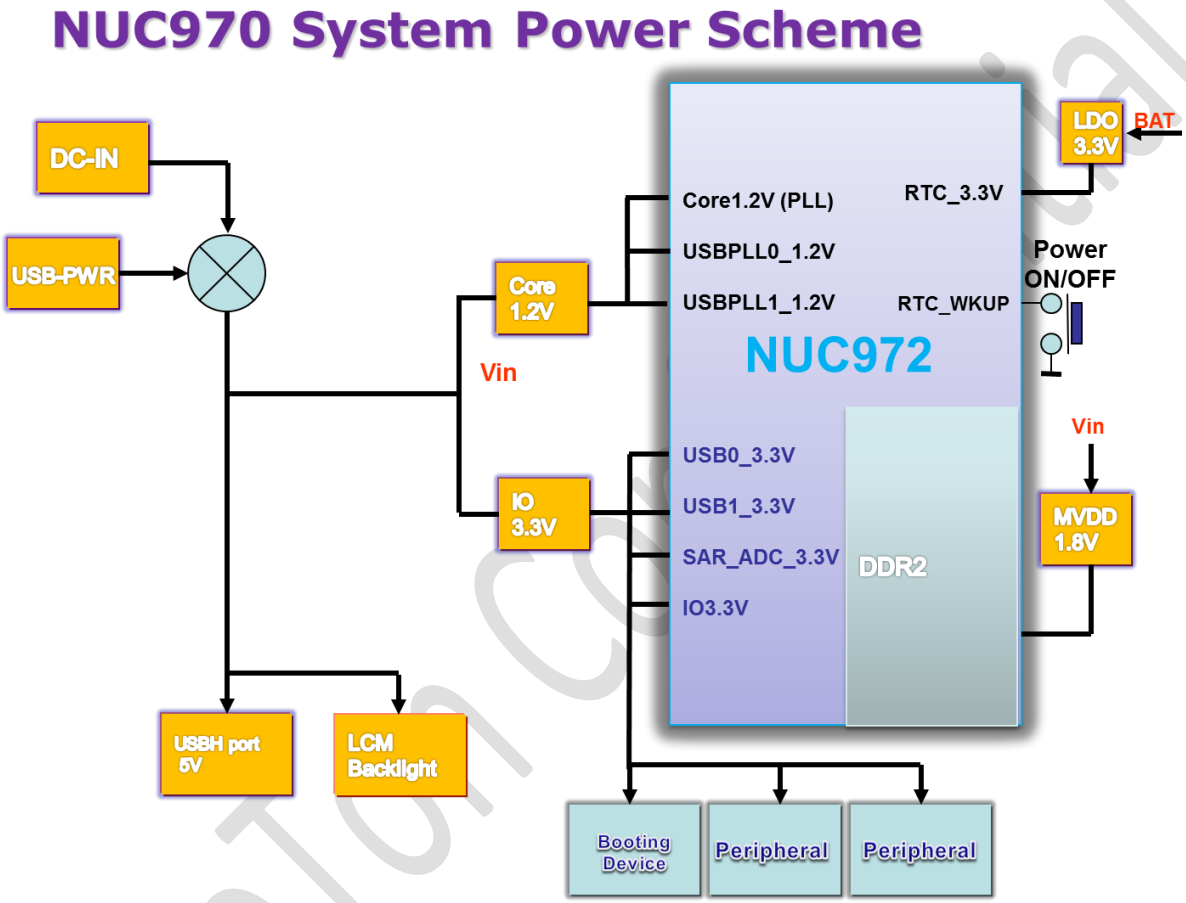
1. nRESET pin is a Schmitt trigger input.

2. Pins of PA, PB, PC, PD, PE, PF, PG, PH, PI and PJ can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=3.63 V, the transition current reaches its maximum value when V_{IN} approximates to 1.5 V.

3.2 System Block Architecture:



3.3 Power Measuement Points:



4. POWER CONSUMPTION MEASUREMENT

4.1 AHB BUS IP Current:

Test Condition

1. **Platform: NUC972 EV-Board**
2. **External clock: 12MHz Crystal**
3. **CPU clock: 300MHz**
4. **HCLK clock: 150MHz**
5. **APB clock: 37.5MHz**
6. **Temperature: 25 ℃**

IP Current Measured at CORE_VDD (VCC1.2V)

IP name	Sample#1 (uA)	Sample#2 (uA)	Sample#3 (uA)	Avg. (uA)	Max. (uA)
PIC	370	382	379	377	382
SRAM	22	10	3	12	22
EBI	48	18	12	26	48
DRAM	39	8	7	18	39
GDMA	967	967	964	966	967
CKO	68	34	31	44	68
EMAC0	2147	2218	2191	2185	2218
EMAC1	2002	2046	2016	2021	2046
USBH	3260	3390	3347	3332	3390
USBD	2685	2773	2890	2783	2890
FMI	1536	1561	1666	1588	1666
NAND	1100	1093	1201	1131	1201
eMMC	133	78	191	134	191
CRYPTO	4790	4995	5102	4962	5102
I2S	1620	1641	1744	1668	1744
LCD	2191	2240	2340	2257	2340
VCAP	2836	2947	3059	2947	3059
SENSOR	57	26	129	71	129
GE2D	2695	2812	2919	2809	2919
JPEG	10945	11367	11447	11253	11447
SDH	55	18	120	64	120
WDT	231	194	307	244	307

WWDT	243	210	301	251	301
RTC	207	196	391	265	391
GPIO	2792	2985	3077	2951	3077
ETIMER0	99	188	244	177	244
ETIMER1	105	193	259	186	259
ETIMER2	92	244	243	193	244
ETIMER3	99	248	248	198	248
TIMER0	131	260	276	222	276
TIMER1	117	235	250	201	250
TIMER2	91	213	252	185	252
TIMER3	160	253	287	233	287
TIMER4	176	221	257	218	257
UART0	22	63	104	63	104
UART1	535	600	631	589	631
UART2	581	660	699	647	699
UART3	400	468	512	460	512
UART4	550	616	653	606	653
UART5	455	492	542	496	542
UART6	606	647	716	656	716
UART7	430	484	543	486	543
UART8	530	611	642	594	642
UART9	525	518	567	537	567
UART10	546	596	637	593	637
I2C0	227	253	297	259	297
I2C1	220	248	297	255	297
SPI0	221	255	301	259	301
SPI1	167	198	246	204	246
CAN0	450	505	552	502	552
CAN1	510	560	597	556	597
SMC0	463	507	557	509	557
SMC1	525	583	629	579	629
ADC	293	344	401	346	401
KPI	351	402	452	402	452
MTPC	190	235	283	236	283

PWM	383	451	500	445	500

Note. Test Code: PWR.BIN

4.2 Normal Operation Mode Current:

Test Condition:
Whole Chip Operting Current: (dataflow test program, turn on GE2D, LCD, JPEG, Cryptographic Engine, EMAC, USBD, USBH and UART1-10 engines for loop test)

1. **Platform: NUC972 EV-Board**
2. **External clock: 12MHz Crystal**
3. **CPU clock: 264MHz**
4. **HCLK clock: 132MHz**
5. **APB clock: 66MHz**
6. **Cache On**
7. **Temperature: 25 ℃**

	Sample#1	Sample#2	Sample#3
RTC_3.3V	94.3uA	91.4uA	93.4uA
MVDD_1.8V	11~38mA	11~39mA	11~39mA
CORE_1.2V+PLL_1.2V	99~157mA	97~154mA	99~157mA
USBPLL0_1.2V	6.67mA	6.7mA	6.83mA
USBPLL1_1.2V	6.67mA	6.7mA	6.83mA
USB0_3.3V	27.84mA	29.85mA	30.1mA
USB1_3.3V	31.76mA	29.96mA	30.4mA
IO_3.3V	5.3mA	5.3mA	5.3mA

Test Condition:
Whole Chip Operting Current: (dataflow test program, turn on GE2D, LCD, JPEG, Cryptographic Engine, EMAC, USBD, USBH and UART1-10 engines for loop test)

1. **Platform: NUC972 EV-Board**
2. **External clock: 12MHz Crystal**
3. **CPU clock: 300MHz**
4. **HCLK clock: 150MHz**
5. **APB clock: 75MHz**
6. **Cache On**
7. **Temperature: 25 ℃**

	Sample#1	Sample#2	Sample#3
RTC_3.3V	93.8uA	90.9uA	94.2uA
MVDD_1.8V	12~42mA	11~42mA	11~41mA

CORE_1.2V+PLL_1.2V	112~176mA	108~174mA	108~171mA
USBPLL0_1.2V	6.67mA	6.35mA	6.81mA
USBPLL1_1.2V	6.67mA	6.35mA	6.81mA
USB0_3.3V	27.9mA	30.8mA	30.1mA
USB1_3.3V	32.0mA	30.2mA	30.4mA
IO_3.3V	5.3mA	5.3mA	5.3mA

4.3 Standardby Mode Power Current:

Test Condition:

1. **Platform: NUC972 EV-Board**
2. **External clock: 12MHz Crystal**
3. **CPU clock: 264MHz**
4. **HCLK clock: 132MHz**
5. **APB clock: 66MHz**
6. **Cache On**
7. **Temperature: 25 ℃**

	CPUCLK/HCLK 264/132 MHz	IO3.3V(mA)	MVDD1.8V(mA)	CORE1.2V(mA)
ES#1	Enable all of IP and entry while(1)	5.36	50.56	63.62
	Except CPU & DDR On and entry while(1), all IP Off	5.35	48.92	33.65
	Enable all IP and DRAM enter self-refresh mode, CPU off	2.42	3.98	63.3
	Disable all IP and CPU Off & DDR enter self-refresh mode	2.42	3.98	4.75
ES#2	Enable all of IP and entry while(1)	5.22	50.18	63.18
	Except CPU & DDR On and entry while(1), all IP Off	5.21	48.71	33.19
	Enable all IP and DRAM enter self-refresh mode, CPU off	2.28	2.18	62.8
	Disable all IP and CPU Off & DDR enter self-refresh mode	2.28	2.18	4.41
ES#3	Enable all of IP and entry while(1)	5.26	50.79	63.21
	Except CPU & DDR On and entry while(1), all IP Off	5.26	49.3	33.31
	Enable all IP and DRAM enter self-refresh mode, CPU off	2.33	2.75	62.9
	Disable all IP and CPU Off & DDR enter self-refresh mode	2.33	2.75	4.83

Test Condition:

1. **Platform: NUC972 EV-Board**
2. **External clock: 12MHz Crystal**
3. **CPU clock: 300MHz**
4. **HCLK clock: 150MHz**
5. **APB clock: 75MHz**
6. **Cache On**

7. Temperature: 25 ℃

	CPUCLK/HCLK 300/150 MHz	IO3.3V(mA)	MVDD1.8V(mA)	CORE1.2V(mA)
ES#1	Enable all of IP and entry while(1)	5.36	53.89	65.45
	Except CPU & DDR On and entry while(1), all IP Off	5.35	52.32	36.12
	Enable all IP and DRAM enter self-refresh mode, CPU off	2.43	4	65.17
	Disable all IP and CPU Off & DDR enter self-refresh mode	2.43	4	4.82
ES#2	Enable all of IP and entry while(1)	5.2	53.64	65.76
	Except CPU & DDR On and entry while(1), all IP Off	5.2	52.1	35.71
	Enable all IP and DRAM enter self-refresh mode, CPU off	2.28	2.19	65.14
	Disable all IP and CPU Off & DDR enter self-refresh mode	2.28	2.18	4.47
ES#3	Enable all of IP and entry while(1)	5.27	54.5	65.71
	Except CPU & DDR On and entry while(1), all IP Off	5.27	52.94	35.77
	Enable all IP and DRAM enter self-refresh mode, CPU off	2.33	2.76	65.38
	Disable all IP and CPU Off & DDR enter self-refresh mode	2.33	2.76	4.88

4.4 Deep Standby Mode Current:

Deep standby mode current (After SYS_PWREN)

	Sample#1	Sample#2	Sample#3	Unit
IO_3.3V	3.2	3.6	3.7	uA
AVDD_3.3V	23	23	23	µA
USB0_3.3V	0	0	0	µA
USB1_3.3V	0	0	0	uA
Core1.2V	2.65	2.54	3.21	mA
USBPLL0_1.2V	8.59	3.99	4.43	µA
USBPLL1_1.2V	8.59	3.99	4.43	uA
MVDD_1.8V	2.79	2.13	2.16	mA

4.5 Power Down Mode Current:

Power down mode current (Before SYS_PWREN) (System Off, RTC powered only)

	Sample#1	Sample#2	Sample#3	Unit
RTC_3.3V	7.44	7.24	7.28	µA

4.6 Application Current

Test Condition:

Set GP-F & GPE port as RMII interface for ping test with Ethernet PHY

1. **Platform: NUC972 DEV-Board**
2. **External clock: 12MHz Crystal**
3. **CPU clock: 300MHz**
4. **HCLK clock: 150MHz**
5. **APB clock: 75MHz**
6. **Cache On**
7. **Temperature: 25 ℃**

	Core1.2V (AVG.)	MVDD1.8V (Max.)	IO_3.3V
EMAC0 (GPF0 ~ GPF9) only	70.7mA	53.2mA	5.3mA
EMAC1 (GPE2 ~ GPE11) only	70.5mA	53.2mA	5.3.mA
EMAC0 & EMAC1 rotation ON	73.3mA	53.2mA	5.3.mA
EMAC0 & EMAC1 concurrently	83.9mA	52.9mA	5.3mA

Note. AVDD_3.3V & USB0 & USB1 power current can be ignored by IP disable