we innovate
nuvoTon

NUC976/977 Thermal Report

July 28, 2015

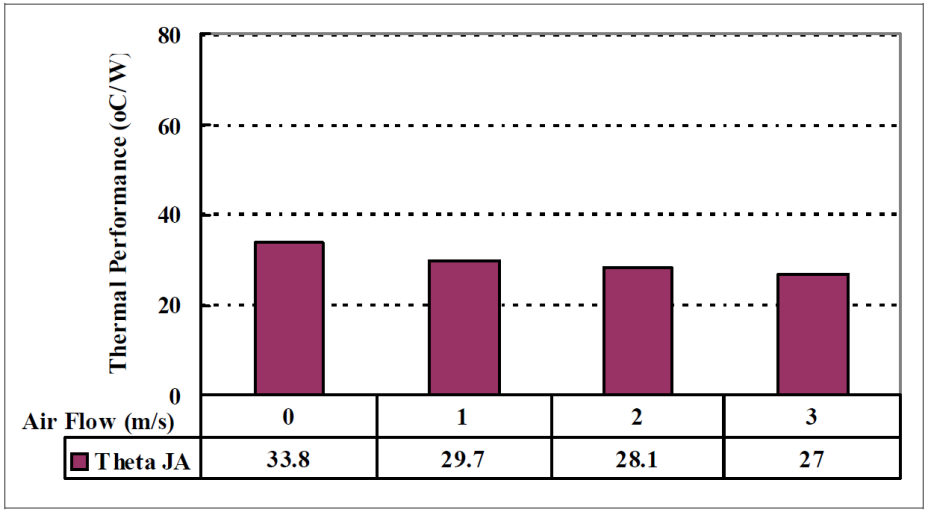
Nuvoton Technology Corp.

Introduction

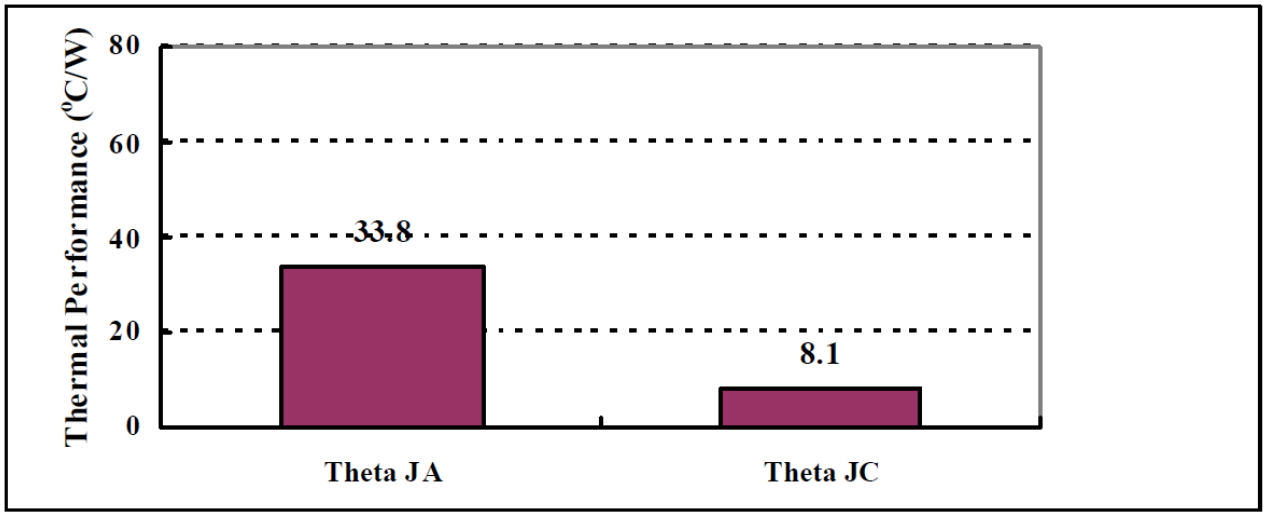
- In this report, we present the thermal characteristic for 128-pin Low-Profile Quad Flat Packages with stack die (SLQFP 128) mounted on 4-layer PCB using the Finite Element Modeling (FEM) method.

- The junction-to-ambient thermal resistance is utilized to evaluate thermal performance for this package and then to predict the power dissipation capability by given ambient and maximum junction temperatures.

Result Summaries



Thermal Performance of SLQFP under Forced Convection



Thermal Performance of SLQFP under Natural Convection

Conclusion

- From the simulation results, we can obtain the chip junction temperatures (T_J) and the case temperatures (T_C).
- Since the input power (P) and ambient temperature (T_A) are controlled variables, we can calculate the shown above thermal resistance of θ_{JA} according to $\theta_{JA} = (TJ - TA)/P$
- Assuming ambient temperature of 65℃ and maximum junction temperature of 125 ℃, we can predict the power dissipation capability of this package as below table:

Air Flow (m/s)	0	1	2	3
Power Dissipation (watt)	1.78	2.02	2.14	2.22

Assembly Condition

Package	Type		128-pin SLQFP
	Device Name		NUC976DK62Y/ NUC977DK62Y
	L/F Drawing No.		L37527 Rev.C
	Dimension (L x W)		14 x 14 mm^2
	Chip Size	Top die	4.47 x 5.2 x 0.1524 mm (176 x 204 x 6 mil)
		Bottom die	5.37 x 4.08 x 0.1524 mm (211 x 160 x 6 mil)
	Die Pad Size		7.92 x 7.58 mm^2 (312 x 298 mil^2)
	Thickness		1.4 mm
	Die Attached Thickness		0.0254 mm
PCB	PCB Dimension (L x W)		3” x 4.5”
	PCB Thickness		1.6 mm
	Number of Cu Layer-PCB		4 layers

Thermal Modeling Method

A. Simulation Conditions

Input Power	Top die: 0.6 W Bottom die: 0.6W
Test Board (PCB)	4 layers
Control Condition	Air Flow = 0,1, 2, 3 m/s

B. Material Property

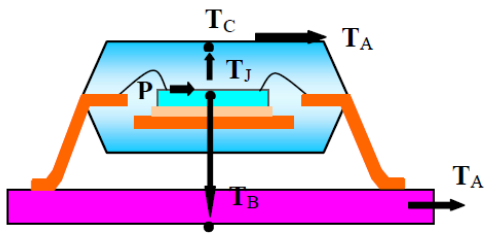
Item		Material	Thermal Conductivity K (w/m-k)
Package	Die	Silicon	147
	Lead Frame	CDA7025	168
	Silver Paste	1033BF	1.0
	Mold Compound	G631	0.9
PCB		FR4	0.2
		Cu	400

Appendix -Terminology

- ***TJ*: the maximum junction temperature;**
- ***TA*: the ambient or environment temperature;**
- ***TC*: the top center of compound surface temperature;**
- ***TB*: the bottom center of PCB surface temperature;**
- ***P*: total input power**

1. Junction to ambient thermal resistance, θ_{JA}, **defined as:**

$$\theta_{JA} = \frac{T_J - T_A}{P} \; ; \qquad (1)$$

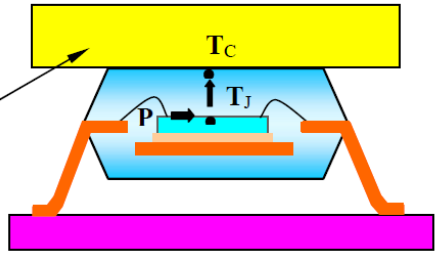


Thermal Dissipation of LQFP package

2 .Junction to case thermal resistance, θ_{JC}, **defined as:**

$$\theta_{JC} = \frac{T_J - T_C}{P} \; ; \qquad (2)$$

Attach a block with constant temperature onto package.



Estimation for Typical 4-Layers PCB

Item	Volt	Current (mA)	Power (mW)	T_J @ 4-layer PCB (℃)						
				Incease	T_A = 25℃	T_A = 40℃	T_A = 50℃	T_A = 60℃	T_A = 70℃	T_A =85℃
IO	3.3	10.0	33.0	1.1	45.4	60.4	70.4	80.4	90.4	105.4
Core	1.2	185.0	222.0	7.5						
SARADC	3.3	3.0	9.9	0.3						
USBPLL	1.2	15.0	18.0	0.6						
USBH0_2.0	3.3	35.0	115.5	3.9						
USBH1_2.0	3.3	35.0	115.5	3.9						
DDR2	1.8	50.0	90.0	3.0						
Total	-	-	**603.9**	**20.4**						
Tc, PKG Surface temperature					40.5	55.5	65.5	75.5	85.5	100.5
ΘA=	**33.8**									
ΘC=	**8.1**									

$\theta JA = (TJ - TA)/P$ θJC =(TJ – TC)/ P

Note. Test program, NUC970 dataflow.BIN