ARM® ARM926EJ-S Based
32-bit Microprocessor

NUC970 Series
Product Brief

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www.nuvoton.com

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1 GENERAL DESCRIPTION

The NUC970 series targeted for general purpose 32-bit microcontroller embeds an outstanding CPU core ARM926EJ-S, a RISC processor designed by Advanced RISC Machines Ltd., runs up to 300 MHz, with 16 KB I-cache, 16 KB D-cache and MMU, 56KB embedded SRAM and 16 KB IBR (Internal Boot ROM) for booting from USB, NAND and SPI FLASH.

The NUC970 series integrates two 10/100 Mb Ethernet MAC controllers, USB 2.0 HS HOST/Device controller with HS transceiver embedded, TFT type LCD controller, CMOS sensor I/F controller, 2D graphics engine, DES/3DES/AES crypto engine, I^2S I/F controller, SD/MMC/NAND FLASH controller, GDMA and 8 channels 12-bit ADC controller with resistance touch screen functionality. It also integrates UART, SPI/MICROWIRE, I^2C, CAN, LIN, PWM, Timer, WDT/Windowed-WDT, GPIO, Keypad, Smart Card I/F, 32.768 KHz XTL and RTC (Real Time Clock).

In addition, the NUC970 series integrates a DRAM I/F, that runs up to 150MHz with supporting DDR or DDR2 type SDRAM, and an External Bus Interface (EBI) that supports SRAM and external device with DMA request and ack.

2 FEATURES

2.1 NUC970 Series Features

- Core
  - ARM® ARM926EJ-S™ processor core runs up to 300 MHz
  - Support 16 KB instruction cache and 16 KB data cache
  - Support MMU
  - Support JTAG Debug interface
- External Bus Interface (EBI)
  - Support SRAM and external I/O devices
  - Support 8/16-bit data bus width
  - Support up to five chip selects for SRAM and external I/O devices
  - Support programmable access cycle
  - Support four 32-bit write buffers
- DDR SDRAM Controller
  - Support DDR and DDR2 SDRAM
  - Clock speed up to 150 MHz
  - Support 16-bit data bus width
  - Memory size depended on embedded SDRAM configuration by different part number.
- Embedded SRAM and ROM
  - Support 56K bytes embedded SRAM
  - Support 16K bytes Internal Boot ROM (IBR)
  - Support up to four booting modes
  - Boot from USB
  - Boot from eMMC
  - Boot from NAND Flash
  - Boot from SPI Flash
- Clock Control
  - Support two PLLs, up to 500 MHz, for high performance system operation
  - External 12 MHz high speed crystal input for precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low speed clock source
- Ethernet MAC Controller
  - Support up to 2 Ethernet MAC controllers
  - Support IEEE Std. 802.3 CSMA/CD protocol
  - Support packet time stamping for IEEE Std. 1588 protocol
  - Support 10 and 100 Mbps operations
  - Support Half- and Full-duplex operations
  - Support RMII interface to Ethernet physical layer PHY
  - Support Ethernet physical layer PHY management through MDC and MDIO interface
  - Support flow control in Full-duplex mode to receive, recognize and transmit PAUSE frame
  - Support CAM-like function to recognize 48-bit Ethernet MAC address
  - Support Wake-On-LAN by detecting Magic Packet
  - Support 256 bytes transmit FIFO and 256 bytes receive FIFO
  - Support DMA function
  - Support internal loop back mode for diagnostic
- USB 2.0 Controller
  - Support USB Revision 2.0 specification
  - Support one set of USB 2.0 High-Speed (HS) Device/Host with embedded transceiver

- Support one set of USB 2.0 High-Speed (HS) Host with embedded transceiver
- Support Control, Bulk, Interrupt, Isochronous and Split transfers
- Support USB host function compliant to Enhanced Host Controller Interface (EHCI) 1.0 specification to connect with USB 2.0 High-Speed (HS) device.
- Support USB host function compliant to Open Host Controller Interface (OHCI) 1.0 specification to connect with USB 1.1 Full-Speed (FS) and Low-Speed (LS) devices
- Support USB High-Speed (HS) and Full-Speed (FS) device function
- Support USB device function with 1 endpoint for Control IN/OUT transfers and 12 programmable endpoints for Bulk, Interrupt and Isochronous IN/OUT transfers
- Support suspend, resume and remote wake-up capability
- Support DMA function
- Support 2048 Bytes internal SRAM for USB host function and 4096 Bytes internal SRAM for USB device function

- Flash Memory Interface
  - Support NAND flash interface
  - Support 8-bit data bus width
  - Support SLC and MLC type NAND flash device
  - Support 512 B, 2 KB, 4 KB and 8 KB page size NAND flash device
  - Support ECC4, ECC8, ECC12, ECC15 and ECC24 BCH algorithm for ECC code generation, error detection and error correction.
  - Support eMMC flash interface
  - Support DMA function to accelerate the data transfer between system memory and NAND and eMMC flash.
- I^2S Controller
  - Support I^2S interface
    - Support both mono and stereo
    - Support both record and playback
    - Support 8-bit, 16-bit 20-bit and 24-bit data precision
    - Support master and slave mode
  - Support PCM interface
    - Support 2 slots mode to connect 2 device
    - Support 8-bit, 16-bit 20-bit and 24-bit data precision
    - Support master mode
  - Support four 8x24 (8 24-bit) buffer for left/right channel record and left/right playback
  - Support DMA function to accelerate the data transfer between system memory and internal buffer
  - Support 2 buffer address for left/right channel and 2 slots data transfer
- LCD Display Controller
  - Support 8/9/16/18/24-bit data with to connect with 80/68 series MPU type LCD module
  - Support resolution up to 1024x768
  - Support data format conversion from RGB444, RGB565, RGB666, RGB888, YUV422 and YUV444 to RGB444, RGB565, RGB666, RGB888, YUV422 and YUV444 for display output
  - Support CCIR-656 (with VSYNC, HSYNC and data enable sync signal) 8/16-bit YUV data output to connect with external TV encoder
  - Support 8/16 bpp OSD data with video overlay function to facilitate the diverse graphic UI
  - Support linear 1X to 8X image scaling up function
  - Support Picture-In-Picture display function
  - Support hardware cursor
- Capture (CMOS Sensor Interface)
  - Support CCIR601 & CCIR656 interfaces to connect with CMOS image sensor
  - Support resolution up to 3M pixels

- Support YUV422 and RGB565 color format for data output by CMOS image sensor
- Support YUV422, RGB565, RGB555 and Y-only color format for data storing to system memory
- Support planar and packet data format for data storing to system memory
- Support image cropping and the cropping window is up to 4096x2048
- Support image scaling-down:
- Support vertical and horizontal scaling-down for preview mode
- Support N/M scaling factor where N is equal to or less than M
- Support 2 pairs of configurable 16-bit N and 16-bit M
- Support to combine two interlace-fields to a single frame for data output by TV-decoder.
- Support 3 color processing effects
- Negative picture
- Sepia picture
- Posterization

- 2D Graphic Engine
  - Support 2D Bit Block Transfer (BitBLT) functions defined in Microsoft GDI
  - Support Host BLT
  - Support Pattern BLT
  - Support Color/Font Expanding BLT
  - Support Transparent BLT
  - Support Tile BLT
  - Support Block Move BLT
  - Support Copy File BLT
  - Support Color/Font Expansion
  - Support Rectangle Fill
  - Support RGB332/RGB565/RGB888 data format.
  - Support fore/background colors and all Microsoft 256 ternary raster-operation codes (ROP)
  - Support both inside and outside clipping function
  - Support alpha-blending for source/destination picture overlaying
  - Support fast Bresenham line drawing algorithm to draw solid/textured line
  - Support rectangular border and frame drawing
  - Support picture re-sizing
  - Support down-scaling from 1/255 to 254/255
  - Support up-scaling from 1 to 1.996 (1+254/255)
  - Support object rotation with different degree
  - Support L45 (45 degree left rotation) and L90 (90 degree left rotation)
  - Support R45 (45 degree right rotation) and R90 (90 degree right rotation)
  - Support M180 (mirror/flop)
  - Support F180 (up-side-down (flip) and X180 (180 degree rotation)
- JPEG Codec
  - Support Baseline Sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard
  - Planar Format
  - Support to encode interleaved YCbCr 4:2:2/4:2:0 and gray-level (Y only) format image
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image
  - Support to decode YCbCr 4:2:2 transpose format
  - Support arbitrary width and height image encode and decode
  - Support three programmable quantization-tables
  - Support standard default Huffman-table and programmable Huffman-table for decode
  - Support arbitrarily 1X~8X image up-scaling function for encode mode
  - Support down-scaling function for encode and decode modes

- Support specified window decode mode
- Support quantization-table adjustment for bit-rate and quality control in encode mode
- Support rotate function in encode mode
- Packet Format
- Support to encode interleaved YUYV format input image, output bit stream 4:2:2 and 4:2:0 format
- Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0 format image
- Support decoded output image RGB555, RGB565 and RGB888 formats.
- The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
- Support arbitrary width and height image encode and decode
- Support three programmable quantization-tables
- Support standard default Huffman-table and programmable Huffman-table for decode
- Support arbitrarily 1X~8X image up-scaling function for encode mode
- Support down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode
- Support specified window decode mode
- Support quantization-table adjustment for bit-rate and quality control in encode mode

- Crypto Engine
  - PRNG
  - Support 64-bit, 128-bit, 192-bit and 256-bit key generation
  - DES
  - Support FIPS 46-3
  - Support both encryption and decryption
  - Support ECB, CBC, CFB, OFB and CTR modes
  - 3DES
  - Support FIPS NIST 800-67
  - Implements according to the X9.52 standard
  - Support 112-bit and 168-bit key
  - Support both encryption and decryption
  - Support ECB, CBC, CFB, OFB and CTR modes
  - AES
  - Support FIPS NIST 197
  - Support SP800-38A & addendum
  - Support 128-bit, 192-bit and 256-bit key
  - Support both encryption and decryption
  - Support ECB, CBC, CFB, OFB , CTR, CBC-CS1, CBC-CS2 and CBC-CS3 modes
  - Support Key Expander
  - SHA/HMAC
  - Support FIPS NIST 180, 180-1, 180-2
  - Support SHA-160, SHA-224, SHA-256, SHA-384, SHA-512 and corresponding HMAC algorithm
  - Support 128-bit MTP key
- GDMA (General DMA)
  - Support 2 channels GDMA for memory-to-memory data transfer without CPU intervention
  - Support increment and decrement for source and destination address calculation
  - Support 8-bit, 16-bit and 32-bit width data transfer
  - Support four 8-bit/16-bit/32-bit burst transfer
- UART
  - Support up to 11 UART controllers
  - Support 1 UART (UART 1) port with full model function (TXD, RXD, CTS, RTS, CDn, RIn, DTR and DSR) and 64-byte FIFO
  - Support 5 UART (UART 2/4/6/8/10) ports with flow control (TXD, RXD, CTS and RTS) and 64-byte FIFO

- Support 5 TXD/RXD only UART ports (UART 0/3/5/7/9) with 16-byte FIFO for standard device
- Support IrDA (SIR) and LIN function
- Support RS-485 9-bit mode and direction control
- Support programmable baud-rate generator up to 1/16 system clock

- C-CAN
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1M bit/s
  - 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Support power down wake-up function
- Smart Card Host (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separate receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detecting the card removal
- Timer
  - Support 5 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Support one-shot, periodic, toggle and continuous operation modes
- Enhanced Timer
  - Support 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Support one-shot, periodic, toggle and continuous operation modes
  - Supports external pin capture for interval measurement
  - Supports external pin capture for timer counter reset
- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time out period from 1.6ms ~ 26.0sec (depends on clock source)
  - WDT can wake-up from power down or idle mode
  - Interrupt or reset selectable on watchdog timer time-out
- Windowed-Watchdog Timer
  - 6-bit down counter with 11-bit pre-scale for wide range window selected
  - Interrupt on windowed-watchdog timer time-out
  - Reset on windowed-watchdog timer time out or reload in an unexpected time window
- Real Time Clock (RTC)
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)

- Supports Alarm registers (second, minute, hour, day, month, year)
- Selectable 12-hour or 24-hour mode
- Automatic leap year recognition
- Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports battery power pin (VBAT)
- Supports wake-up function

- PWM
  - Built-in up to two 16-bit PWM generators provide four PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit pre-scale, two 16-bit counters, and one Dead-Zone generator
- SPI
  - Built-in up to two sets of SPI controller
  - Support SPI master mode
  - Support single/dual/quad bit data bus width
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Support burst mode operation that transmission and reception can be executed up to four times in a transfer
  - Support 2 slave/device select lines
- I^2C
  - Up to two sets of I2C device
  - Support master mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Support software mode to generate I2C signaling
- Advanced Interrupt Controller
  - Support 58 interrupt sources, including 8 external interrupt sources
  - Support programmable normal or fast interrupt mode (IRQ, FIQ)
  - Support programmable edge-triggered or level-sensitive for 8 external interrupt sources
  - Support programmable low-active or high-active for 8 external interrupt sources
  - Support encoded priority methodology to allow for interrupt daisy-chaining
  - Support lower priority interrupt automatically mask out for nested interrupt
  - Support to clear interrupt flag automatically if interrupt source is programmed as edge-triggered
- GPIO
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Support pull-up and pull-down control
- ADC
  - 12-bit SAR ADC with 800K/160K SPS
  - Up to 8-ch single-end input

- Support 4-wire or 5-wire resistance touch screen interface
- Support touch pressure measurement for 4-wire touch screen application
- Support pen down detection
- Support battery measurement
- Support keypad scan

- KPI
  - Matrix keypad interface supported.
  - Maximum 4X8 and minimum 3X3 keypad matrix supported.
  - Configurable key de-bounce supported.
  - Low power wakeup mode supported.
  - Configurable three-key reset supported.
- MTP
  - Support 256-bit programmable memory for key of Crypto functionality
  - Support up to 15 times of programming and erase.
- Low Voltage Detect (LVD) and Low Voltage Reset (LVR)
  - Support two, 2.6V and 2.8V, voltage detection levels
  - Interrupt when low voltage detected
  - Reset when low voltage detected
  - Low voltage reset threshold voltage levels: 2.4 V
- Power Management
  - Advanced power management including Power Down, Deep Standby, CPU Standby and Normal Operating modes
  - Normal Operating mode
    - CPU run normally and all clocks on, the current consumption of CORE_VDD is around 185 mA (at CPU/DRAM clock is 300/150 MHz CPU).
  - CPU Standby mode
    - CPU clock stop, and all other clocks on.
  - Deep Standby mode
    - All clocks stop, except LXT, with SRAM retention, and the current consumption of CORE_VDD is typicaly 3 mA
  - Power Down mode
    - All powers are off except RTC_VDD (3.3V) and the current consumption of RTC_VDD is typicaly 7uA with RTC functionality on.
- Operating Voltage
  - 1.2V for core logic operating
  - 1.8V for DDR or DDR2 SDRAM I/O operating
  - 3.3V for normal I/O operating
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 216-pin
  - LQFP 128-pin

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NUC970 Series Part Number Naming Guide

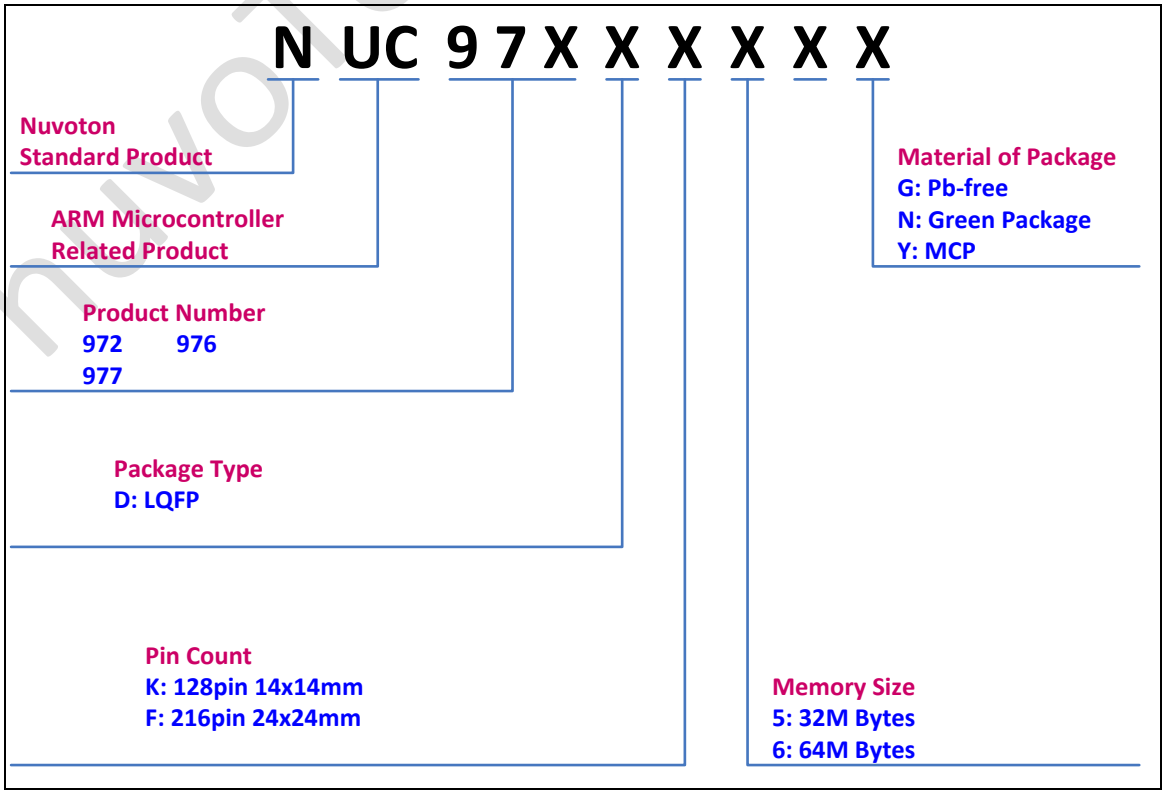


Figure 3-1 NUC970 Series Part Number Naming Guide

3.2 NUC970 Series Part Selection Guide

ARM970 Series

Part No.	Memory		Storage			MAC	USB		GFX	LCD	Timer						Analog				Peripheral										Package	Operating Temp. Range1 (°C)
																	ADC															
	DDR2 RAM(MB)	SPI Flash, No. of I/O Pins	NAND Flash, No. of ECC bits	EMMC	SD / SDIO	Ethernet 10/100 MAC	USB 2.0 Host (480M bps)	USB 2.0 HS Device	2D Graphics	TFT LCD	Real-Time Clock (RTC)	Timer (32-bit)	Enhanced Timer	Watchdog Timer	Window Watchdog Timer	PWM	Touch Screen Controller	No. of Channels	Speed (Samples per second)	LVD/LVR	External Bus Interface	GPIO (Max)	UART	CAN BUS	I2C (Master Only)	SPI	ISO-7816-3	KPI	CMOS Interface	I2S/AC97		
NUC972DF62Y	64	1	24	√	2	2	2	1	√	√	√	5	4	√	√	4	√	8	200K*	√	√	146	11	2	2	2	2	√	√	1	LQFP216	-40 to +85
NUC976DK62Y	64	1	-	√	2	1	2	1	√	√	√	5	1	√	√	4	√	4	200K*	√	-	80	6	1	2	2	2	√	√	1	LQFP128	-40 to +85
NUC976DK51Y	32	1	-	√	2	1	2	1	√	√	√	5	1	√	√	4	√	4	200K*	√	-	80	6	1	2	2	2	√	√	1	LQFP128	-40 to +85
NUC977DK62Y	64	1	24	√	2	1	2	1	√	√	√	5	2	√	√	4	-	-	-	√	-	87	8	1	2	2	2	√	√	1	LQFP128	-40 to +85
NUC977DK51Y	32	1	24	√	2	1	2	1	√	√	√	5	2	√	√	4	-	-	-	√	-	87	8	1	2	2	2	√	√	1	LQFP128	-40 to +85

3.3 Pin Configuration

3.3.1 NUC972DFxxY Pin Diagram

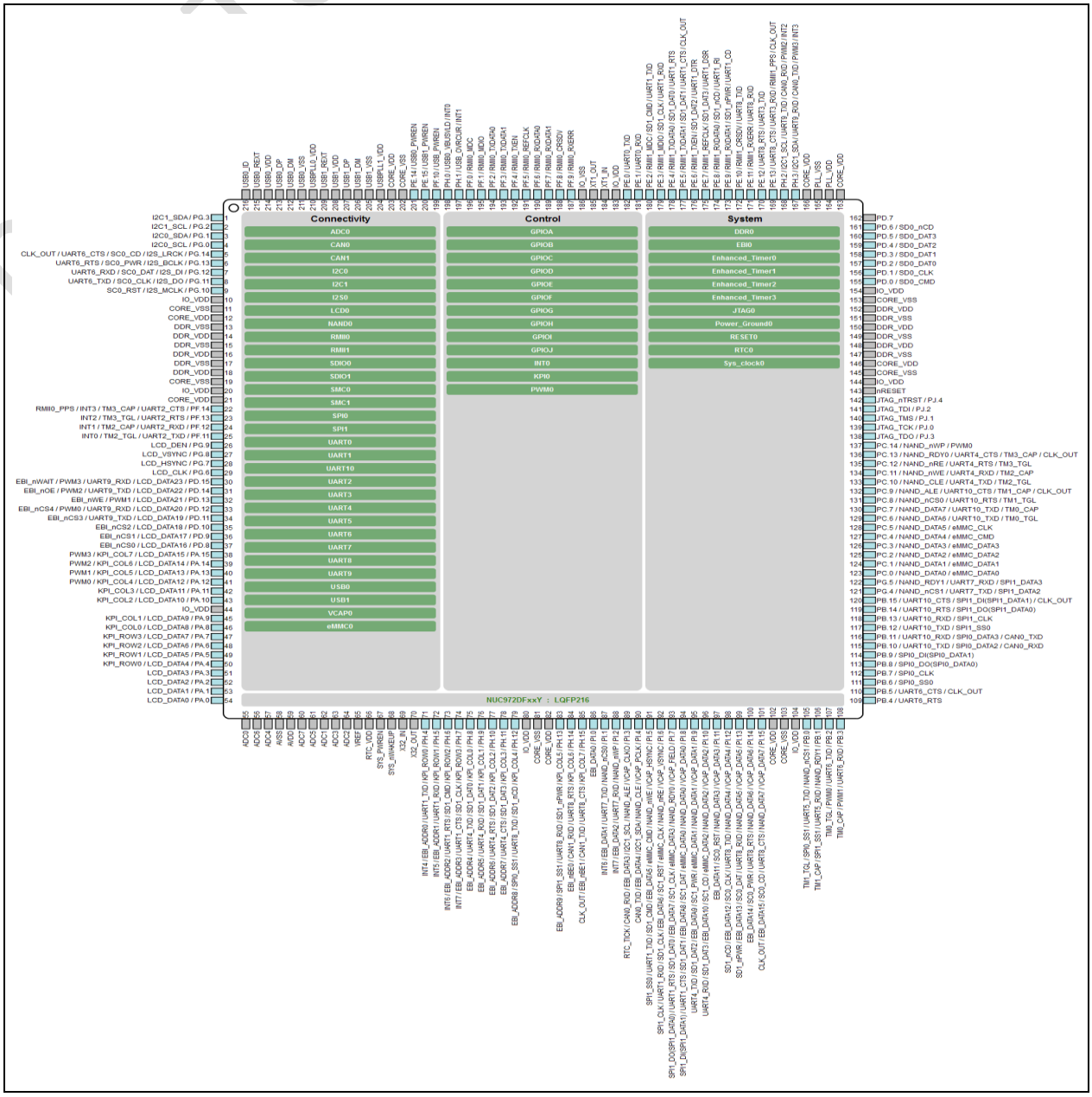


Figure 3.3-1 NUC972DFxxY LQFP 216-pin Pin Diagram

3.3.2 NUC976DKxxY Pin Diagram

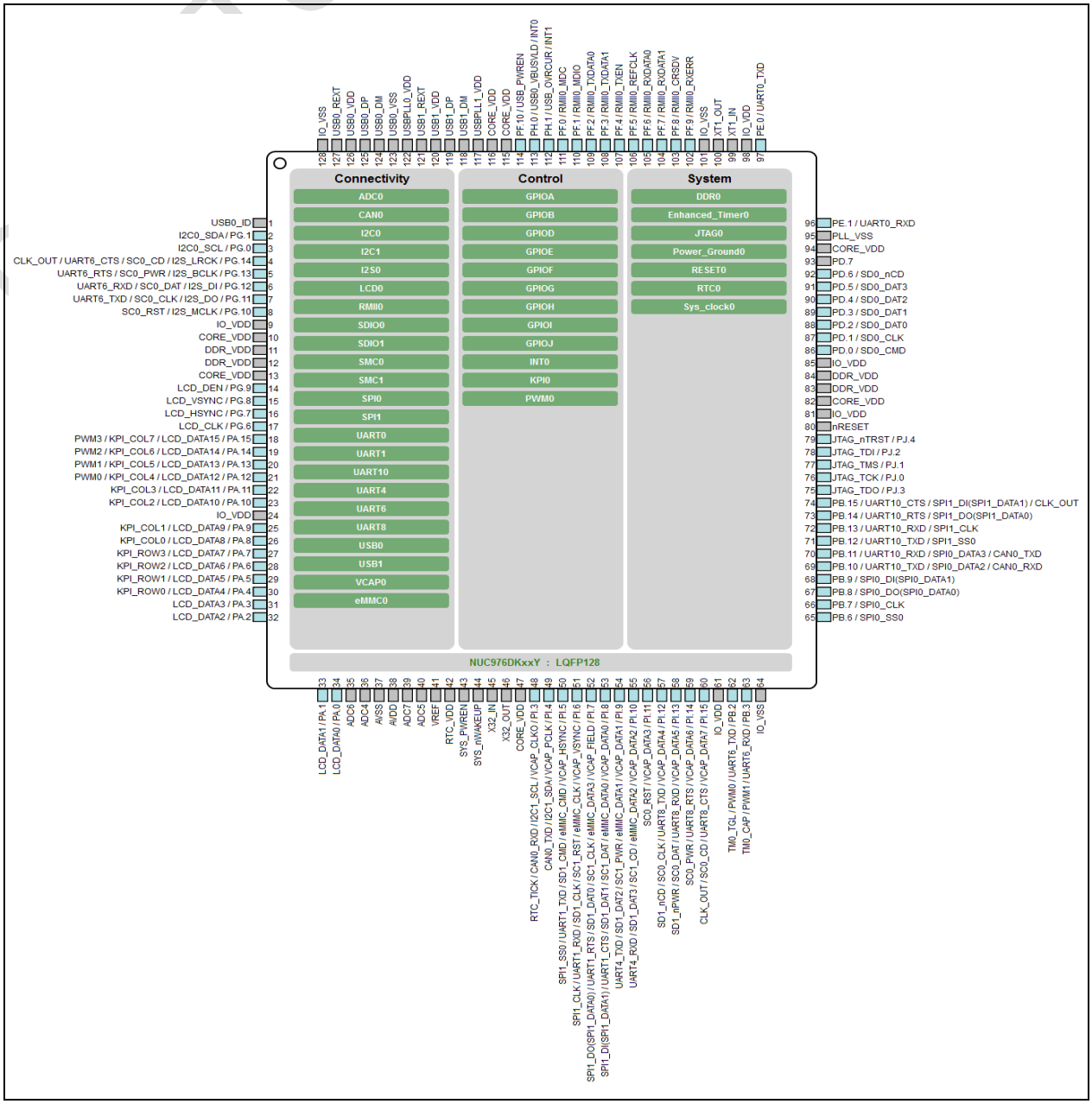


Figure 3.3-2 NUC976DKxxY LQFP 128-pin Pin Diagram

3.3.3 NUC977DKxxY Pin Diagram

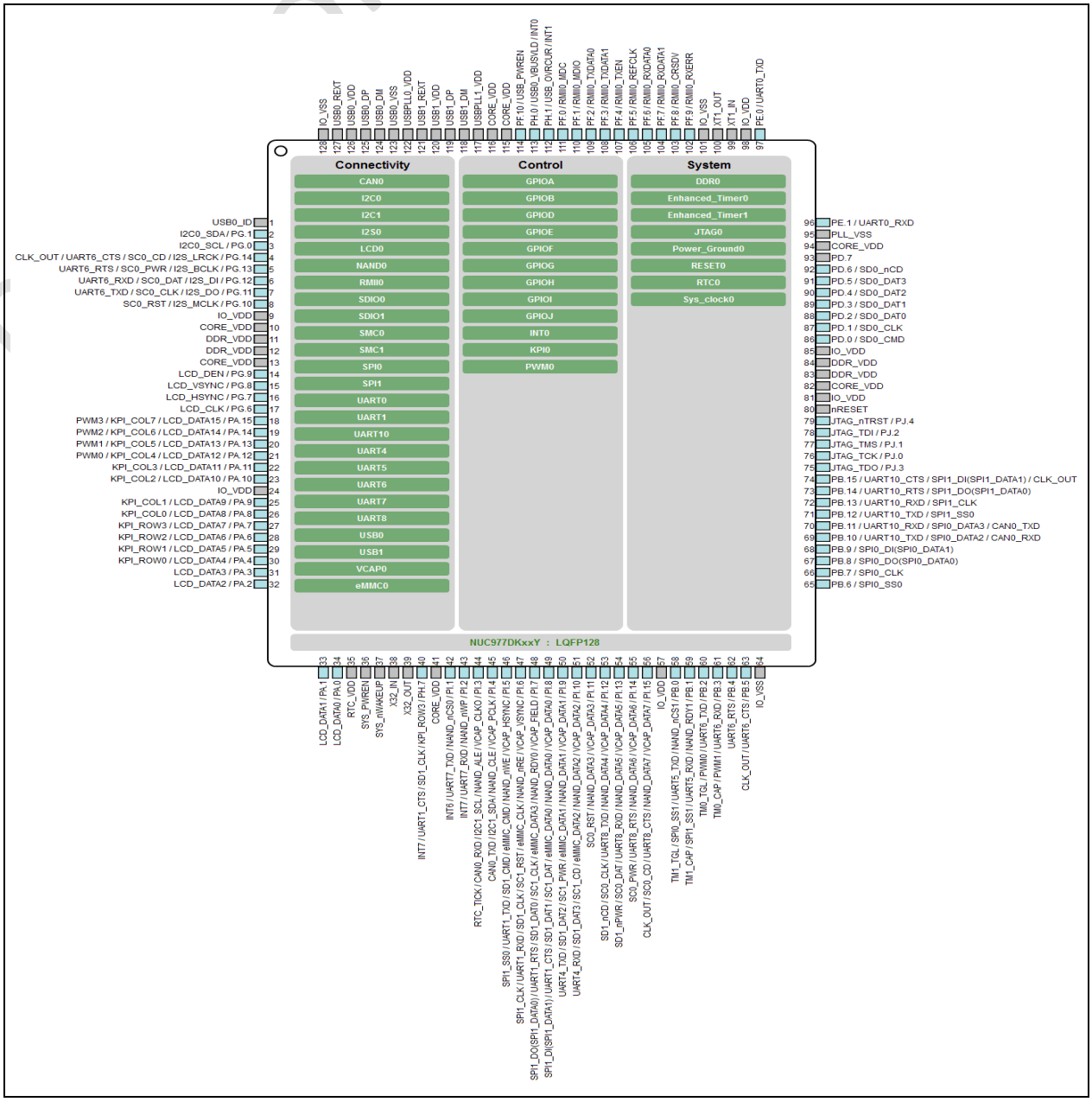


Figure 3.3-3 NUC977DKxxY LQFP 128-pin Pin Diagram

4 BLOCK DIAGRAM

4.1 NUC970 Series Block Diagram

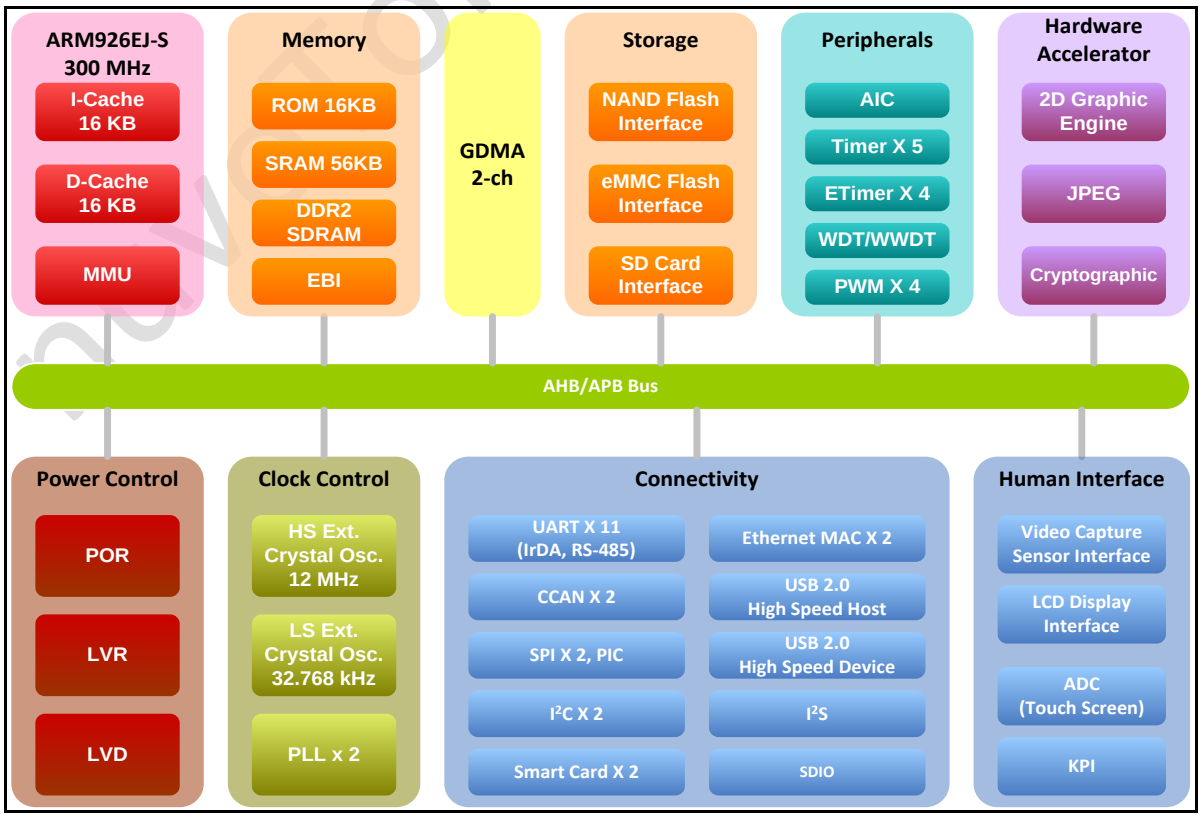
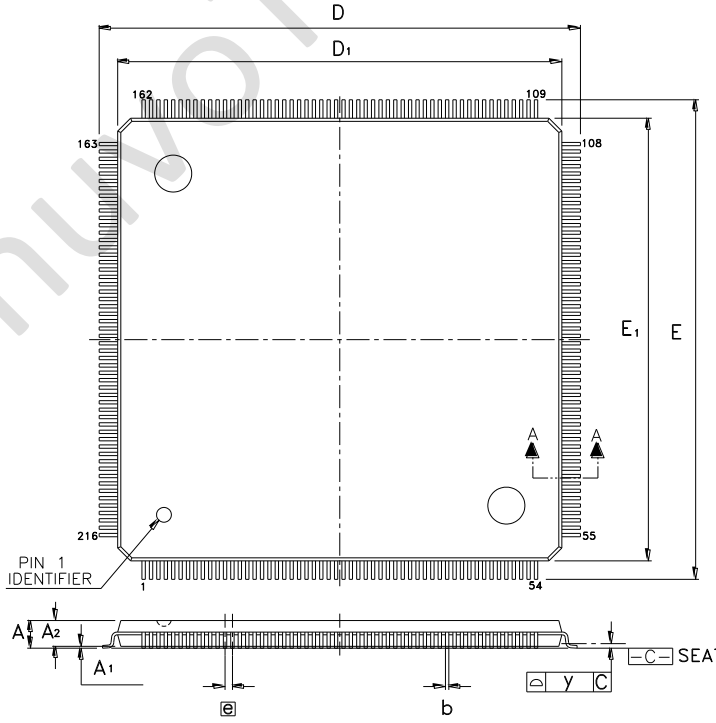
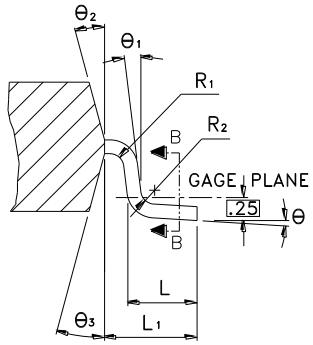


Figure 4.1 NUC970 Series Block Diagram

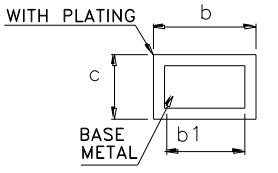
5 PACKAGE DIMENSIONS

5.1 216L LQFP (24x24x1.4mm footprint 2.0mm)





SECTION A–A

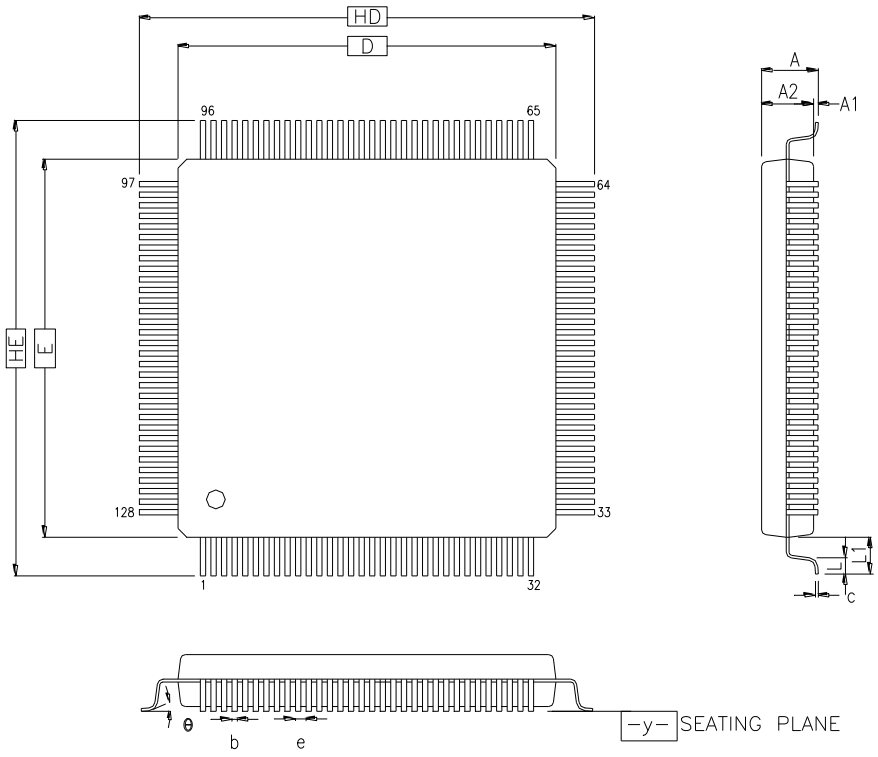


SECTION B–B

Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	0.14	0.20	0.004	0.006	0.008
D	25.85	26.00	26.15	1.018	1.024	1.030
D1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.40 BSC			0.0157 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
y	0.08			0.00314		

5.2 128L LQFP (14x14x1.4mm footprint 2.0mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

6 REVISION HISTORY

Date	Revision	Description
May 12, 2015	1.00	1. Preliminary version.
July 14, 2015	1.10	1. Revised part no. NUC976DK52Y and NUC977DK52Y to be NUC976DK51Y and NUC977DK51Y.
July 29, 2015	1.15	1. Updatded pin diagrams.
Nov. 25, 2015	1.20	1. Addded NUC978YOxxY part 2. Modifying part selection guide, pin diagram and updated QFN88 PKG dimension. 3. NUC973 series EOL
Dec.15, 2015	1.30	4. Removed NUC978YOxxY part
Feb. 23, 2016	1.31	5. Fatures updated of ADC

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.