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NUC970 Power ON Setting

Design Note

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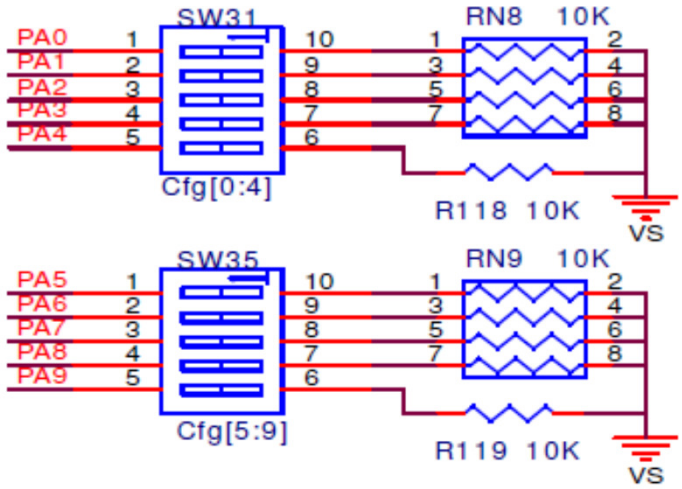
Nuvoton Technology Corp.

Power-On Setting

- After power on reset, Power-On setting registers are latched to configure this chip. It is used to configure the chip to enter the specified state.
- Since each pin of power on setting has an internal pulled-up resistor at while reset period. If application needs to set the configuration to “0”, the proper pull-down resistor must be added for corresponding.
- The Application circuitry is listed as below:

  Note:
  - 1 = OFF, 0 = ON (Pulled down with 10K)
  - PA [9:0] = PWRON [9:0]

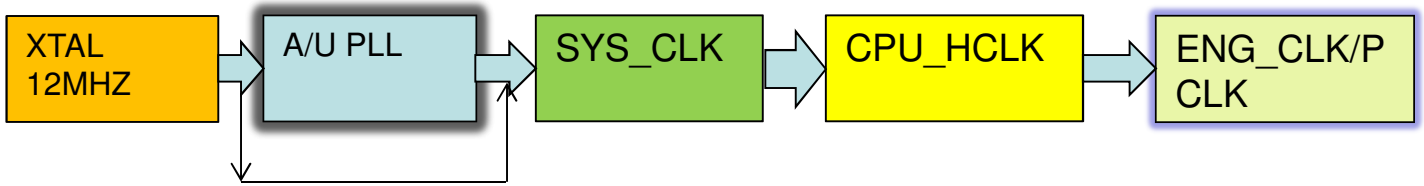


Boot Source Selection

Power-On Setting Pin	Description	Power-On Setting Register Bit
PA[1:0]	**Boot Source Selection** 00 = Boot from USB and pin PH.0 used as the USB0_VBUSVLD. 01 = Boor from eMMC and pin PC[5:0] or PI[10:5] used as the eMMC functionality[1]. 10 = Boot from NAND Flash and pin PC[14:0] or PI[15:1] used as the NAND functionality[2,3]. 11 = Boot from SPI Flash and pin PB[9:6] used as the SPI0 functionality. Note 1: PC[5:0] used as the eMMC functionality in NUC972 and NUC973 while PI[10:5] used as the eMMC functionality in NUC976 and NUC977. Note 2: PC[14:0] used as the NAND functionality in NUC972 and NUC973 while PI[15:1] used as the NAND functionality in NUC977. Note 3: NUC976 doesn't support NAND interface.	PWRON[1:0]

System Clock Source Selection

Power-On Setting Pin	Description	Power-On Setting Register Bit
PA.2	**System Clock Source Selection** 0 = System clock is from 12 MHz crystal. 1 = System clock is from UPLL output.	PWRON[2]



Watchdog Timer (WDT) Enabled/Disabled Selection

Power-On Setting Pin	Description	Power-On Setting Register Bit
PA.3	**Watchdog Timer (WDT) Enabled/Disabled Selection** 0 = WDT Disabled after power-on. 1 = WDT Enabled after power-on.	PWRON[3]

JTAG Interface ON/OFF Selection

Power-On Setting Pin	Description	Power-On Setting Register Bit
PA.4	**JTAG Interface ON/OFF Selection** 0 = Pin PJ[4:0] used as GPIO pin. 1 = Pin PJ[4:0] used as JTAG interface.	PWRON[4]

UART 0 Debug Message Output ON/OFF Selection

Power-On Setting Pin	Description	Power-On Setting Register Bit
PA.5	**UART 0 Debug Message Output ON/OFF Selection** 0 = UART 0 debug message output ON and pin PE[1:0] used as the UART0 functionality. 1 = UART 0 debug message output OFF and pin PE[1:0] used as the GPIO functionality.	PWRON[5]

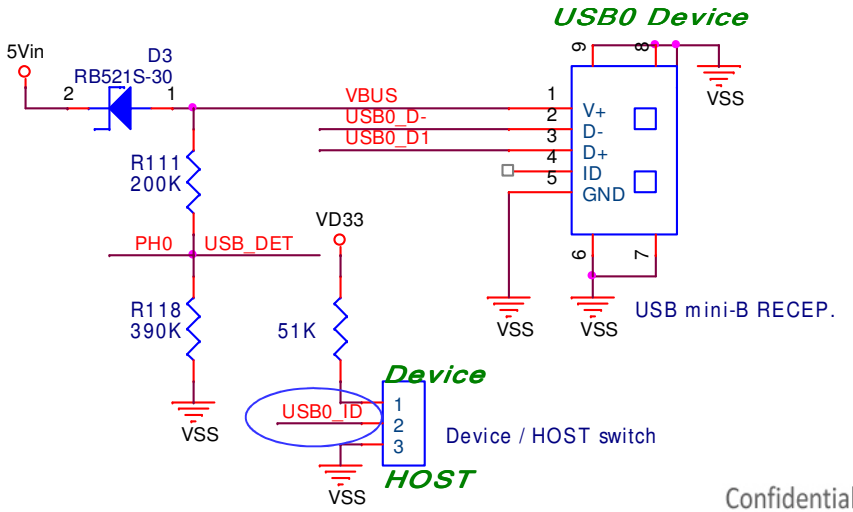
NAND Flash Page Size & ECC Selection

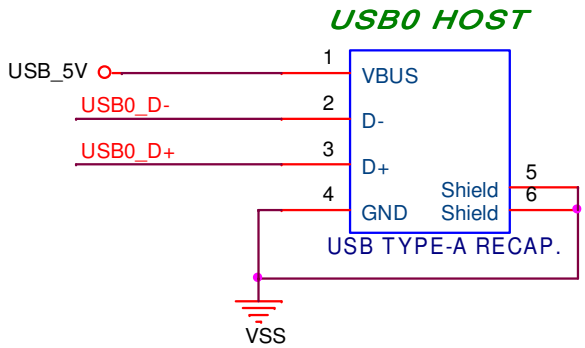
Power-On Setting Pin	Description	Power-On Setting Register Bit
PA[7:6]	**NAND Flash Page Size selection** 00 = NAND Flash page size is 2KB. 01 = NAND Flash page size is 4KB. 10 = NAND Flash page size is 8KB. 11 = Ignore Power-On Setting.	PWRON[7:6]
PA[9:8]	**NAND Flash ECC Type Selection** 00 = NAND Flash ECC type is BCH T12. 01 = NAND Flash ECC type is BCH T15. 10 = NAND Flash ECC type is BCH T24. 11 = Ignore Power-On Setting.	PWRON[9:8]

USB0 Setting

- The table shown below describes the definition of USB0 power-on setting
- As the reference circuitry, user can use the pin of USB0_ID to define USB0 port for acting device or host function

Power-On Setting Pin	Description	Power-On Setting Register Bit
USB0_ID	**USB Port 0 Role Selection** 0 = USB Port 0 act as a USB host. 1 = USB Port 0 act as a USB device.	PWRON[16]





Power-On setting register

- PA [9:0] status will map to SYS_PWRON [9:0]
- USB0_ID status will map to SYS_PWRON [16]

Power-On Setting Register (SYS_PWRON)

Register	Offset	R/W	Description	Reset Value
SYS_PWRON	SYS_BA+0x004	R/W	Power-On Setting Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved			Reserved	DID			
23	22	21	20	19	18	17	16
Reserved						TICMOD	USBID
15	14	13	12	11	10	9	8
Reserved						NECCSEL	
7	6	5	4	3	2	1	0
NPAGESEL		URDBGON	JTAGON	WDTON	SYSCKSEL	BTSSEL	