codasip	Western Digital SweRV		
	EH1	EH2	EL2
Architecture			
Pipeline Stages	9	9	4
In-order/Out-of-Order	in-order	in-order	in-order
Dual issue	yes	yes	no
Dual thread	no	optional	no
Number of registers	32	32	32
Instruction set			
Base instruction set	RV32IMC	RV32IMC	RV32IMC
Compressed instructions	yes	yes	yes
FPU	no	no	no
Multiplication	Parallel three-cycles	Parallel three-cycles	Parallel one-cycle
Division	Out of pipe 2-34 cycles	Out of pipe 2-34 cycles	Out of pipe 2-34 cycles
Atomics	no	yes (limited to memory addresses mapped to the core's DCCM)	no
Branch Predictor			
RAS size	2/3/4/5/6/7/8	2/3/4/5/6/7/8	2/3/4/5/6/7/8
BTB size	32/48/64/128/256/512	32/48/64/128/256/512	32/48/64/128/256/512
BHT size	32/64/128/256/512/1024/2048	32/64/128/256/512/1024/2048/4096	32/64/128/256/512/1024/2048
GHR (GSHARE)	yes	yes	yes
JTAG			
Type	4pin	4pin	4pin
LSU address/store data breakpotints	4 (also load data)	4 (also load and AMO data)	4
DEC address breakpoints	4 for each issue	4 for each thread	4
Instruction Cache			
Enabled	optional	optional	optional
ECC protection	optional (otherwise partity)	optional (otherwise partity)	optional (otherwise partity)
Number of ways	4	2/4	2/4
Size	16/32/64/128/256 kB	8/16/32/64/128/256 kB	8/16/32/64/128/256 kB
Ways packed into one RAM module	no	optional	optional
ICCM			
Enabled	optional	optional	optional
ECC protection	yes	yes	yes
Number of banks	4/8/16	4/8/16	2/4/8/16
Size	4/8/16/32/64/128/256/512 kB	4/8/16/32/64/128/256/512 kB	4/8/16/32/64/128/256/512 kB
DCCM			
Enabled	optional	optional	optional
ECC protection	yes	yes	yes
Number of banks	4/8/16	2/4/8/16	2/4
Size	4/8/16/32/64/128/256/512 kB	4/8/16/32/64/128/256/512 kB	4/8/16/32/64/128/256/512 kB
PIC			
Enabled	yes	yes	yes
Computation cyles number	1/2	1/2	1/2
PICM size	32/64/128/256 kB	32/64/128/256 kB	32/64/128/256 kB
LSU			
Store Buffer size	2/4/8	2/4/8	2/4/8
Non Blocking Loads number (CAM)	2/4/8	2/4/8	2/4/8
Load to use latency	-	0/1 cycle	0/1 cycle
Bus load to use latency	-	0/1 cycle	-
Other			
MPU	Possibility to divide memory to 16 regions and make access to part of it illegal (mask + start address)		
Bus protocol	AXI/AHB	AXI	AXI/AHB
FPGA optimize	optional	optional	optional
DMA buffer size	2/4	2/4/5	2/4/5
Fast Interrupt Redirect	no	optional	optional
Number of ALUs	2/4	4	1
NMI vector	overrideable	overrideable	overrideable
RST vector	overrideable	overrideable	overrideable

configurable