C P U MODULE

This module contains the central processing unit of the computer system. Also on the board there are: 4 MHz clock logic
Reset logic
Memory bank logic

Pin description:

AØ - A15	tri state, output. System address bus, a buffered Z-8Ø A bus
DØ - D7	tri state, bidirectional. System data bus, a buffered Z-8Ø A bus
BSØ - BS3	output, tri state. Bank select lines. Select one of 16 memory banks. Writing to I/O port ØFFH changes the bank select digit. $\overline{\text{BUSAK}}$ will float these lines.
$\overline{\text{MREQ}}$	tri state, output. Buffered Z-8Ø A line
$\overline{\text{IORQ}}$	tri state, output. BUffered Z-8Ø A line
$\overline{\text{RD}}$	tri state, output. Buffered Z-8Ø A line
$\overline{\text{WR}}$	tri state, output. Buffered Z-8Ø A line
$\overline{\text{M1}}$	output. Buffered Z-8Ø A line
$\overline{\text{BUSRQ}}$	input, open drain. Z-8Ø A line. Unbuffered !
$\overline{\text{BUSAK}}$	output. Buffered Z-8Ø A line. Floats all tri state outputs.
$\overline{\text{HALT}}$	output. Buffered Z-8Ø A line. Lights LED
$\overline{\text{RFSH}}$	output. Buffered Z-8Ø A line.
$\overline{\text{RESIN}}$	input. BufferedZ Z-8Ø A reset line. Open drain
RESET	output. Affected by $\overline{\text{RESIN}}$ or reset switch.
$\overline{\text{RESET}}$	output. Affected by $\overline{\text{RESIN}}$ or reset switch.
$\overline{\text{INT}}$	input, open drain. Z-8Ø A line. Unbuffered !
$\overline{\text{NMI}}$	input, open drain. Z-8Ø A line. Unbuffered !
$\overline{\text{INTA}}$	output. Interrupt acknowledge. Buffered. Active, if both $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ are active.
$\overline{\text{WAIT}}$	input, open drain. Z-8Ø A line. Unbuffered !
CLCK	output. 4MHz system clock. Buffered.

Power-on: An automatic reset signal is generated when the power is turned on. The bank select lines are switched to Ø on reset. They are also switched to Ø on $\overline{\text{INTA}}$ and the first time M1 goes low after an $\overline{\text{NMI}}$.

Still Problems with Power-On Reset