System configuration:

The system is modular, mounted in a 19" frame on Euro - boards with DIN 41612 connectors.

Central Processing Unit:

CPU is a Z8ØA operating at 4 MHz. Also on the CPU module board there is a latch selecting one of sixteen 60 Kbyte memory pages (banks). This latch can be written to at I/O address FFH. The latch contents are then output to the BSØ - BS3 bus lines. After a BUSRQ the BSØ - BS3 lines are floated.

Circuitry is provided to automatically switch to bank Ø on a reset, a NMI and an INTA.

A reset switch and a halt LED are provided.

Memory Organization:

A maximum of 964 K bytes are addressible. The BSØ - BS3 lines select one of sixteen 60 K bytes memory pages (banks) which reside at ØØØØ - EFFF hexadecimal. A 4 K bytes control memory block is always resident at FØØØ - FFFF hexadecimal.

Banks Ø - 3 contain system ROM and ROM utilities. Banks 4 - 7 are main memory. Bank 4 usually contains user programs or a system in CP/M manner. Banks 5, 6, 7 contain data or background pages of long programs. Banks 8 - 11 are reserved for pseudo - disk or bubble-memory operation. Banks 12 - 15 are set aside for terminal operation such as programmable character generators, screen refresh memory and hi-resolution graphics.

I/O Organization:

At this level of construction the I/O devices are:

I/O address		device
ØØH - Ø5H	out	display digits Ø - 5
	in	keyboard rows Ø - 5
Ø6H - Ø7H	out	don't use, clears display
	in	keyboard rows 6 - 7
Ø8H - ØFH	out	don't use, clears display
	in	just returns FFH
1ØH		CTC timer channel Ø
11H		CTC timer channel 1
12H		CTC timer channel 2
13H		CTC timer channel 3
14H - FEH		not used
FFH		Bank select latch

more - See Serial Interface

Control module, CTC, Mikroterminal Interface:

This special module contains a 4 K bytes control memory block, resident at FØØØ H - FFFF H which can be battery-backed and write-protected (switch). Also on the board, there is a Z 8Ø A CTC counter/timer circuit used mainly for system timing such as display refresh, multiprogramming and input scanning. Channels 2 and 3 may be used as a combined timer in order to get delays up to a few seconds. To accomplish this, the ZC/TO 2 is connected to the TRG/CLK 3 pin. (See CTC data sheet for details and programming). The module also contains all circuitry necessary to interface the Microterminal, a pocket-calculator-like device designed to program and debug at system-level. The Microterminal has 4Ø function keys and a 6 digit number display. It is used together with the Microterminal Monitor (see software manual for details). I/O addresses are mentionned above.

INterrupt handling:

In general, the module plugged in at the leftmost position has the highest I/O interrupt priority. Going from left to the right the modules have less and less priority. Modules with no interrupt I/O on them may be plugged in between I/O interrupt modules freely. Yet, in order not to interrupt the daisy-chain (IEI, IEO : see bus description) all I/O interrupt modules must be in a contiguous block of modules starting at slot 18 (see marker hole) besides the power supply module.

Interrupts are normally vectored, i. e. if an I/O device, that has sent an interrupt, receives an interrupt acknowledge it sends an interrupt vector back to the CPU which is treated as specified for Z 80 interrupt mode 2. On interrupts memory bank Ø is always selected.

The NMI (non-maskable interrupt) will be used by the runtime control module (which controls safe multi-user operation) and also selects bank Ø automatically.