<table>
<tr><th>Sr. No.</th><th>Tutorial 1</th></tr>
<tr><td>1</td><td>Introduction to data representation
a. Number Systems
b. Complements
c. Fixed-Point Representation
d. Floating-Point Representation</td></tr>
<tr><td colspan="2">Tutorial 2</td></tr>
<tr><td>1</td><td>A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.
a. How many selection inputs are there in each multiplexer?
b. What size of multiplexers are needed?
c. How many multiplexers are there in the bus?</td></tr>
<tr><td>2</td><td>Represent the following conditional control statement by two register transfer statements with control functions.
If (P=1) then (R1← R2) else if (Q = 1) then (R1← R3)</td></tr>
<tr><td>3</td><td>The following transfer statements specify a memory. Explain the memory operation in each case.
a. R2 ← M[AR]
b. M[AR] ← R3
c. R5 ← M[R5]</td></tr>
<tr><td>4</td><td>Starting from an initial value of R = 11011101, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left.</td></tr>
<tr><td colspan="2">Tutorial 3</td></tr>
<tr><td>1</td><td>The adder-subtractor circuit has the following values for inputs mode M and data inputs A and B. In each case, determine the values of the outputs: S3, S2, S1, S0 and C4.
<table>
<tr><th></th><th>M</th><th>A</th><th>B</th></tr>
<tr><td>1</td><td>0</td><td>0111</td><td>0110</td></tr>
<tr><td>2</td><td>0</td><td>0011</td><td>1001</td></tr>
<tr><td>3</td><td>1</td><td>1100</td><td>1000</td></tr>
<tr><td>4</td><td>1</td><td>0101</td><td>1010</td></tr>
<tr><td>5</td><td>1</td><td>0000</td><td>0001</td></tr>
</table></td></tr>
<tr><td>2</td><td>A computer uses a memory unit with 256K words of 32 bit each. A binary instructions code is store in one word of memory. The instructions have four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.
a. How many bits are there in the operation code, the register code part, and the address part?
b. Draw instruction word formant and indicate the number of bits in each part.
c. How many bits are there in the data and address inputs of the memory?</td></tr>
<tr><td>3</td><td>The following control inputs are active in the bus system shown in figure of Basic computer registers connected to a common bus. For each case, specify the register transfer that will be executed during the next clock transition.
<table>
<tr><th></th><th>S2</th><th>S1</th><th>S0</th><th>LD of Register</th><th>Memory</th><th>Adder</th></tr>
<tr><td>a</td><td>1</td><td>1</td><td>1</td><td>IR</td><td>Read</td><td>--</td></tr>
<tr><td>b</td><td>1</td><td>1</td><td>0</td><td>PC</td><td>--</td><td>--</td></tr>
<tr><td>c</td><td>1</td><td>0</td><td>0</td><td>DR</td><td>Write</td><td>--</td></tr>
<tr><td>d</td><td>0</td><td>0</td><td>0</td><td>AC</td><td>--</td><td>Add</td></tr>
</table></td></tr>
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	Tutorial 4
1	List the assembly language program (of the equivalent binary instructions) generated by a compiler from the following Fortran program. Assume integer variables. SUM = 0 SUM = SUM + A + B DIF = DIF – C SUM = SUM + DIF
2	List the assembly language program (of the equivalent binary instructions) generated by a compiler from the following IF statement: IF (A – B) 10, 20, 30, The program branches to statement 10 if A – B < 0; to statement 20 if A – B = 0; and to statement 30 if A – B > 0.
3	Write a program that evaluates the logic exclusive-OR of two operands.
	Tutorial 5
1	A bus organized CPU has 16 registers with 32 bits in each an ALU, and a destination decoder. a. How many multiplexers are there in the A bus and what is the size of each multiplexer? b. How many selection inputs are needed for MUX A and MUX B? c. How many inputs and outputs are there in decoder? d. How many inputs and outputs are there in the ALU for data, including input and output carries?
2	Specify the control word that must be applied to the processor of ALU to implement the following micro-operations. a. R1 ← R2+R3 b. R4 ← $\overline{R4}$ c. R5 ← R5-1 d. R6 ← SHL R1 e. R7 ← INPUT
3	The memory unit of a computer has 256k words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the in instruction is in one memory word.
	Tutorial 6
1	Convert the following arithmetic expression from infix to reverse polish notation. a. A*B+C*D+E*F b. A*B+A*(B*D+C*E) c. A+B*[C*D+E*(F+G)] d. A*[B+C*(D+E)] / F*(G+H)
2	Convert the following numerical arithmetic expression into reverse polish notation and show the stack operations for evaluating numerical result a. (3+4) [10(2+6)+8] b. (5*4)/[(12+3)*7]
	Tutorial 7
1	Write a Program to evaluate the arithmetic statement. X = A – B + C + (D * E – F) / G + H * K

	a. Using a general register computer with three address instructions. b. Using a general register computer with two address instructions. c. Using a general register computer with one address instructions. d. Using a general register computer with zero address operation instructions.
2	An 8-bit Computer has a register R. Determine the values of status bits, C, S, Z, and V (As per the Status register bits diagram) after each of the following instructions. The initial value of register R in each case is hexadecimal 71. The numbers below are also in hexadecimal. a. Add immediate operand C6 to R. b. Add immediate operand IE to R. c. Subtract immediate operand 9A from R. d. AND immediate operand 8D to R. e. Exclusive-OR R with R.
Tutorial 8	
1	Draw a space time diagram for a six-segment pipeline showing the time it takes to process eight tasks.
2	Determine the number if clock cycles that it takes to process 200 tasks in a six-segment pipeline.
3	A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?
Tutorial 9	
1	Show the contents of registers E, A, Q, and SC (as Table) during the process of multiplication of two binary numbers, 11111 (multiplicand) and 10101 (multiplier). The signs are not included.
2	Explain the Booth's algorithm with the help of flowchart also show the steps for (-12) * (+18) using Booth's Algorithm.
Tutorial 10	
1	Show the step-by-step multiplication process using booth algorithm, when the following binary numbers are multiplied. Assume 5-bit registers that hold signed numbers. The multiplicand in both cases is +15. a. (+15) * (+13) b. (+15) * (-13)
Tutorial 11	
1	a. How many 128*8 RAM chips are needed to provide a memory capacity of 2048 bytes? b. How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? c. How many lines must be decoded for chips select? Specify the size of the decoders.
2	A computer uses RAM chips of 1024 * 1 capacity. a. How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes? b. How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus.

Head of Department