Enroll. No._____

MARWADI UNIVERSITY

Faculty of Engineering

Computer Engineering B. Tech.

SEM: 4th **MU FINAL EXAM** **MAY: 2023**

Subject: - (Computer Organization and Architecture) (01CE1402)
Date:- 01-05-2023

Total Marks:-100 **Time: - 3 Hours**

Instructions:
1. **All Questions are Compulsory.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Do not write/sign/indication/tick mark anything other than Enroll No. at a specific place on the question paper.**

Question: 1.

(a) [10]

1. If value of bit number 15 is 0 then addressing mode is
   A. Immediate
   B. Direct
   C. Indirect
   D. Register
2. D = A + B' + 1 represents _____ microoperation
   A. Add with carry
   B. Add
   C. Subtract
   D. Subtract with borrow
3. Application of Logic Micro operations are ____
   A. selective-set
   B. selective-clear
   C. selective-complement
   D. All of the options
4. If selective complement operation of A(1100) is performed with respect to B(0101) then new value of A will be
   A. 1100
   B. 1001
   C. 0011
   D. 1010
5. Size of DR Register?
   A. 8
   B. 12
   C. 16
   D. 32
6. Which of the following is not a register for Basic Computer?
   A. PC
   B. IR
   C. AR
   D. IT
7. Which of the following is not a Memory Reference Instruction?
   A. AND
   B. ADD
   C. SUB
   D. LDA

8. How Many Phases in Instruction Cycle?
   A. 1 B. 2
   C. 3 D. 4
9. Which of the following is not a Pseudo Instruction?
   A. ORG B. END
   C. START D. DEX
10. Which of the following is a type of Asynchronous Data Transfer methods?
    A. Strobe Pulse B. Handshaking
    C. Both A & B D. None of Above

(b) Short Que. [10]

1. What is the size of TR register?
2. Convert the binary number to decimal number – 1001
3. Find the 1's complement of the Binary number – 1010
4. Find the 2's complement of the Binary number – 1000
5. Define Assembler
6. Full form of SPA.
7. Full form of CIR
8. Full form of PSW
9. Write down any two interrupts name?
10. Write down any two Pseudo Instruction name?

Question: 2.

(a) Explain 4-bit arithmetic circuit with function table. [08]

(b) Explain instruction cycle [08]

OR

(b) What is an interrupt? Draw and explain interrupt cycle [08]

Question: 3.

(a) Explain memory reference instructions by taking suitable value for example [08]

(b) List out any 4 Input-output Instruction name with short and full form. [04]

(c) Draw space time diagram for 6 - segment pipeline with 8 tasks [04]

OR

(a) Draw and explain 4 bit- Binary adder.
Perform Selective Set Operation, Selective Complement Operation, Selective Clear Operation, Mask Operation for A = 1010 and B = 1100. [08]

(b) A computer uses a memory unit with 256K words of 32 bit each. A binary instruction code is store in one word of memory. The instructions have four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.
a. How many bits are there in the operation code, the register code part, and the address part?
b. Draw instruction word formant and indicate the number of bits in each part.
c. How many bits are there in the data and address inputs of the memory? [04]

(c) Convert the following numerical arithmetic expression into reverse polish notation and show the stack operations for evaluating numerical result.
a. (3+4) [10(2+6)+8] [04]

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Question: 4.

(a) Explain any eight addressing modes. [08]

(b) Draw and explain first pass assembler.
Write an assembly language program for the following statement.
DIF = DIF – C [08]

OR

(a) Convert the expression X = (A+B) * (C+D) in all instruction formats. [08]

(b) List the assembly language program (of the equivalent binary instructions) generated by a compiler from the following program. Assume integer variables.
SUM = 0
SUM = SUM + A + B
DIF = DIF – C
SUM = SUM + DIF [08]

Question: 5.

(a) Explain Arithmetic pipeline with suitable details [06]

(b) Differentiate between RISC vs CISC [06]

(c) Briefly explain source-initiated handshaking [04]

OR

(a) Explain 4 segment instruction pipeline with flow chart [06]

(b) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? [06]

(c) Briefly explain destination transfer using handshaking [04]

Question: 6.

(a) Multiply (+15) x (-13) using Booth multiplication algorithm [08]

(b) Draw flow chart to show communication between CPU-IOP. [04]

(c) Differentiate between SRAM vs DRAM [04]

OR

(a) Multiply (-12) x (+18) using Booth multiplication algorithm [08]

(b) Draw DMA controller diagram. [04]

(c) Discuss direct mapping in organization of cache memory. [04]

---Best of Luck---

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– Bloom'S Taxonomy Report –

Sub: Computer Organization and Architecture
Sem. 4th
Branch: CE

Que. Paper weightage as per Bloom's Taxonomy

LEVEL	% of weightage	Question No.	Marks of Que.
Remember/Knowledge	23	1A, 1B, OR 2B,3B, OR 6C, 3C	10,10,8,4,4,4
Understand	35	2A, 2B, 3A, 4A, 5A, OR 5A, 5C, OR 5C, OR 3B, OR 3C	8,8,8.8,6, 6,4,4,4,4
Apply	19	OR 3A, 6B, OR 6B, 4B, OR 4B	8, 4, 4,8,8
Analyze	14	5B, 6C, OR 4A, OR 5B	6,4,8,6
Evaluate	9	6A, OR 6A	8,8
Higher order Thinking/ Creative	0	-	-

Chart/Graph of Bloom's Taxonomy