AIM

To design and implement gate level and MSI circuits of flip-flops

Software Required

Proteus Software

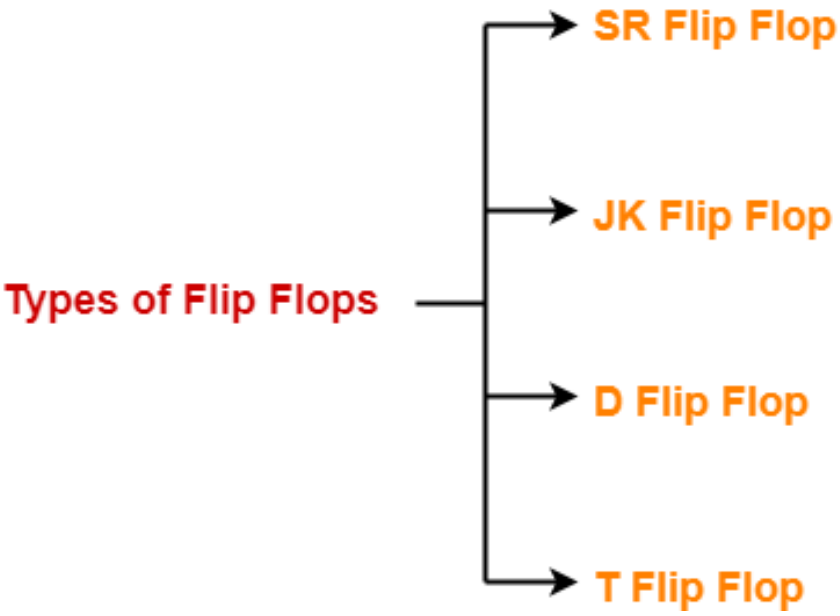
Theory

❖ Introduction to Flip Flop:

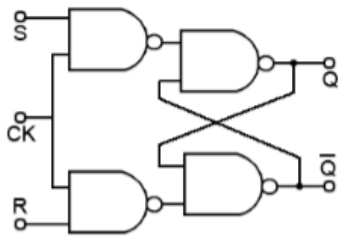
A flip-flop is a device which stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic in electronics.

❖ Types of Flip Flop:

Flip-flops can be divided into common types: the SR ("set-reset"), D ("data" or "delay"), T ("toggle"), and JK. The behaviour of a particular type can be described by what is termed the characteristic equation, which derives the "next" (i.e., after the next clock pulse) output, Qnext in terms of the input signal(s) and/or the current output, Q.



❖ S/R Flip Flop:



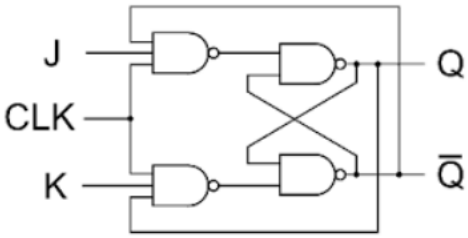
The inputs are generally designated S and R for Set and Reset respectively. Because the NAND inputs must normally be logic 1 to avoid affecting the latching action, the inputs are considered to be inverted in this circuit (or active low).
The circuit uses feedback to "remember" and retain its logical state even after the controlling input signals have changed. When the S and R inputs are both high, feedback maintains the Q outputs to the previous state.

TRUTH TABLE

S	R	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

❖ J/K Flip Flop:

The JK flip-flop augments the behaviour of the SR flip-flop (J: Set, K: Reset) by interpreting the J = K = 1 condition as a "flip" or toggle command. Specifically, the combination J = 1, K = 0 is a command to set the flip-flop; the combination J = 0, K = 1 is a command to reset the flip-flop; and the combination J = K = 1 is a command to toggle the flip-flop, i.e., change its output to the logical complement of its current value. Setting J = K = 0 maintains the current state. To synthesize a D flip-flop, simply set K equal to the complement of J (input J will act as input D). Similarly, to synthesize a T flip-flop, set K equal to J. The JK flip-flop is therefore a universal flip-flop, because it can be configured to work as an SR flip-flop, a D flip-flop, or a T flip-flop.

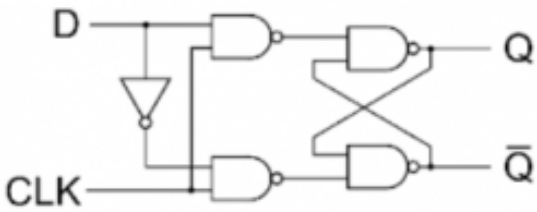


TRUTH TABLE

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

❖ D Flip Flop:

The D flip-flop is widely used. It is also known as a "data" or "delay" flip-flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line.

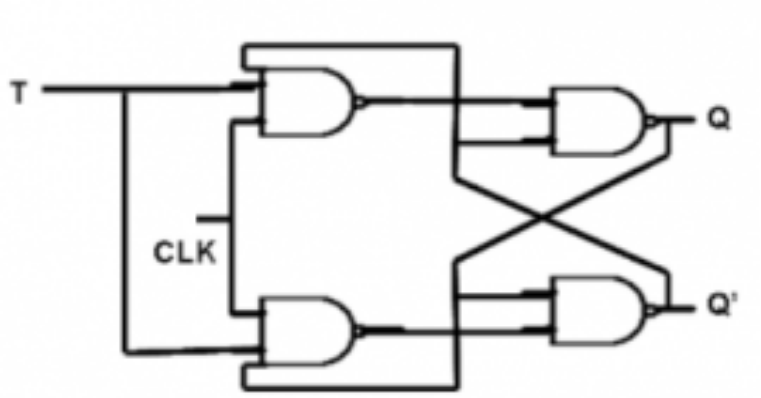


Truth Table

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

❖ T Flip Flop:

If the T input is high, the T flip-flop changes state ("toggles") whenever the clock input is strobed. If the T input is low, the flip-flop holds the previous value.



When T is held high, the toggle flip-flop divides the clock frequency by two; that is, if clock frequency is 4 MHz, the output frequency obtained from the flip-flop will be 2 MHz This "divide by" feature has application in various types of digital counters. A T flip-flop can also be built using a JK flip-flop (J & K pins are connected together and act as T) or a D flip-flop (T input XOR $Q_{previous}$ drives the D input).

Truth Table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

❖ Applications of Flip-Flops

These are the various types of flip-flops being used in digital electronic circuits and the applications of Flip-flops are as specified below.

- Counters
- Frequency Dividers
- Shift Registers
- Storage Registers
- Bounce elimination switch
- Data storage
- Data transfer
- Latch
- Registers
- Memory

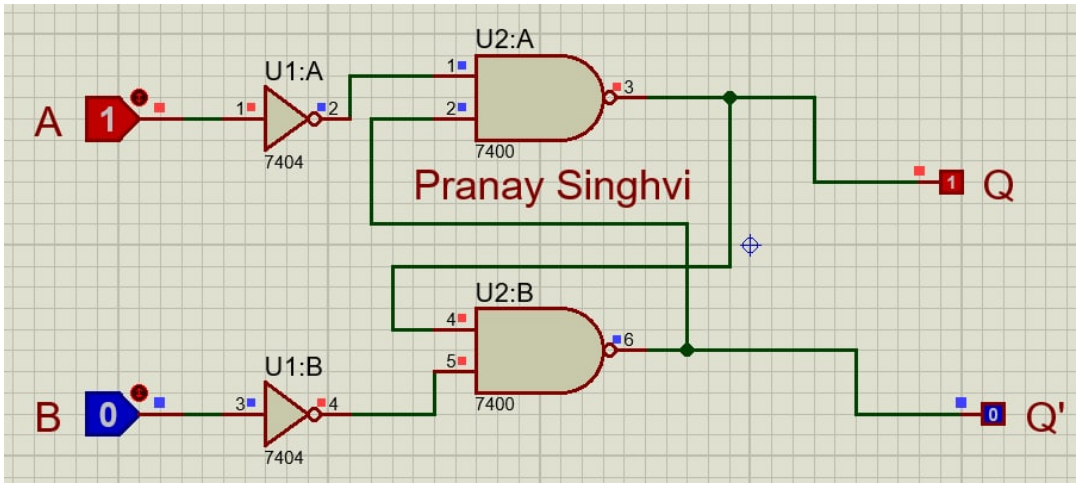
Procedure

1) Open a new project in protecus
2) Click on Device from the left-side tools.
3) Choose the of required IC device and place in its places.
4) Connect all the device and set the binary digit .
5) Note the binary digit of output.
6) Take a Screen shot of all the Types of different Flip Flop.
7) Make different revised Flip Flop in a given Type of Flip Flop
8) Then Run Stimulation.

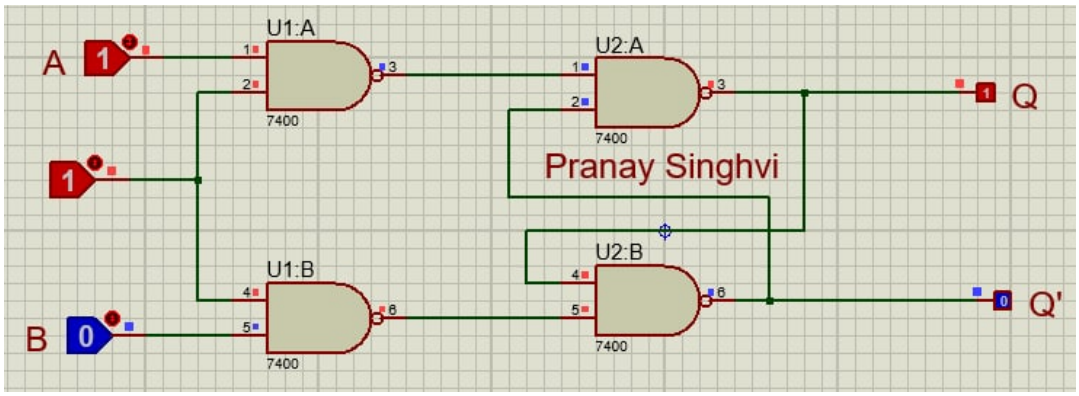
Results and Observations

❖ S/R

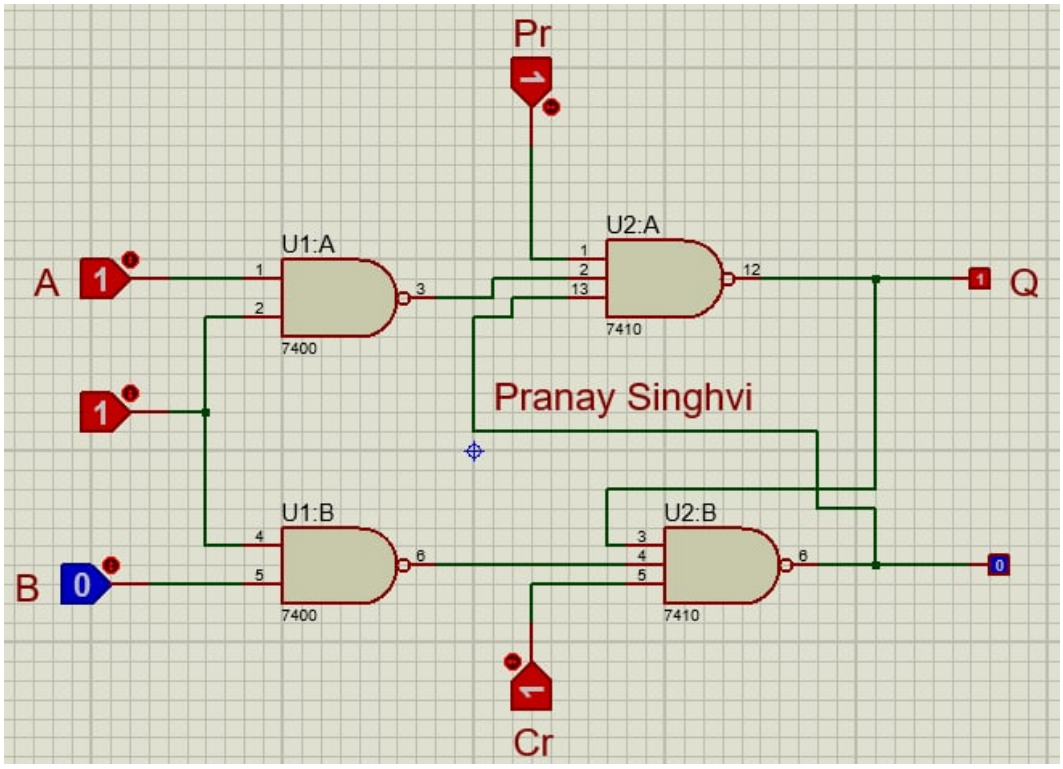
○ Revise 1



○ Revise 2

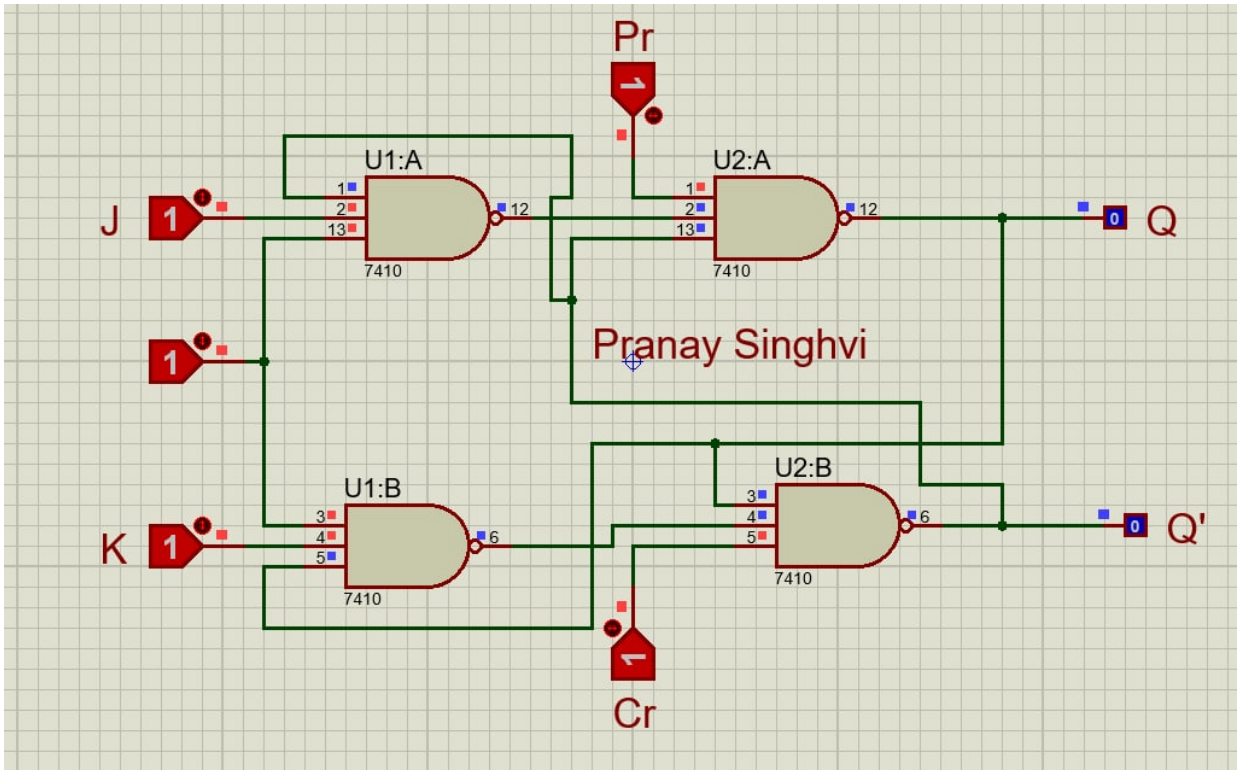


○ Revise 3

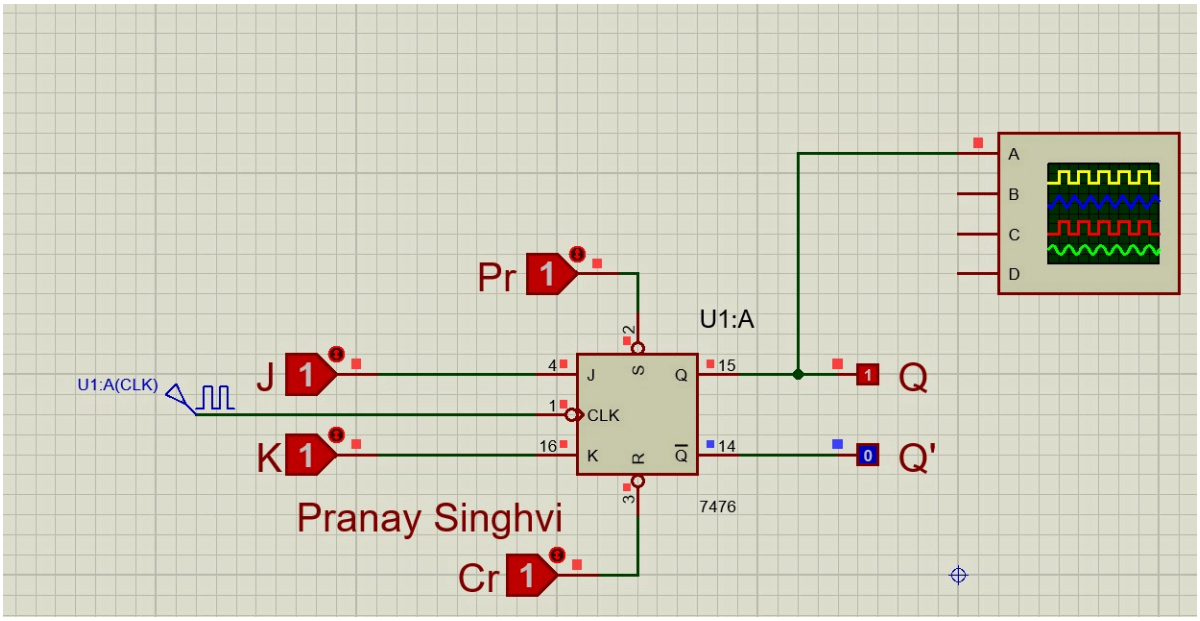


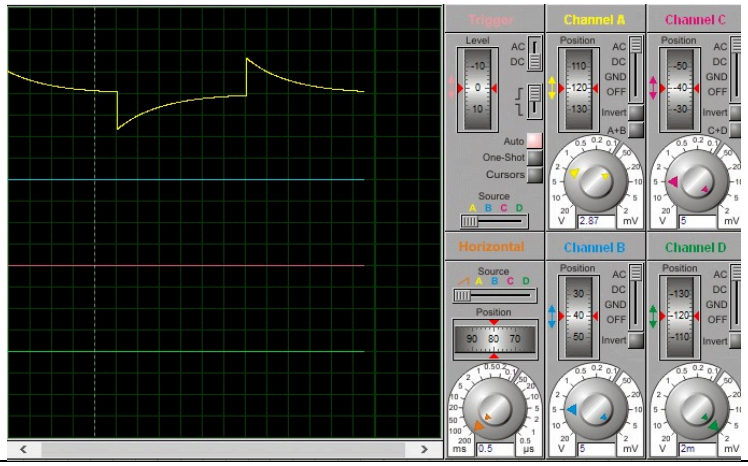
❖ J/K Flip Flops

○ With NAND Gates



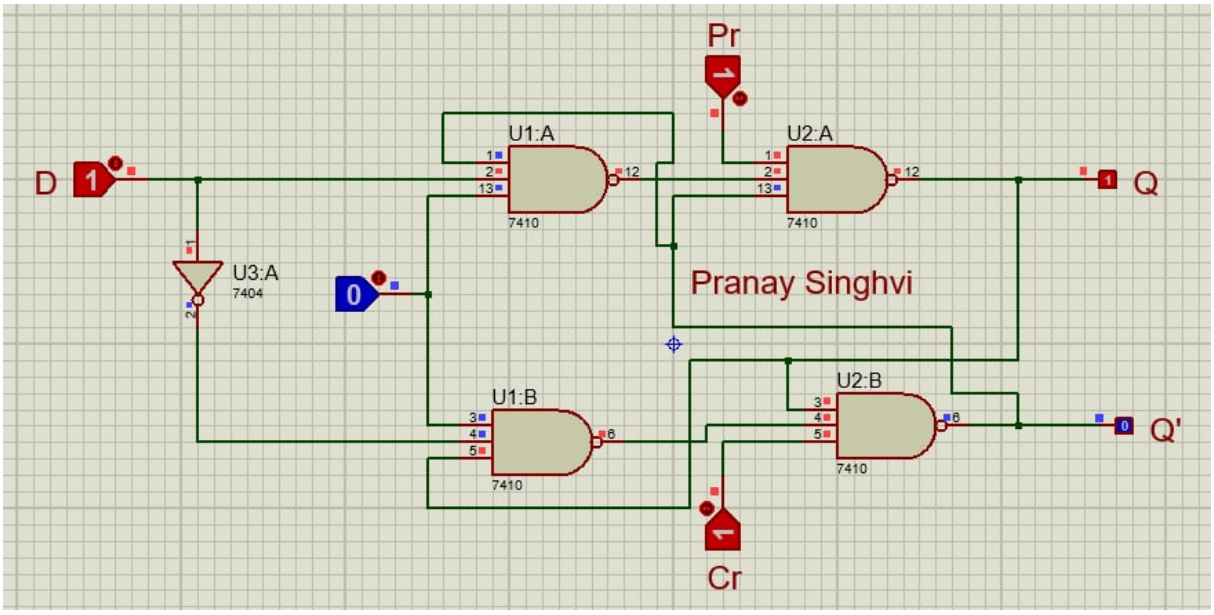
○ With IC7476



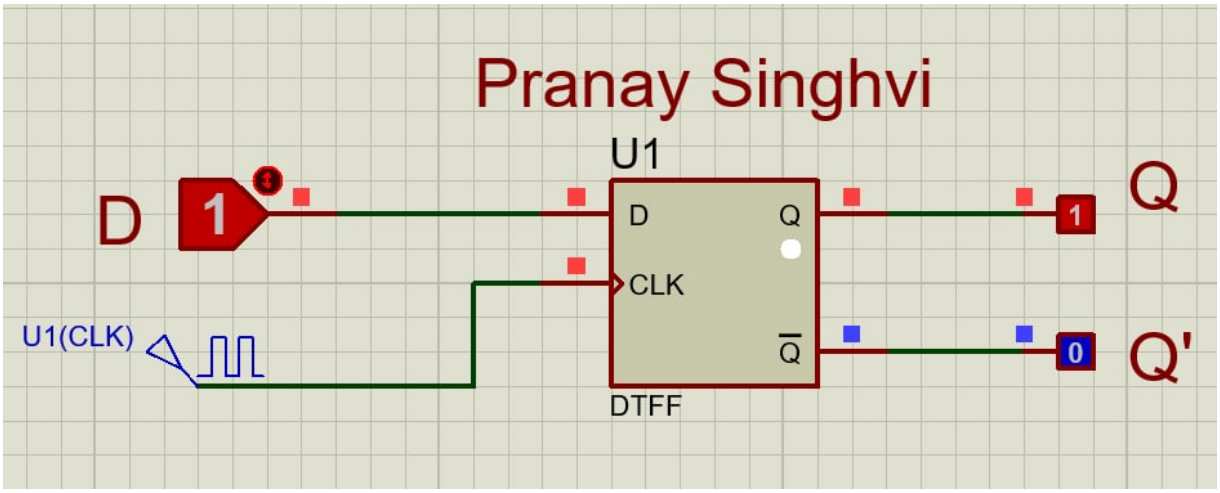


❖ D Flip Flop:

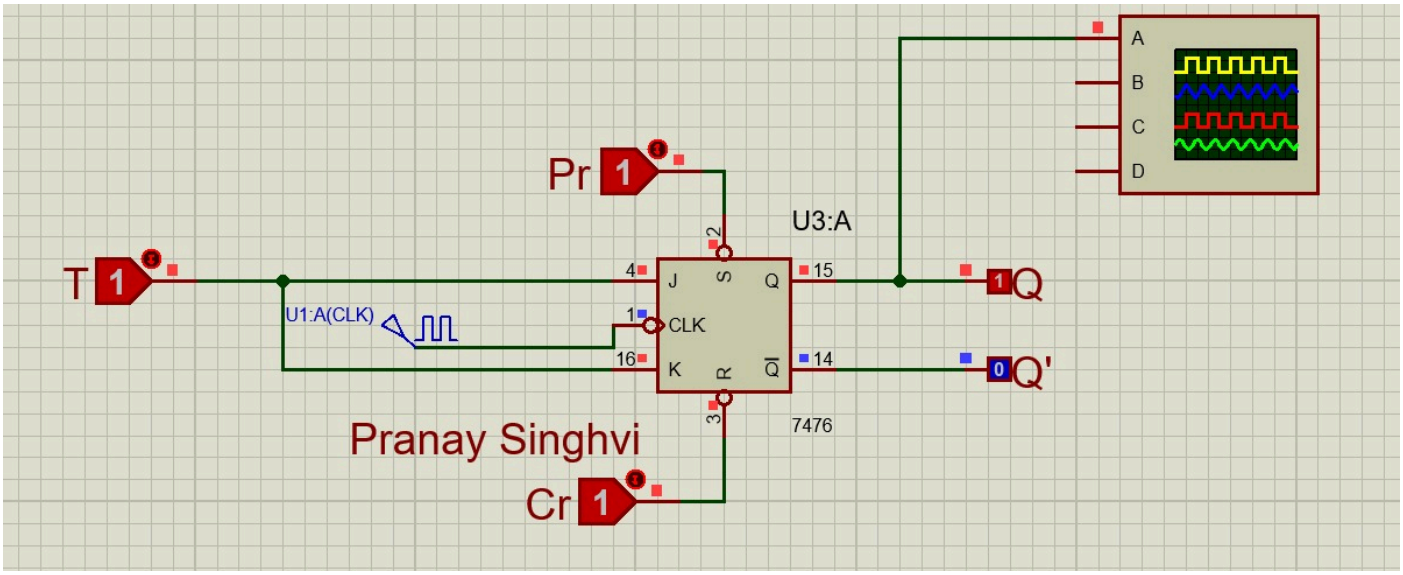
○ With NAND Gates:

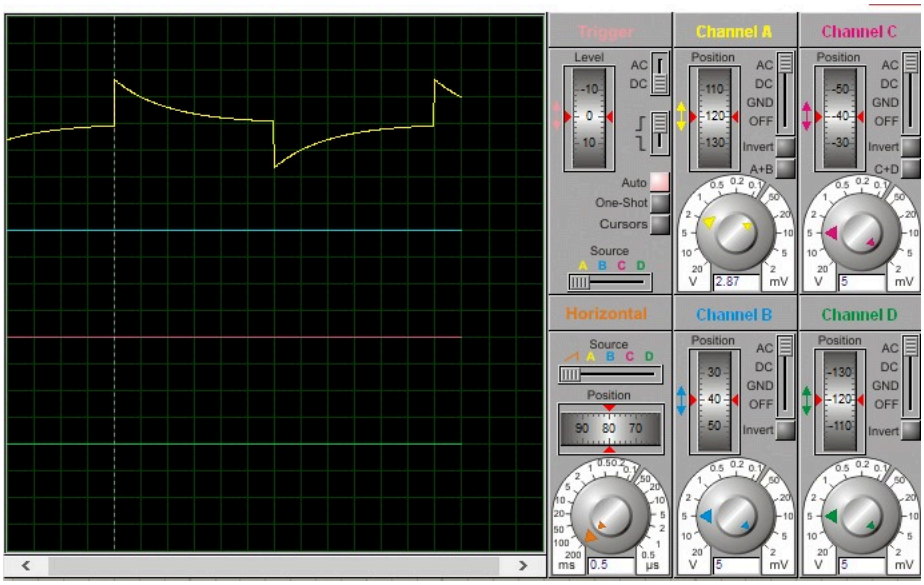


○ With DTFF IC



❖ T Flip Flop:





Conclusion

We Conclude that Flip Flop are divided into four type which are S/R, J/K, D, T Flip Flop. There are 3 Revise Flip Flop in S/R Flip Flop. First with NOT Gate connected with NAND Gate. Second Revised of S/R includes clock. Third revised circuit of S/R Flip Flop has Preset and Clear function. J/K Help to define the condition in which J and K are both 1.