Practical Memory Safety with *REST*

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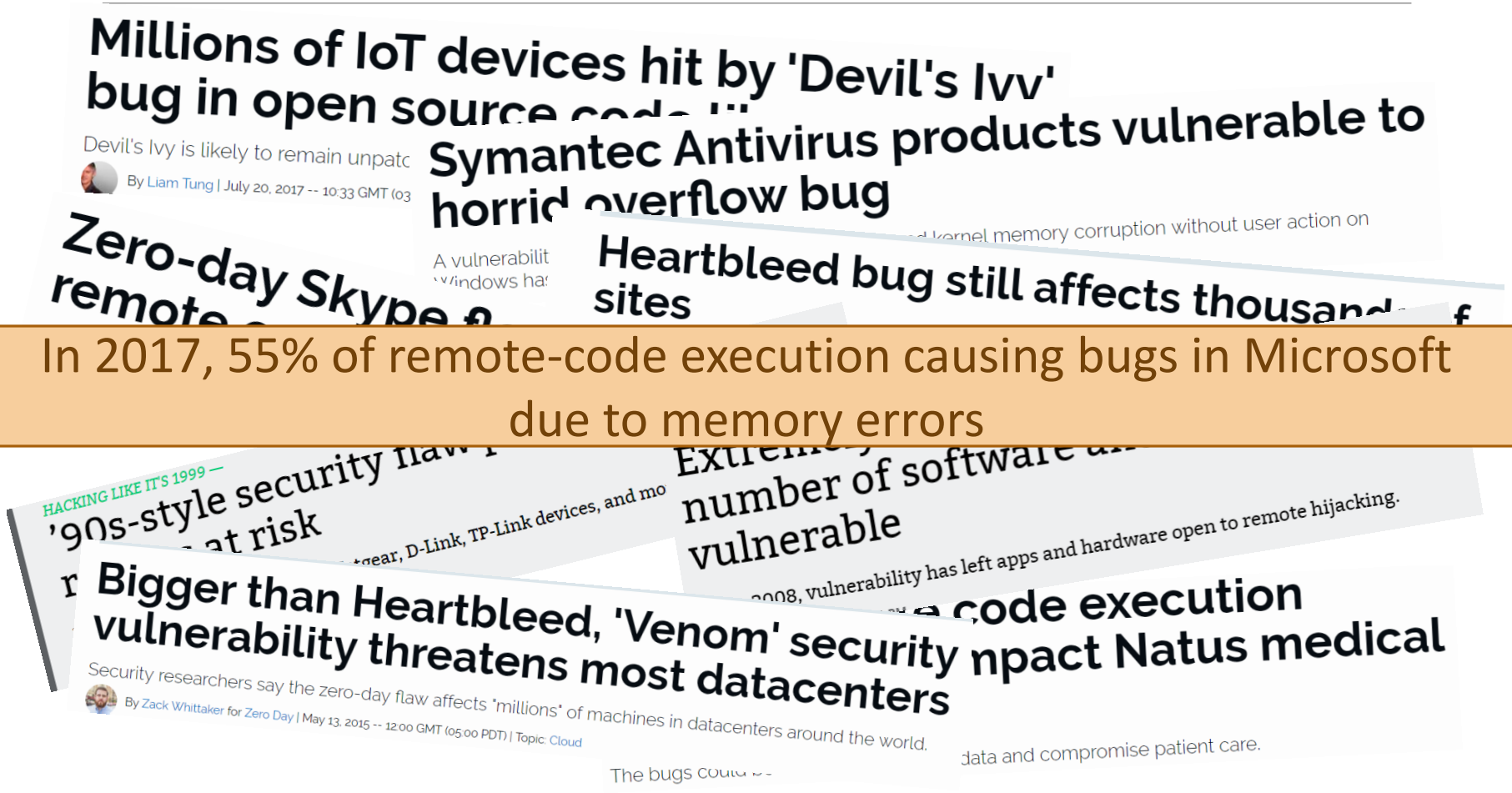
Is memory safety relevant?



In 2017, 55% of remote-code execution causing bugs in Microsoft due to memory errors

Is memory safety relevant?

Yes!

Practical memory safety

Presenting…

Random Embedded Security Tokens or *REST*

Core H/W primitive: Insert known 64B random value (*token*) in program and detect accesses to them.

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Practical memory safety

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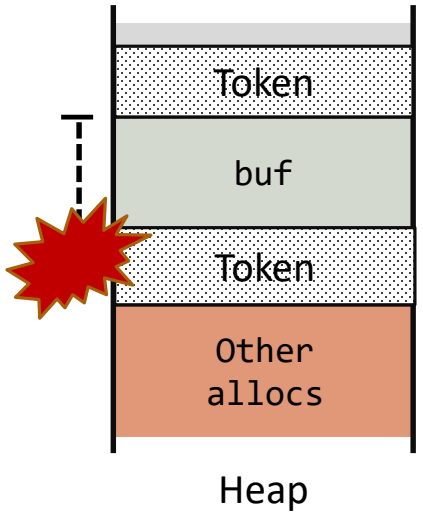


Practical memory safety

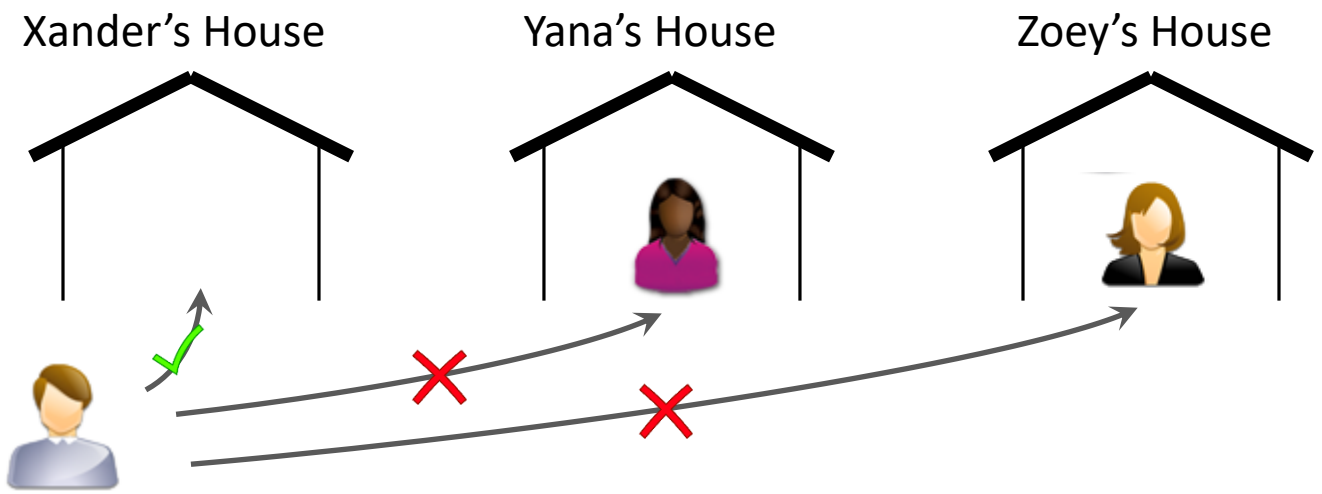
Presenting…

Random Embedded Security Tokens or *REST*

Core H/W primitive: Insert known 64B random value (*token*) in program and detect accesses to them.

- Trivial hardware implementation
- Software framework based on *AddressSanitizer*
- Provides heap safety for legacy binaries

Background: Spatial Memory Safety



Background: Spatial Memory Safety

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char *ptr_buf = malloc(BUF_LEN);
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ptr_buf[in_bounds] = X;
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ptr_buf[out_of_bounds] = Y;
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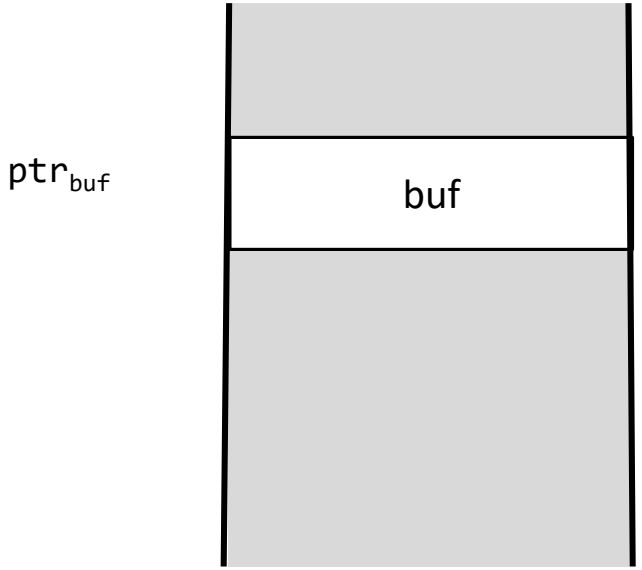

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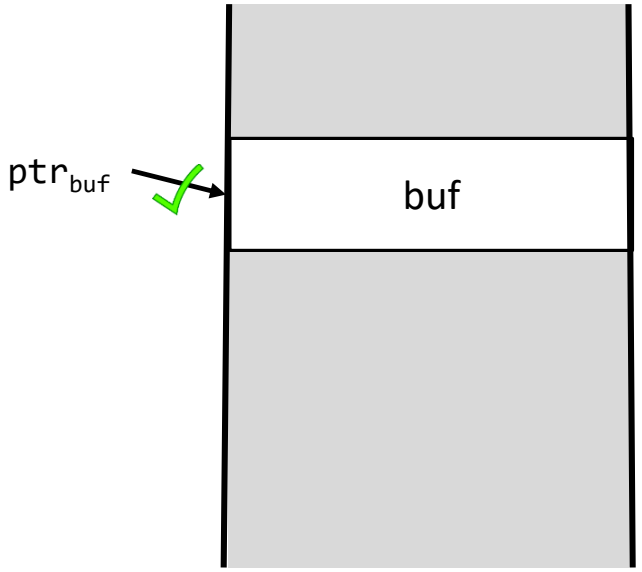

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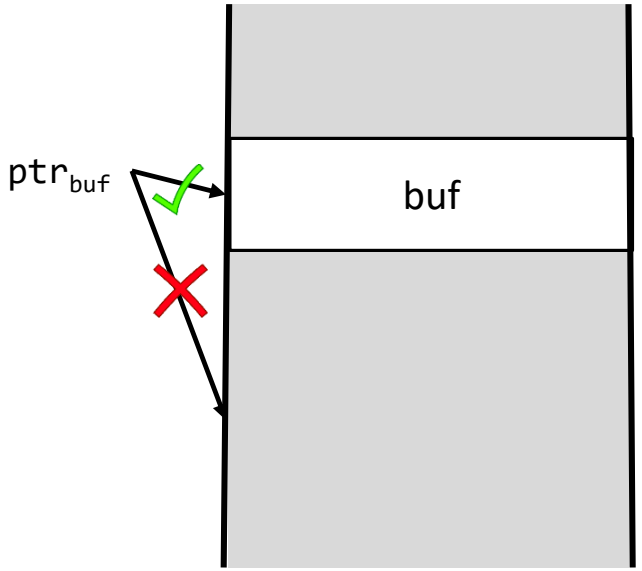
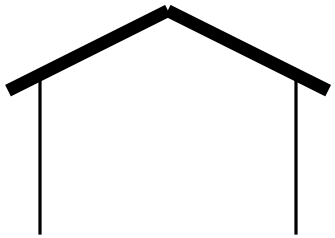


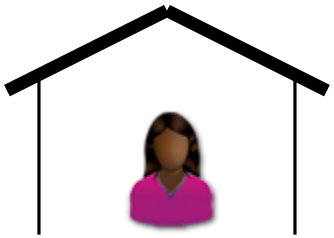
Background: Temporal Memory Safety

Xander moves out, Will moves in

Xander's House



Yana's House



Zoey's House

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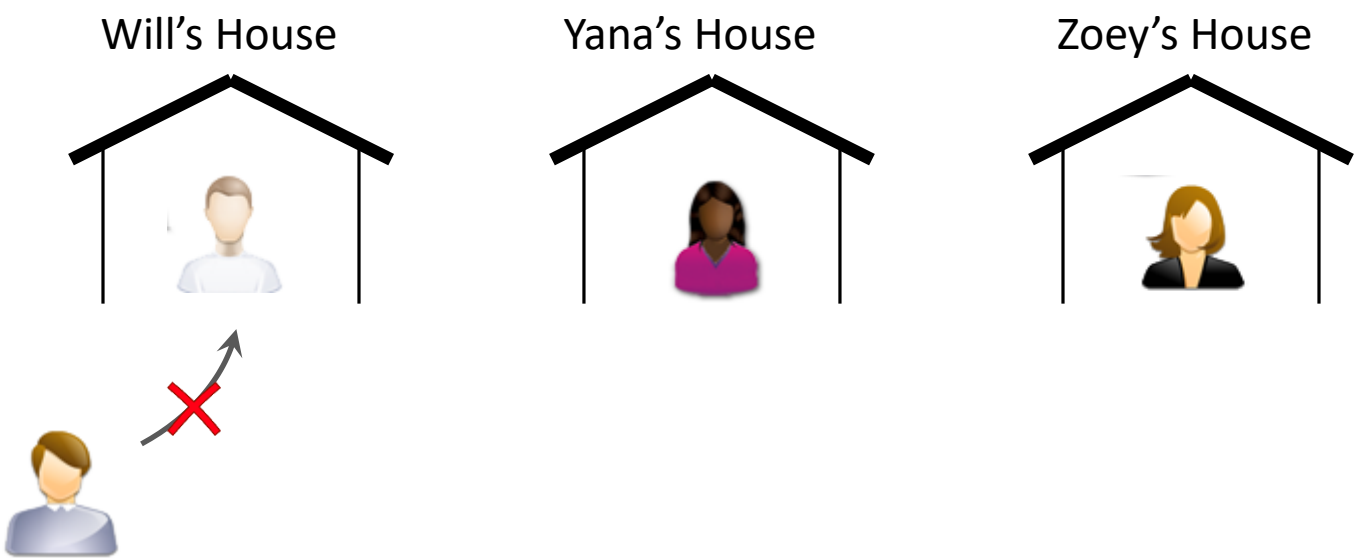

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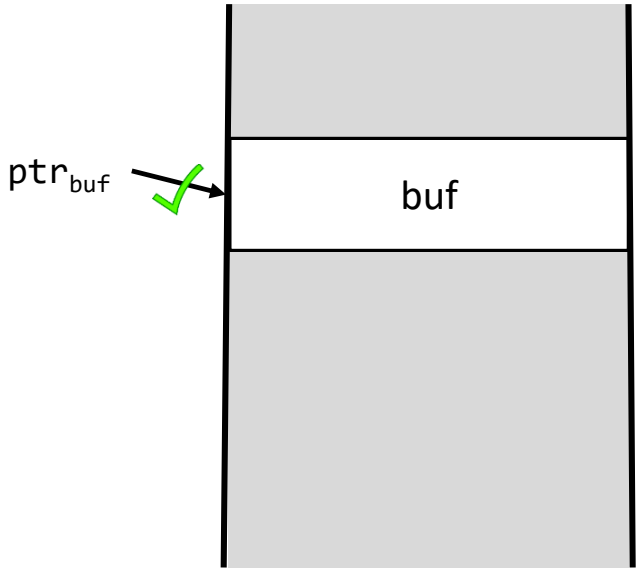

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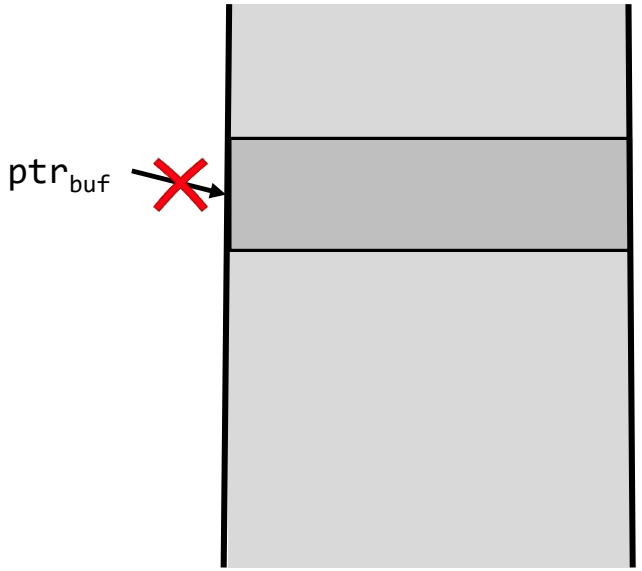

Previous H/W Solutions

Mainly categorizable into 2 types.

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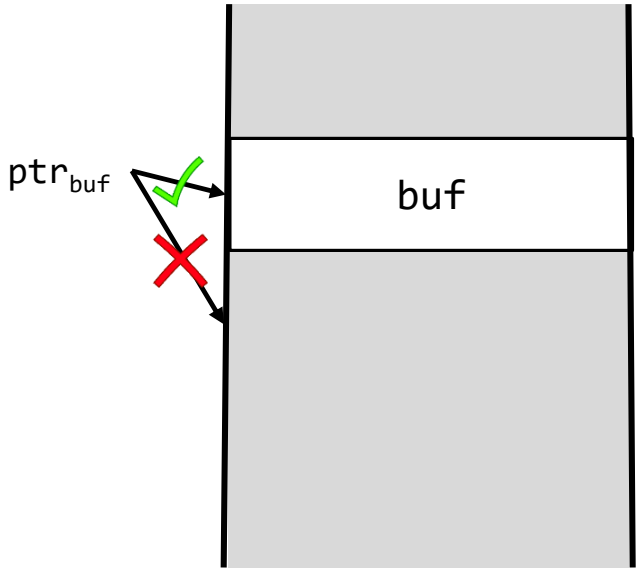
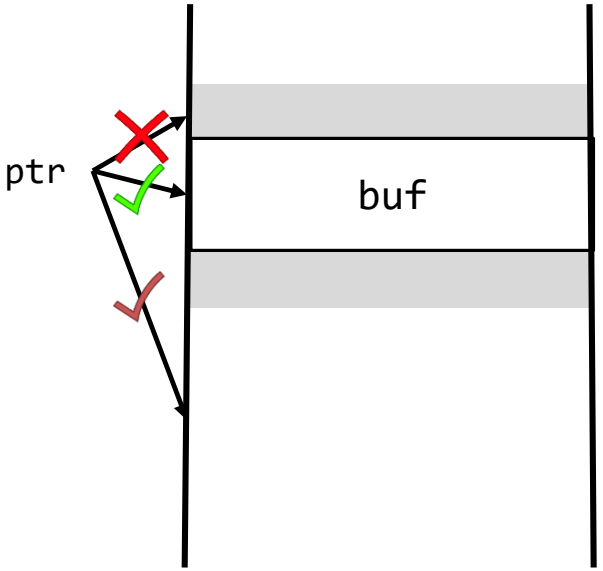
- **Whitelisting:** Pointer based
  - \+ Good coverage
  - \+ Temporal safety (for some)
  - \- Performance overhead
  - \- Implementation overhead
  - \- Imprecise



Previous H/W Solutions

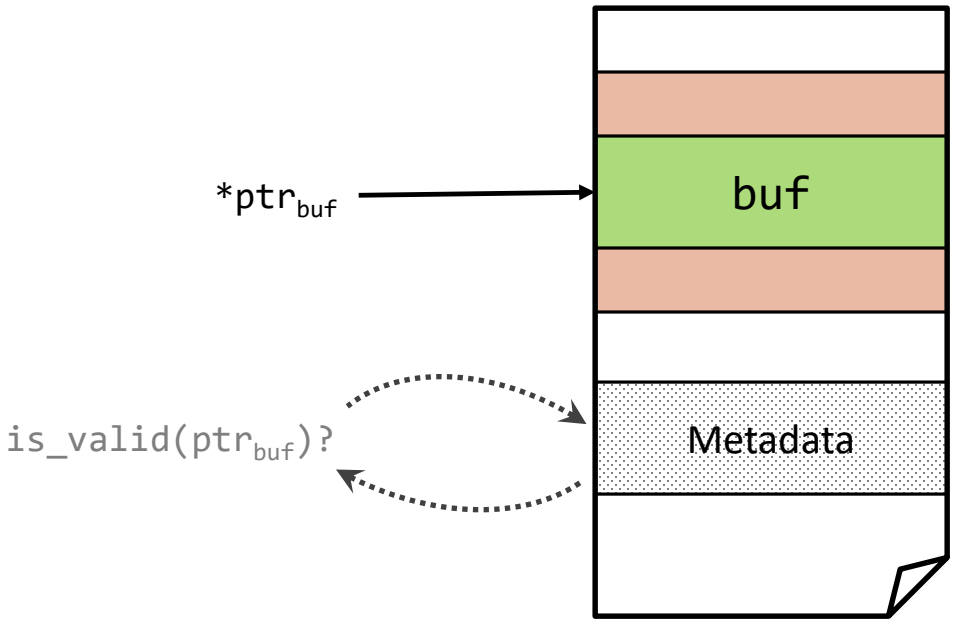
Mainly categorizable into 2 types.

- **Whitelisting:** Pointer based
  - \+ Good coverage
  - \+ Temporal safety (for some)
  - \- Performance overhead
  - \- Implementation overhead
  - \- Imprecise
- **Blacklisting:** Location based
  - \+ Fast
  - \- Weaker coverage (has false negatives)
  - \- Implementation overhead
  - \- No temporal protection



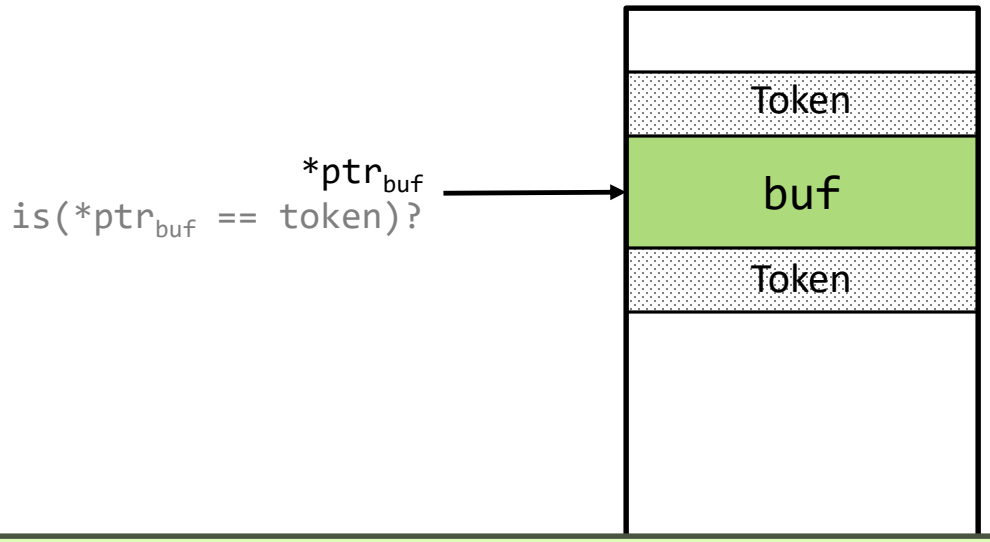
Previous H/W Solutions

Tag-based



REST: Primitive Overview

Content-based blacklisting



REST primitive has trivial complexity, overhead

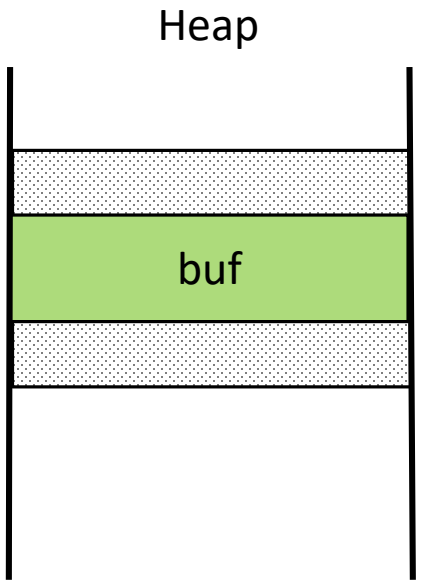
REST: Spatial Memory Safety

REST: Temporal Memory Safety

REST Software

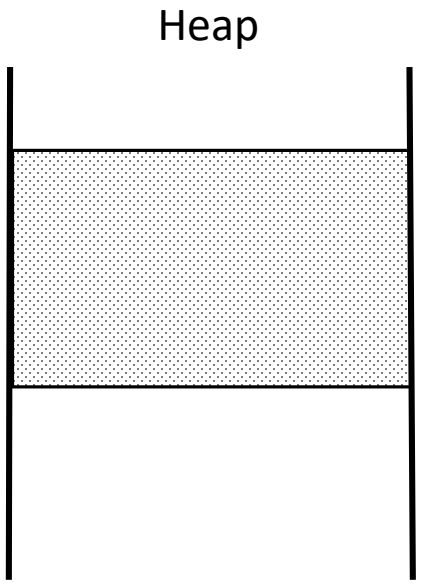
Heap Safety

- Allocate and bookend region, `malloc` to program



Heap Safety

- Allocate and bookend region, `malloc` to program
- REST'ize at `free`
- Do not reallocate region until heap sufficiently consumed



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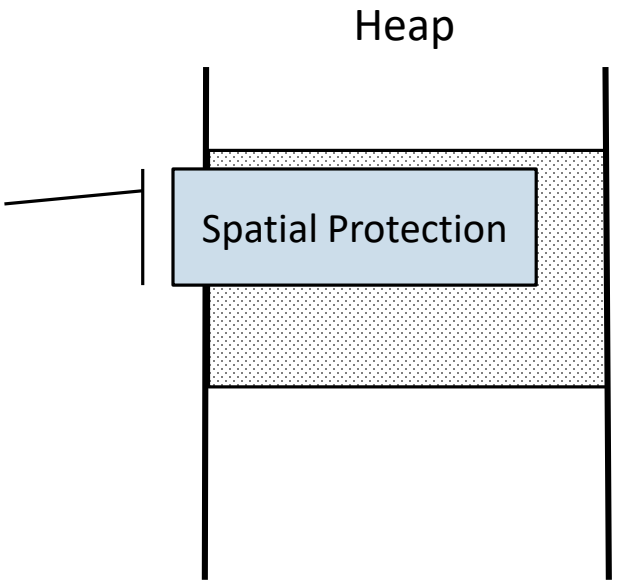

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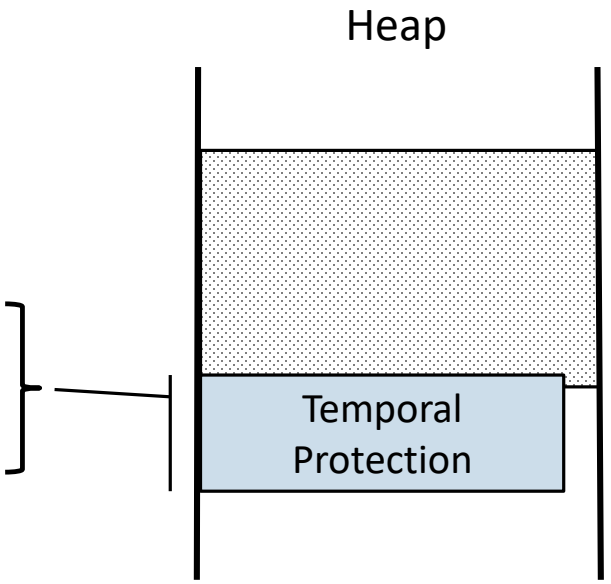
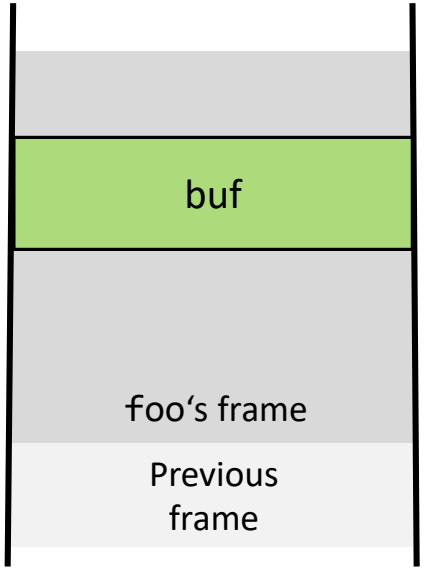


Can be enabled for legacy binaries

Stack Safety

```
void foo() {
    char buf[64];
    …
    return;
}
```



Stack Safety

```
void foo() {
    char rz1[64];
    char buf[64];
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    arm(rz1);
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    …
    disarm(rz1);
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}
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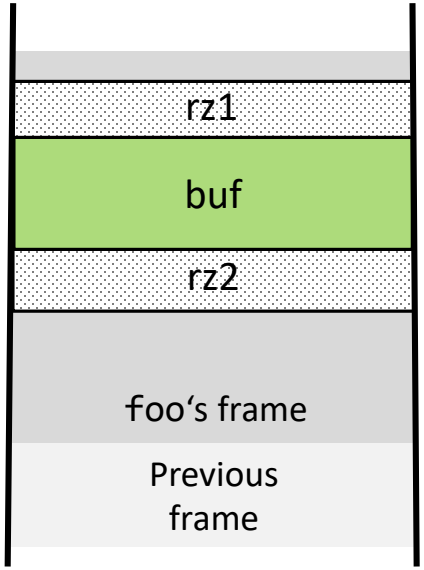

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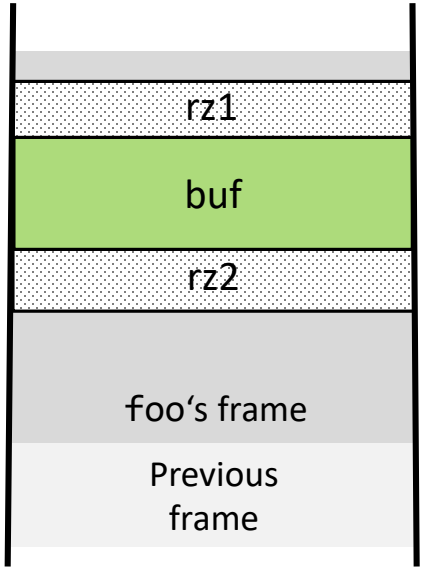

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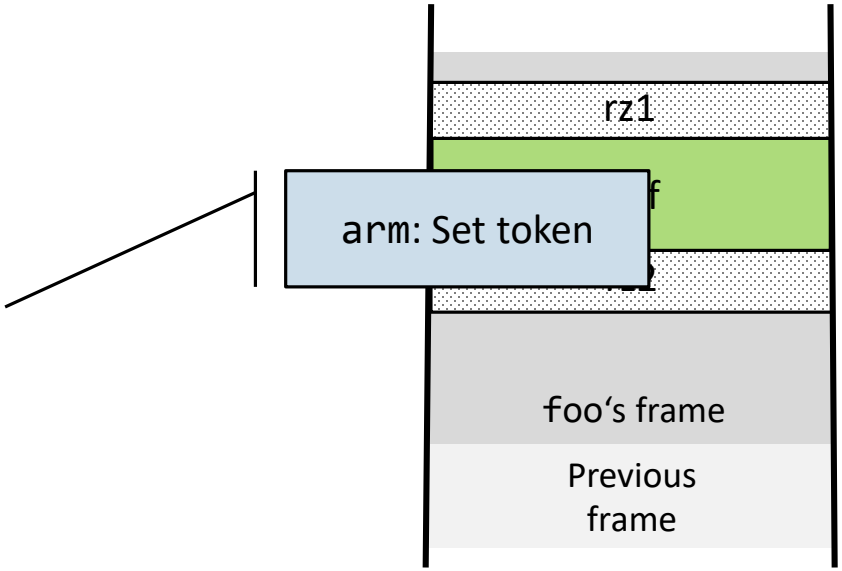

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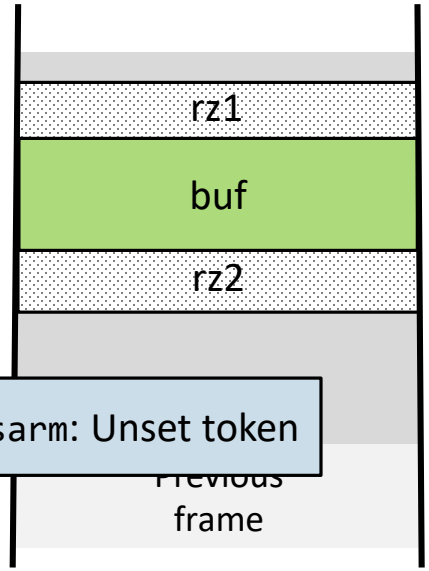

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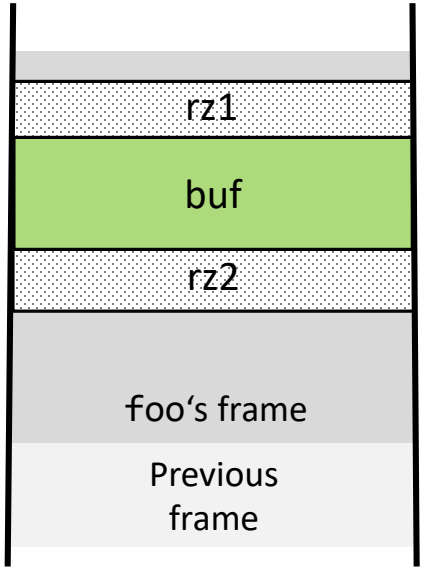
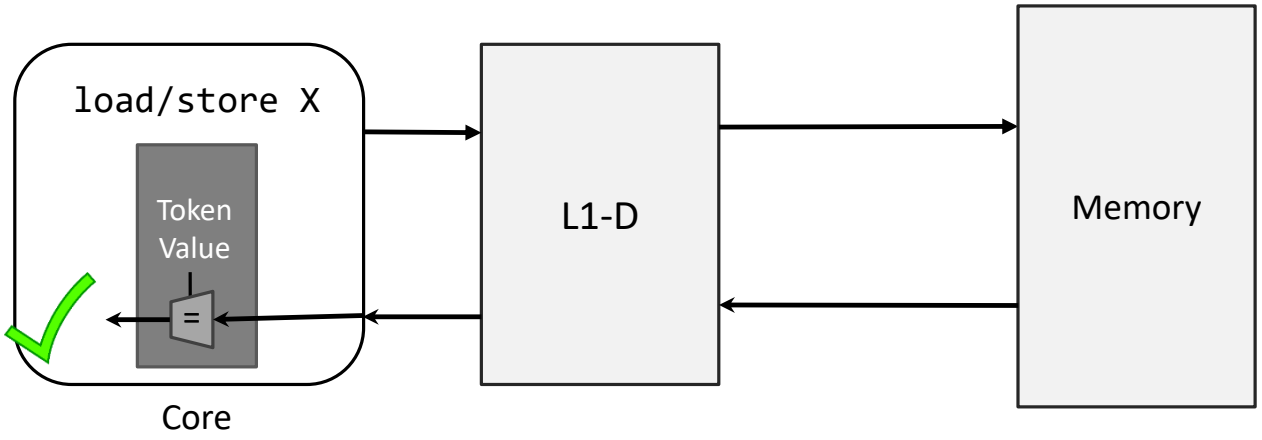


Requires recompilation with *REST* plugin

REST Hardware

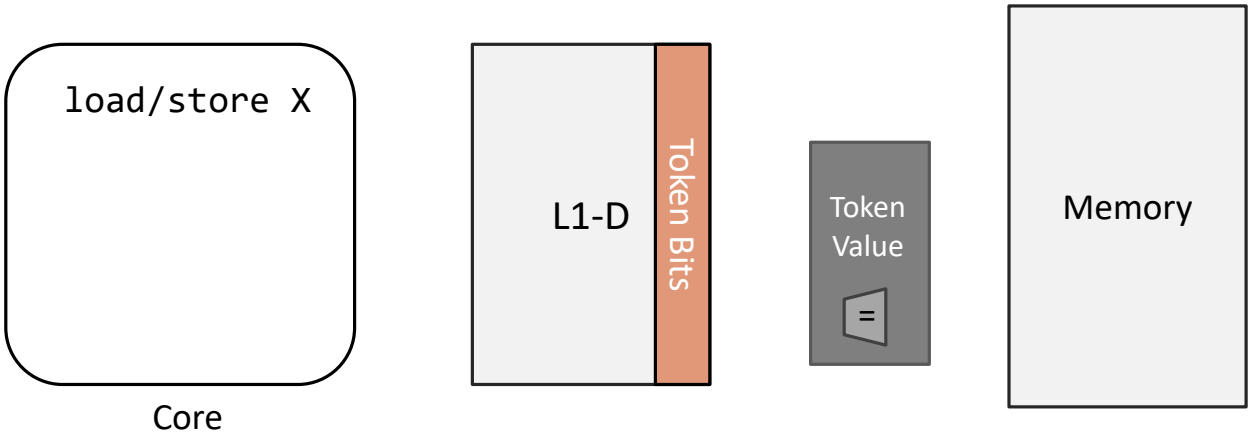
Naïve Design

Every store involves an extra load → Complicated and expensive

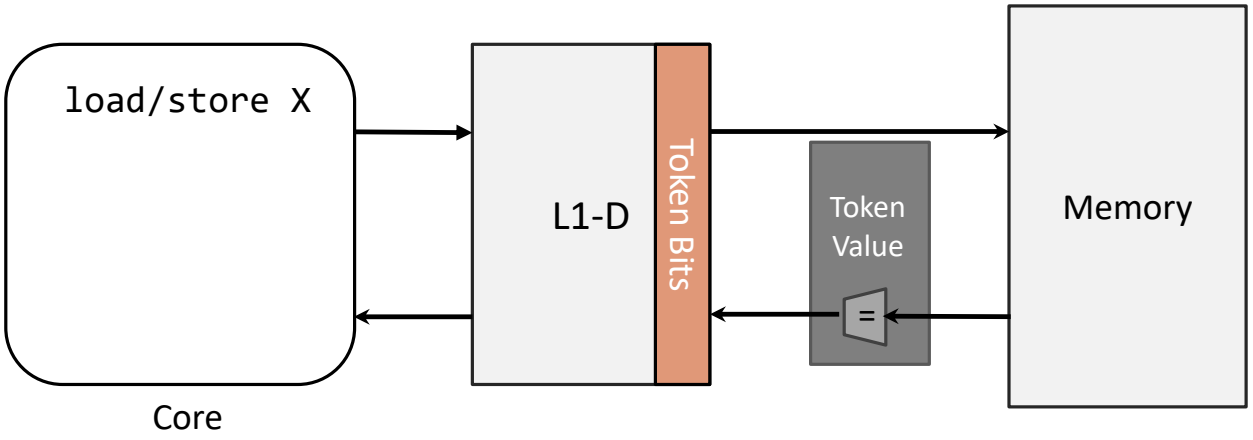


Cache Modifications

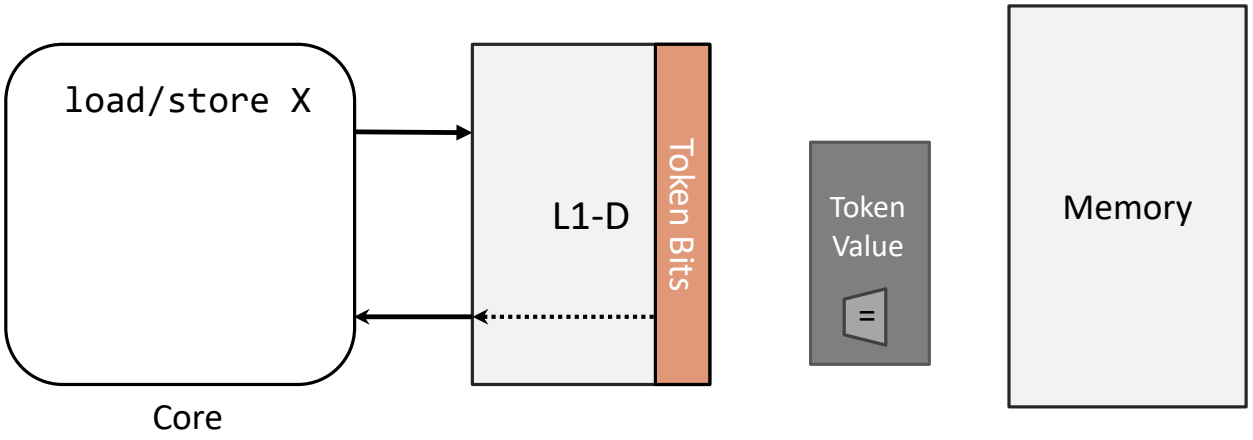
Comparator at L1-D mem interface + 1b per L1-D line



Cache Miss

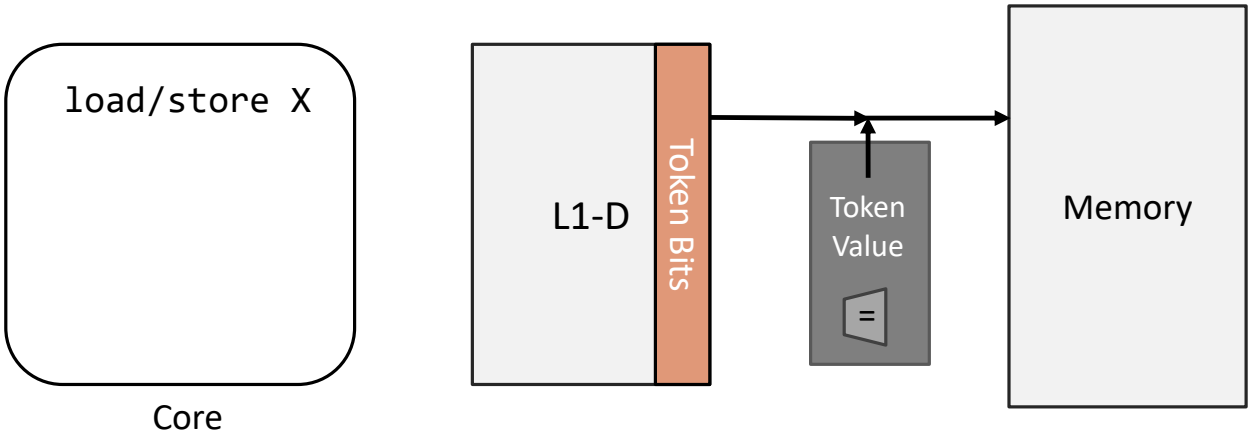


Cache Hit



Cache Eviction

Armed outgoing line filled with token value



What about the core?

TODO: Have to support arms and disarms

- 512b writes
- Special semantics: can only touch token with `disarm`

LSQ design concerns:

- Forwarding would break semantics
- 512b data entries
- How to match unaligned token access?

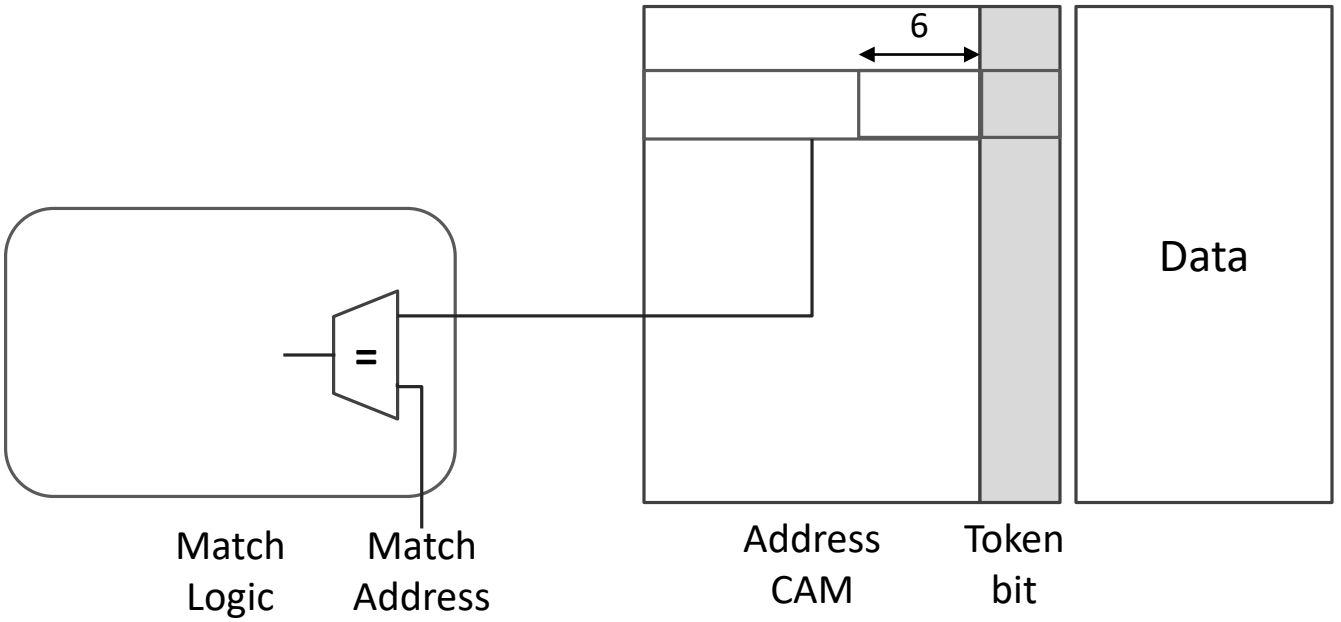
Load-Store Queue

- Forwarding breaks semantics
- 512b data entries
- Detecting unaligned token access

Add 1b tag

Only update token bit

Split regular match logic



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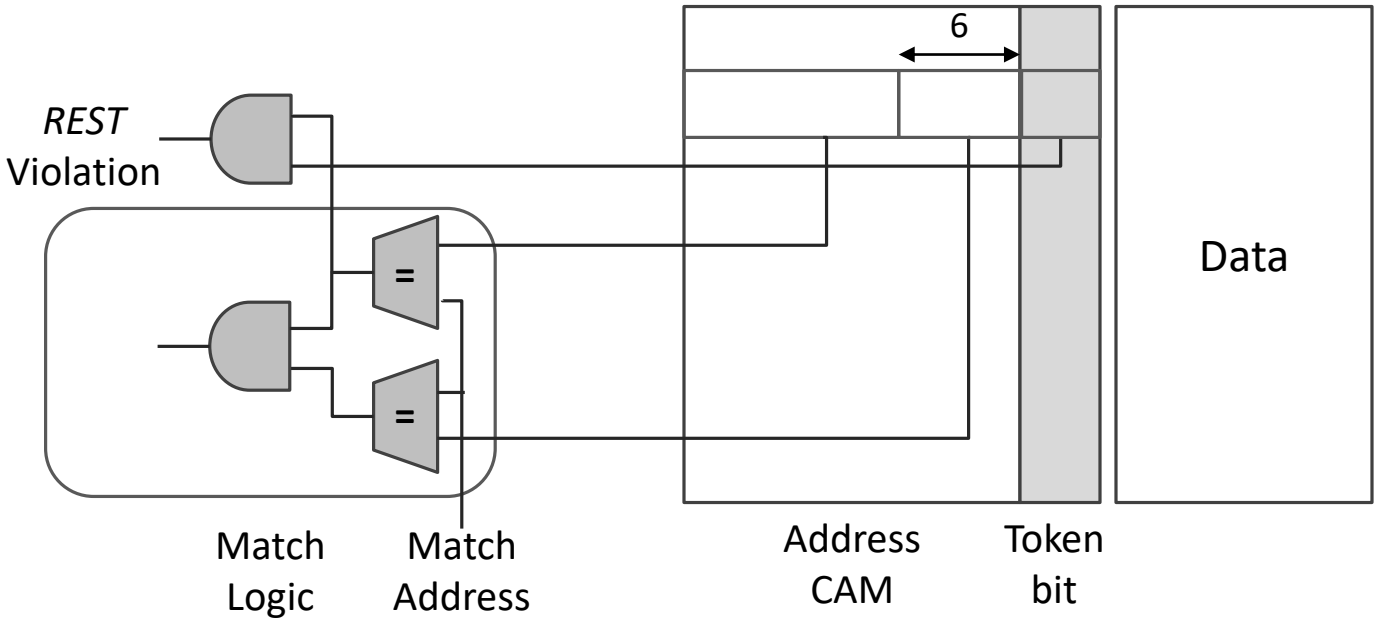
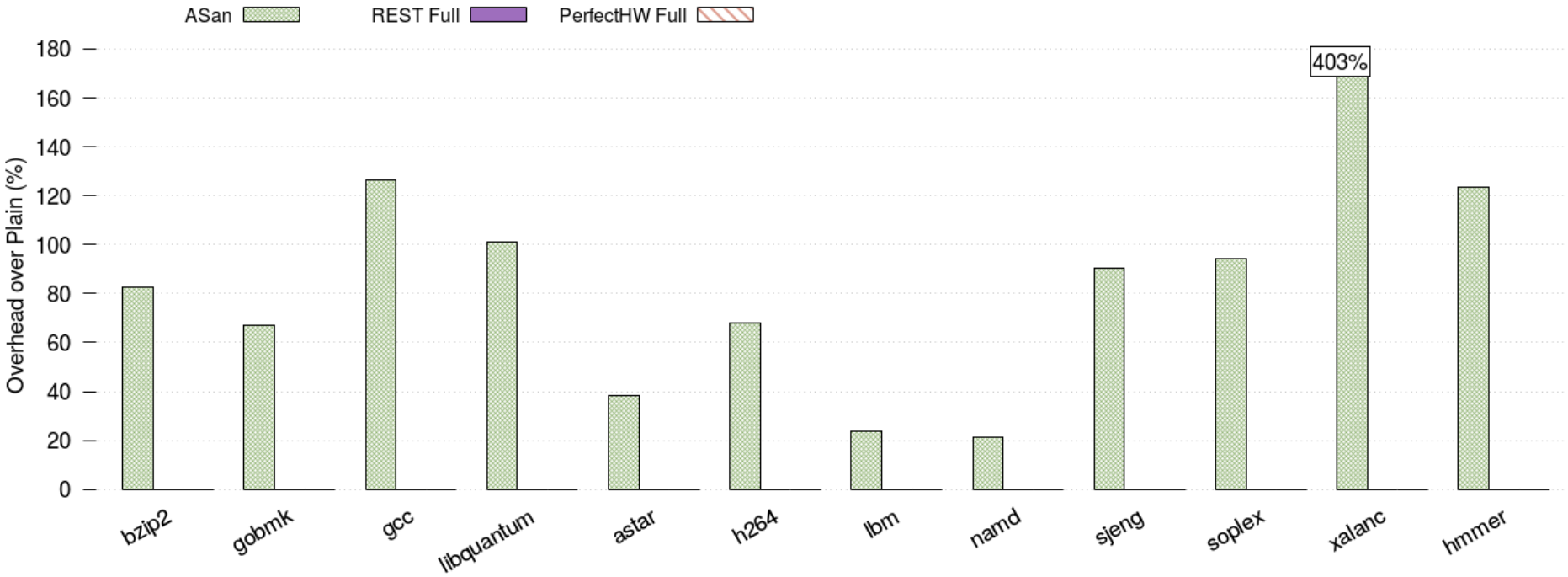


REST Overhead

REST Performance



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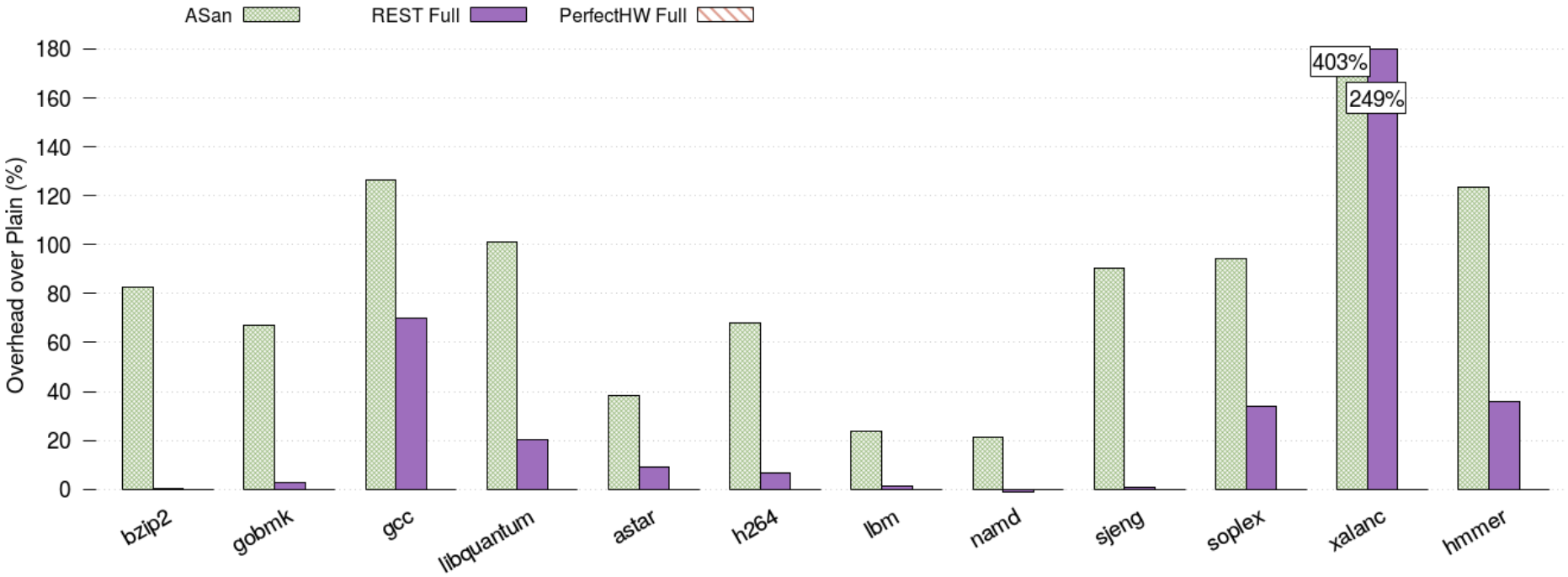

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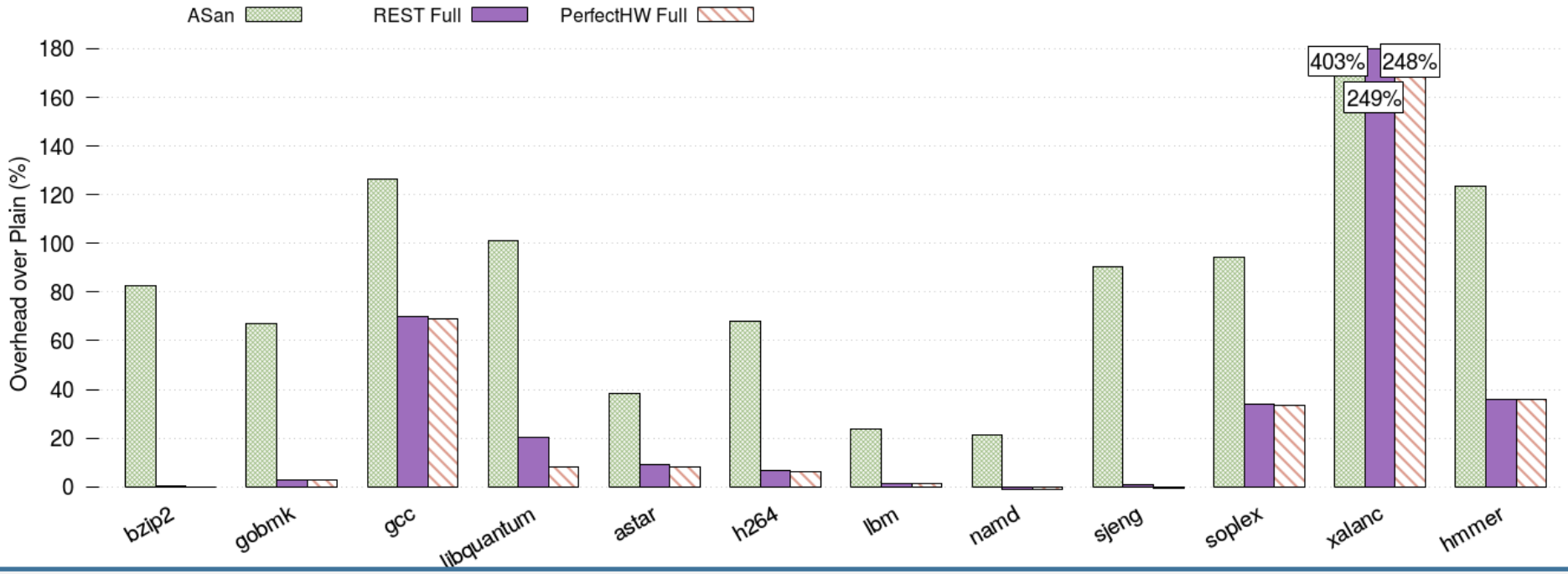

REST primitive overhead near-zero.

Software overhead mostly from allocator.

To conclude…

REST: Hardware/software mechanism to detect common memory safety errors

- Low overhead, low complexity hardware implementation
- Heap safety for legacy binaries

22-90% faster than comparable software solution on SPEC CPU

Questions?