Divider / PFD

조교 조성근

개요

- TSPC DFF
- Divider
- PFD

D Flip-Flop

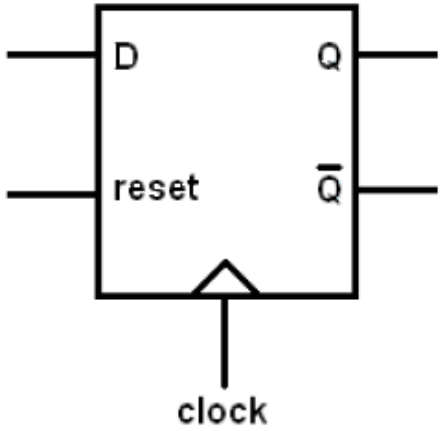


Fig. 1 Block Diagram

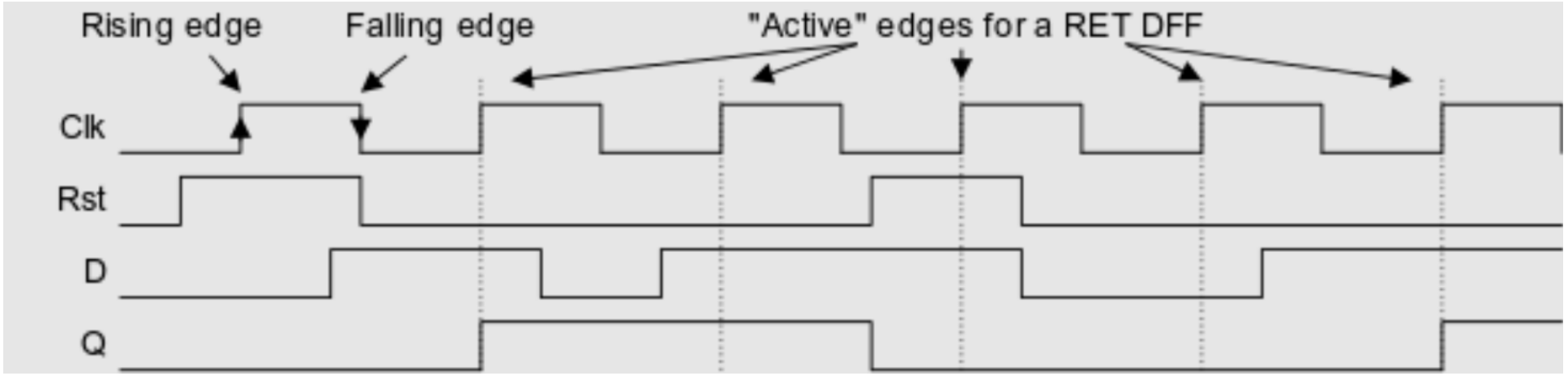
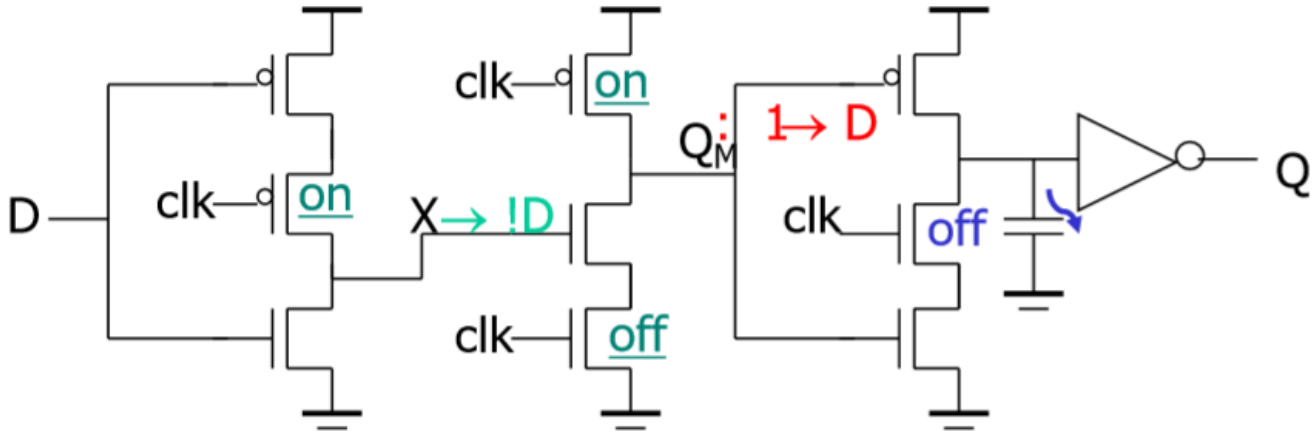
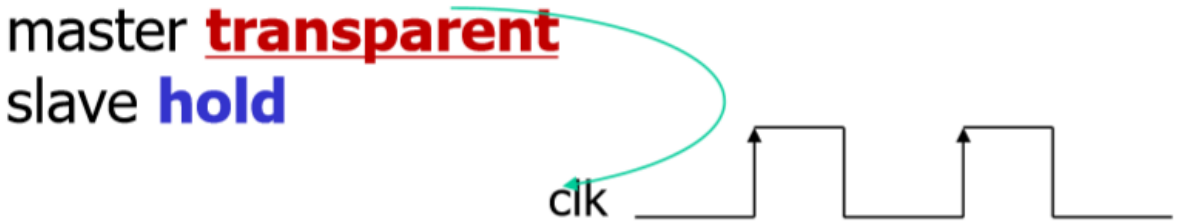


Fig. 2 Timing Diagram

TSPC(True Single Phase Clocked) FF

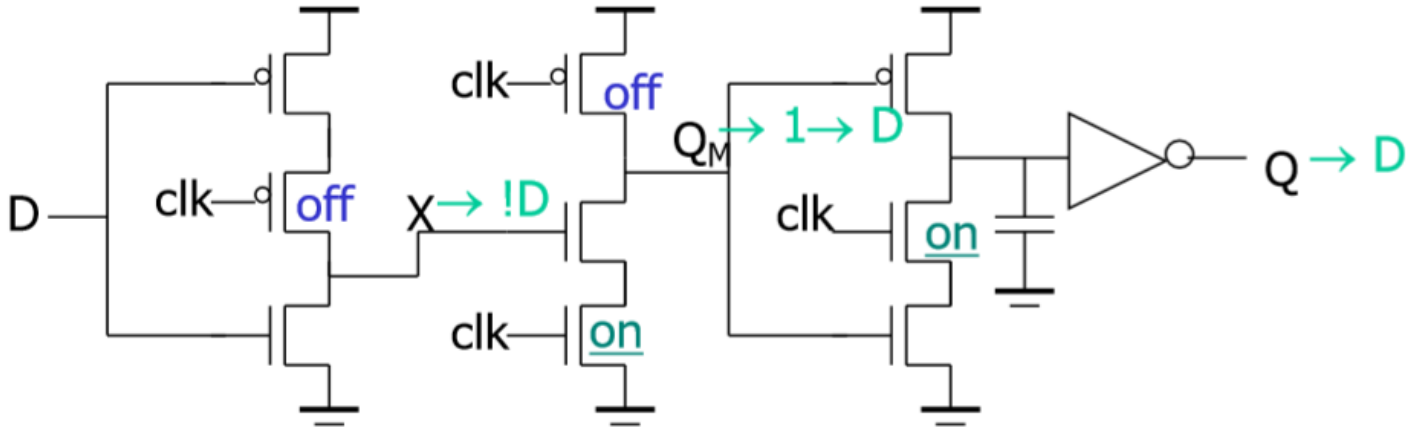
- Clock Low

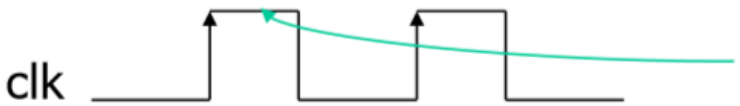




TSPC(True Single Phase Clocked) FF

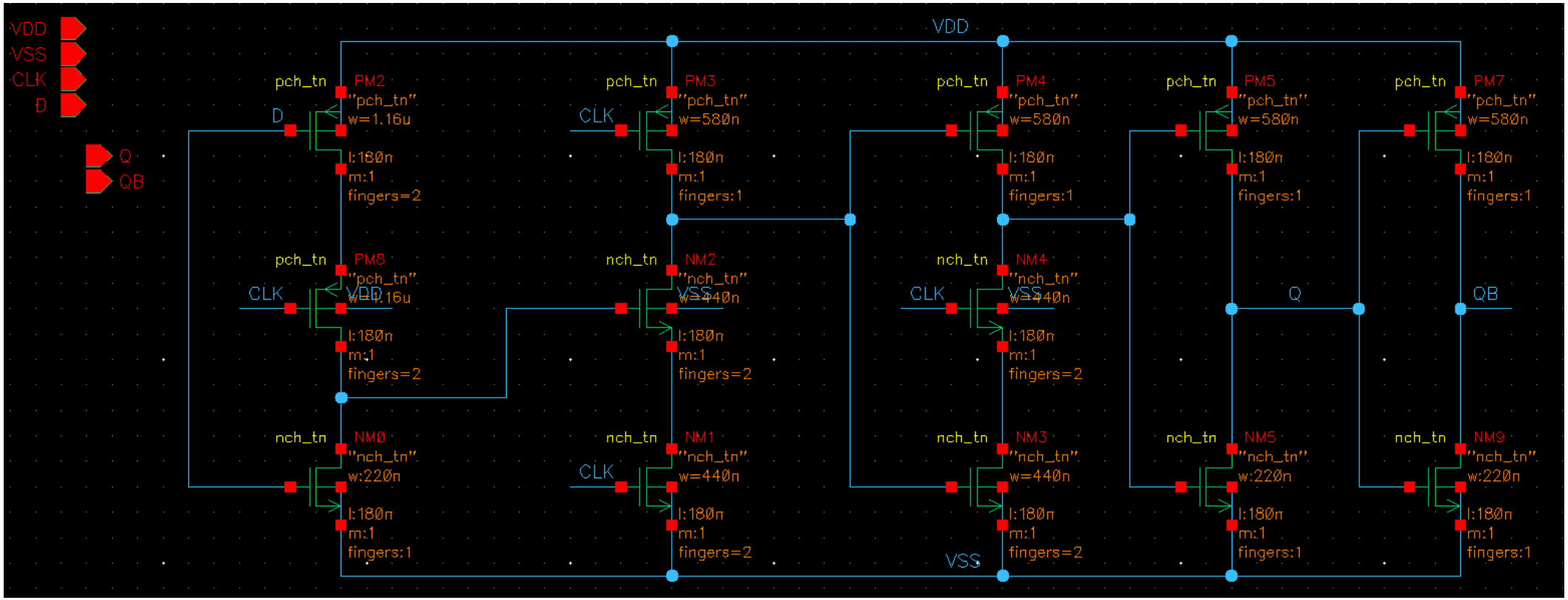
- Clock High





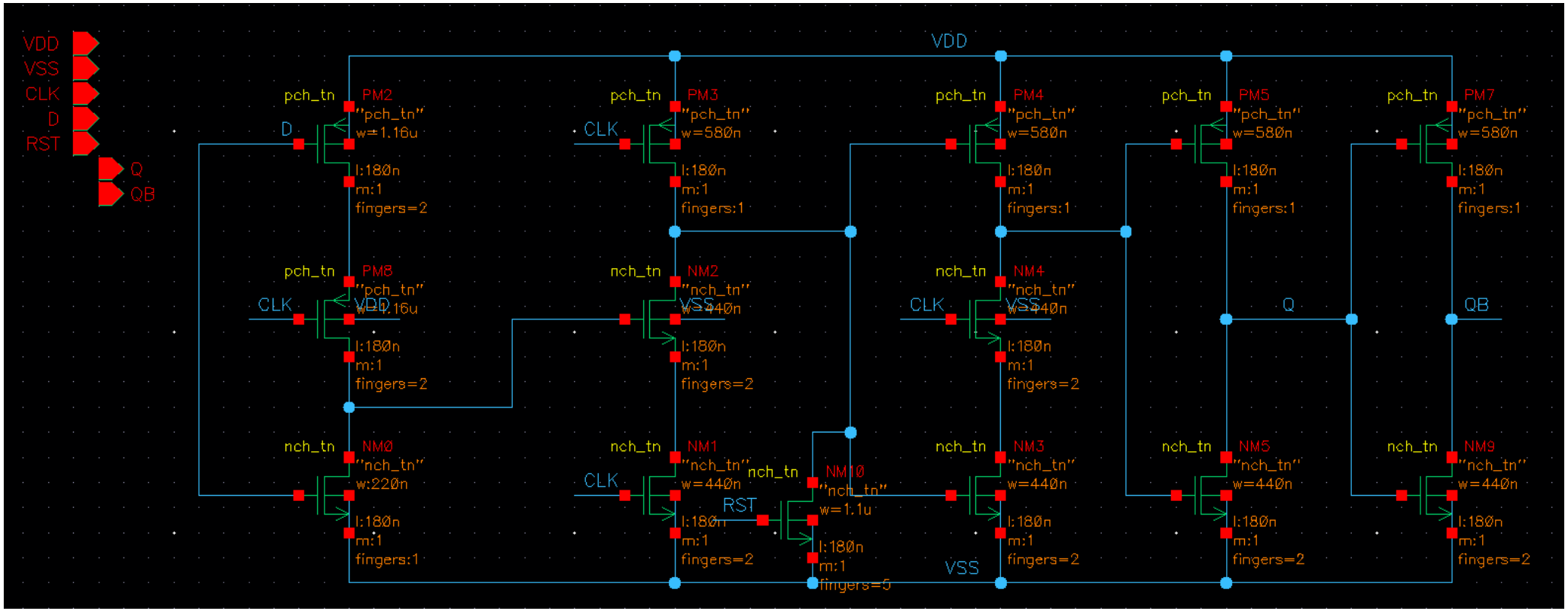
master **hold**
slave **transparent**

TSPC_DFF



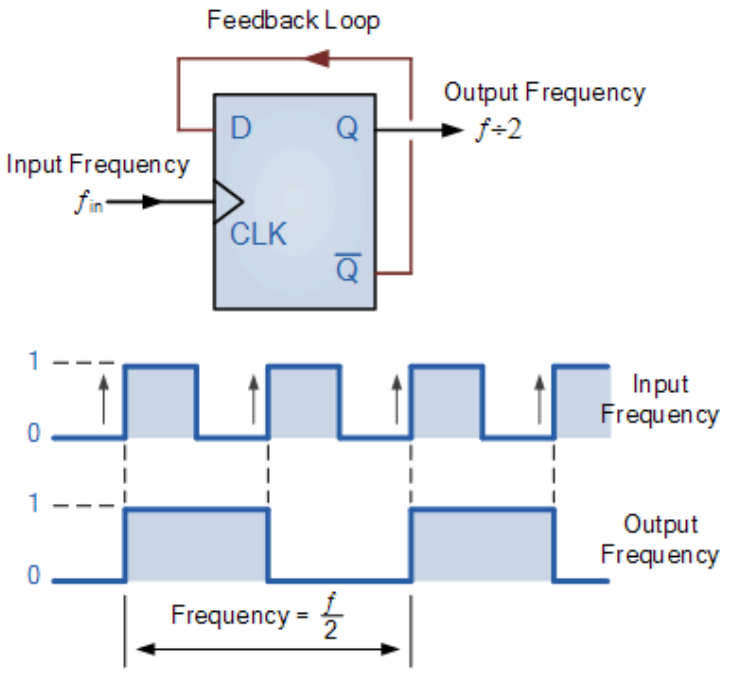
- CLK : 1GHz
- D : 1.3GHz

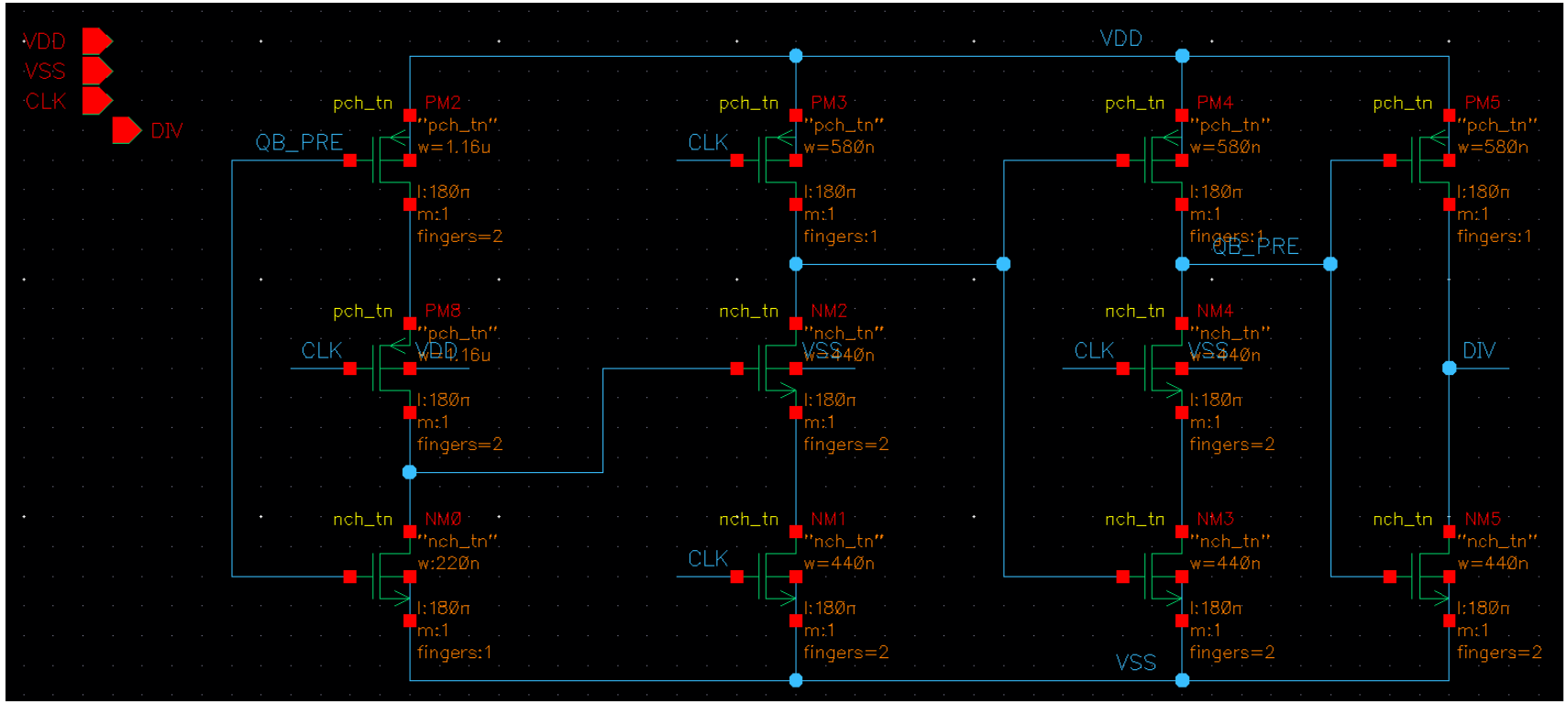
TSPC_DFF_RST



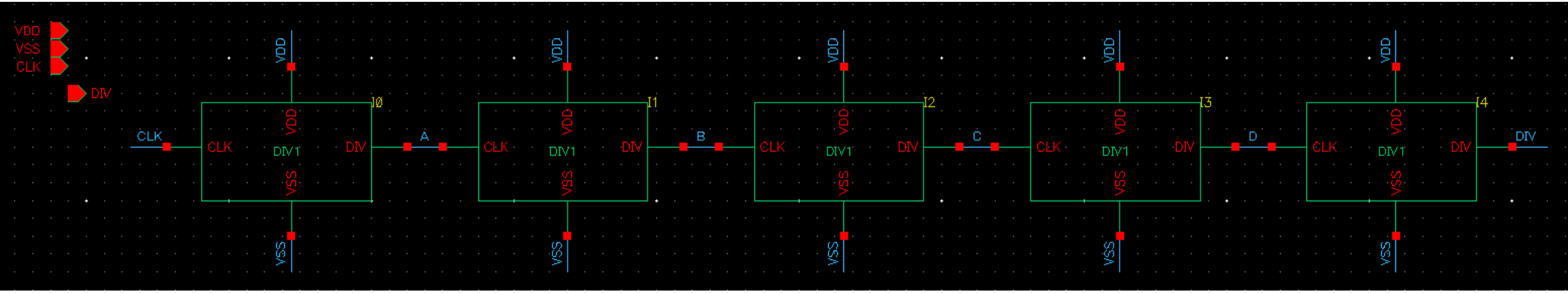
※ 과제

Divider


Feedback Loop
Output Frequency
$f \div 2$
D
Q
Input Frequency
f_{in}
CLK
$\overline{Q}$
1
0
Input Frequency
1
0
Output Frequency
Frequency = $\frac{f}{2}$

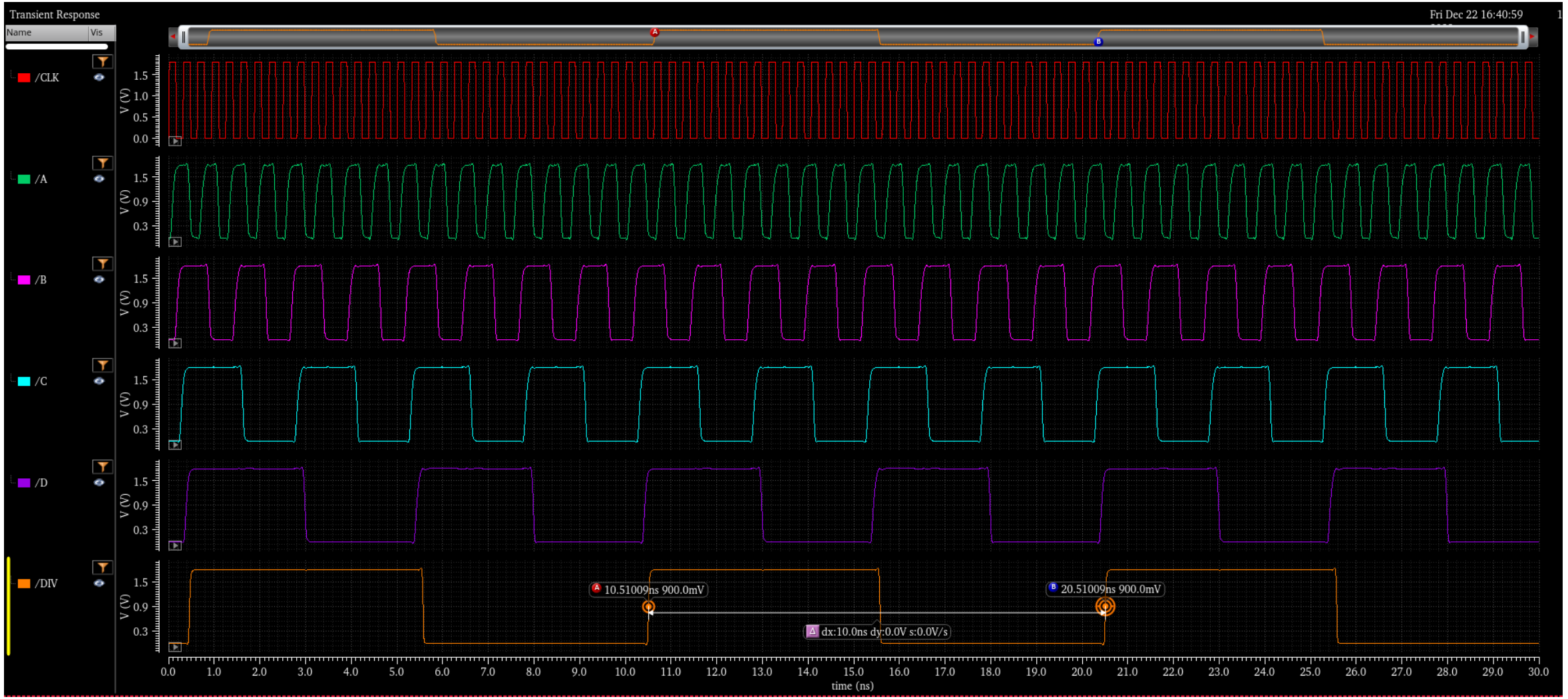

VDD
VSS
CLK
DIV
QB_PRE
pch_tn
nch_tn
PM2
PM3
PM4
PM5
PM8
NM0
NM1
NM2
NM3
NM4
NM5
"pch_tn"
"nch_tn"
w=1.16u
w=580n
w=440n
w:220n
l:180n
m:1
fingers=2
fingers:1

Divider x5

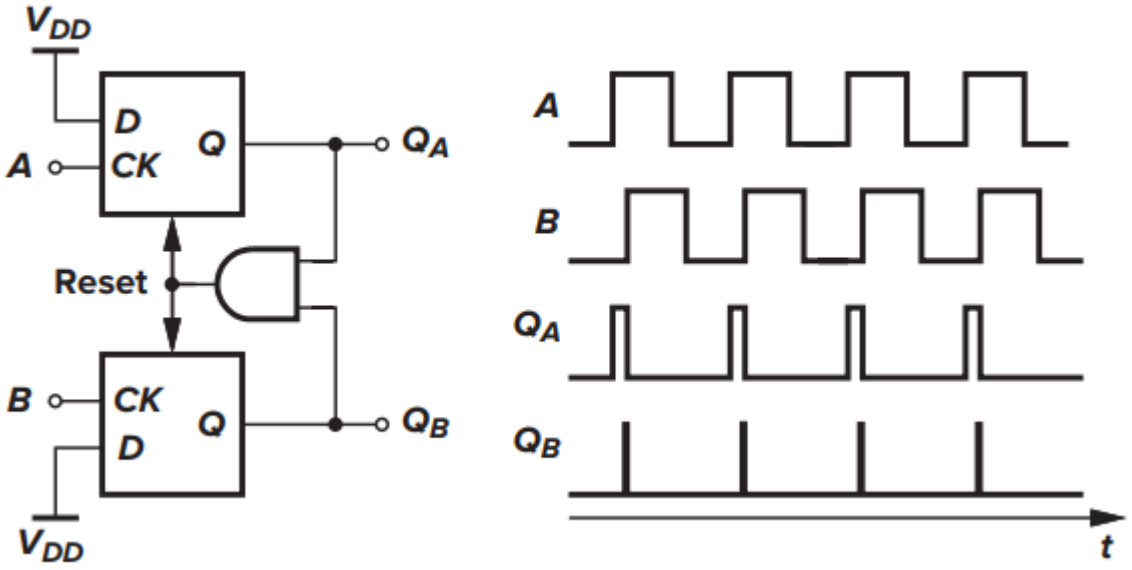


- PLL Target
- Ref. CLK : 100 MHz
- Target CLK : 3.2GHz

Divider x5

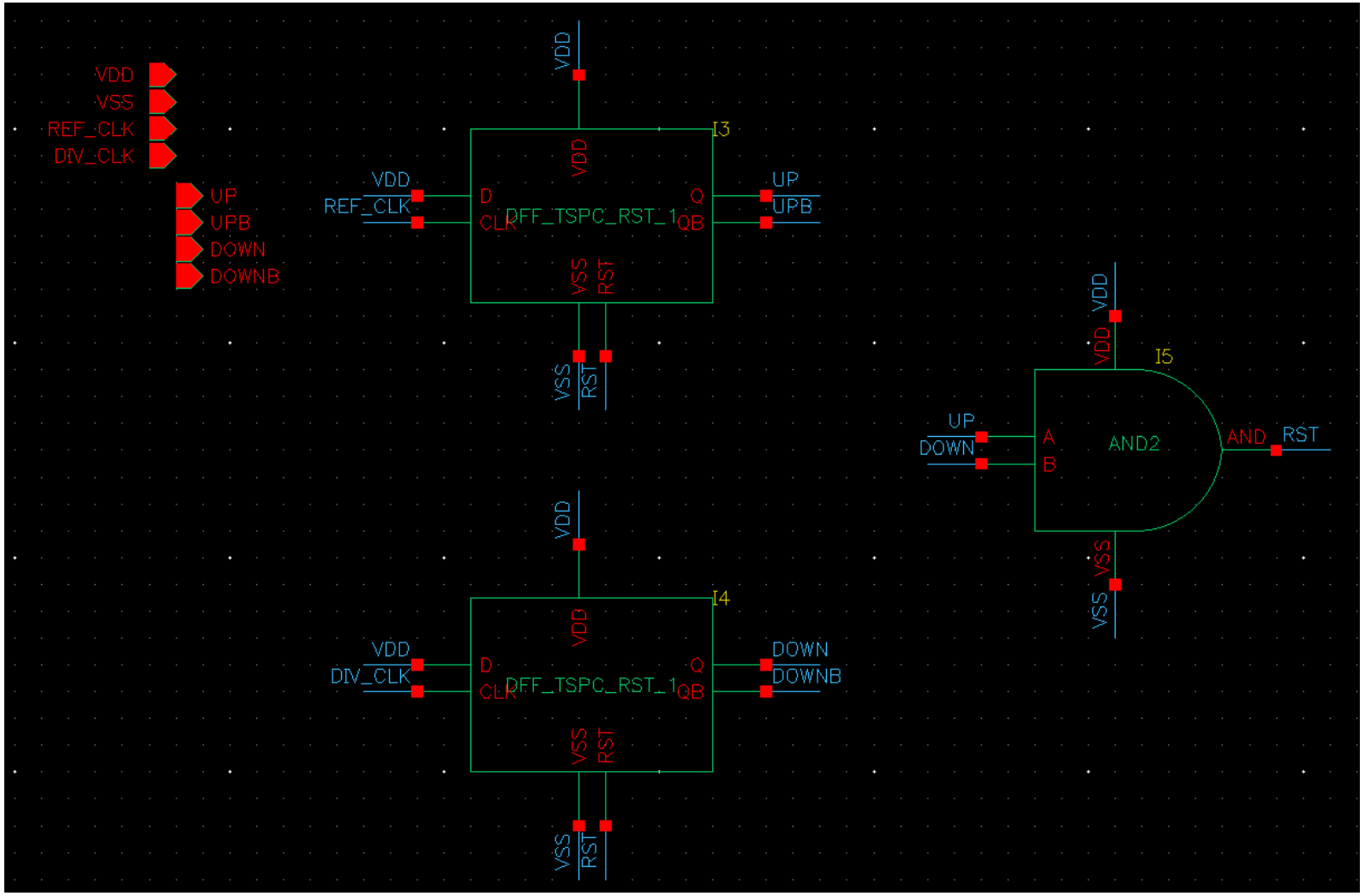

Transient Response
Fri Dec 22 16:40:59
Name
Vis
/CLK
/A
/B
/C
/D
/DIV
V (V)
10.51009ns 900.0mV
20.51009ns 900.0mV
dx:10.0ns dy:0.0V s:0.0V/s
time (ns)

PFD 동작 원리

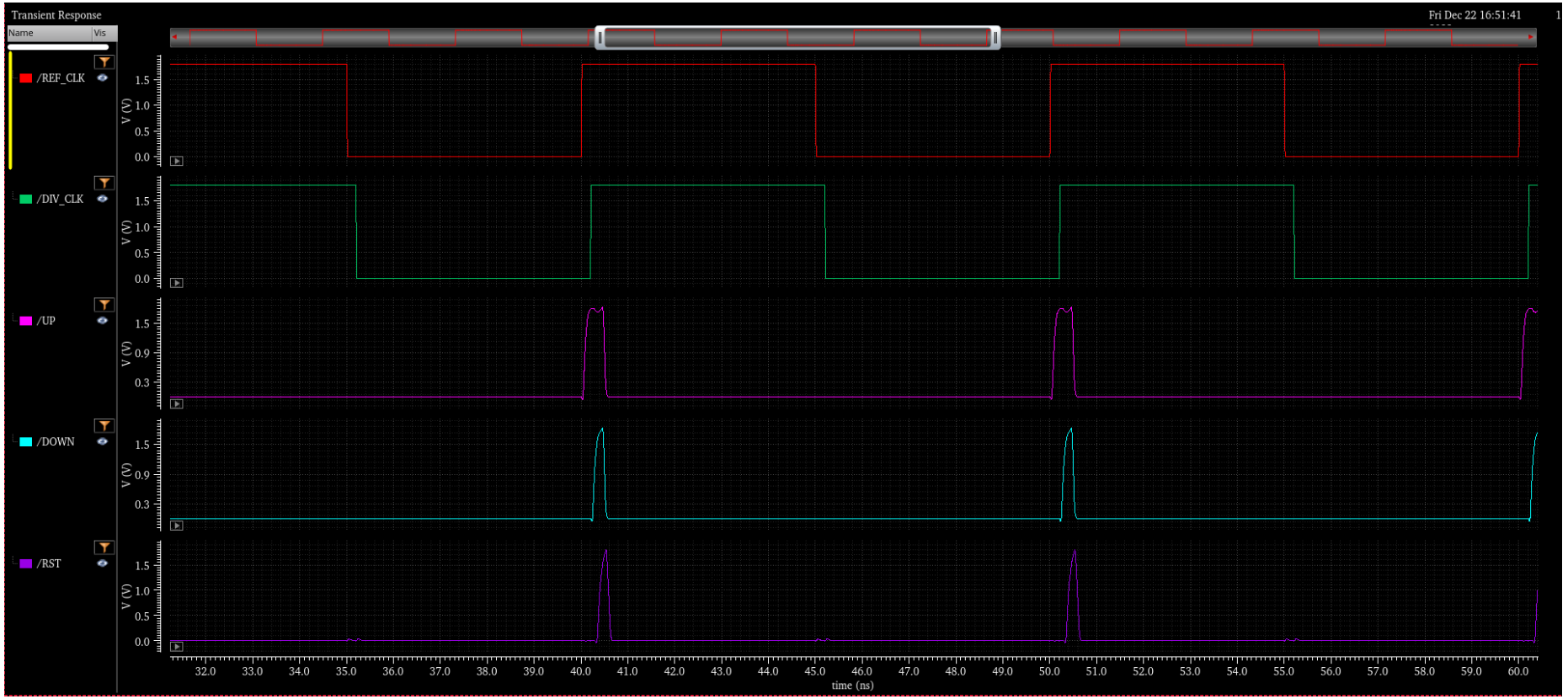


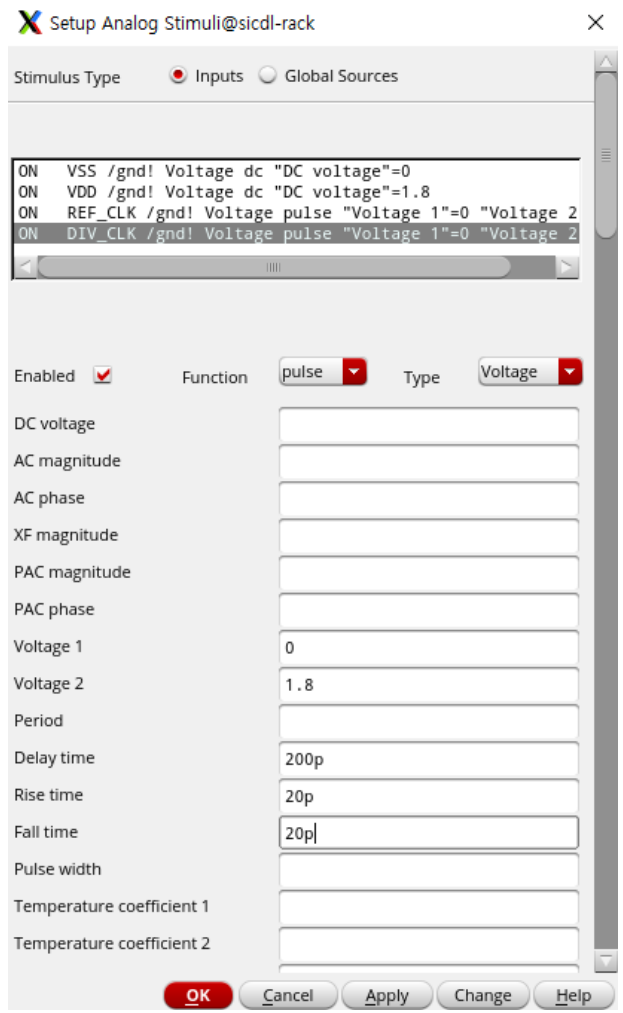
- 위상 정보를 전압으로 출력
- Q_A : UP 신호
- Q_B : DOWN 신호
- UP 신호가 출력되면 주파수 UP
- DOWN 신호가 출력되면 주파수 DOWN

PFD schematic



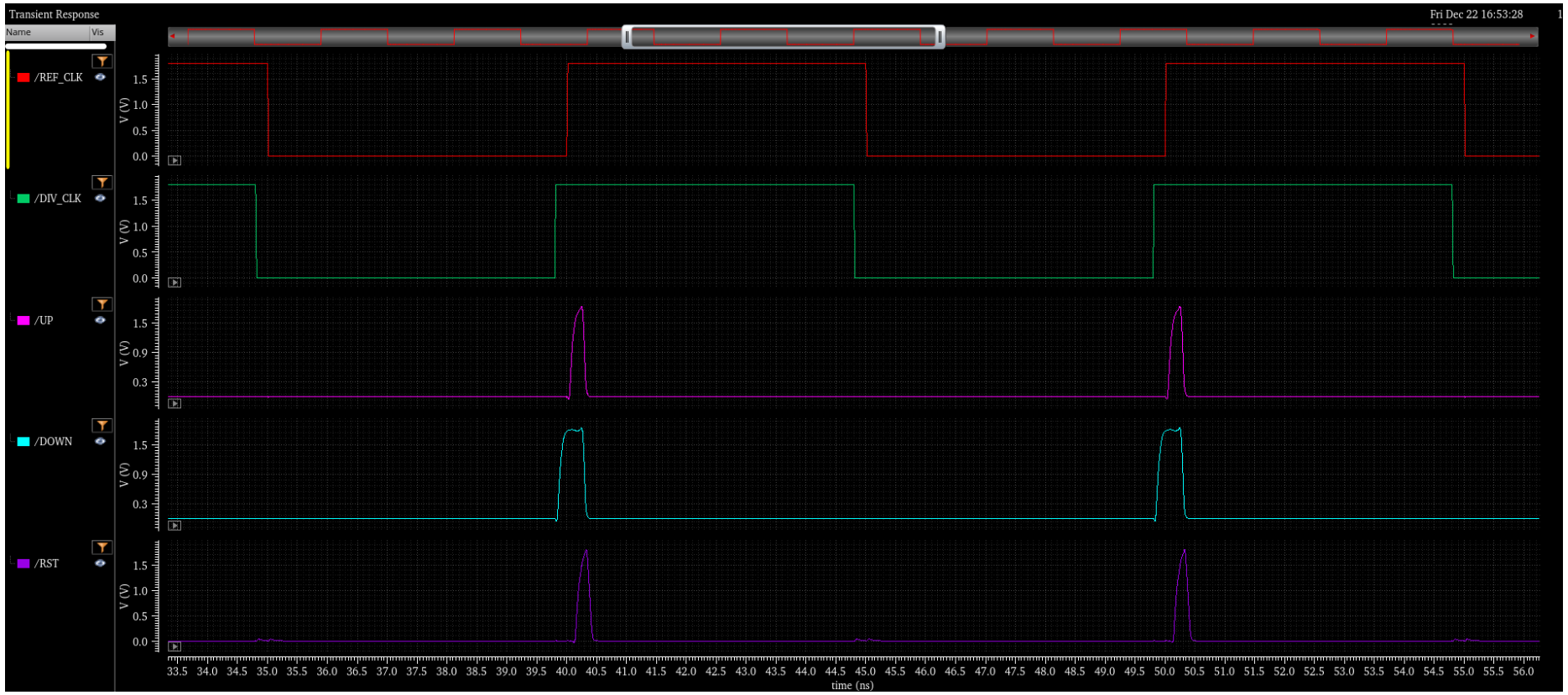
PFD_Simulation (과제)

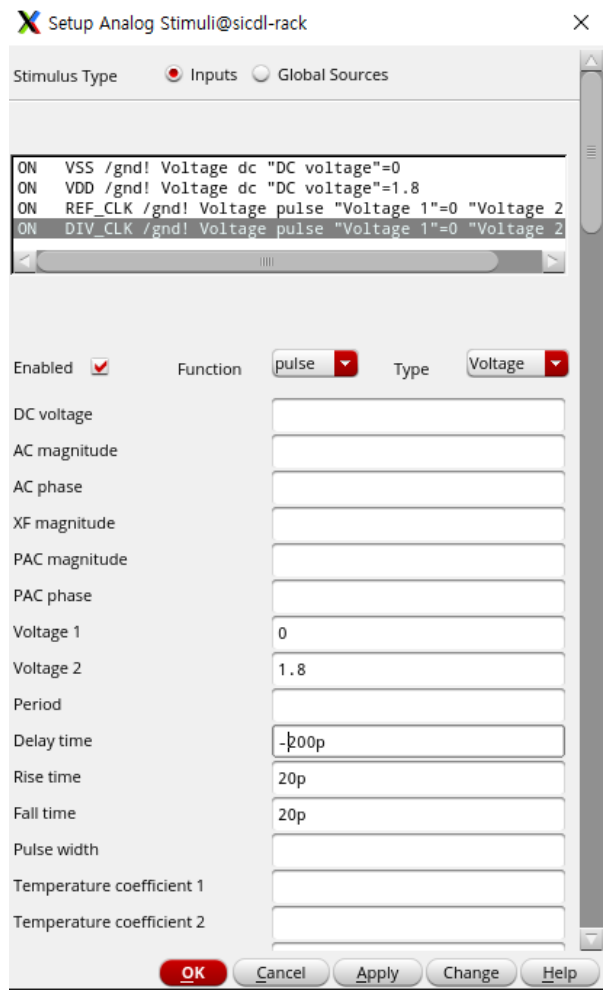




- REF_CLK : 100MHz, DIV_CLK : 100MHz
- Delay : 200ps

PFD_Simulation (과제)





- REF_CLK : 100MHz, DIV_CLK : 100MHz
- Delay : -200ps