research_apprx_computing

Post-Layout Based Comparison of InXA Adder Cell

A Comparative Study on Pass Gate-Based Adder Cell Structures for Approximate Computing

Circuits and System Laboratory, Inha University

Jun Yeong Chang (jjy1019@inha.edu)

2025-05-09

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3	성능 비교 결과 요약 (표)	#1. 지표 : - Tr. 개수 - 면적 - 소비 전력 - 지연 시간 - 출력 전압 스윙범위
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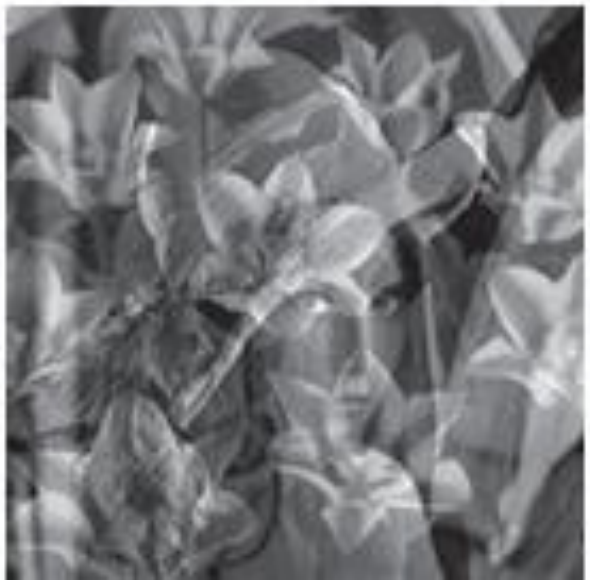
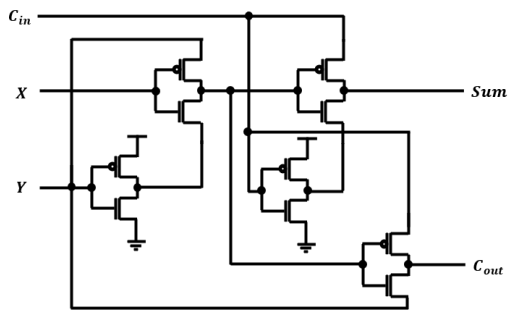
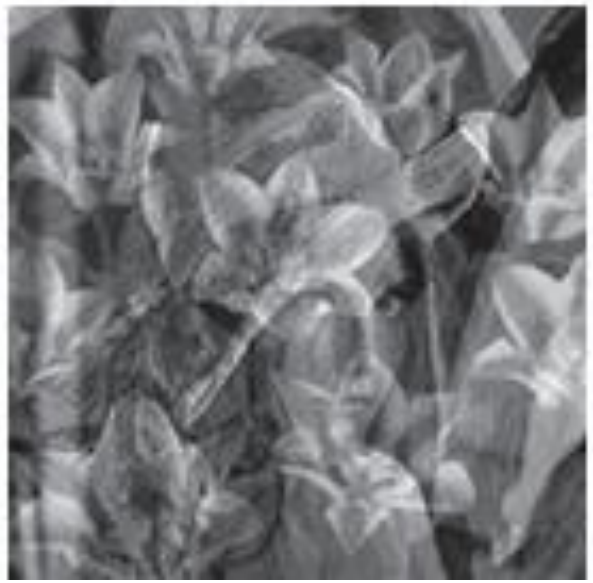
1. 연구 배경 및 기존 논문 한계

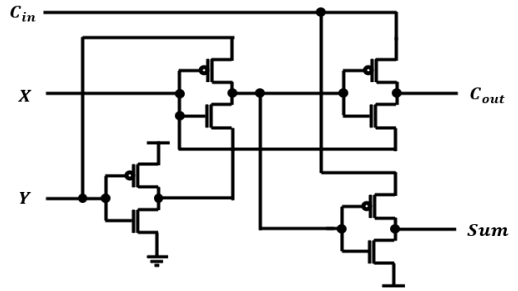
1. 정확하지 않아도 괜찮은 연산, 왜 필요할까?





Accurate Adder



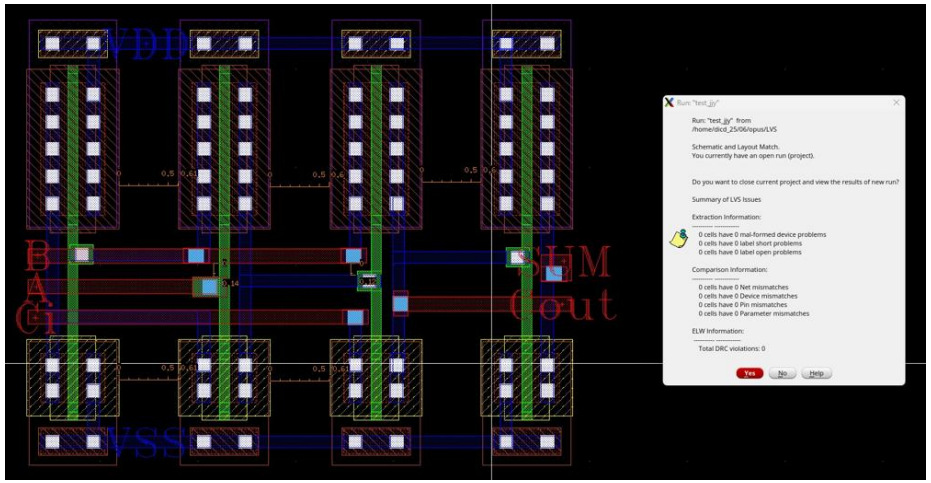


In-exact Adder

2. 실제 회로 구현 후 검증 미흡

Inputs			Exact Outputs		Proposed Inexact Adder Cells					
					InXA1		InXA2		InXA3	
X	Y	C_{in}	Sum	C_{out}	Sum	C_{out}	Sum	C_{out}	Sum	C_{out}
0	0	0	0	0	0✓	0✓	0✓	0✓	1✗	0✓
0	0	1	1	0	1✓	1✗	1✓	0✓	1✓	0✓
0	1	0	1	0	1✓	0✓	1✓	0✓	1✓	0✓
0	1	1	0	1	0✓	1✓	1✗	1✓	0✓	1✓
1	0	0	1	0	1✓	0✓	1✓	0✓	1✓	0✓
1	0	1	0	1	0✓	1✓	1✗	1✓	0✓	1✓
1	1	0	0	1	0✓	0✗	0✓	1✓	0✓	1✓
1	1	1	1	1	1✓	1✓	1✓	1✓	0 ✗	1✓

VS.



2. 연구 방법 (설계 방식)

1. 왜 Pass Gate로 구현했는가?

1) Pros
- 적은 트랜지스터 개수
- 고속 저전력 회로에 유리

2) Cons
- Output Voltage Drop

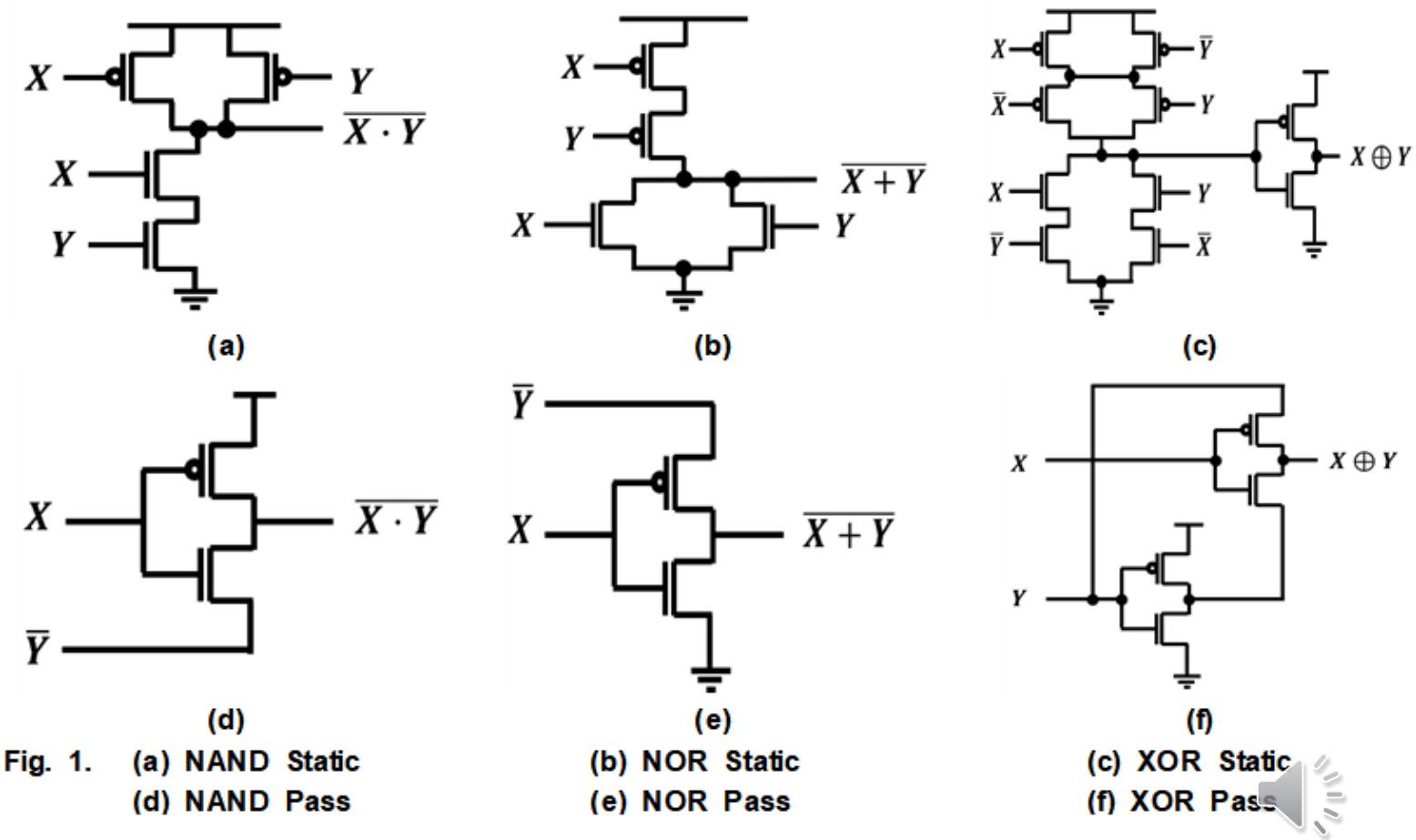


Fig. 1. (a) NAND Static (b) NOR Static (c) XOR Static
(d) NAND Pass (e) NOR Pass (f) XOR Pass

2. Post-Layout Simulation

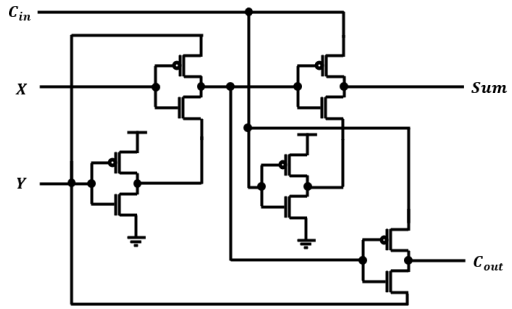
[설계 및 시뮬레이션, 공정 조건]
- 설계 / 시뮬레이션 Tool : Cadence Virtuoso / Spectre
- PDK : GPDK 90nm
- Supply Voltage : $V_{DD} = 1.2(V), V_{SS} = 0(V)$

[동작 조건]
- 온도 : 25℃
- Corner : NN (Normal-Normal)
- Input signal : $A(T_A = 4ns), B(T_B = 2ns), C_{in}(T_{C_{in}} = 1ns)$ / Rising&Falling time = 10(ps)

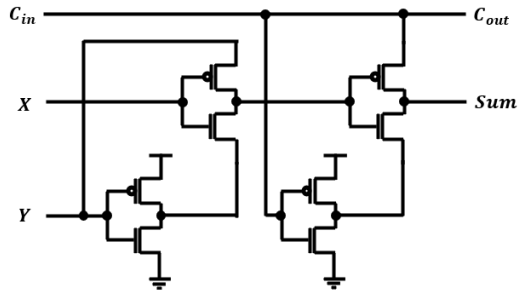
[측정 항목]
- Transistor 개수
- Layout 면적
- 소비 전력
- 전파 지연
- 출력 전압 스윙

3. Post-Layout Simulation 결과

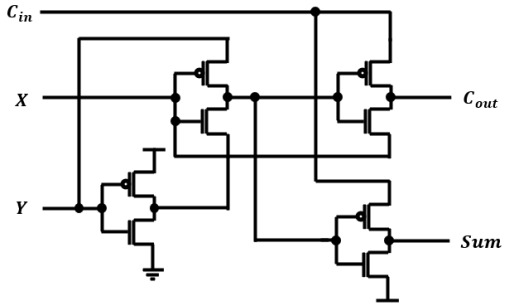
1. Transistor 개수



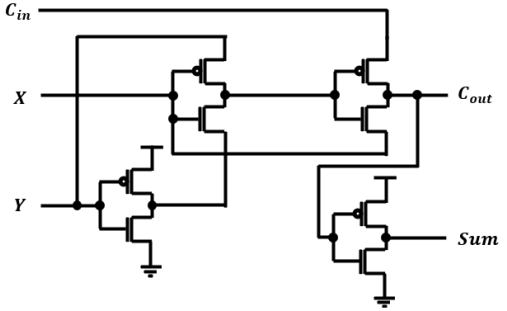
Accurate



InXA1

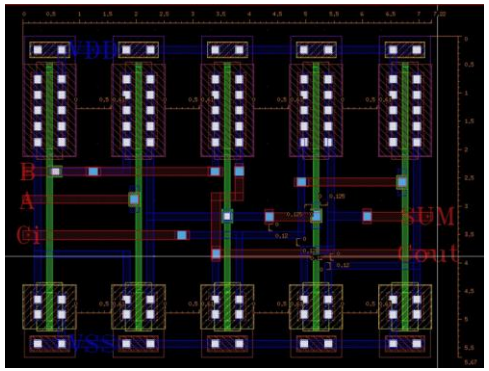


InXA2

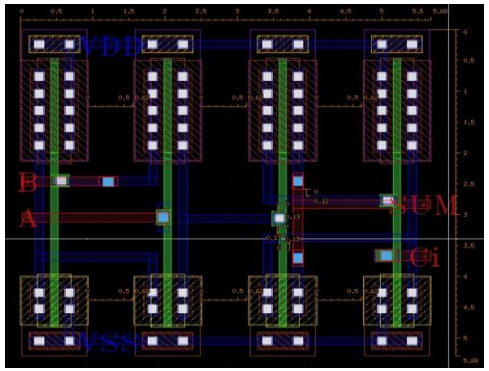


InXA3

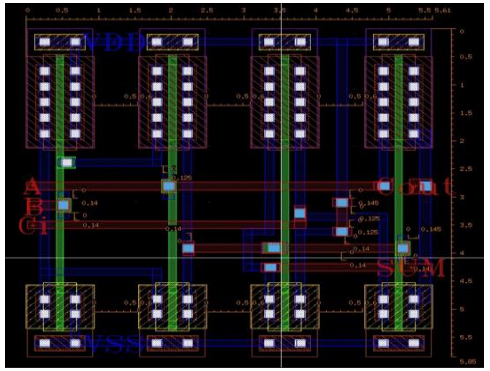
2. Layout 면적



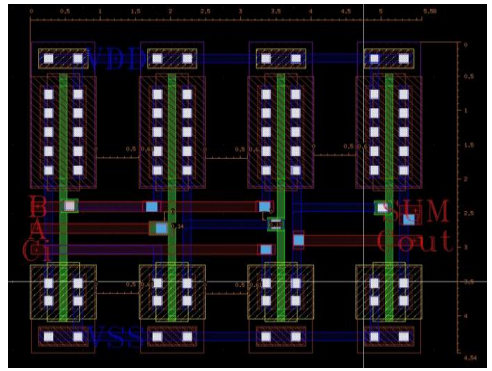
Accurate



InXA1



InXA2



InXA3

3. 소비 전력

	Expression	Value
1	average(getData...	21.84E-6

Accurate

	Expression	Value
1	average(getData...	22.50E-6

InXA1

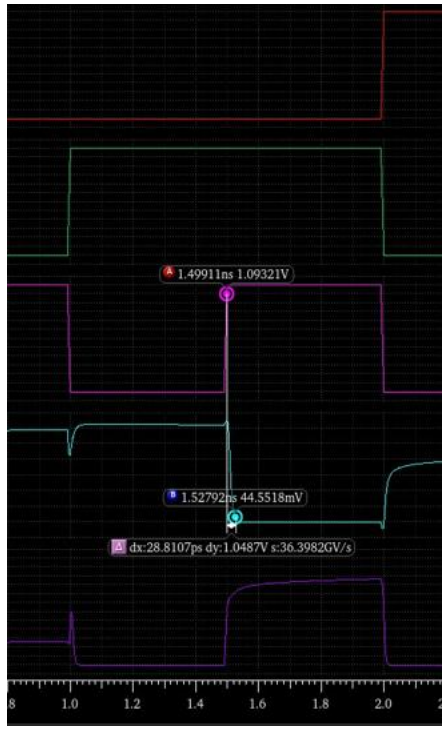
	Expression	Value
1	average(getData...	10.61E-6

InXA2

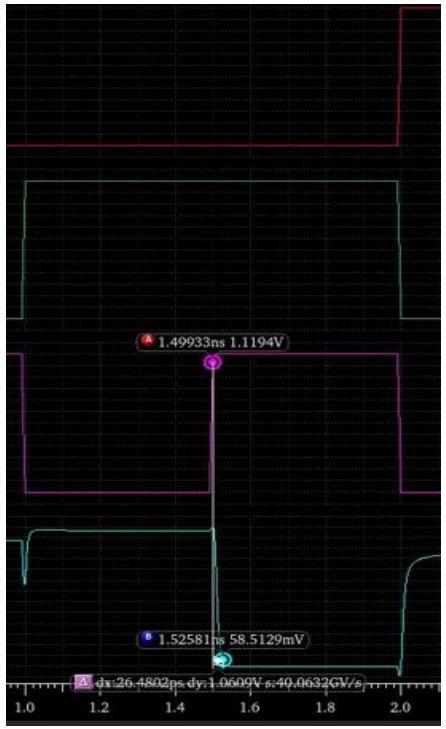
	Expression	Value
1	average(getData...	20.08E-6

InXA3

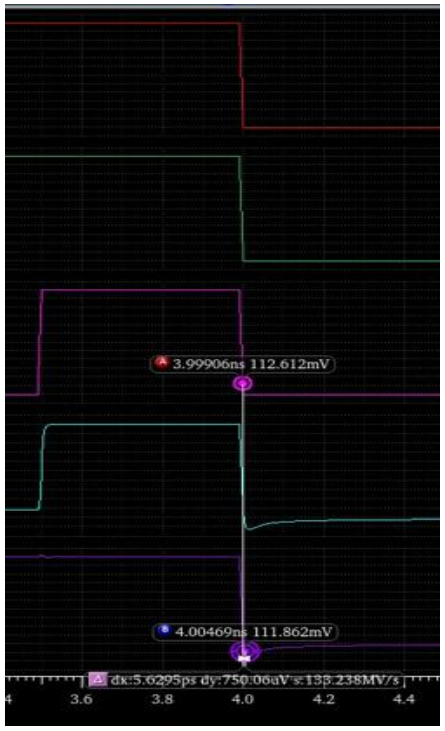
4. 지연 시간



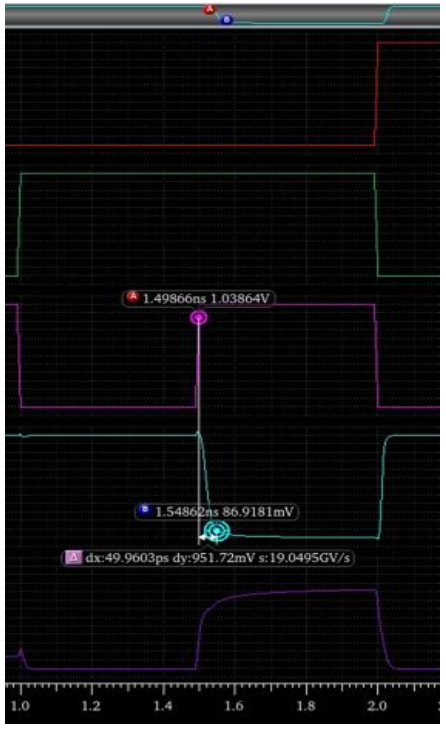
Accurate



InXA1

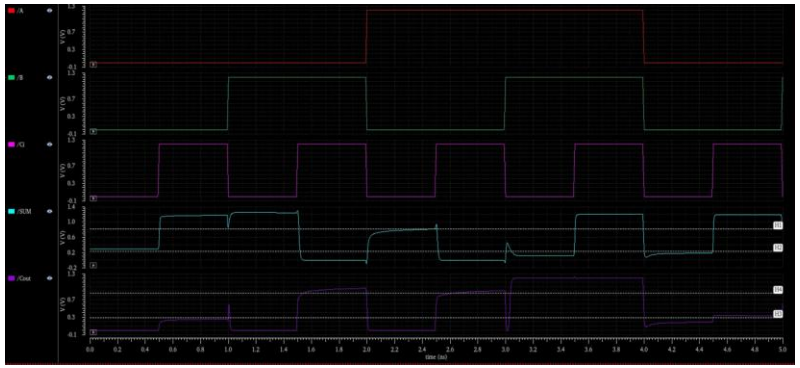


InXA2

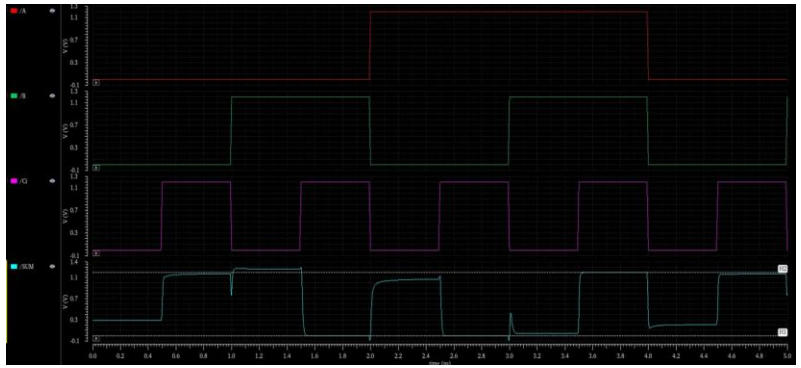


InXA3

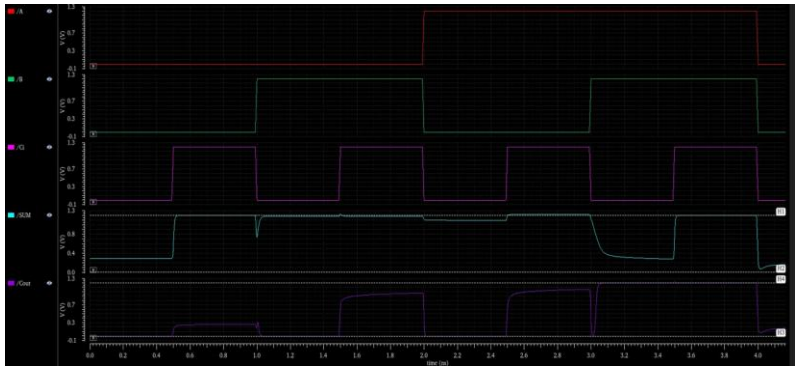
5. 출력 스윙



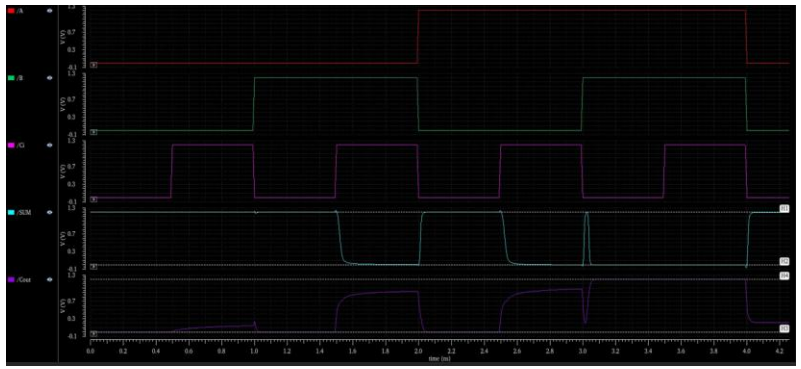
Accurate



InXA1



InXA2



InXA3

6. Post-Layout Simulation 결과 비교

구조	Transistor 개수	면적($\mu m \times \mu m$)	소비 전력(μW)	지연 시간(ps)	출력 스윙(V)
Accurate	10	7.22 × 5.67	21.84	28.81	• Sum : 0.24 ~ 0.82 • Cout : 0.3 ~ 0.85
InXA1	8	5.68 × 5.28	22.50	26.48	• Sum : 0.29 ~ 1.06 • Cout : 0.0 ~ 1.2
InXA2	8	5.61 × 5.85	10.61	5.61	• Sum : 0.29 ~ 1.2 • Cout : 0.38 ~ 0.95
InXA3	8	5.58 × 4.54	20.08	49.96	• Sum : 0.01 ~ 1.2 • Cout : 0.22 ~ 0.93

4. 결론 및 시사점

1. 직접 설계해 보니...

[연구 요약]
- InXA1~3 구조를 동일한 Pass Gate 방식으로 설계 및 Layout
- Post-Layout 시뮬레이션으로 실제 회로 수준 성능 비교

[시사점]
- Logic Simulation만으로는 실제 회로 성능 판단이 불가능.
- Approximate Computing Adder Cell도 실제 회로 수준에서의 성능 검증 필요.

[향후 계획]
- 새로운 Approximate Computing Adder Cell 탐색 : Transistor 개수를 감소시키는 방향.