

조교 조성근

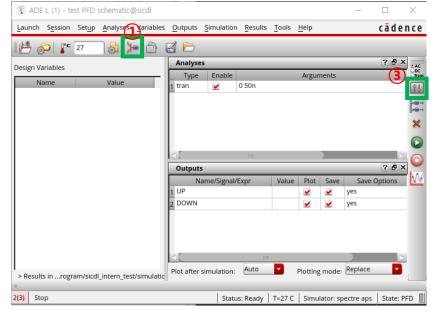
개요

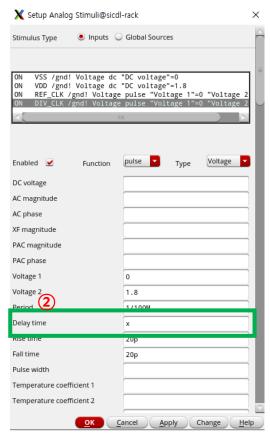
- PFD simulation
- Parametric Analysis
- PFD Gain

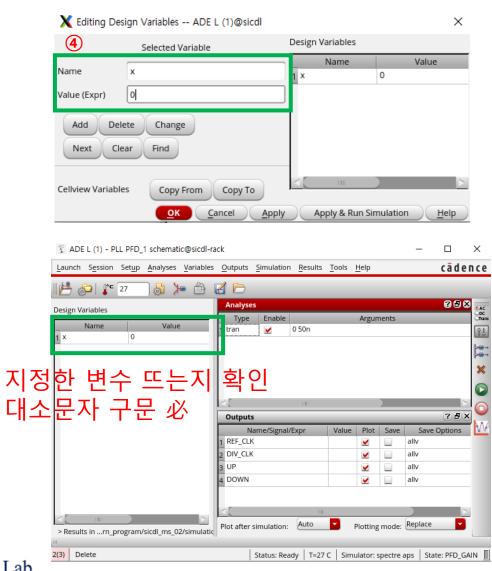
VCO

Parametric Analysis

• 변수 지정

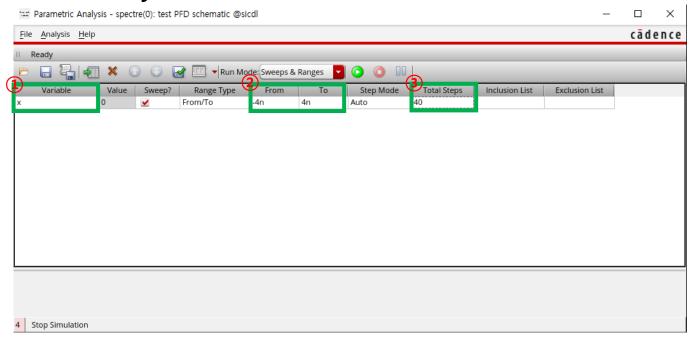






Parametric Analysis

Tools -> Parametric Analysis



- ① 앞서 지정한 변수 선택
- ② Simulation 진행할 시작점과 끝지점 값 입력
- ③ Simulation 진행할 Step 수 입력

PFD Gain 보는 법

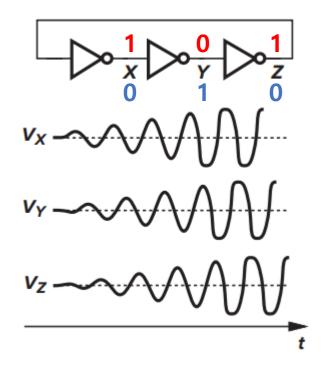


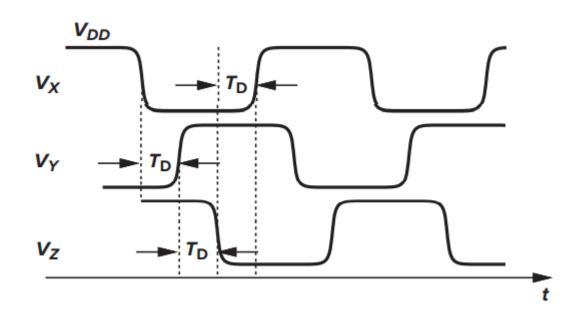
System Integrated Circuit Design Lab.

5

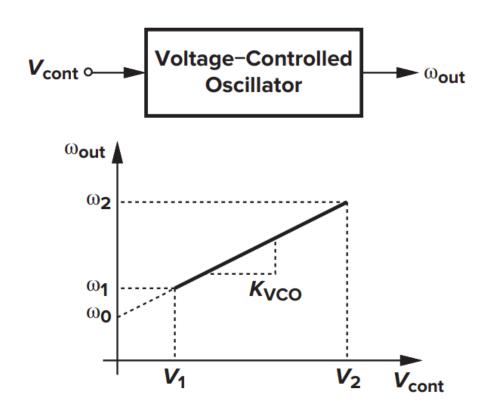
Oscillator

Ring Oscillator





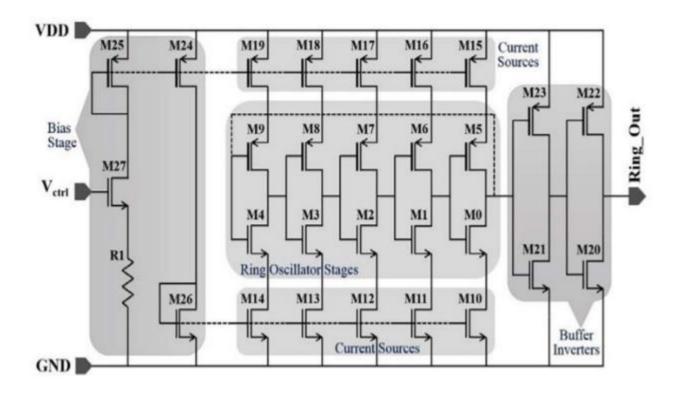
Voltage Controlled Oscillator



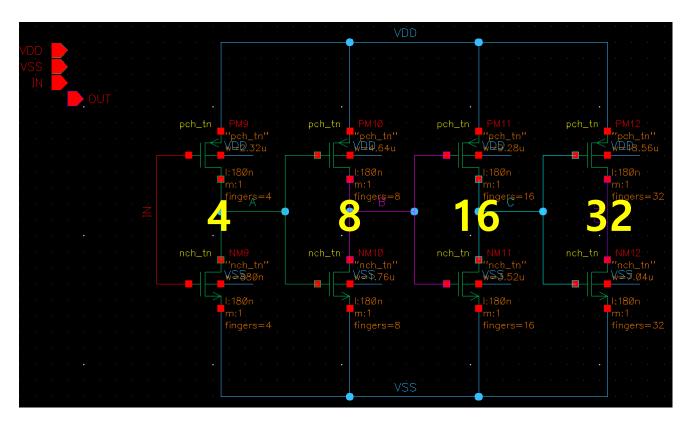
- $\omega_{out} = \omega_0 + K_{VCO}V_{cont}$
- *K_{VCO}* : 이득(감도)
- ω₂ ω₁ : 튜닝 범위
- 성능 파라미터
- ① 중심 주파수
- ② 튜닝범위
- 잡음 영향 최소화를 위해 K_{VCO} 가 낮아야 함. 이는 튜닝 범 위와 trade-off
- ③ 튜닝 선형도
- PLL 설계 시 안정화 양상을 악화

VCO

Current Starved Ring Oscillator

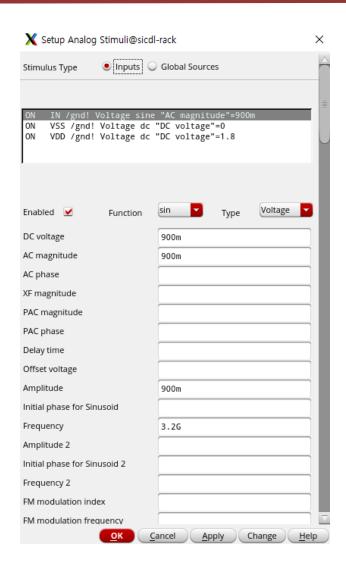


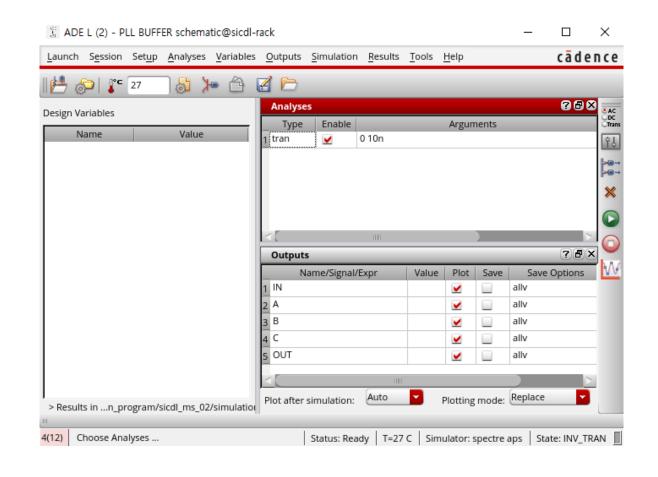
Buffer



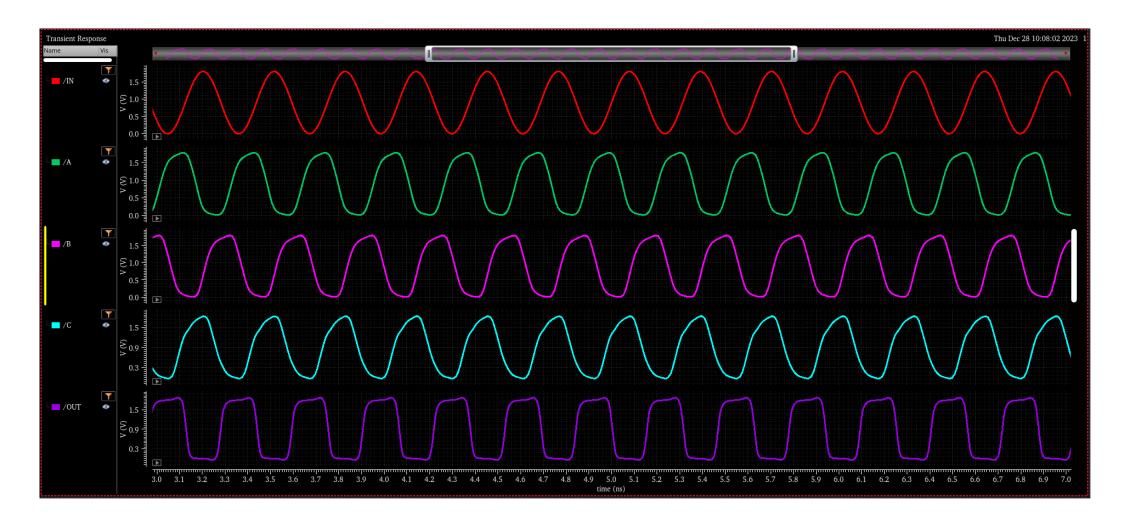
- Time Delay가 필요할 때
- 큰 부하를 감당해야할 때(=신호를 살릴 때)

Buffer



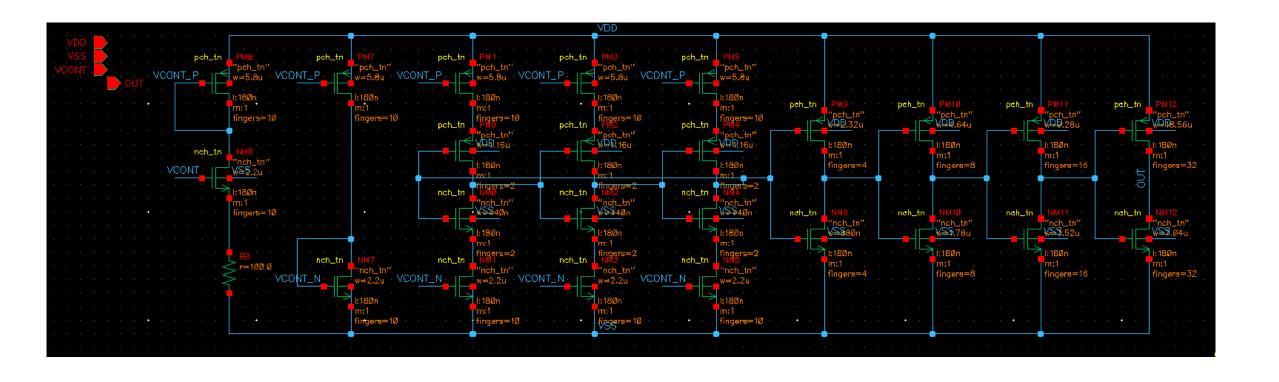


Buffer

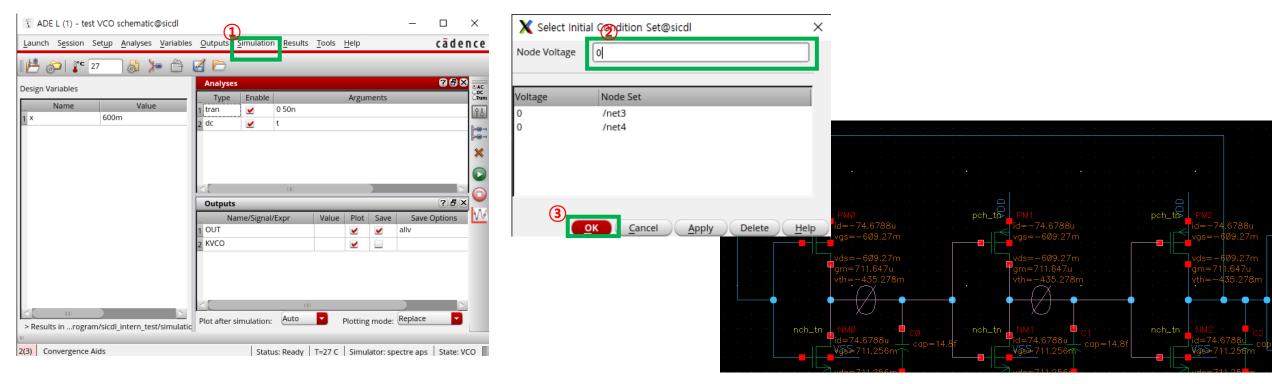


VCO

Current Starved Ring Oscillator

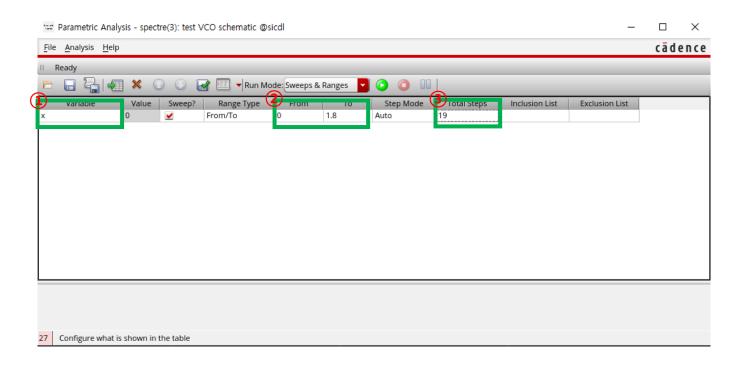


Initial Condition



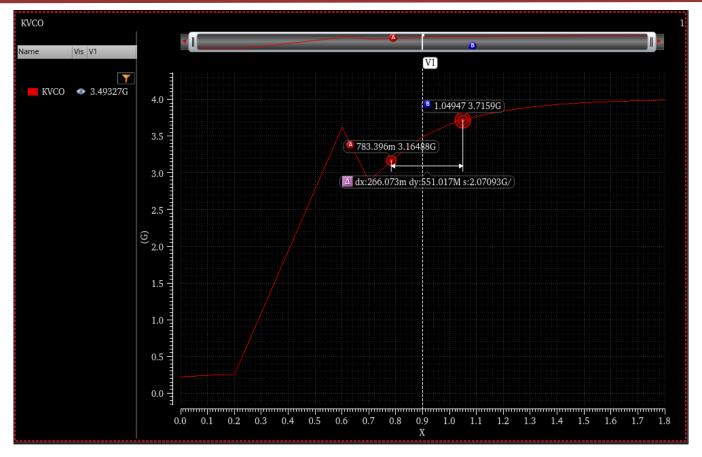
- ① Simulation -> Convergence Aids -> Initial Condition
- ② schematic에서 원하는 node 선택

전압 vs 주파수 그래프 보는 법



- ① 앞서 지정한 변수 선택
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- ③ Simulation 진행할 Step 수 입력

전압 vs 주파수 그래프 보는 법



- Target: 3.2GHz @ 0.9V
- 수식 : frequency(v("/OUT" ?result "tran"))