Loop Filter
PLL simulation

조교 조성근

개요

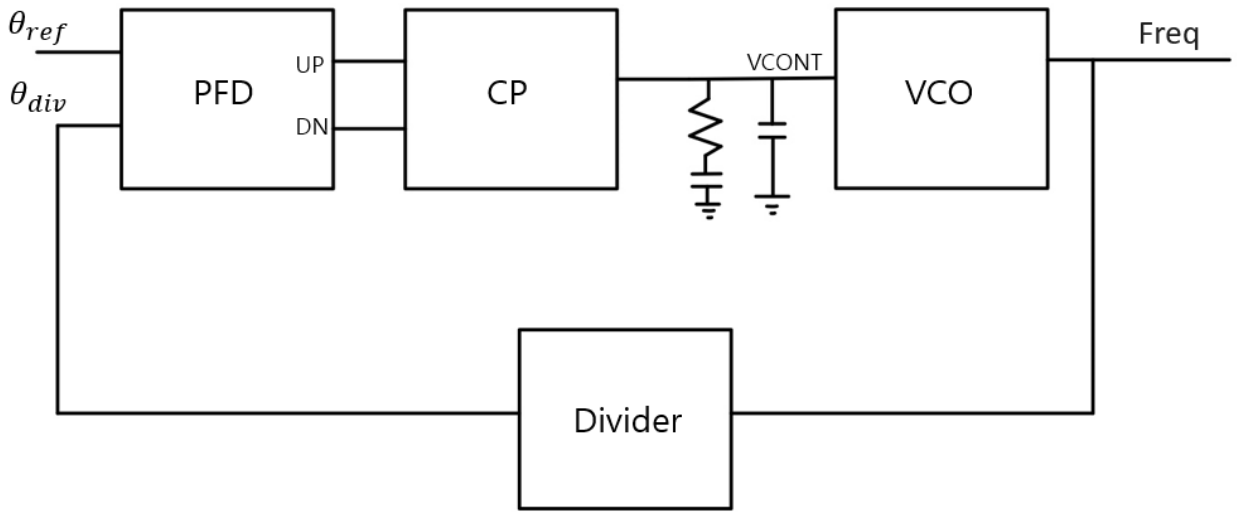
- Loop Filter
- PLL Simulation
- Nonideality_PFD
- Nonideality_CP
- 보고서 필수사항

PLL이란

- PLL (Phase Locked Loop) : 위상 동기 루프

- Reference clock을 입력으로 받아 원하는 주파수의 clock을 출력
- Reference clock은 crystal oscillator를 사용하여 생성. Noise가 거의 없는 깨끗한 clock.
- But, crystal oscillator로는 높은 주파수의 clock 생성이 어려움 (보통 100MHz 이하)

- Top Block Diagram



① PFD (Phase Frequency Detector)
- 출력과 입력 clock의 phase 및 frequency 비교

② CP (Charge Pump)
- 비교 출력에 따른 전류 크기 출력

③ Loop Filter
- 안정성을 고려하여 전류를 전압으로 전환

④ VCO (Voltage Controlled Oscillator)
- 전압에 따른 clock 생성

⑤ Divider
- 출력 clock을 저주파로 전환

Loop Filter

- PLL의 지터 현상

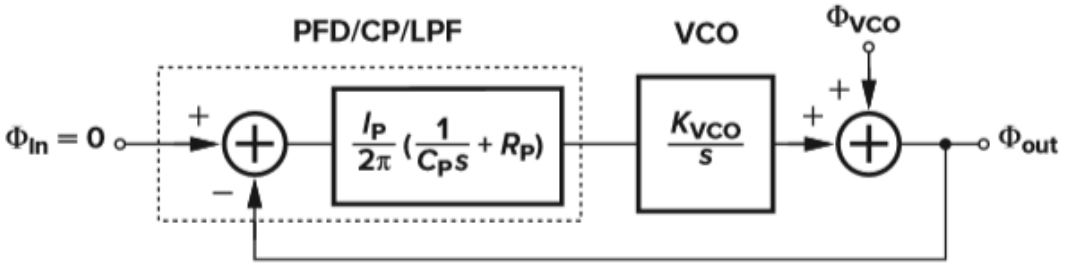
① 입력이 지터를 보여줄 때

: 전달함수에 저역 통과 특성이 있으므로 PLL이 $\emptyset_{in}(t)$를 저역 통과 필터링한다

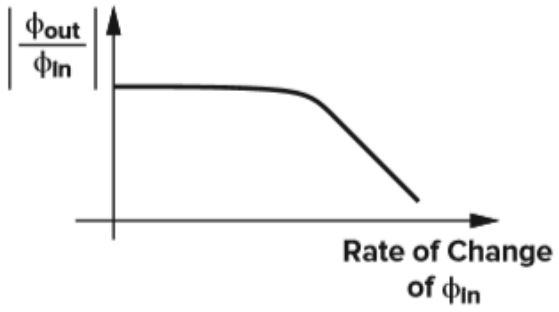
$$\rightarrow H(s) = \frac{\omega_n^2\left(\frac{2\zeta}{\omega_n}s+1\right)}{s^2+2\zeta\omega_n s+\omega_n^2}$$

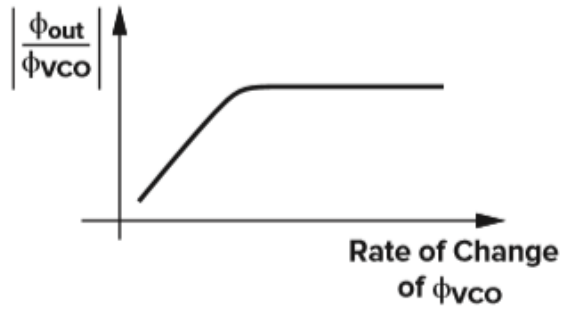
② VCO가 지터를 발생할 때

: $\frac{\Phi_{out}}{\Phi_{VCO}}(s) = \frac{s^2}{s^2+2\zeta\omega_n s+\omega_n^2}$이므로 고역 통과 성질을 가진다

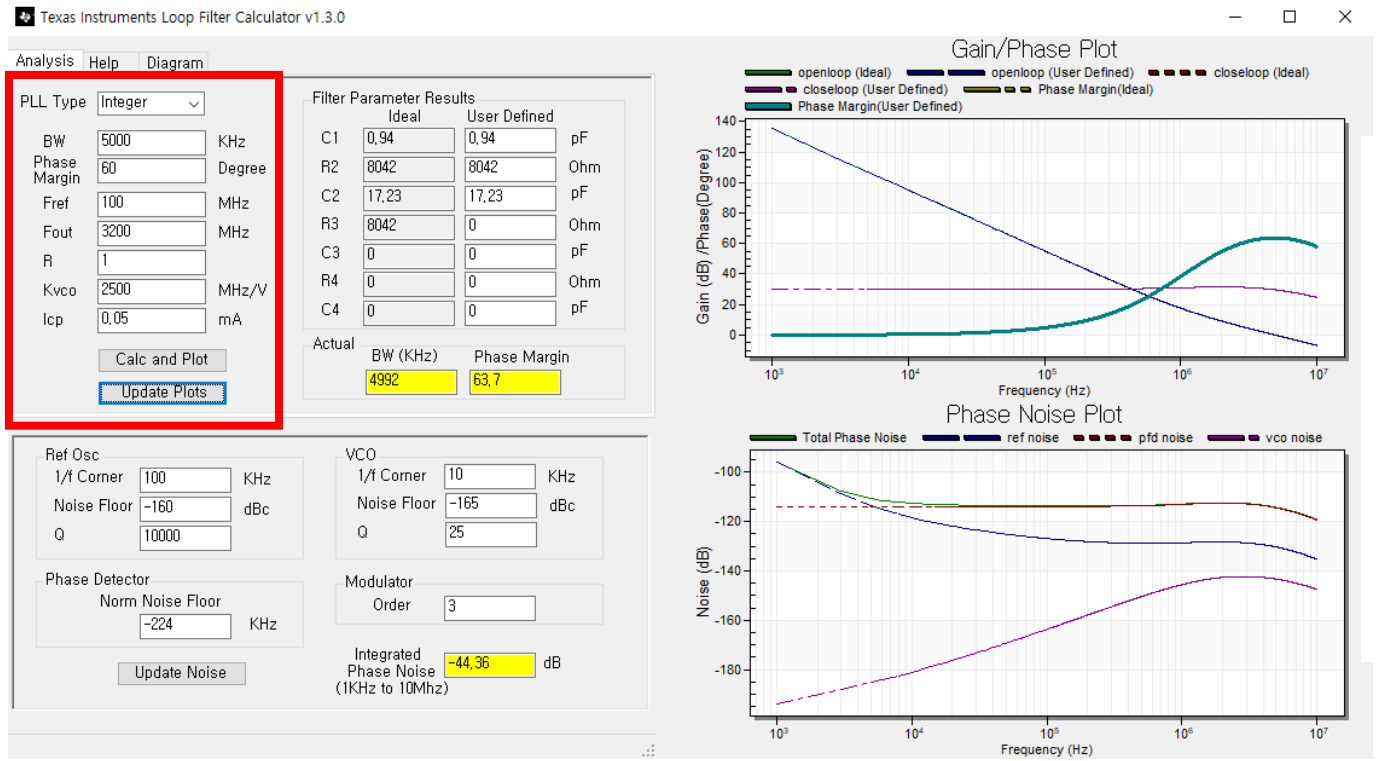


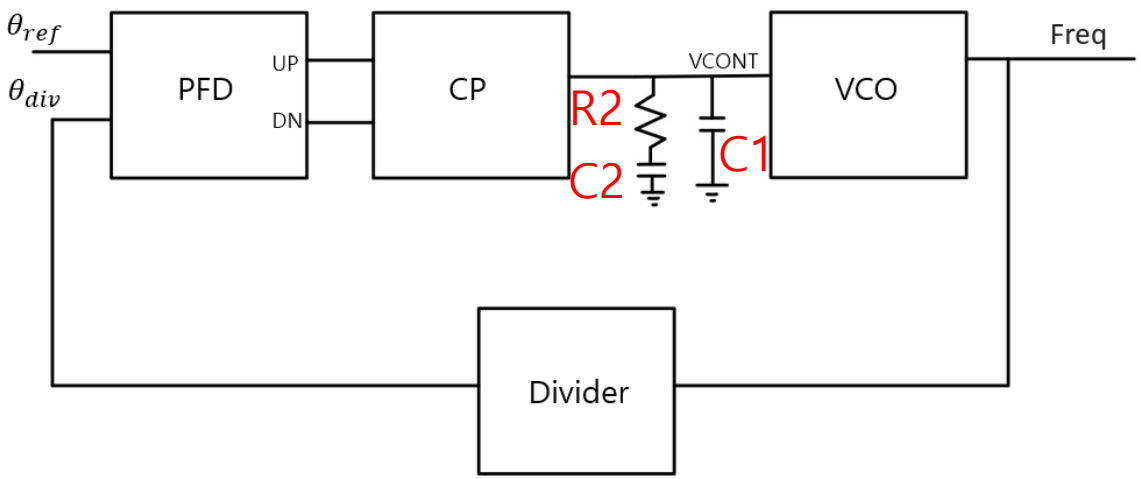
→ loop 대역폭 선정에 있어 위 두 지터를 고려한 최적화된 값이 요구된다



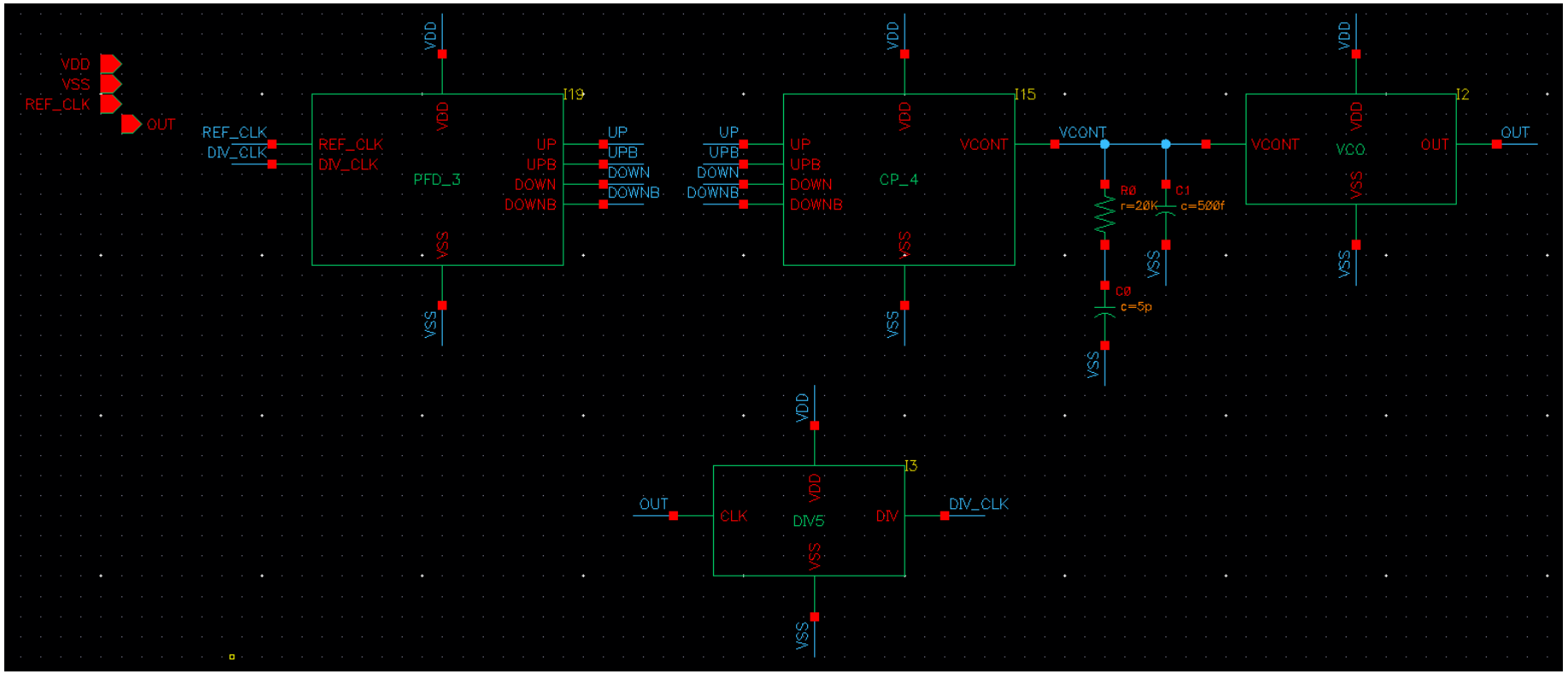


Loop Filter


Texas Instruments Loop Filter Calculator v1.3.0
Analysis
Help
Diagram
PLL Type
Integer
BW
5000
KHz
Phase Margin
60
Degree
Fref
100
MHz
Fout
3200
MHz
R
1
Kvco
2500
MHz/V
Icp
0,05
mA
Calc and Plot
Update Plots
Filter Parameter Results
Ideal
User Defined
C1
0,94
0,94
pF
R2
8042
8042
Ohm
C2
17,23
17,23
pF
R3
8042
0
Ohm
C3
0
0
pF
R4
0
0
Ohm
C4
0
0
pF
Actual
BW (KHz)
Phase Margin
4992
63,7
Ref Osc
1/f Corner
100
KHz
Noise Floor
-160
dBc
Q
10000
VCO
1/f Corner
10
KHz
Noise Floor
-165
dBc
Q
25
Phase Detector
Norm Noise Floor
-224
KHz
Modulator
Order
3
Update Noise
Integrated Phase Noise (1KHz to 10Mhz)
-44,36
dB
Gain/Phase Plot
openloop (Ideal)
openloop (User Defined)
closeloop (Ideal)
closeloop (User Defined)
Phase Margin(Ideal)
Phase Margin(User Defined)
Gain (dB) /Phase(Degree)
Frequency (Hz)
Phase Noise Plot
Total Phase Noise
ref noise
pfd noise
vco noise
Noise (dB)
Frequency (Hz)


θ_{ref}
θ_{div}
PFD
UP
DN
CP
VCONT
R2
C2
C1
VCO
Freq
Divider

PLL Simulation

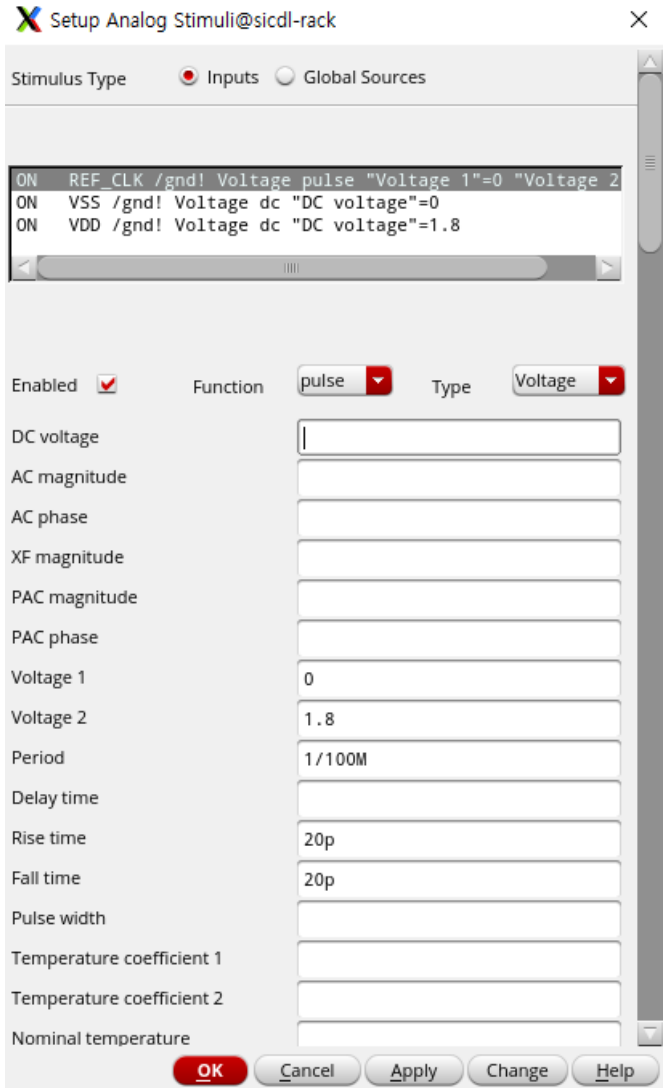


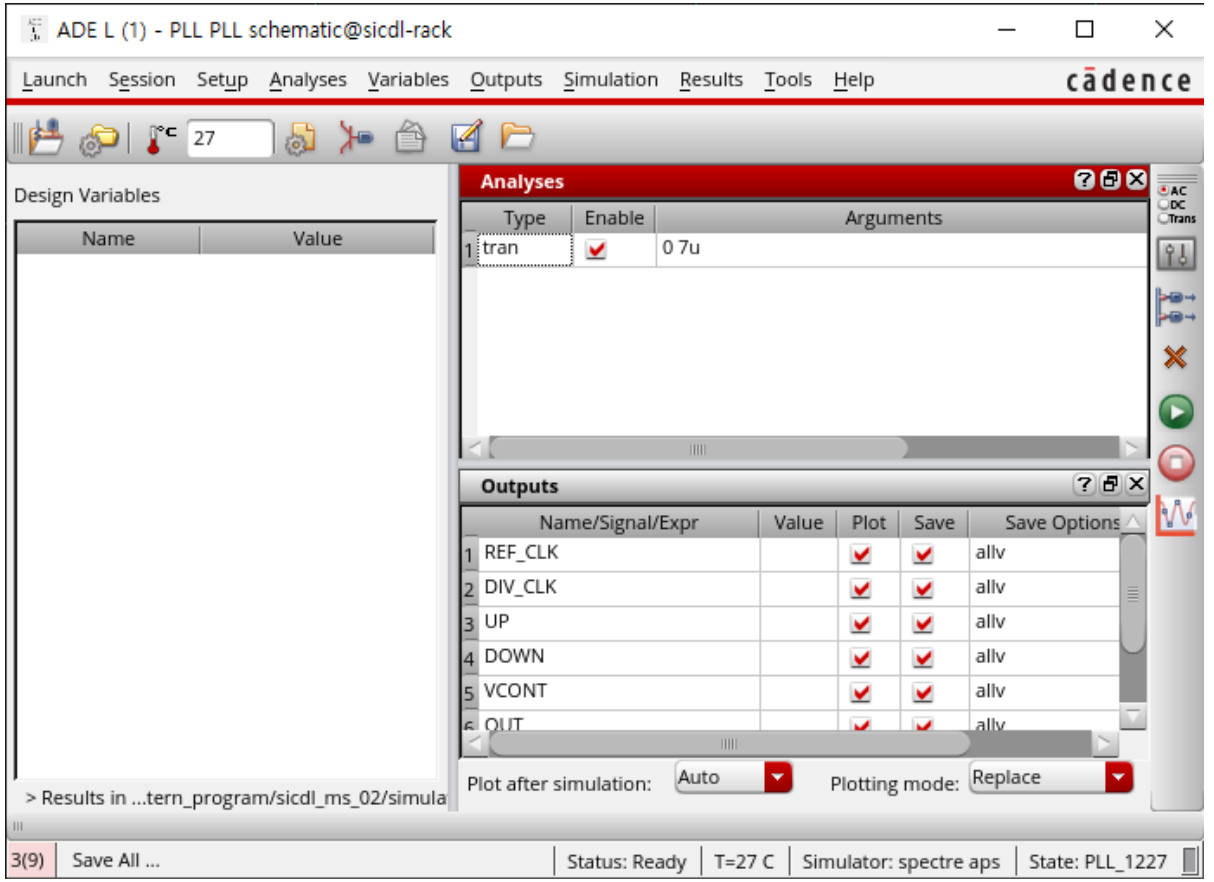
- SPEC

- REF CLK : 100MHz
- Target Freq. : 3.2GHz

- Peak-to-Peak Jitter : 1ps
- Lock Time : 1us
- Power : only 측정

PLL Simulation

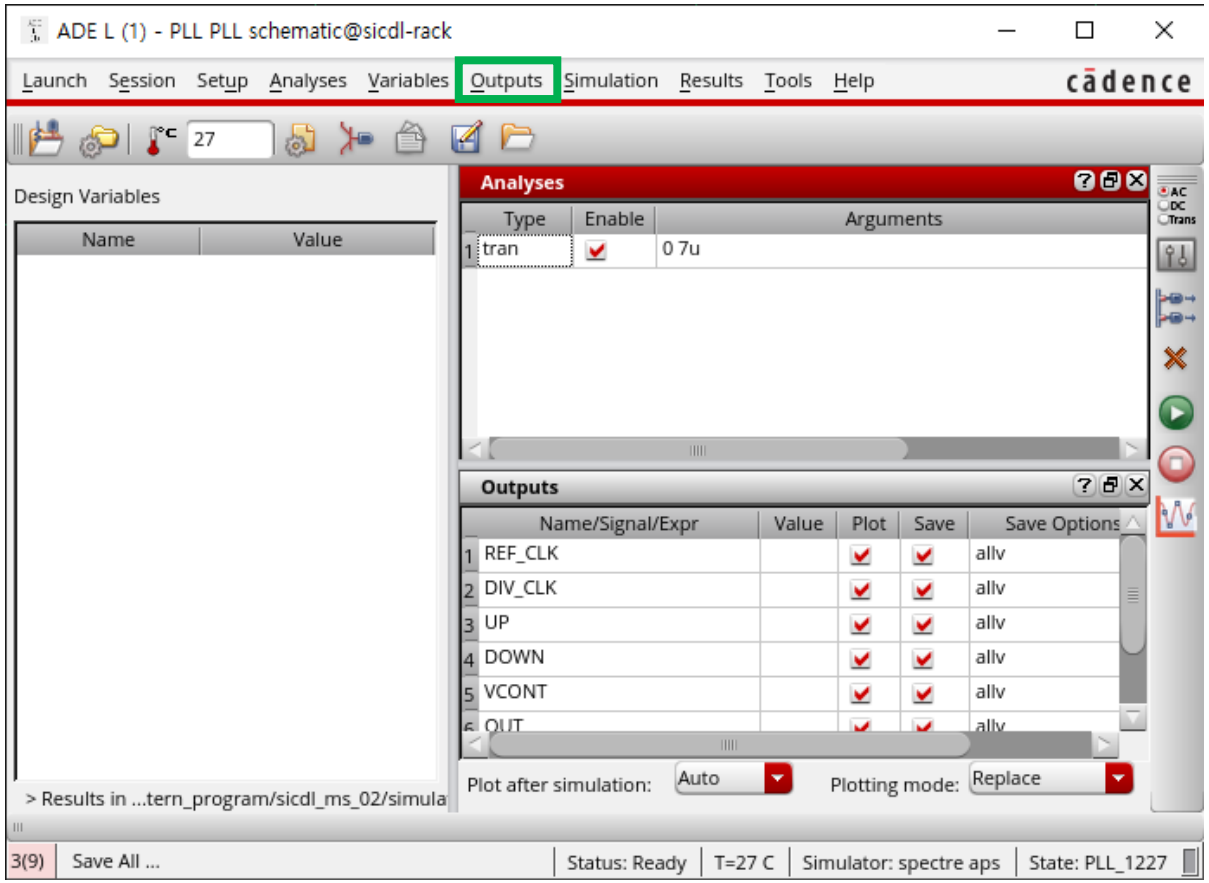


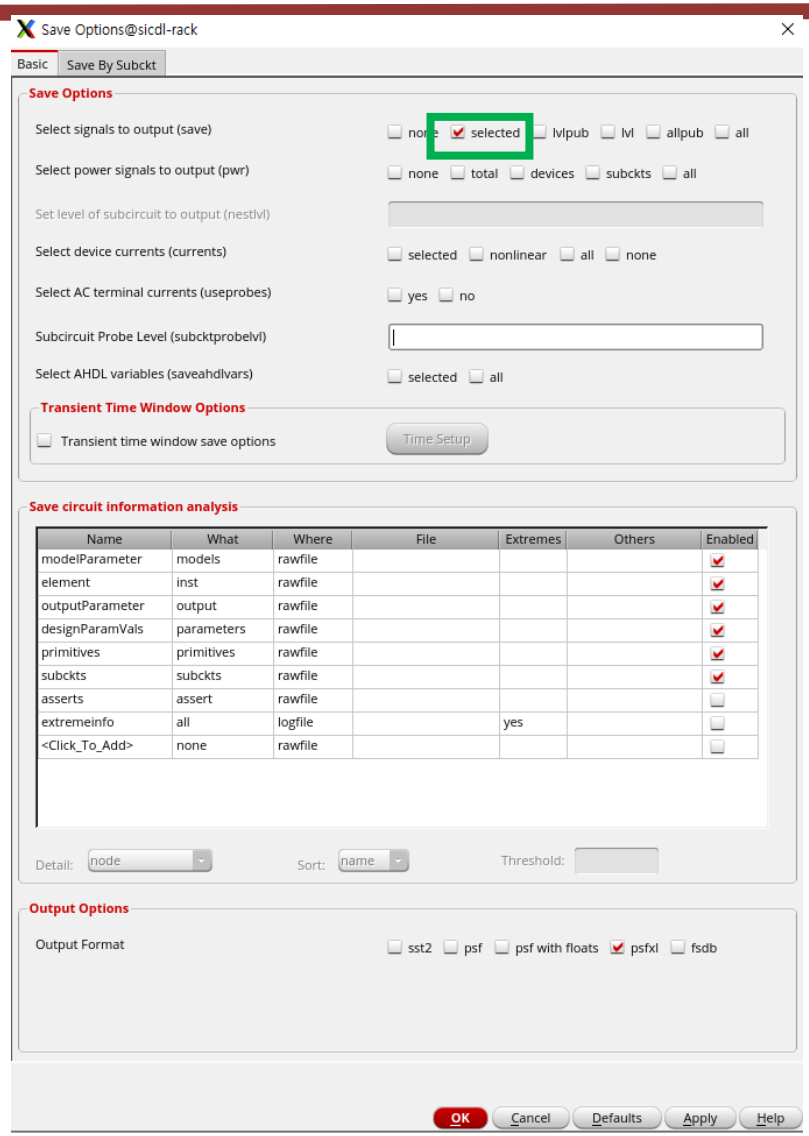


PLL Simulation

- Outputs -> Save All

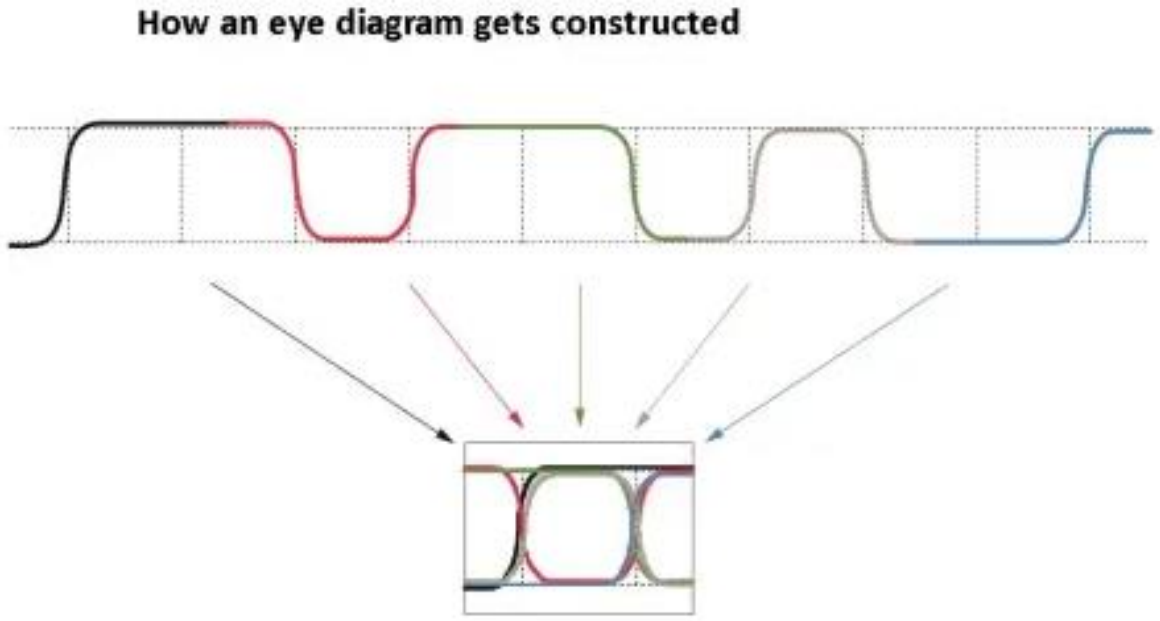
: Simulation 시간 단축



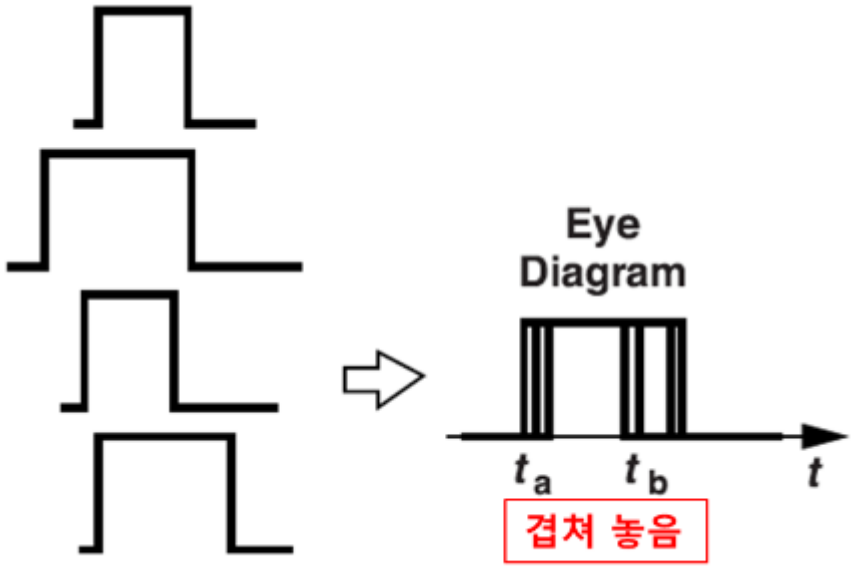


PLL Simulation_P2P Jitter

- eyeDiagram이란

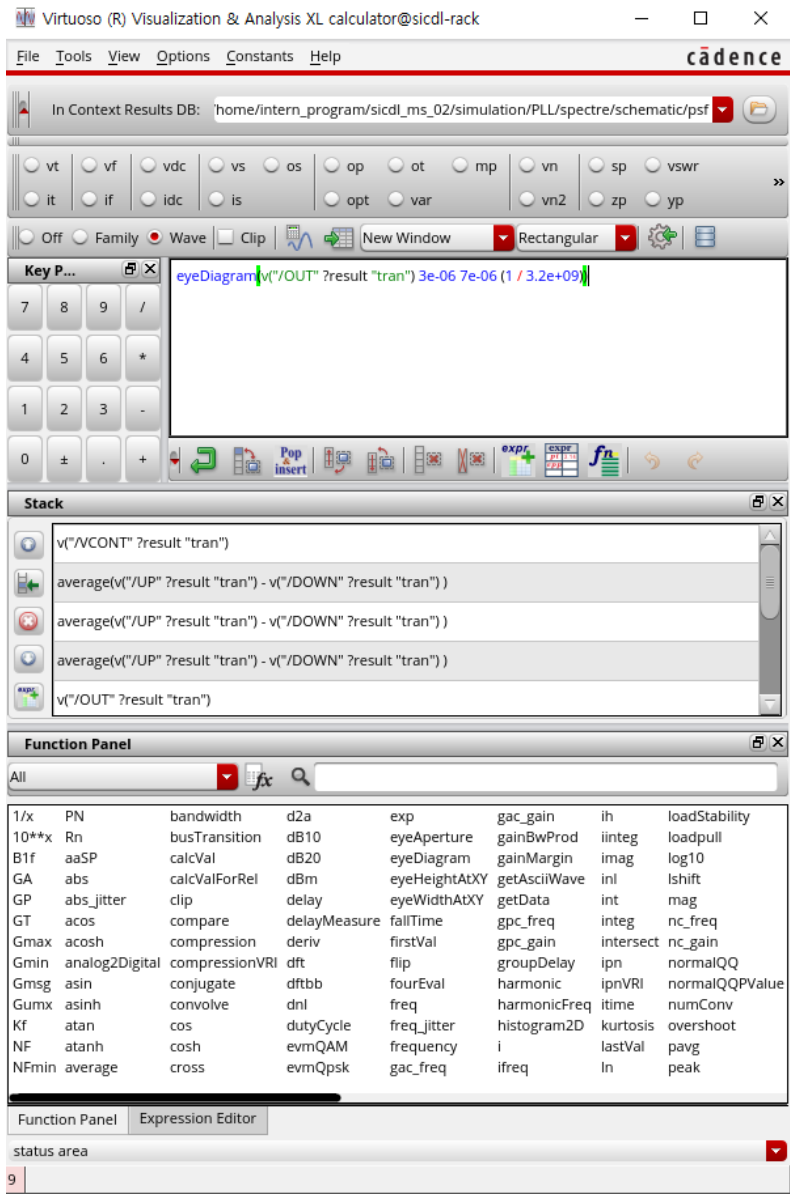


(a)



(b)

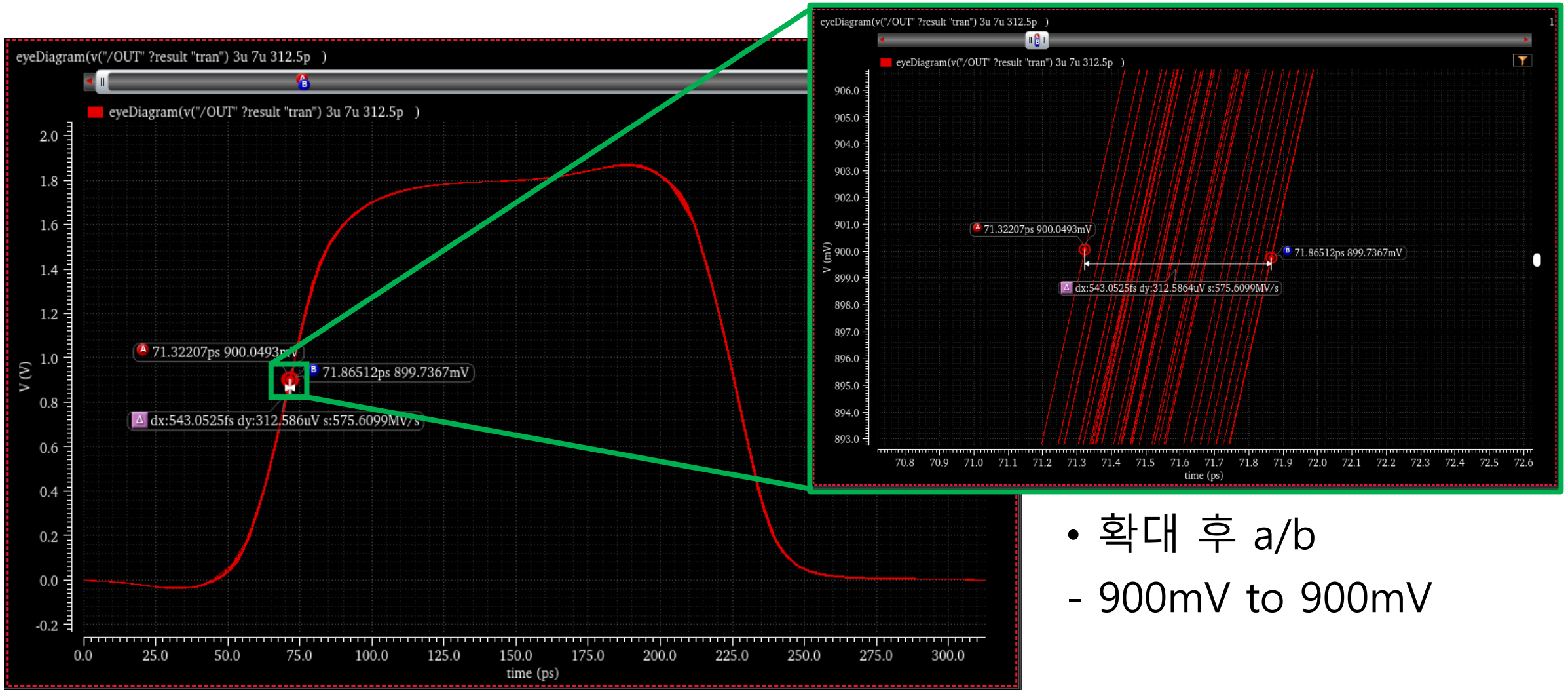
PLL Simulation_P2P Jitter



- 계산기 사용

: eyeDiagram(v("/OUT" ?result "tran") 3e-06 7e-06 3.125e-10)

PLL Simulation_P2P Jitter

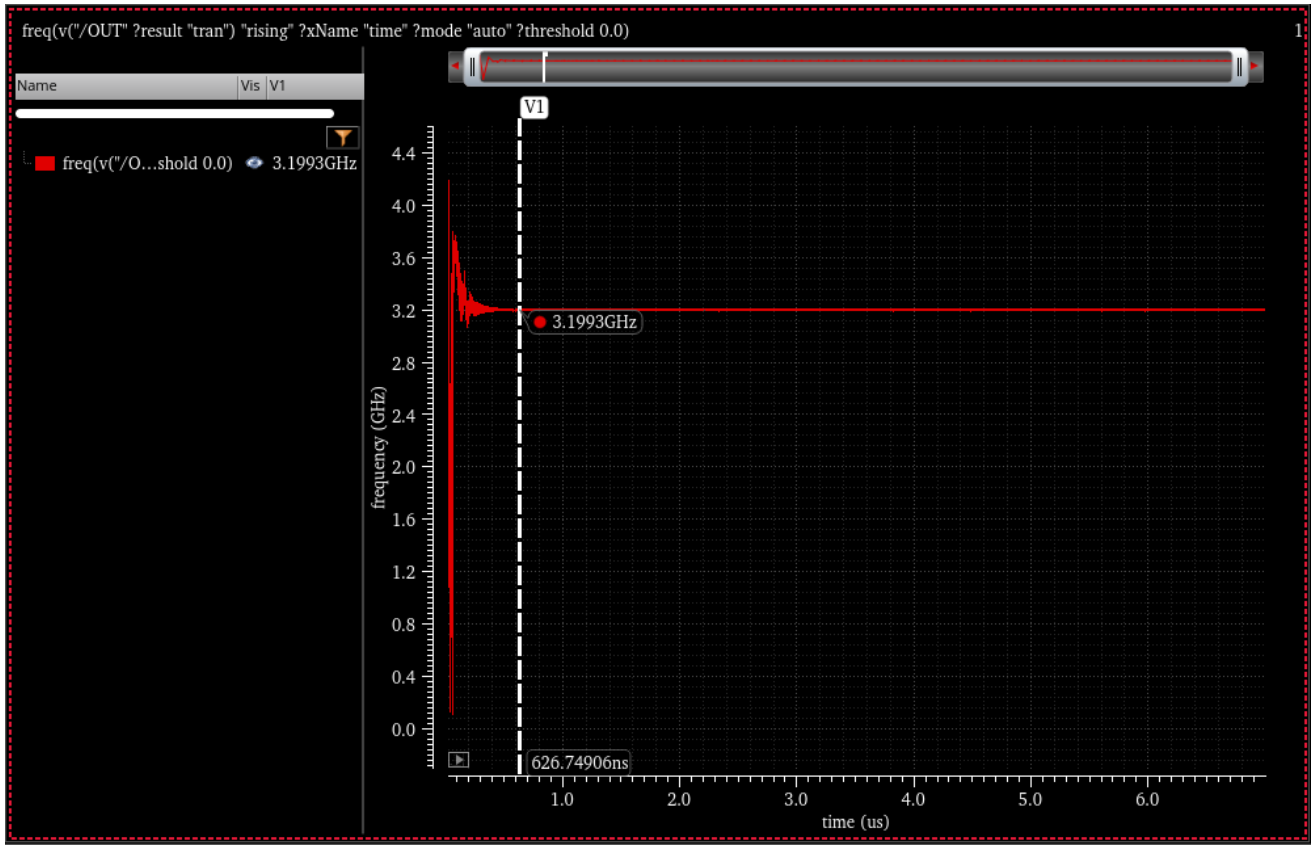


- 확대 후 a/b
  - 900mV to 900mV

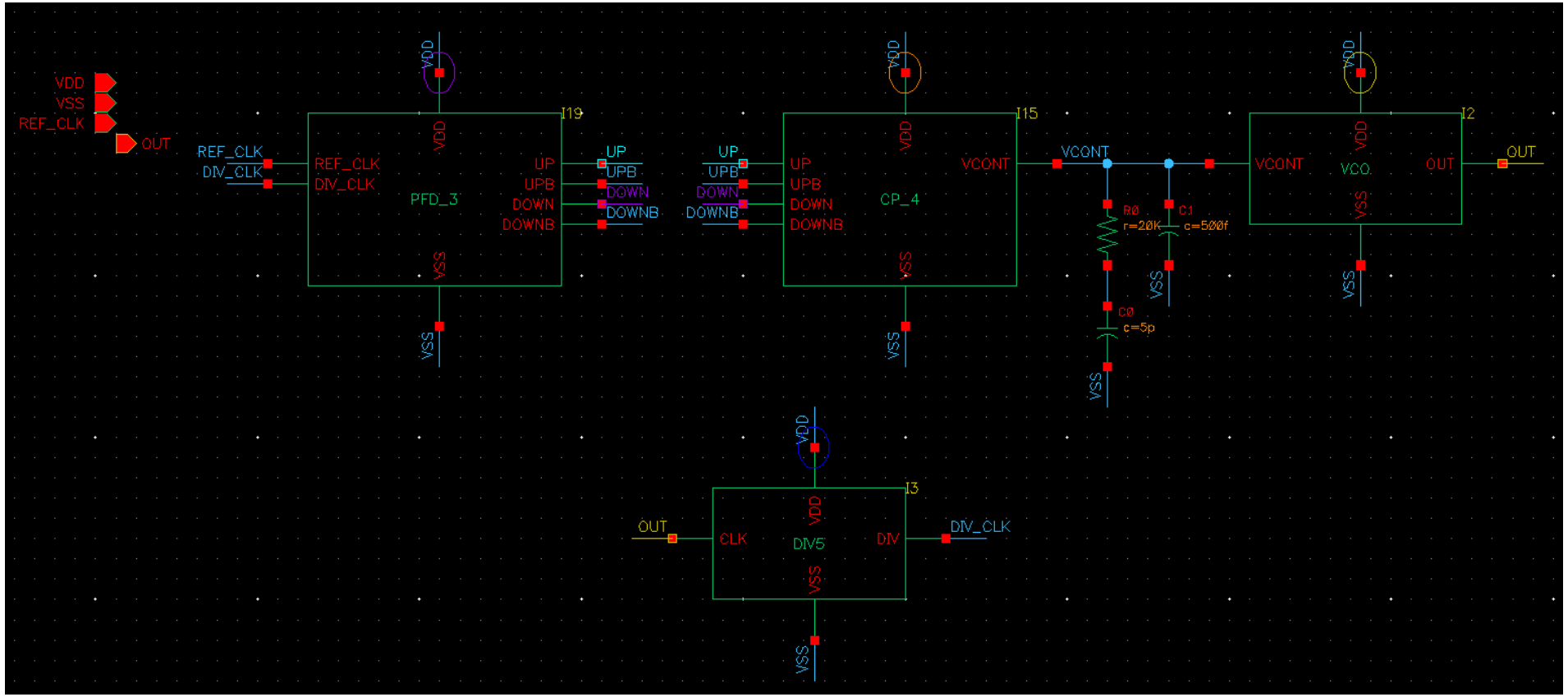
PLL Simulation_Lock Time

- 계산기 사용

: freq(v("/OUT" ?result "tran") "rising" ?xName "time" ?mode "auto" ?threshold 0.0)

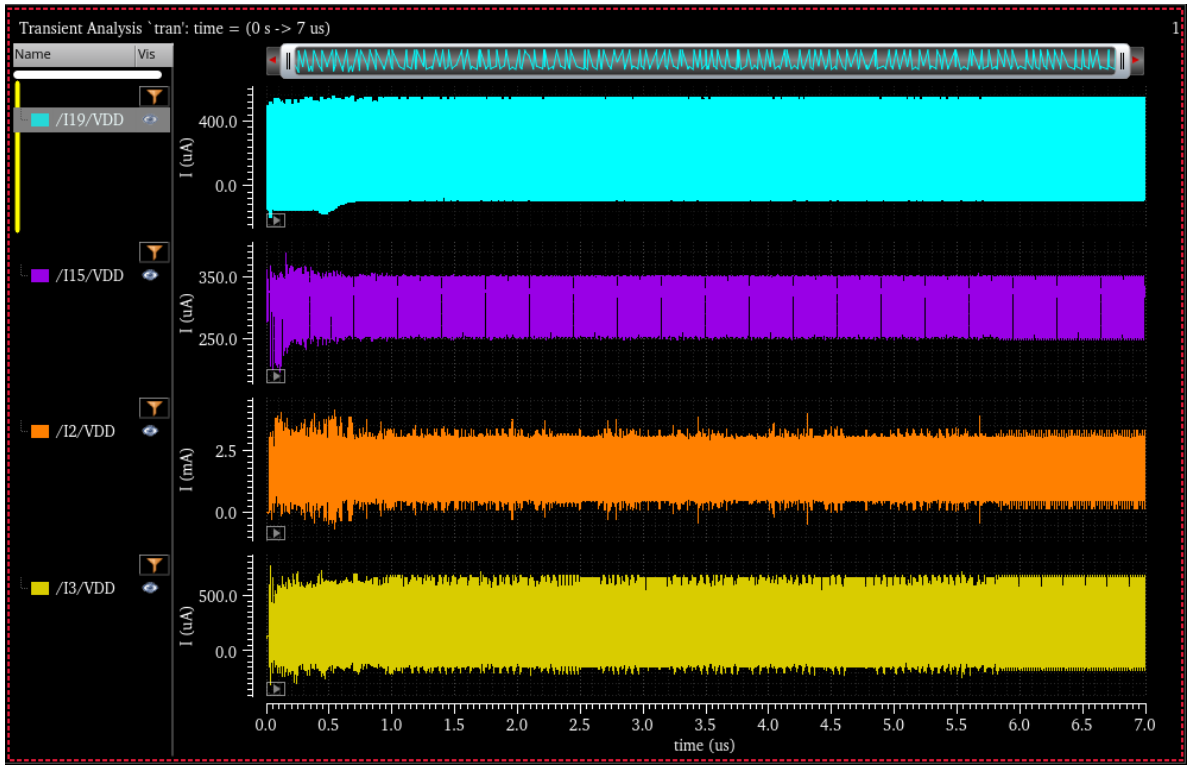


PLL Simulation_ Power



- 모든 Block의 VDD node를 선택하여 측정

PLL Simulation_ Power



- 계산기

: integ(i("/I19/VDD" ?result "tran") 2u 7u " ") /5u *1.8

PLL Simulation_ Power

- (적분 값) / (측정 시간) = (평균 전류)
- (전력) = (전압) * (전류)

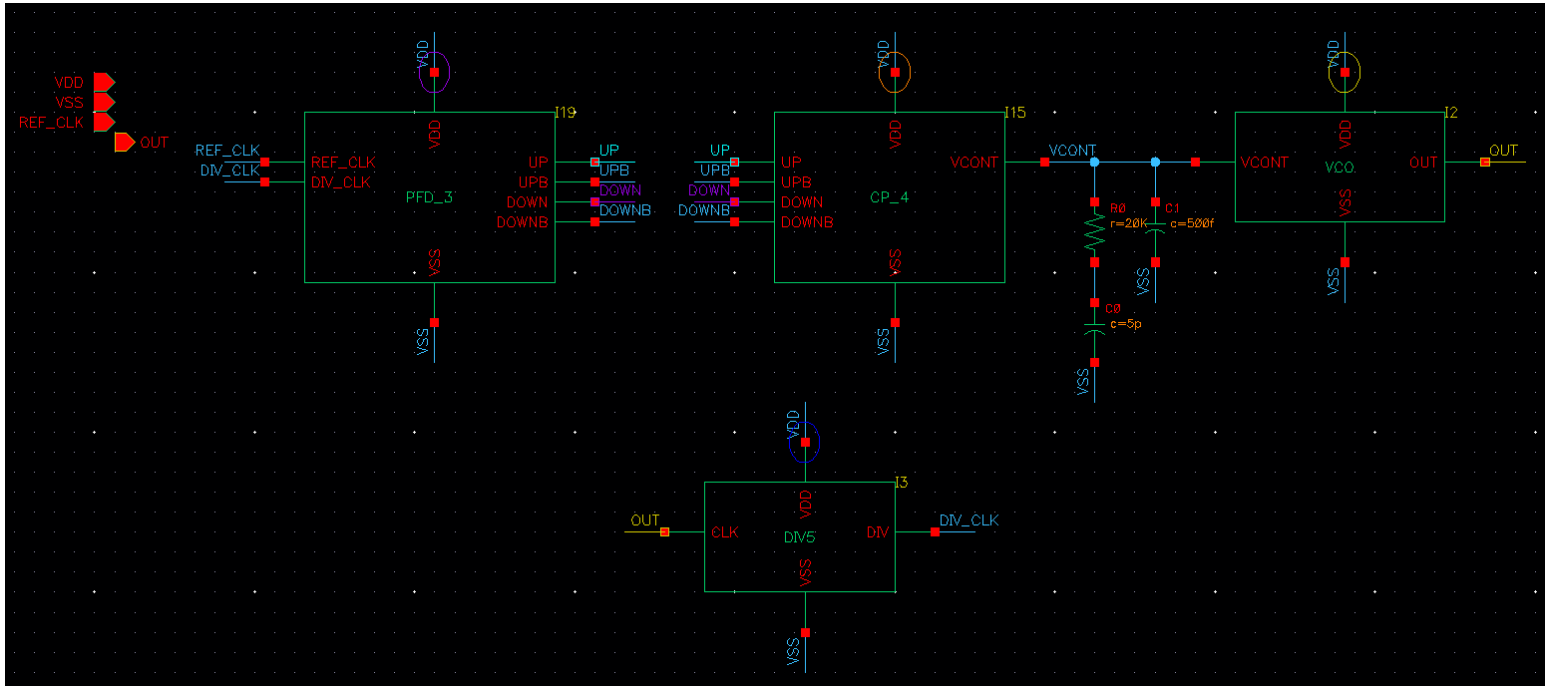
- integ(i("/I19/VDD" ?result "tran") 2u 7u " ") /5u *1.8

-> 본인 block에 맞게 숫자만 바꿔서 사용

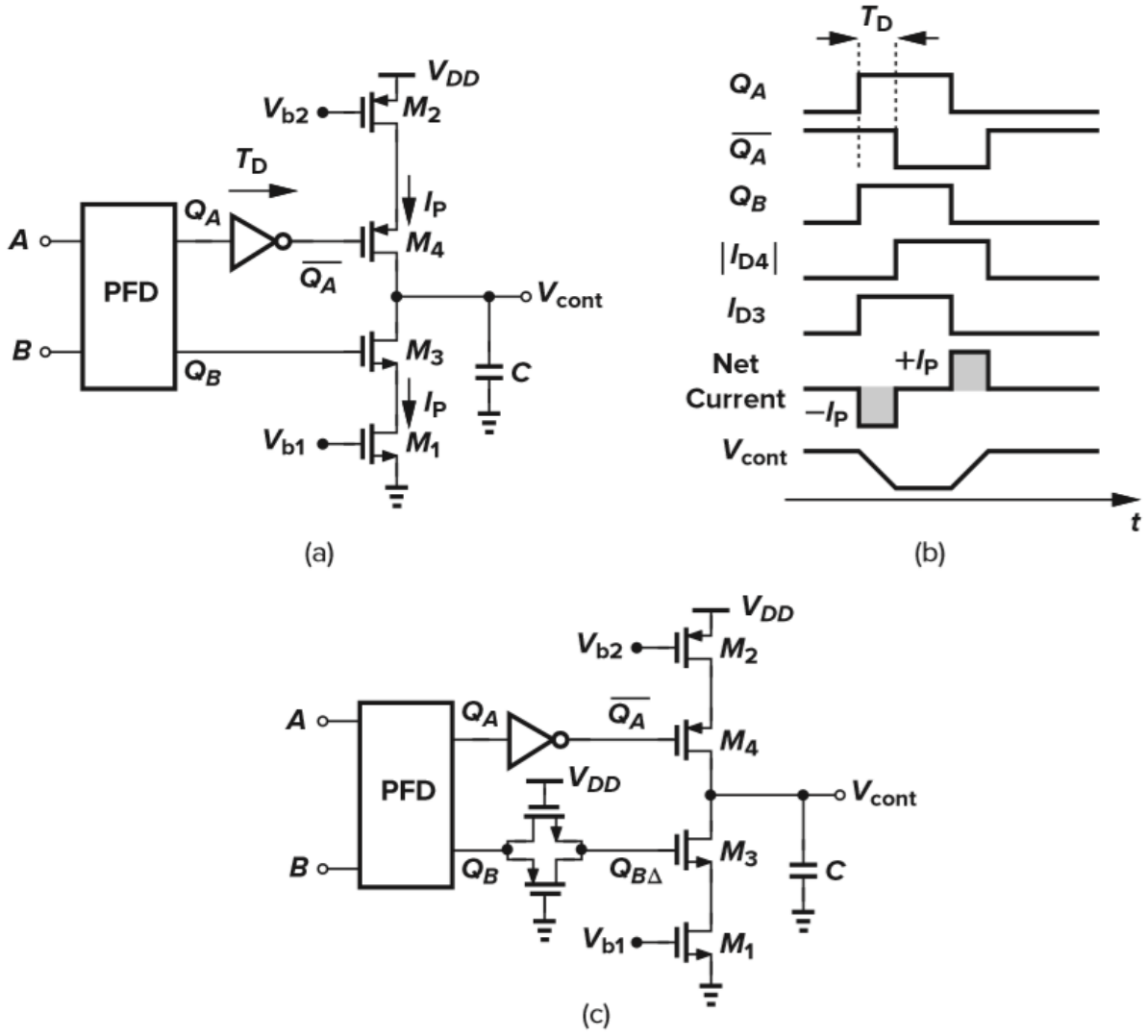
PLL Simulation_ Power

- PFD : 25.34uW
- CP : 585.4uW
- VCO : 2.599mW
- DIV : 253.7uW

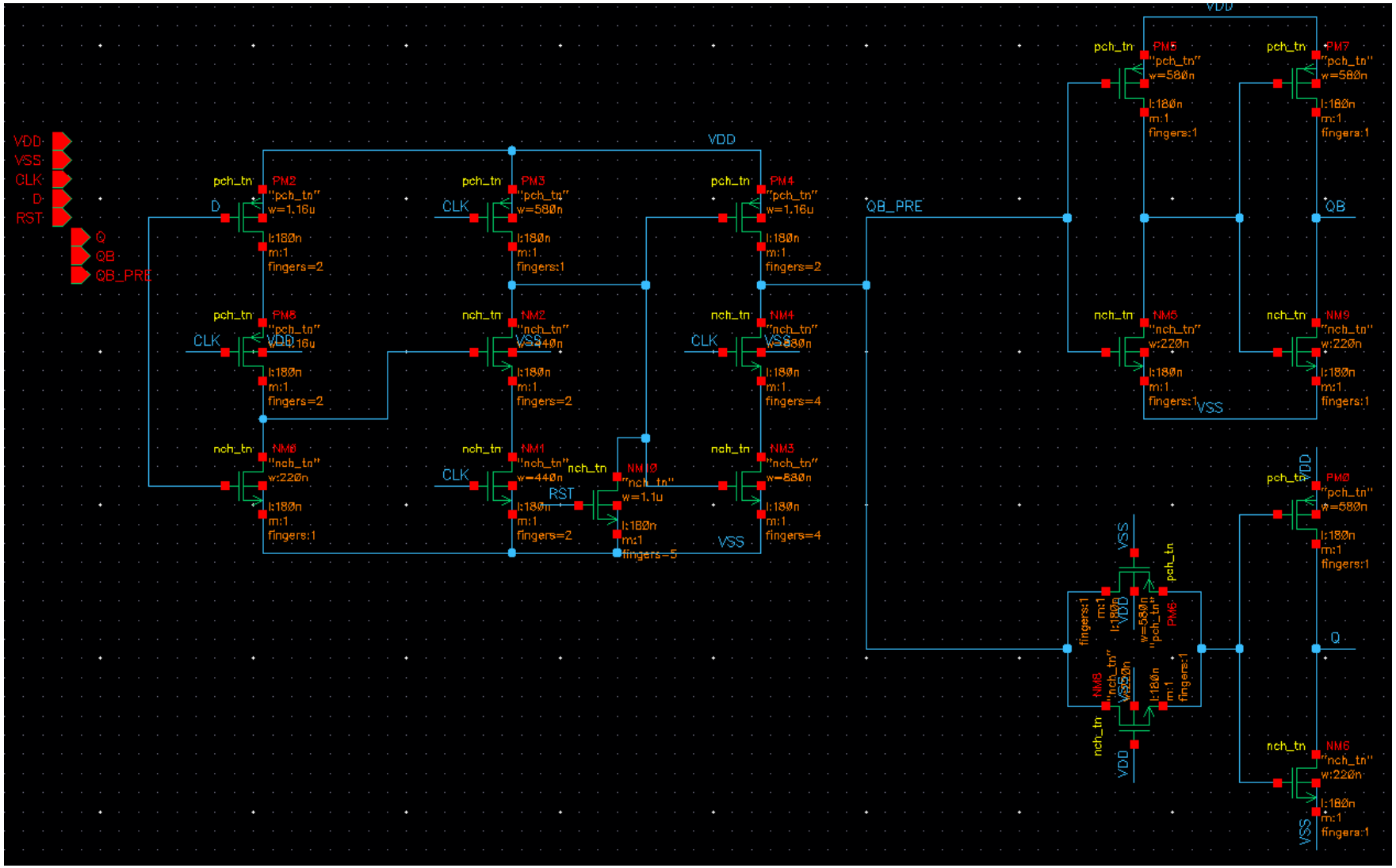
- 총 전력 : 약 3.46mW



Nonideality_PFD

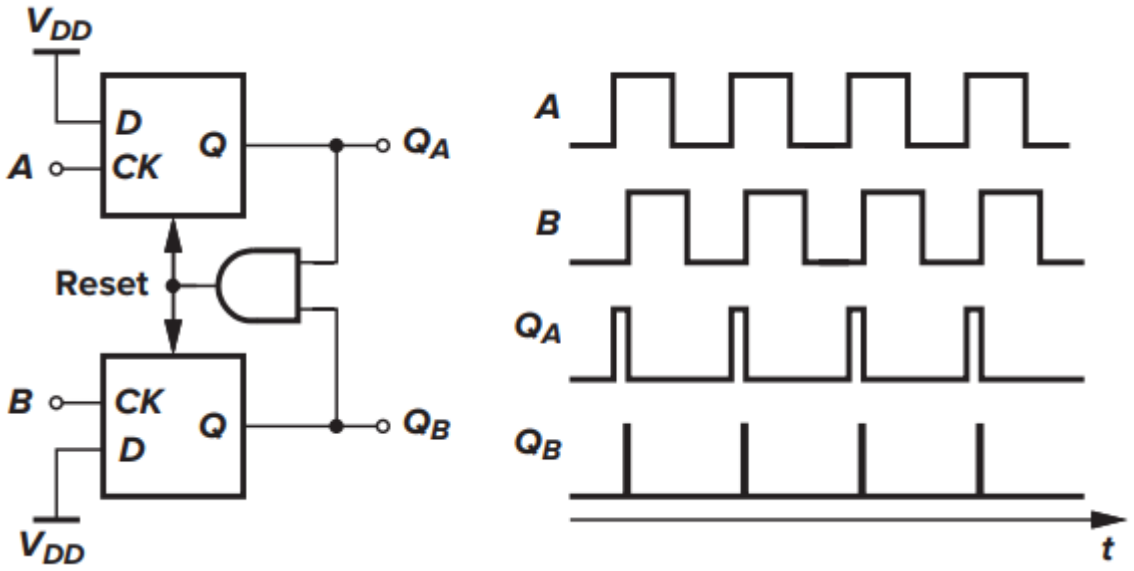


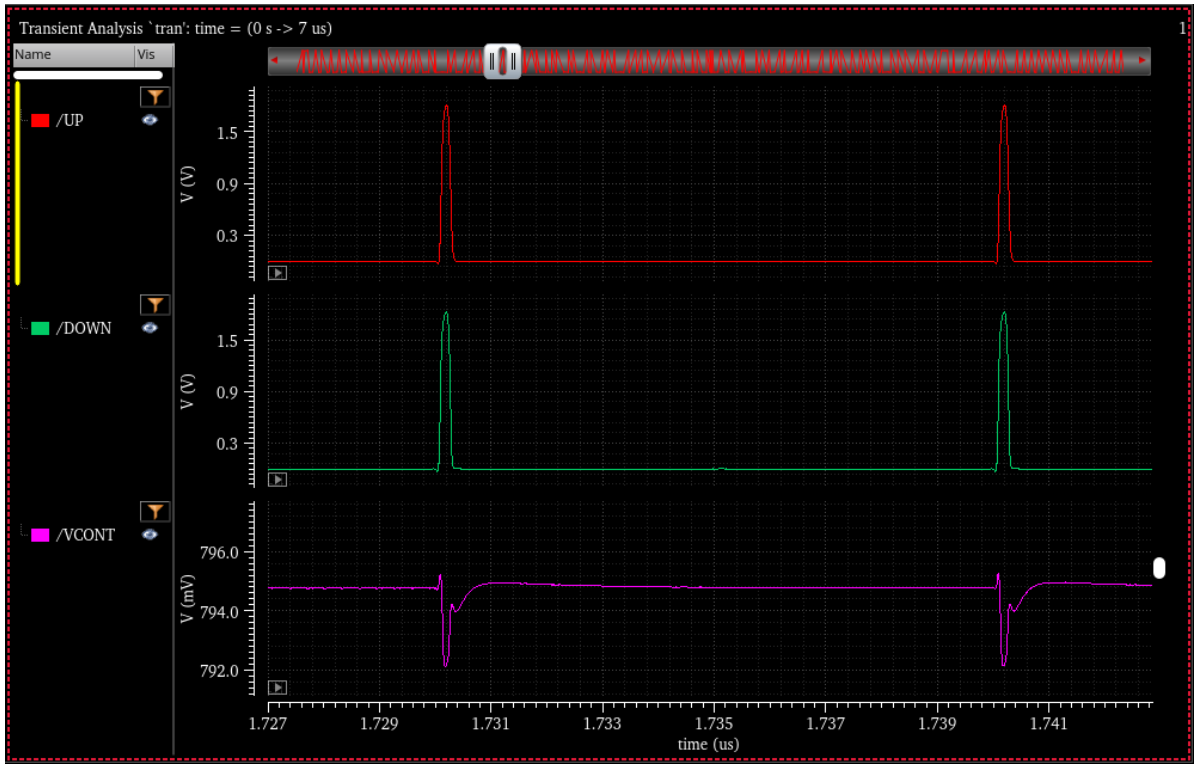
Nonideality_PFD



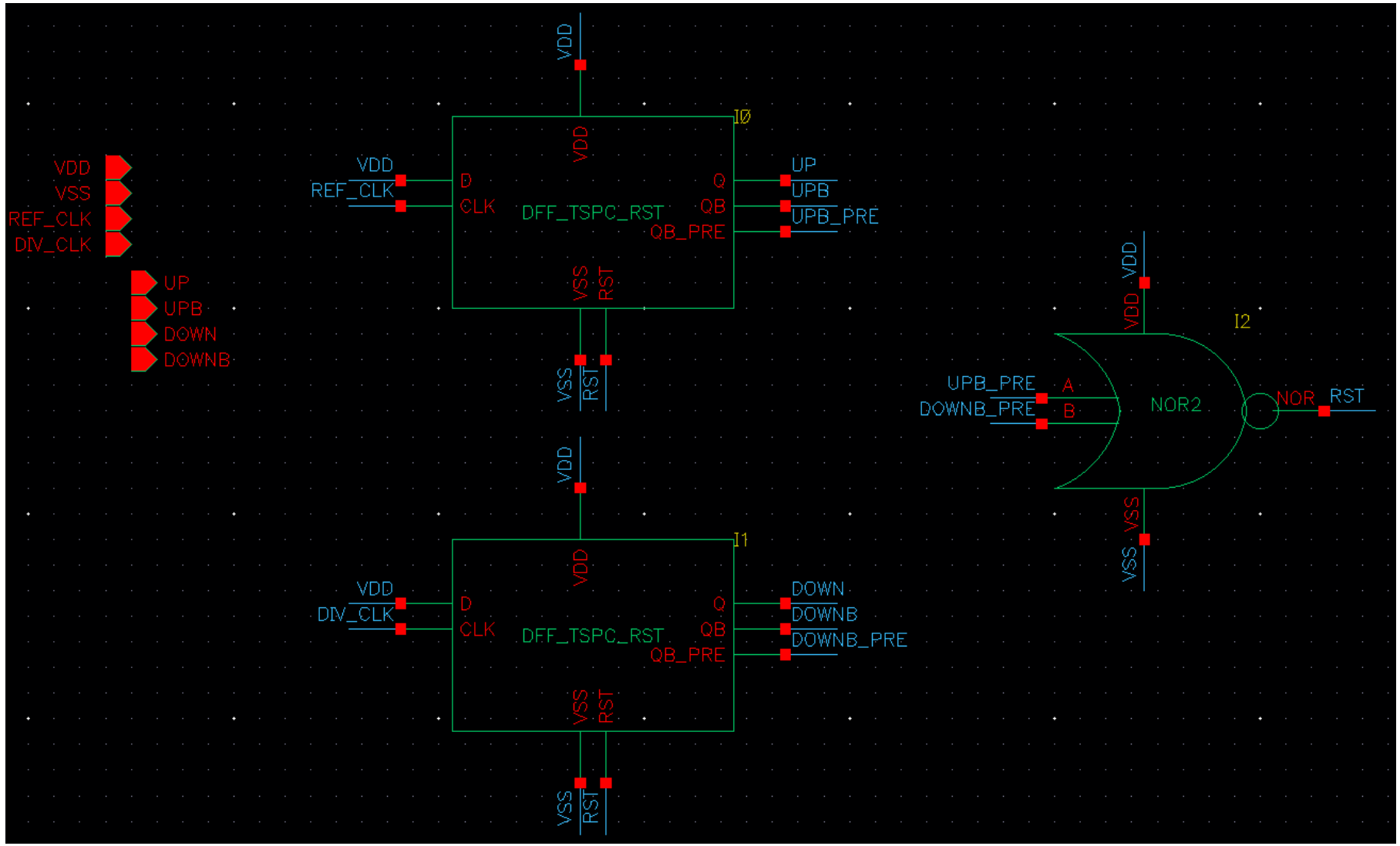
Nonideality_PFD

- Reset 시간 단축





Nonideality_PFD



Nonideality_CP

- Bootstrapping

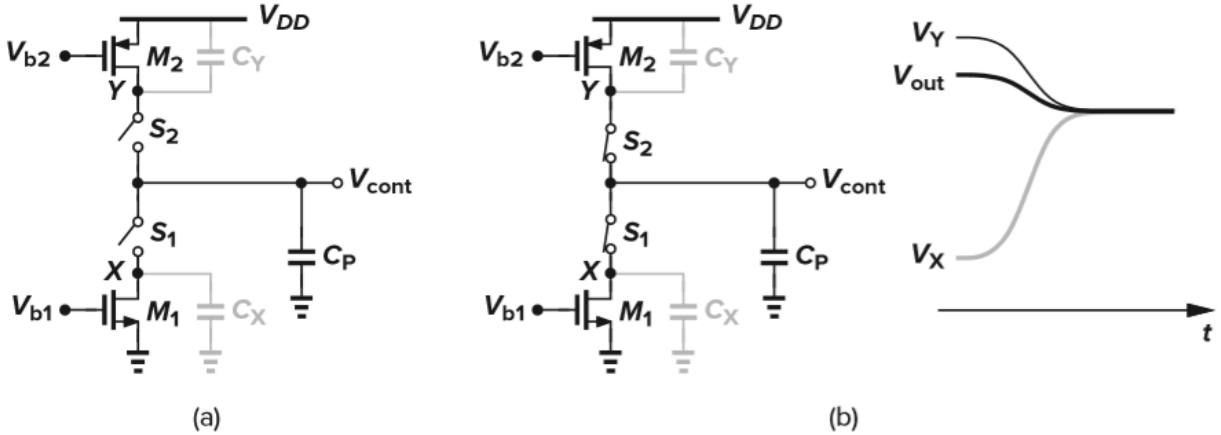


Figure 16.46 Charge sharing between C_P and capacitances at X and Y.

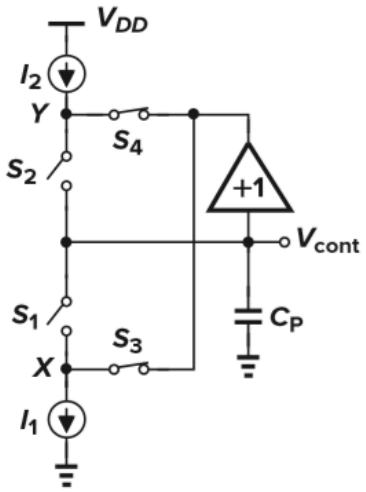
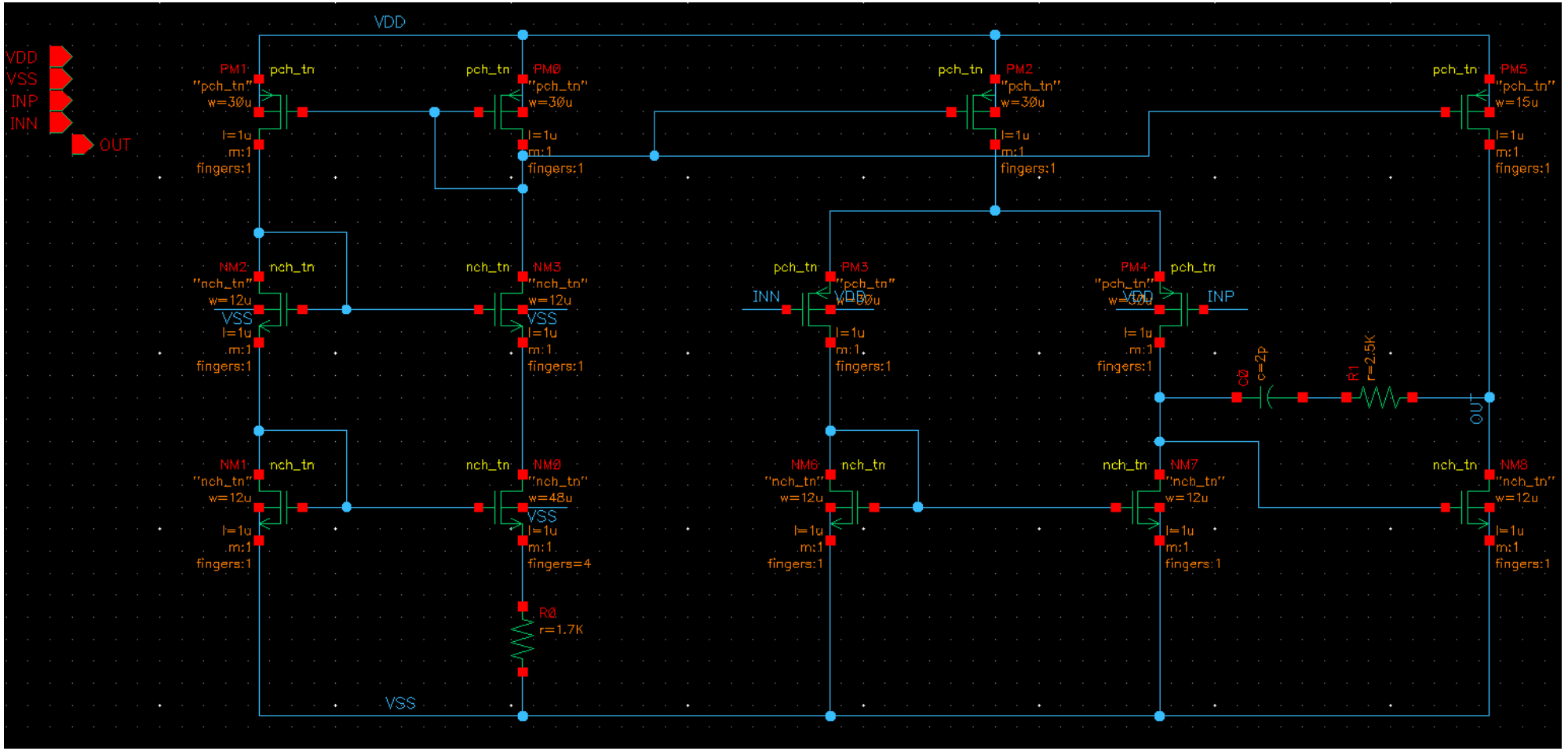


Figure 16.47 Bootstrapping X and Y to minimize charge sharing.

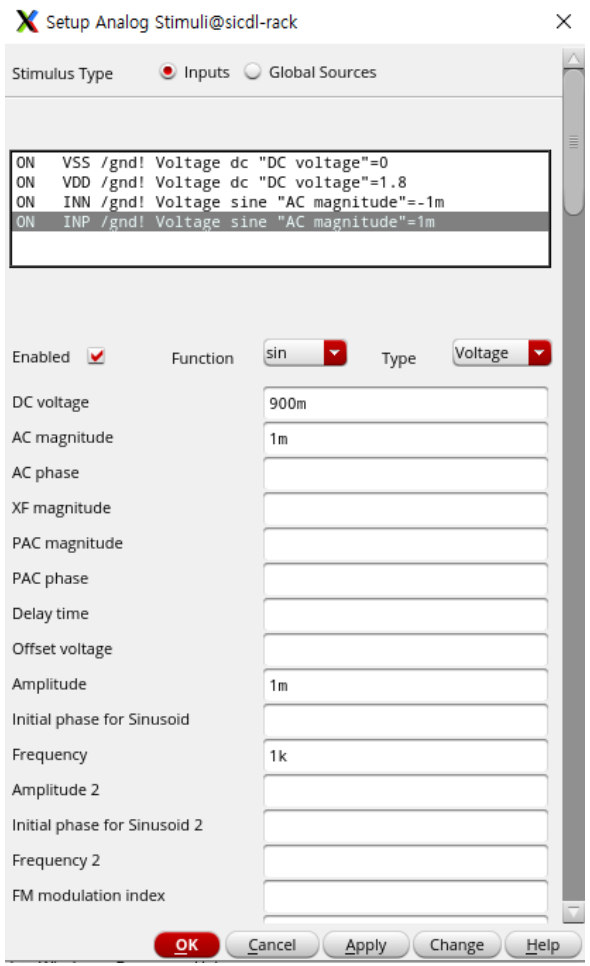
Nonideality_CP

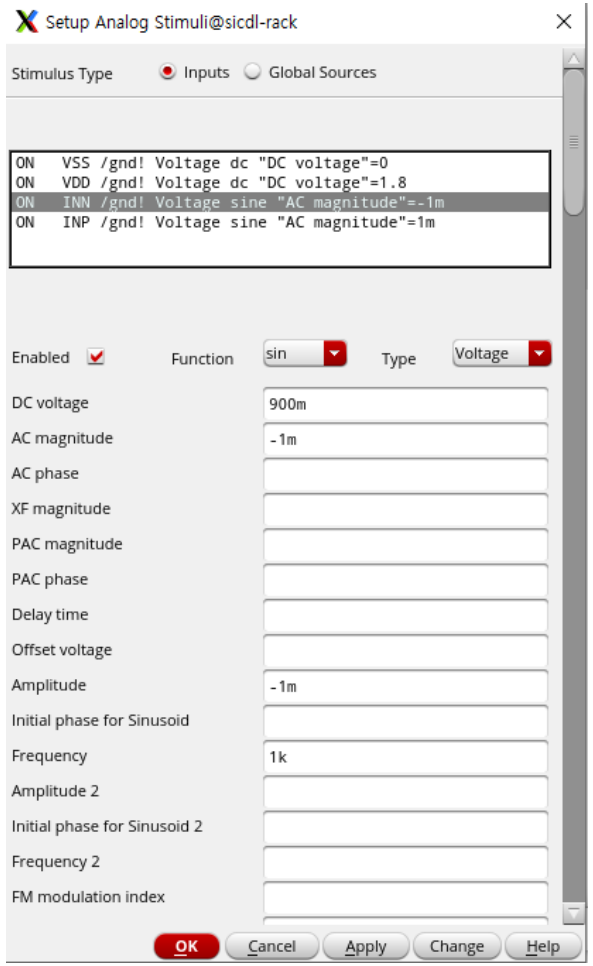
- OPAMP

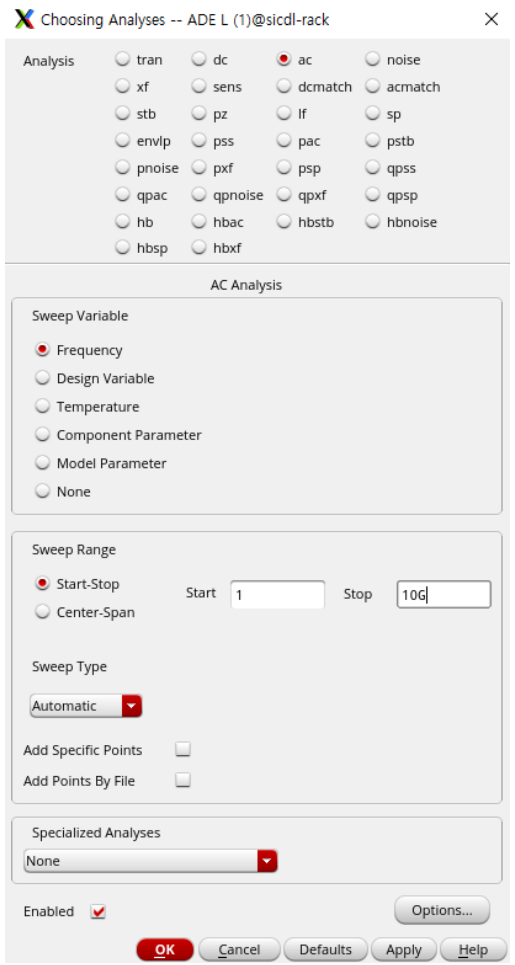


Nonideality_CP

- OPAMP



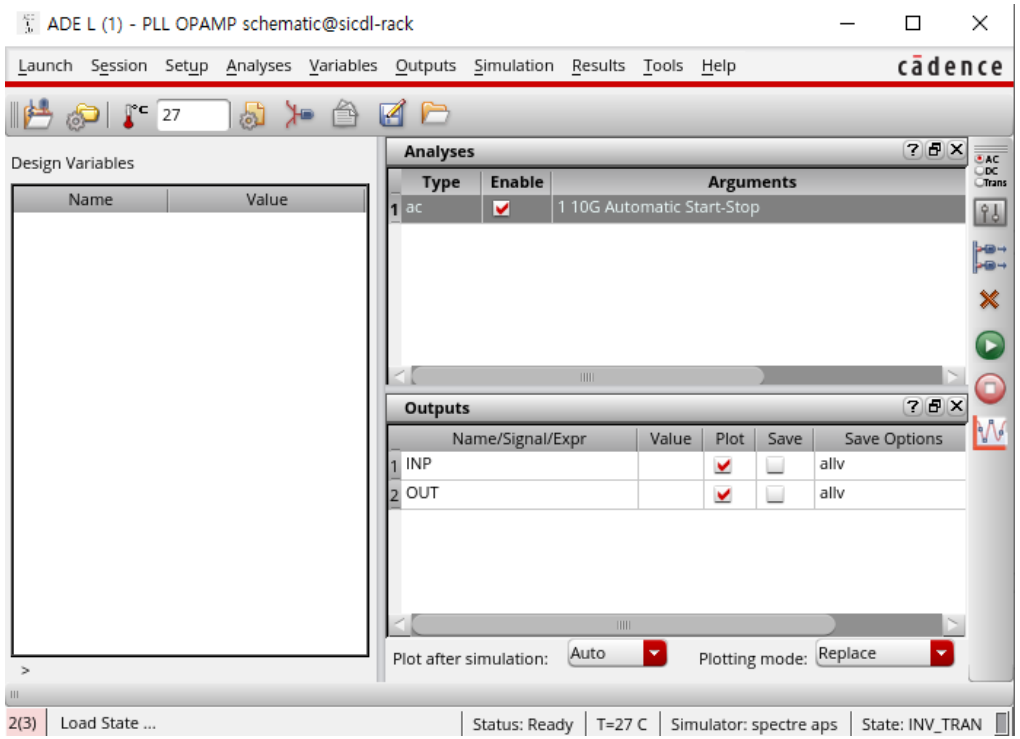




System Integrated Circuit Design Lab.

Nonideality_CP

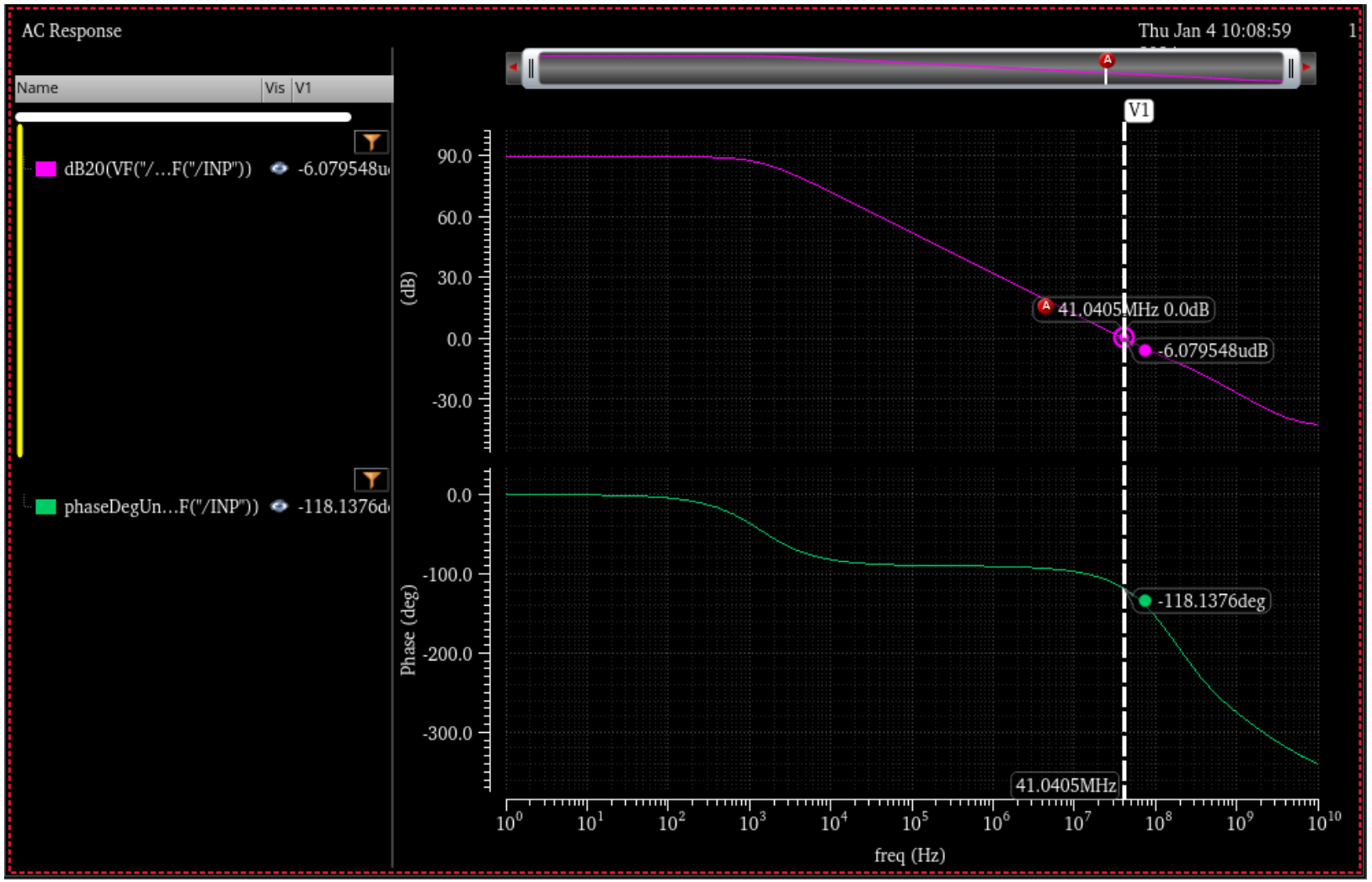
- OPAMP



- 시뮬 먼저 한 번 돌리기
- Results -> Direct Plot -> AC Gain & Phase
- 출력 노드와 입력 노드 순서대로 찍기

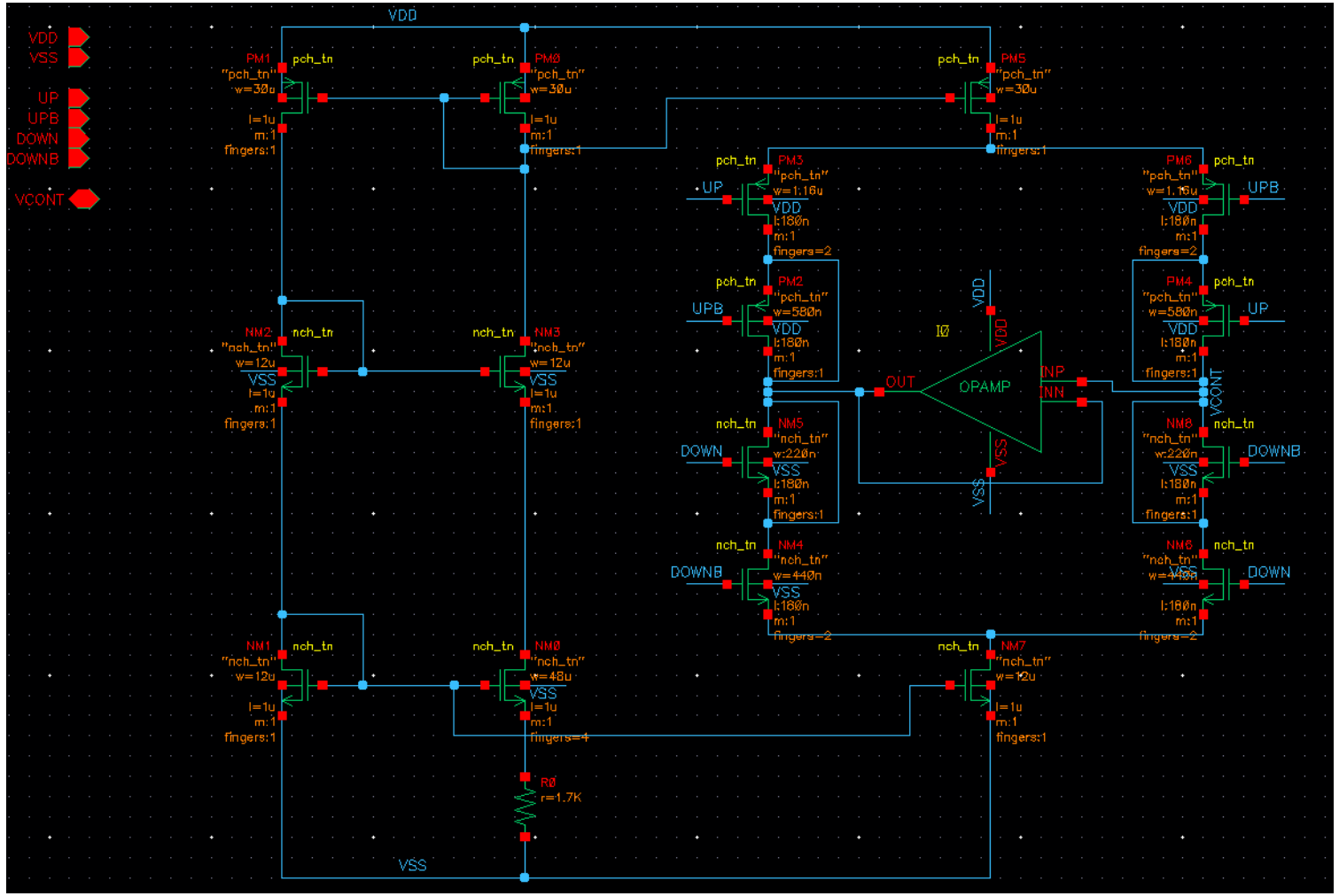
Nonideality_CP

- OPAMP



Nonideality_CP

- CP 설계



보고서 필수사항

- PLL 전체 동작 설명

- 각 Block별 동작 설명

- 각 Block 별 설계 시 유의사항
- 고려사항 유/무에 따른 PLL Spec. 변화

- PLL spec.
- P2P Jitter
- Lock Time
- Power