GIK INSTITUTE
of Engineering Science & Technology

Assignment 2

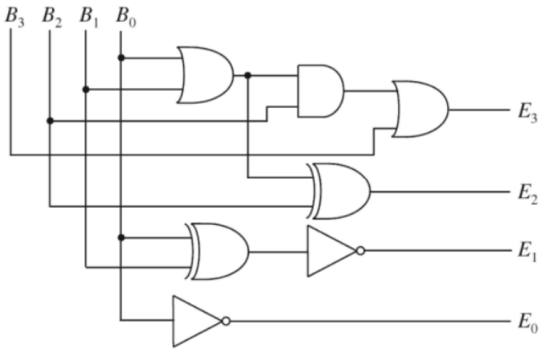
Course Name: **Digital Logic Design** Course Code: **CE 221**

Semester: **Fall 2025** Class: **BS CE** (Batch 34)

Total Marks: **20**

Question 1: Design a circuit using logic gates to convert 4-bit Gray code to its equivalent Binary number. Provide the corresponding truth table, simplified equations, and circuit diagram.

Question 2: Consider the circuit below. Determine the logic equation for each output. Let the input to this circuit is a 4-bit BCD number (0000 → 1001), draw a single truth table enlisting all the inputs and outputs. What does this circuit do? Design another circuit which takes $E_3E_2E_1E_0$ as input and generates $B_3B_2B_1B_0$ as output.



Question 3: You are required to design an adder that can perform selective addition and subtraction of two 3-bit numbers. You may use carry-in as the select line such that if it is "0", your circuit performs addition operation, and when it is "1", the circuit performs subtraction operation. No other logic gate should be used

Question 4: Design a combinational circuit with three inputs x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is twice the input. When the binary input is 4, 5, 6, or 7, the binary output is half the input. Implement the circuit using minimum number of logic gates.

Question 5: Implement the combinational circuit designed in Question 4, using decoders and OR gates only.

Question 6: Design a 3-bit priority encoder. The inputs to the encoder are {A, B, C} and the outputs are {X, Y}. A is the highest priority input followed by B, whereas, C has the lowest priority. The output of the circuit should indicate which input is "1", i.e. if A is high, the output should be "11", if B is high, the output should be "10", if C is high, the output should be "01", and if no input is high, the output should be "00". If more than one inputs are high, the output should correspond to the higher priority input.

Submission Deadline: 12 November 2025