STM32
CubeMX

1. Description

1.1. Project

Project Name	STM32L431CBT6_UNI_MEMS
Board Name	custom
Generated with:	STM32CubeMX 6.8.1
Date	04/08/2024

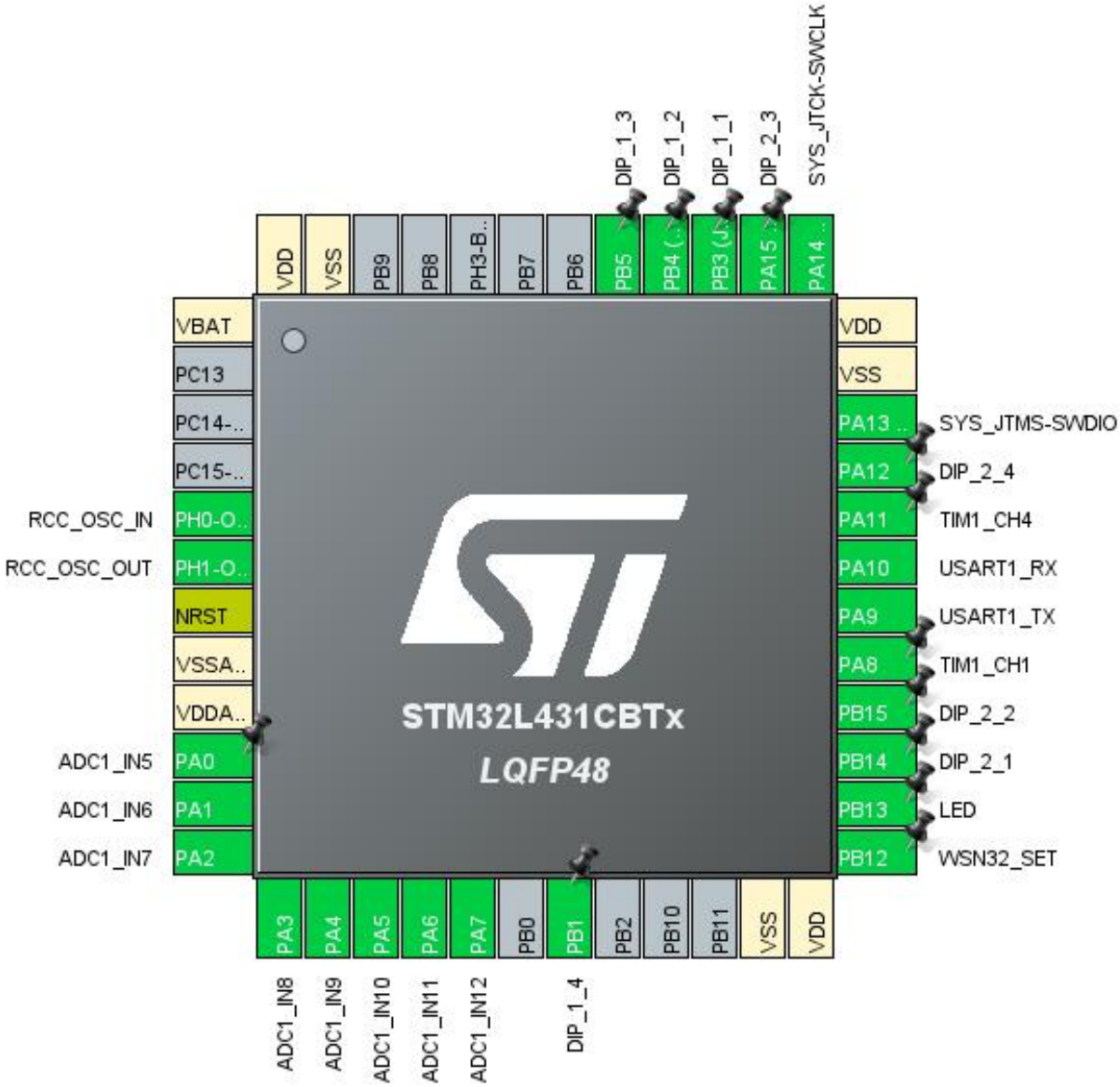
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x1
MCU name	STM32L431CBTx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

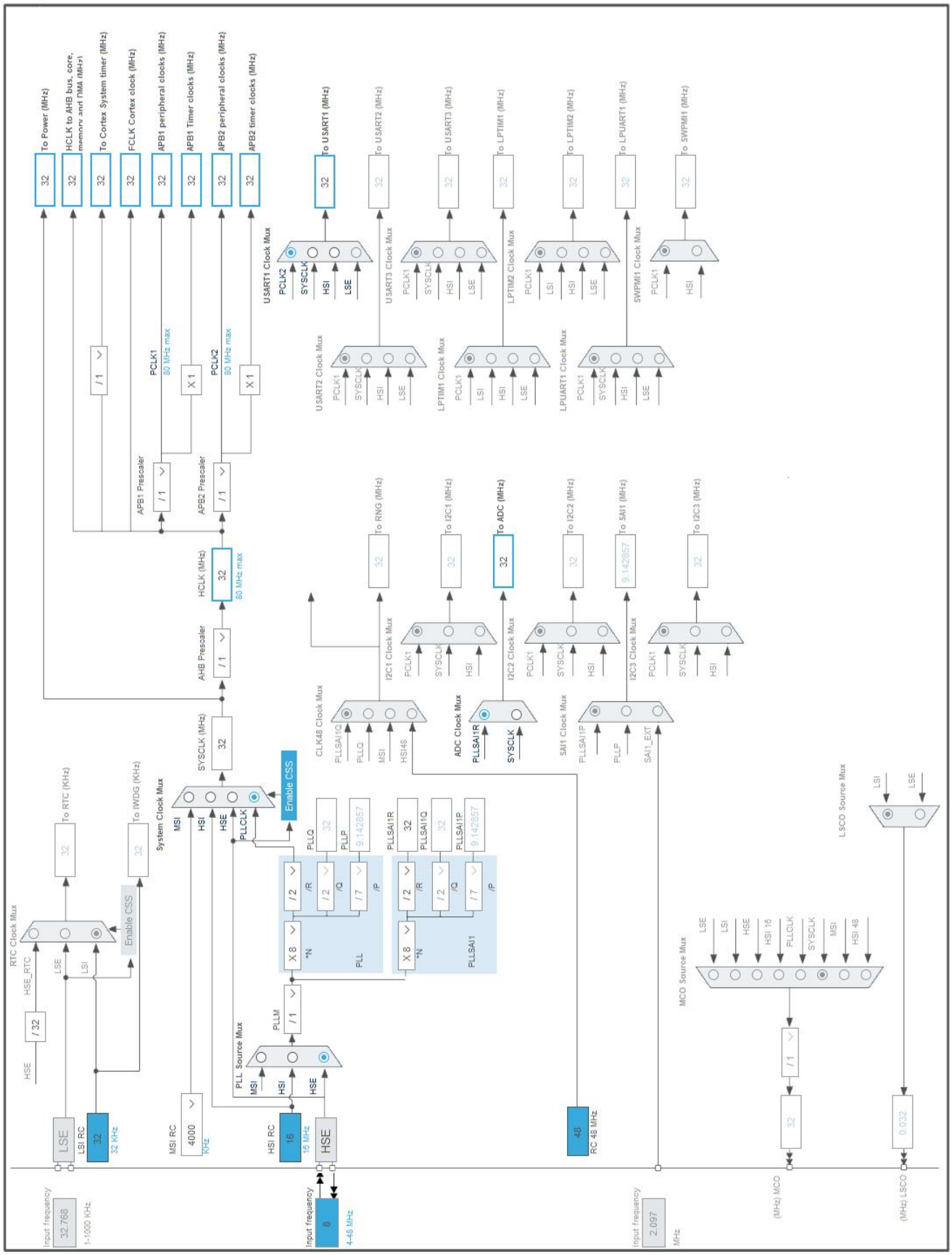


3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA/VREF+	Power		
10	PA0	I/O	ADC1_IN5	
11	PA1	I/O	ADC1_IN6	
12	PA2	I/O	ADC1_IN7	
13	PA3	I/O	ADC1_IN8	
14	PA4	I/O	ADC1_IN9	
15	PA5	I/O	ADC1_IN10	
16	PA6	I/O	ADC1_IN11	
17	PA7	I/O	ADC1_IN12	
19	PB1 *	I/O	GPIO_Input	DIP_1_4
23	VSS	Power		
24	VDD	Power		
25	PB12 *	I/O	GPIO_Output	WSN32_SET
26	PB13 *	I/O	GPIO_Output	LED
27	PB14 *	I/O	GPIO_Input	DIP_2_1
28	PB15 *	I/O	GPIO_Input	DIP_2_2
29	PA8	I/O	TIM1_CH1	
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
32	PA11	I/O	TIM1_CH4	
33	PA12 *	I/O	GPIO_Input	DIP_2_4
34	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	
38	PA15 (JTDI) *	I/O	GPIO_Input	DIP_2_3
39	PB3 (JTDO-TRACESWO) *	I/O	GPIO_Input	DIP_1_1
40	PB4 (NJTRST) *	I/O	GPIO_Input	DIP_1_2
41	PB5 *	I/O	GPIO_Input	DIP_1_3
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32L431CBT6_UNI_MEMS
Project Folder	C:\Users\niwangze\STM32CubeIDE\workspace_1.12.1\STM32L431CBT6_UNI_
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART1_UART_Init	USART1
5	MX_ADC1_Init	ADC1
6	MX_TIM2_Init	TIM2
7	MX_TIM1_Init	TIM1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x1
MCU	STM32L431CBTx
Datasheet	DS11453_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

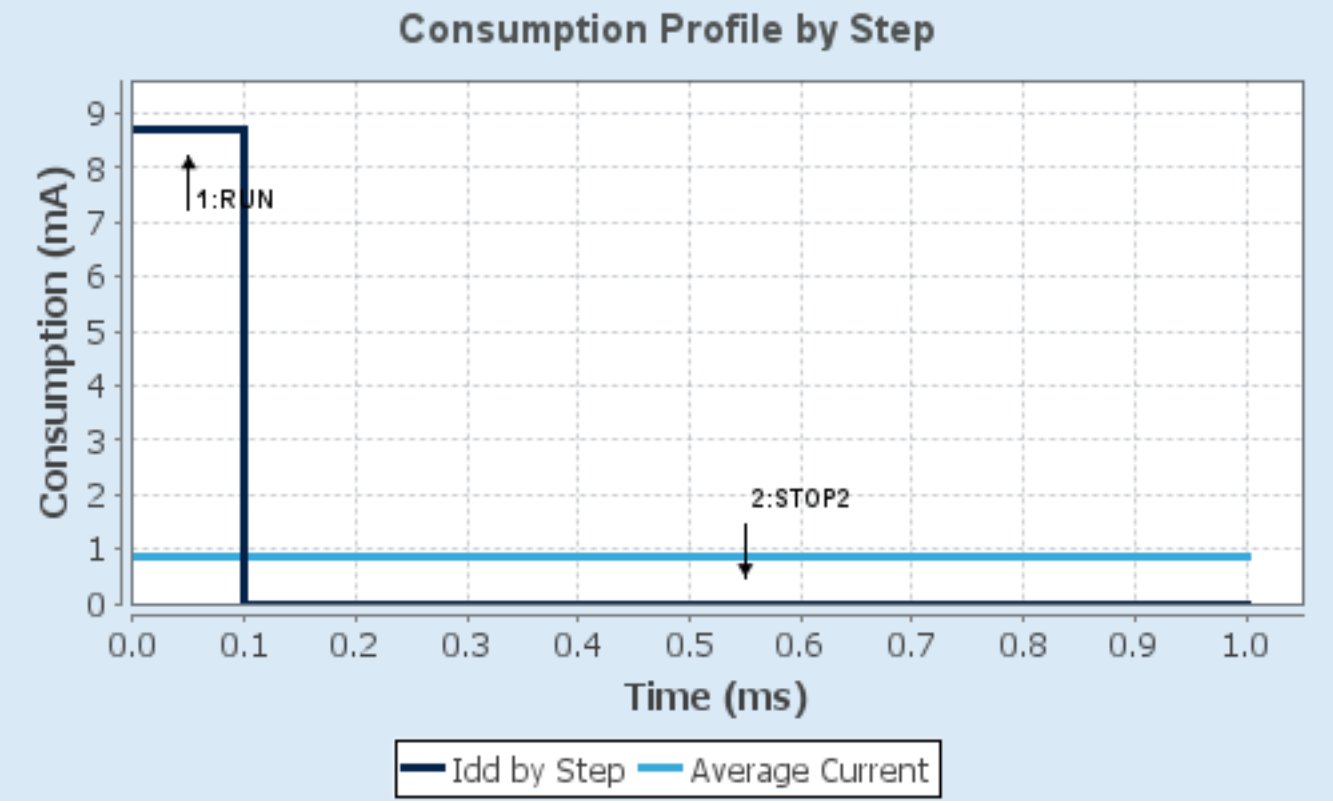
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	8.71 mA	1.06 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.51	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	871.95 µA
Battery Life	5 months, 9 days, 16 hours	Average DMIPS	100.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
9
8
7
6
5
4
3
2
1
0
1:RUN
2:STOP2
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN5: IN5 Single-ended

IN6: IN6 Single-ended

IN7: IN7 Single-ended

IN8: IN8 Single-ended

IN9: IN9 Single-ended

IN10: IN10 Single-ended

IN11: IN11 Single-ended

mode: IN12

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	**Asynchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**8 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 5
Sampling Time	**640.5 Cycles ***
Offset Number	No offset
Rank	**2 ***
Channel	**Channel 6 ***
Sampling Time	**640.5 Cycles ***
Offset Number	No offset
Rank	**3 ***

Channel	**Channel 7 ***
Sampling Time	**640.5 Cycles ***
Offset Number	No offset
Rank	**4 ***
Channel	**Channel 8 ***
Sampling Time	**640.5 Cycles ***
Offset Number	No offset
Rank	**5 ***
Channel	**Channel 9 ***
Sampling Time	**640.5 Cycles ***
Offset Number	No offset
Rank	**6 ***
Channel	**Channel 10 ***
Sampling Time	**640.5 Cycles ***
Offset Number	No offset
Rank	**7 ***
Channel	**Channel 11 ***
Sampling Time	**640.5 Cycles ***
Offset Number	No offset
Rank	**8 ***
Channel	**Channel 12 ***
Sampling Time	**640.5 Cycles ***
Offset Number	No offset
ADC_Injected_ConversionMode:	
Enable Injected Conversions	Disable
Analog Watchdog 1:	
Enable Analog WatchDog1 Mode	false
Analog Watchdog 2:	
Enable Analog WatchDog2 Mode	false
Analog Watchdog 3:	
Enable Analog WatchDog3 Mode	false

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.3. SYS

Debug: Serial Wire

Timebase Source: TIM6

7.4. TIM1

Trigger Source: ITR3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel4: PWM Generation CH4

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**79 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***
Slave Mode Controller	Slave mode disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**700 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	**700 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.5. TIM2

Clock Source : Internal Clock

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**49999 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**499 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

7.6. USART1

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.7. FREERTOS

Interface: CMSIS_V1

7.7.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**30000 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled

CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.7.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

7.7.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN5	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN6	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN7	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN8	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN9	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN10	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN11	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
	PA7	ADC1_IN12	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PB1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_1_4
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WSN32_SET
	PB13	GPIO_Output	Output Push Pull	**Pull-up ***	Low	LED
	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_2_1
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_2_2
	PA12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_2_4

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA15 (JTDI)	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_2_3
	PB3 (JTDO-TRACESWO)	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_1_1
	PB4 (NJTRST)	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_1_2
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIP_1_3

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
USART1_RX	DMA1_Channel5	Peripheral To Memory	**Medium ***
USART1_TX	DMA1_Channel4	Memory To Peripheral	**Medium ***

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 channel1 global interrupt	true	5	0
DMA1 channel4 global interrupt	true	5	0
DMA1 channel5 global interrupt	true	5	0
USART1 global interrupt	true	5	0
TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts	true	15	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 global interrupt	unused		
TIM1 break interrupt and TIM15 global interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel4 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
USART1 global interrupt	false	true	true
TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32l4_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32l4_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32l4_svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32l4_marketing-pres.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32ulp.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32l4.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstmcsuite.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Magazine Articles	https://www.st.com/resource/en/magazine/design-elektronik_august2017.pdf
Magazine Articles	https://www.st.com/resource/en/magazine/design-elektronik_october2016.pdf
Product Certifications	https://www.st.com/resource/en/certification_document/sesip-2000002-01-cert.pdf
Product Certifications	https://www.st.com/resource/en/certification_document/sesip-2000002-01-st2.pdf

Product Certifications	https://www.st.com/resource/en/certification_document/psa-certificate_stm32l4.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3154-can-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3236-increase-the-number-of-touchkeys-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3960-esd-considerations-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4229-how-to-

	implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4277-using-stm32-device-pwm-shutdown-features-for-motor-control-and-digital-power-conversion-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4299-improve-conducted-noise-robustness-for-touch-sensing-applications-on-mcus-stmicroelectronics.pdf
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