## HW#2a

- ${\bf 1.} \ {\bf Construct} \ {\bf an} \ {\bf NXOR} \ {\bf gate} \ {\bf by} \ {\bf interconnecting} \ {\bf buffers} \ {\bf and} \ {\bf inverters}.$
- 2. Implement the following expression F=AB'+C'D with
  - a) NAND-NAND gates
  - b) NOR-NOR gates