HW #7

1.
a) 12 bits
b) 12 bits
c) Each multiplexer will have 4 inputs and 12 multiplexers are needed.

2. a) branch address field = 12 bits
select field = 8 bits

$4096 = 2^{12}$
$32 - 12 - 12 =$
$20 - n = 8$

b) 4 bits
c) 4 bits

3.a) 60 - 010 000 010 00 00 1000011
61 - 111 100 000 01 01 1000000
62 - 001 001 000 10 10 0111111
63 - 101 110 000 11 11 0111100

b)
In line 61, we cannot write and read off the same time, the operation is impossible.

60- CLRAC (AC←0)
(AC ← $\overline{AC}$) COM REG 67

61- WRITE (M[AR]←DR)
READ (DR← M[AR])
DR (I)
CALL (CAR ← AD if cond=1) REG 64

62- ADD (AC←AC+DR)
SUB (AC←AC-DR)
AC (S)
RET (CAR←SUB)
REG 63

63-
DRTAR (AR← DR(0-10))
INCDR (DR←DR+1)
AC- (Z)
MAP (CAR 0 5...)
REG 60