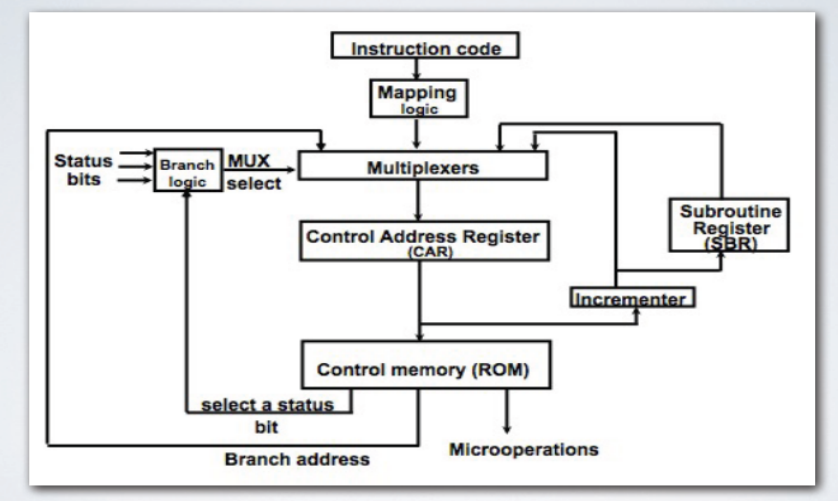
Dr. Cherif Salama
Faculty of Media Engineering
and Technology

CSEN 402 Computer Organization and System Programming
Practice Assignment 10
Spring 2014

NOT to be submitted
To be discussed during tutorial sessions

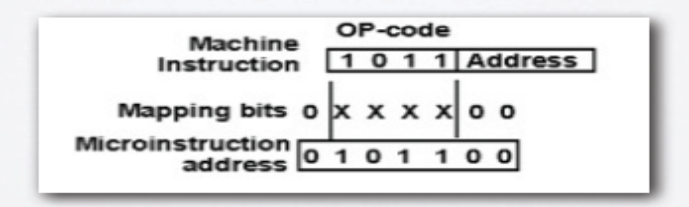
Exercise 1:
The system shown in the figure below uses a control memory of 1024 word of 32 bits each. The microinstruction has three fields as shown in the diagram. The microoperation field has 16 bits.



a. How many bits are there in the branch address field and the select field?
b. If there are 16 status bits in the system, how many bits of the branch logic are used to select a status bit?
c. How many bits are left to select an input for the multiplexers?

Exercise 2:
If the control memory in the figure above has 4096 words of 24 bits each.
a. How many bits are there in the control address register?
b. How many bits are there in each of the four inputs shown going into the multiplexers?
c. What are the number of the inputs in each multiplexer and how many multiplexers are needed?

Exercise 3:
Using the mapping procedure described in the figure below:



Give the first microinstruction address for the following operation codes:

(a) 0010
(b) 1011
(c) 1111

Exercise 4:
Using the tables below:

F1	Microoperation	Symbol
000	None	NOP
001	AC ← AC + DR	ADD
010	AC ← 0	CLRAC
011	AC ← AC + 1	INCAC
100	AC ← DR	DRTAC
101	AR ← DR(0-10)	DRTAR
110	AR ← PC	PCTAR
111	M[AR] ← DR	WRITE

F2	Microoperation	Symbol
000	None	NOP
001	AC ← AC - DR	SUB
010	AC ← AC ∨ DR	OR
011	AC ← AC ∧ DR	AND
100	DR ← M[AR]	READ
101	DR ← AC	ACTDR
110	DR ← DR + 1	INCDR
111	DR(0-10) ← PC	PCTDR

F3	Microoperation	Symbol
000	None	NOP
001	AC ← AC ⊕ DR	XOR
010	AC ← AC'	COM
011	AC ← shl AC	SHL
100	AC ← shr AC	SHR
101	PC ← PC + 1	INCPC
110	PC ← AR	ARTPC
111	Reserved	

Give the 9-bit microoperation field for the following microoperations:

a. AC ← AC + 1, DR ← DR + 1
b. PC ← PC+1, DR ← M[AR]
a. DR ← AC, AC ← DR

Exercise 5:
Using the tables above, convert the following symbolic microoperations to register transfer statements and to binary:

(a) READ, INCPC
(b) ACTDR, DRTAC
(c) ARTPC, DRTAC, WRITE

Exercise 6:
Suppose that we change the ADD routine listed in the table in the appendix, to the following two microinstructions:

```
ADD:    READ I    CALL INDR2
        ADD  U    JMP  FETCH
```

What should be subroutine INDR2?

Exercise 7:
Add the following instructions to the computer you studied (EA is the effective address). Write the symbolic microprogram for each routine as in the table attached. (Note that AC must not change in value unless the instruction specifies a change in the AC).

Symbol	Opcode	Symbolic Function	Description
AND	0100	AC ← AC ∧ M[EA]	AND
SUB	0101	AC ← AC – M[EA]	Subtract
ADM	0110	M[EA] ← M[EA] + AC	Add to memory
BTCL	0111	AC ← AC ∧ complement(M[EA])	Bit clear
BZ	1000	If (AC = 0) then (PC ← EA)	Branch if AC Zero
SEQ	1001	If (AC = M[EA]) then (PC ← PC+1)	Skip if equal
BPNZ	1010	If (AC > 0) then (PC ← EA)	Branch if positive and nonzero

Exercise 8:
Show how outputs 5 and 6 of decoder 3 in the figure below are to be connected to the program counter (PC).

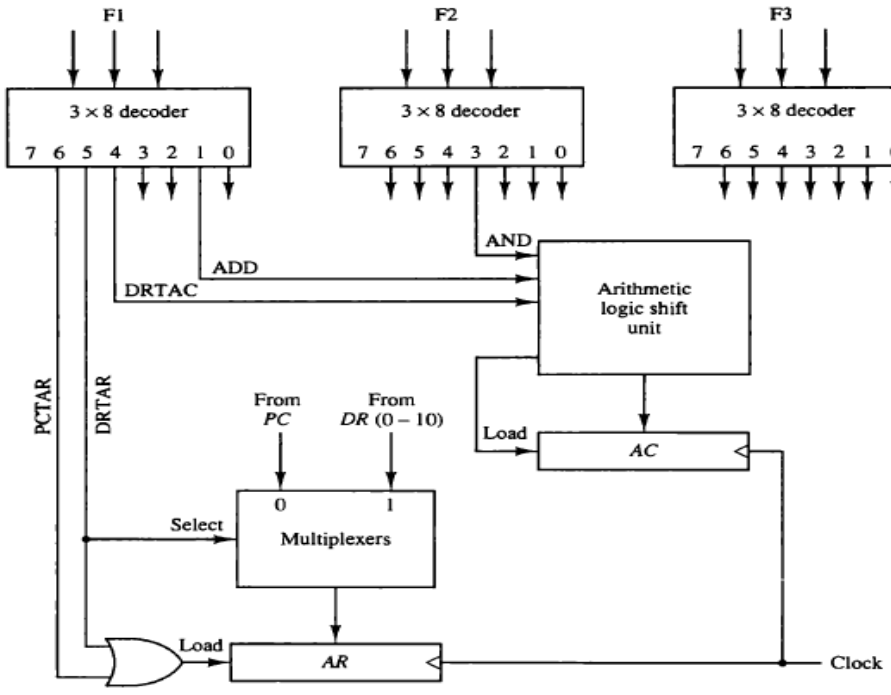


Figure 7-7 Decoding of microoperation fields.

Exercise 9:
A computer has 16 registers, an ALU with 32 operations and a shifter with eight operations, all connected to a common bus system.

a. Formulate a control word for a microinstruction.
b. Specify the number of bits in each field of the control word.
c. Show the bits of the control word that specify the microoperation: R4 ← R5+R6

Appendix: Table needed for Exercises 6 and 7:

TABLE 7-2 Symbolic Microprogram (Partial)

Label	Microoperations	CD	BR	AD
	ORG 0			
ADD:	NOP	I	CALL	INDRCT
	READ	U	JMP	NEXT
	ADD	U	JMP	FETCH
	ORG 4			
BRANCH:	NOP	S	JMP	OVER
	NOP	U	JMP	FETCH
OVER:	NOP	I	CALL	INDRCT
	ARTPC	U	JMP	FETCH
	ORG 8			
STORE:	NOP	I	CALL	INDRCT
	ACTDR	U	JMP	NEXT
	WRITE	U	JMP	FETCH
	ORG 12			
EXCHANGE:	NOP	I	CALL	INDRCT
	READ	U	JMP	NEXT
	ACTDR, DRTAC	U	JMP	NEXT
	WRITE	U	JMP	FETCH
	ORG 64			
FETCH:	PCTAR	U	JMP	NEXT
	READ, INCPC	U	JMP	NEXT
	DRTAR	U	MAP	
INDRCT:	READ	U	JMP	NEXT
	DRTAR	U	RET	