SCHOOL OF COMPUTING & IT
Department of IT/ CSE/ CCE
III Semester; 2nd-Sessional Examination, Nov. 2016
Course: B.Tech
OPEN BOOK EXAMINATION

Subject Code: CS1301 **Subject Name: Computer Organization and Architecture**
Max. Marks: 20 **Duration: 1 hour**

Instructions:	1. All questions are compulsory 2. Missing data if any can be suitably assumed. 3. Numbers in [ ] indicates marks

Q1. Perform multiplication 30 × 63 using carry-save addition of summands method. Also calculate minimum gate delay required to perform multiplication of 16-bit operands using the above method. [4]

Q2. Perform the multiplication of 5-bit operands M = 14 and Q = -9 using Booth algorithm and bit-pair recoding method. [4]

Q3. Perform 23 ÷ 13 by non-restoring division algorithm using 5-bit binary representation of operands. [4]

Q4. Consider that floating point numbers are represented in a 12-bit format with a 5-bit, excess-15 exponent. The 6-bit mantissa is normalized as in the IEEE format, with an implied 1 to the left of the binary point. Represent the numbers A = 12 and B = 0.5 in the above format.
Also perform A + B and A × B, using arithmetic operation rules on floating-point numbers. [5]

Q5. A computer system has a main memory consisting of 1 M (2^{20}) 32-bit words. It also has an 8K word cache organized in the block-set-associative manner, with 2 blocks per set and 64 words per block. Suppose CPU generates the 20-bit Hexadecimal address AB23C to access a 32-bit word, Answer the following:
(a) Specify the set number to which the given address maps.
(b) Mention the tag bits in the given address.
(c) How many tags need to be checked for a matching in the given scenario? [3]